EECS 16B Designing Information Devices and Systems II
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Transistors

Contents

1 Switches

Switches in circuitry denote a boolean value: either "off" (0) or "on" (1). More specifically, there are three components to a switch: the source (S), drain (D), and gate (G).

When the gate is in its "on" state, the switch is closed, and current passes between the source and the drain. Otherwise, no current flows.

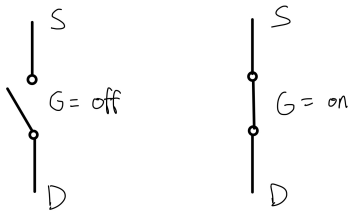

Figure 1: Switch circuit model

2 PMOS and NMOS Transistors

In the most simplified form, transistors are switches whose gate is controlled by a threshold gate voltage, measured as the voltage at the gate (V_G) relative to the voltage at the source (V_S). We denote this voltage as $V_{GS} = V_G - V_S$ and its negation $V_{SG} = -V_{GS} = V_S - V_G$.

In this class, we will cover the CMOS family of transistors, which consist of two types: PMOS and NMOS. Each has a different condition for closing its switch:

- NMOS: when the gate voltage is greater than some positive threshold V_{tn}. In other words, $V_{GS} > V_{tn}$
- PMOS: when the gate voltage is less than some negative threshold $-V_{tp}$. In other words, $V_{GS} < -V_{tp}$ or $V_{SG} > V_{tp}$

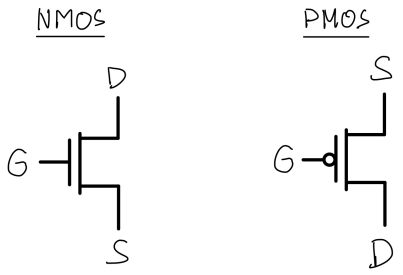

Figure 2: CMOS transistors circuit model

2.1 Transistor Physics

However, transistors are not actually that simple. While an exact model of involves an extensive knowledge in physics and is out of scope for this class, a "charge puddle" model of the transistor can provide us with more detail on how they work.

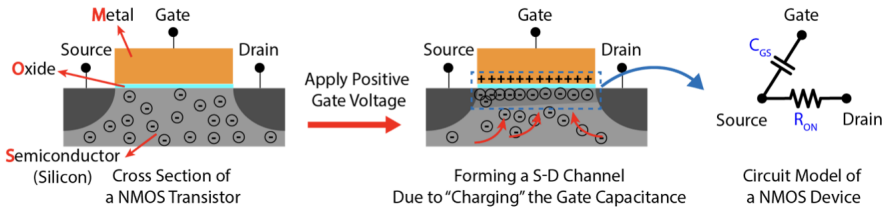

Figure 3: Puddle model of a transistor

The gate and the silicon connecting the source and drain act similar to two ends of a capacitor. An increase in voltage on the gate causes a "puddle" of charge carriers to form on the silicon, which increases until it is large enough to connect the source and drain, allowing current to pass between them. The gate voltage that corresponds to that connection is the threshold voltage.

2.2 Resistor-switch Model

With the charge puddle model in mind, we can construct a better circuit model of the transistor. Since the puddle is not a perfect conductor, there is some resistance between the source and drain of a transistor when they are connected. Additionally, we noted earlier that the gate and silicon acted similar to a capacitor, so we add a capacitor between the gate and the source.

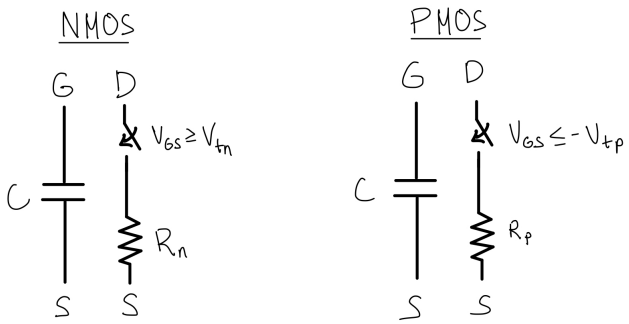

Figure 4: Resistor-switch model of CMOS transistors

As we will see soon, we can use this model to observe some interesting behaviors in circuits involving transistors.

3 Inverters

An inverter is a circuit component that does a "NOT" operation: it maps a 0 (low) input to a 1 (high) output and vice versa. Physically, it's composed of an NMOS and a PMOS transistor that are connected together as such:

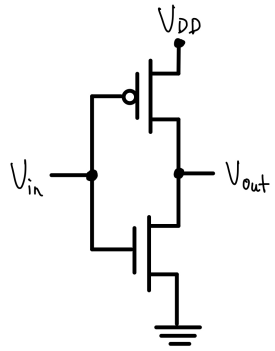

Figure 5: CMOS inverter

For the PMOS transistor, the gate voltage is $V_{SG_p} = V_{DD} - V_{in}$. For our NMOS transistor, it is $V_{GS_n} = V_{in} - 0$.

When the input voltage is high (specifically when $V_{in} > V_{tn}$), the NMOS transistor closes its switch, so ground and V_{out} are connected.

On the other hand, when the input voltage is low (specifically when $V_{in} < V_{DD} - V_{tp}$, and thus $V_{SG_p} > V_{tp}$), the PMOS transistor closes its switch, so V_{DD} and V_{out} are connected.

4 Oscillators

Now, what if we chain an odd number of inverters together into a loop? If we do that, we create what is called an oscillator.

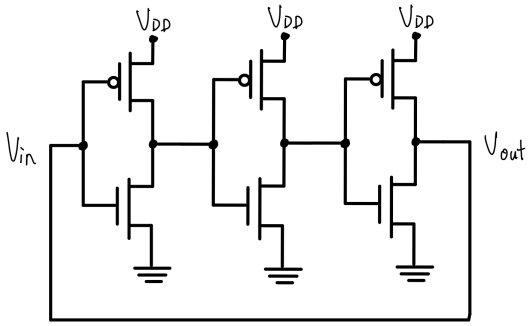

Figure 6: Ring oscillator with 3 CMOS inverters

As the name implies, the voltage of this system oscillates between high and low, and it does so at some constant frequency. That makes it useful for clocks and other digital devices.

We won't prove this here, but you need more than one inverter, otherwise it could converge to some inter-

mediate value. For best results, an odd prime number of inverters should be used due to properties with modular arithemtic.

4.1 Detailed Model

The reason why an oscillator actually oscillates is because the inverters do not immediately invert their voltages, creating a chain of sequential inversions that happen on a delay.

Let's revisit the resistor-switch model of the transistor to take a closer look at why this is the case.

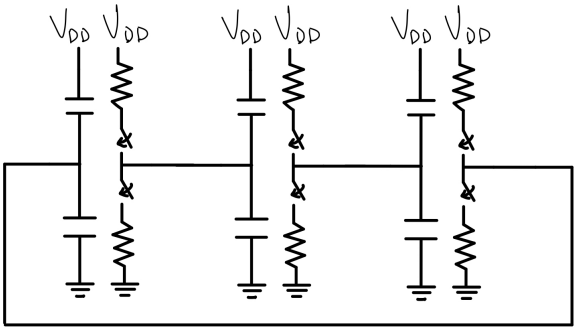

Figure 7: Detailed ring oscillator with resistor-switch transistor model

Let's take a look at specifically the connection between the output of one inverter and the input of the next. When the input voltage to the first inverter is high, the PMOS switch is open and the NMOS switch is closed, making the connection look something like this:

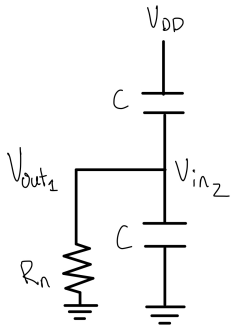

Figure 8: Inverter low output

When the first input voltage is high, the PMOS switch is closed and the NMOS switch is open.

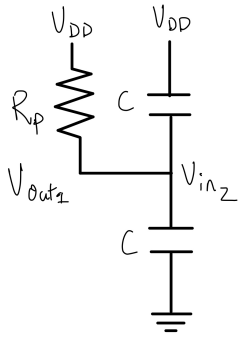

Figure 9: Inverter high output

We can see that the inverters form an RC circuit, charging up the capacitors to the second inverter when the first inverter gives a high output, and discharging the capacitors when the first inverter gives a low output.

Since this charging and discharging is a gradual process, V_{in_2} does not immediately switch between V_{DD} and 0, and thus it takes some duration of time after one inverter flips before the next one does.

In the next section, we will explore the behavior of RC circuits like this further using differential equations.