2023 Digital IC Design Homework 1

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Functional Simulation Result

Stage 1	Pass/Fail	Stage 2	Pass/Fail	Stage 3	Pass/Fail	Stage 4	Pass/Fail

Stage 1

```
-------------Stage 1 : Maximum selection with 4-input MMS-------------

-------------Stage 1 :              Pass!                 -------------
```

Stage 2

```
-------------Stage 2 : Minimum selection with 4-input MMS-------------

-------------Stage 2 :              Pass!                 -------------
```

Stage 3

```
-------------Stage 3 : Maximum selection with 8-input MMS-------------

-------------Stage 3 :              Pass!                 -------------
```

Stage 4

```
-------------Stage 4 : Minimum selection with 8-input MMS-------------

-------------Stage 4 :              Pass!                 -------------
```

Description of your design

首先創建一個 combin module 用來判斷傳入的兩個 number 大小，再在 MMS_4num module 內呼叫 combin 函式分別將 number0,number1 和 number2,number3 比大小後再進行合併，而 MMS_8num module 同理。

```
module combin(n1,n2,sel,out);
    input [7:0] n1;
    input [7:0] n2;
    input sel;
    output[7:0] out;
    reg [7:0] out;
    reg [7:0] min;
    reg [7:0] max;
    reg cmp;
    always@(*)begin
        if(n1<n2)
            cmp = 1'b1;
        else
            cmp = 1'b0;
        case({sel,cmp})
            2'b00:
                out = n1;
            2'b01:
                out = n2;
            2'b10:
                out = n2;
            2'b11:
                out = n1;
        endcase
    end

endmodule
```

```
module MMS_4num(result, select, number0, number1, number2, number3);

    input         select;
    input  [7:0] number0;
    input  [7:0] number1;
    input  [7:0] number2;
    input  [7:0] number3;
    output [7:0] result;

    wire    [7:0]task1_out;
    wire    [7:0]task2_out;

    combin task1(number0,number1,select,task1_out);
    combin task2(number2,number3,select,task2_out);
    combin task3(task1_out,task2_out,select,result);

endmodule
```

```
module MMS_8num(result, select, number0, number1, number2, number3, number4, number5, number6, number7)

input         select;
input  [7:0] number0;
input  [7:0] number1;
input  [7:0] number2;
input  [7:0] number3;
input  [7:0] number4;
input  [7:0] number5;
input  [7:0] number6;
input  [7:0] number7;
output [7:0] result;

wire    [7:0]result1;
wire    [7:0]result2;

MMS_4num task_a(result1, select, number0, number1, number2, number3);
MMS_4num task_b(result2, select, number4, number5, number6, number7);
combin task_c(result1,result2,select,result);

endmodule
```

```
combin task1(number0,number1,select,task1_out);
combin task2(number2,number3,select,task2_out);
combin task3(task1_out,task2_out,select,result);
```