
STM32
CubeMX

1. Description

1.1. Project

Project Name	STM32G491RE_RTC_Timers_LPM_Demo
Board Name	custom
Generated with:	STM32CubeMX 6.8.0
Date	03/17/2023

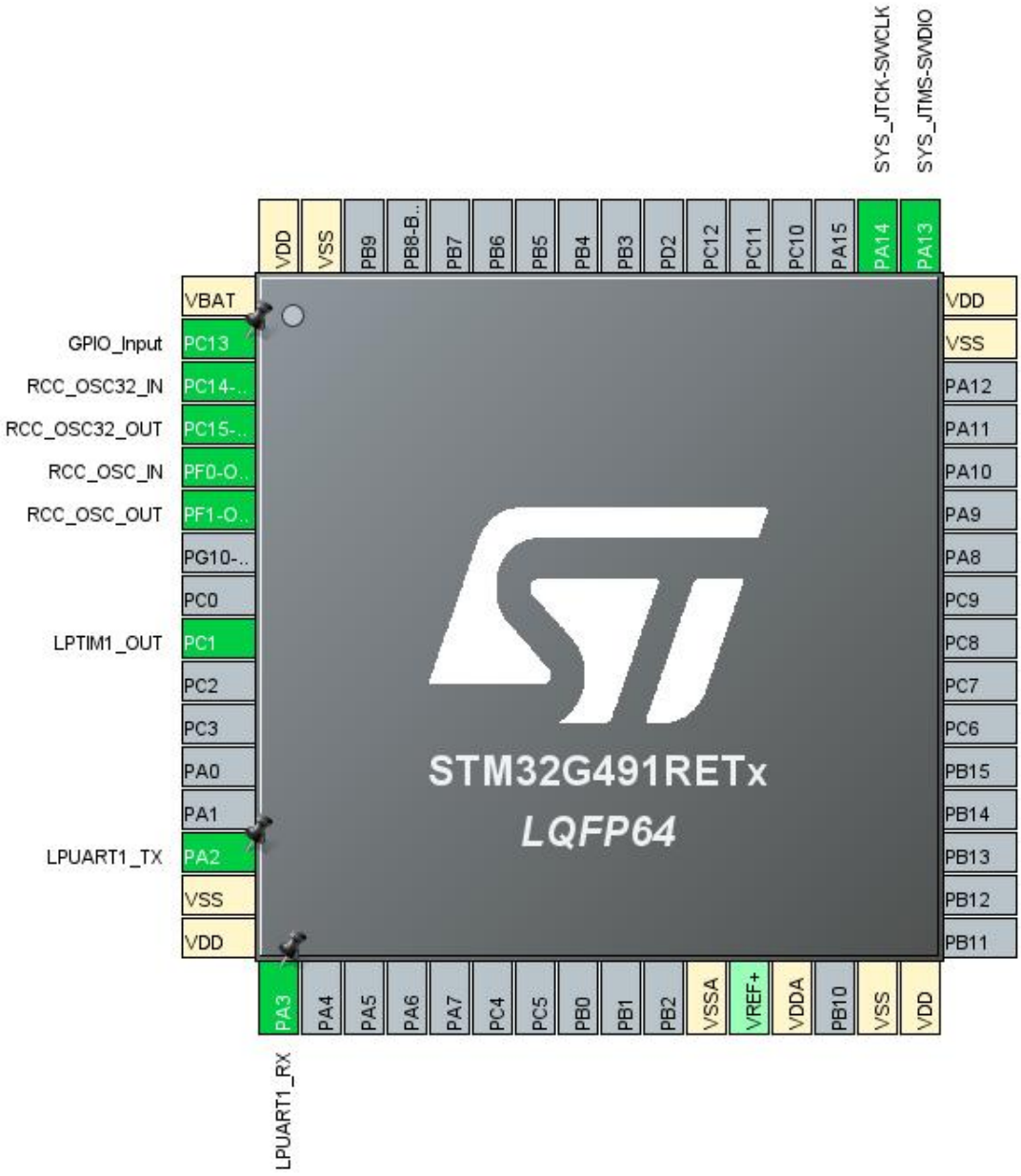
1.2. MCU

MCU Series	STM32G4
MCU Line	STM32G4x1
MCU name	STM32G491RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	ARM Cortex-M4

2. Pinout Configuration

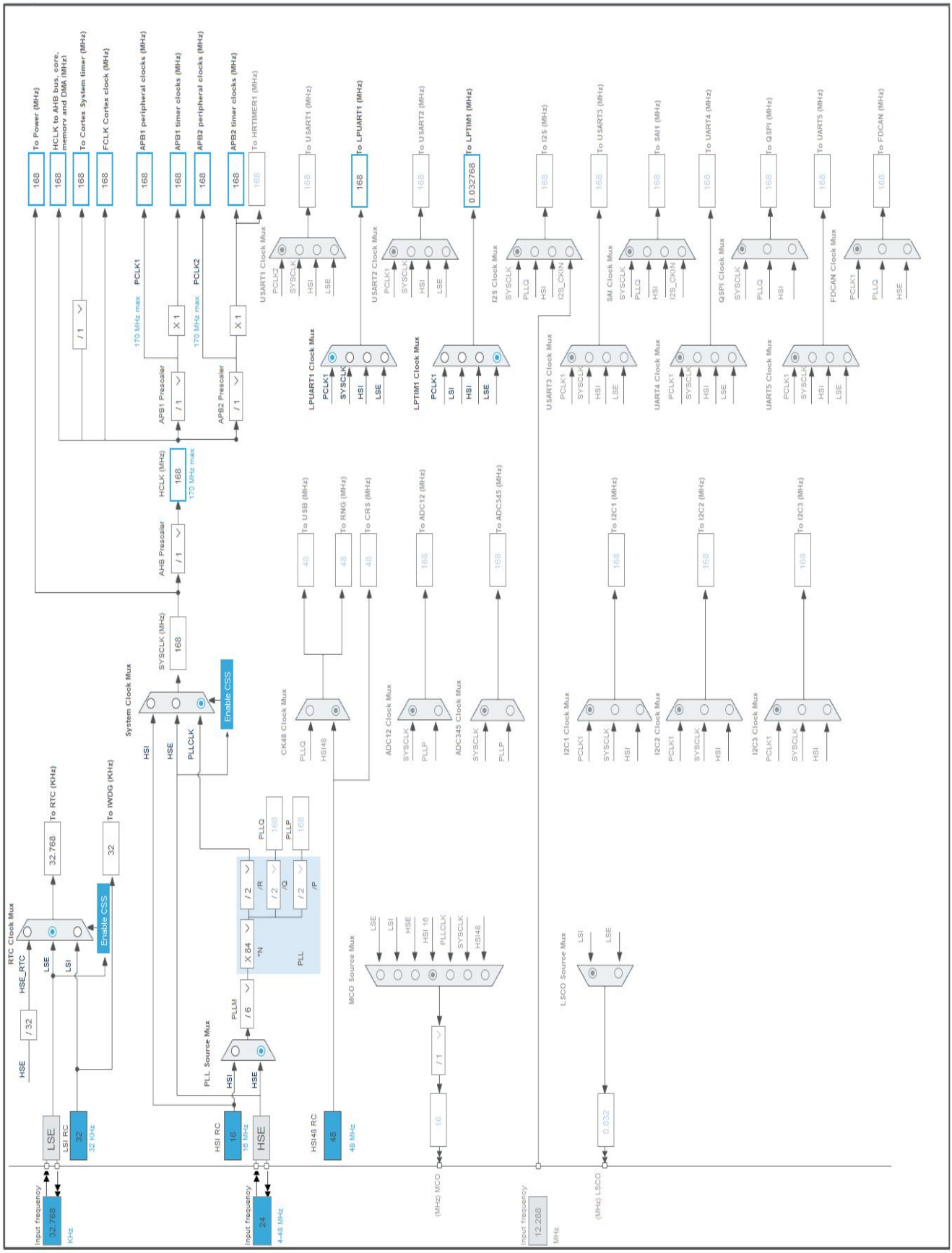


3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
2	PC13 *	I/O	GPIO_Input	
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
9	PC1	I/O	LPTIM1_OUT	
14	PA2	I/O	LPUART1_TX	
15	VSS	Power		
16	VDD	Power		
17	PA3	I/O	LPUART1_RX	
27	VSSA	Power		
29	VDDA	Power		
31	VSS	Power		
32	VDD	Power		
47	VSS	Power		
48	VDD	Power		
49	PA13	I/O	SYS_JTMS-SWDIO	
50	PA14	I/O	SYS_JTCK-SWCLK	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	STM32G491RE_RTC_Timers_LPM_Demo
Project Folder	D:\KEV\Workspace\ST\Nucleo-G491\STM32G491RE_RTC_Timers_LPM_Demo
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_G4 V1.5.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LPUART1_UART_Init	LPUART1
4	MX_IWDG_Init	IWDG
5	MX_LPTIM1_Init	LPTIM1
6	MX_RTC_Init	RTC

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32G4
Line	STM32G4x1
MCU	STM32G491RETx
Datasheet	DS13122_Rev1

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

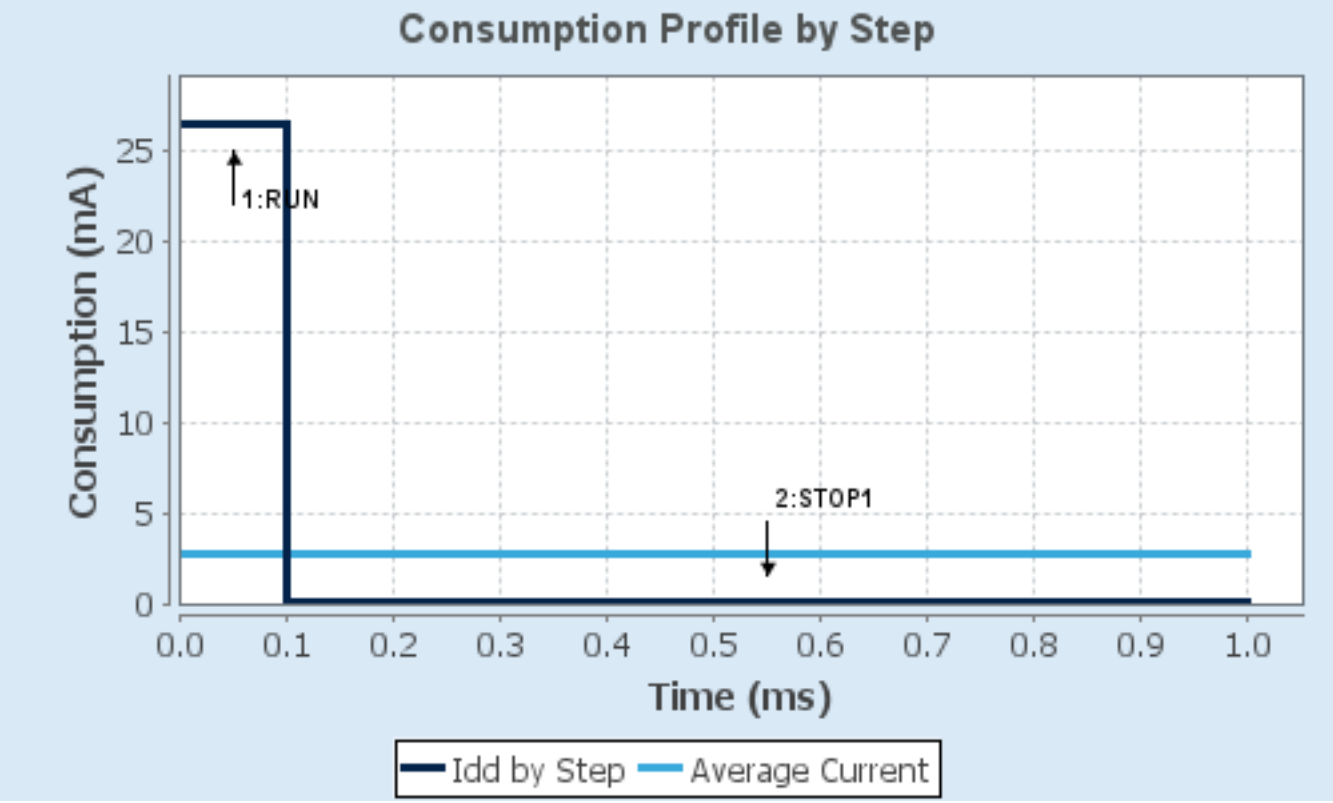
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP1
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Range1-Boost	NoRange
Fetch Type	FLASH/ART	NA
CPU Frequency	170 MHz	0 Hz
Clock Configuration	HSE BYP PLL	LSE LowDrive RTC
Clock Source Frequency	4 MHz	32.768 kHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	26.4 mA	57.3 µA
Duration	0.1 ms	0.9 ms
DMIPS	213.0	0.0
Ta Max	146.08	149.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	2.69 mA
Battery Life	1 month, 22 days, 3 hours	Average DMIPS	212.5 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
25
20
15
10
5
0
1:RUN
2:STOP1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. IWDG

mode: Activated

7.1.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**256 ***
IWDG window value	**2500 ***
IWDG down-counter reload value	**2500 ***

7.2. LPTIM1

Mode: Counts internal clock events

mode: Waveform Generation

7.2.1. Parameter Settings:

Clock:

Clock Prescaler	**Prescaler Div32 ***

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

Output:

Output Polarity	Output Polarity High

7.3. LPUART1

Mode: Asynchronous

7.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	**115200 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	FIFO mode disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	64
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1 boost

Peripherals Clock Configuration:

Generate the peripherals clock configuration	TRUE

7.5. RTC

mode: Activate Clock Source
mode: Activate Calendar
WakeUp: Internal WakeUp

7.5.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127
Synchronous Predivider value	255

Calendar Time:

Data Format	BCD data format
Hours	0
Minutes	0
Seconds	0
Day Light Saving: value of hour adjustment	**Daylightsaving Add1h ***
Store Operation	Storeoperation Reset

Calendar Date:

Week Day	**Sunday ***
Month	January
Date	1
Year	0

Wake UP:

Wake Up Clock	**1 Hz ***
Wake Up Counter	**10 ***

7.6. SYS

Debug: Serial Wire

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
LPTIM1	PC1	LPTIM1_OUT	Alternate Function Push Pull	No pull-up and no pull-down	Low	
LPUART1	PA2	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA3	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
GPIO	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
RTC wake-up interrupt through EXTI line 20	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/38/39/40/41	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
LPTIM1 global interrupt	unused		
FPU global interrupt	unused		
LPUART1 global interrupt	unused		

8.3.2. NVIC Code generation

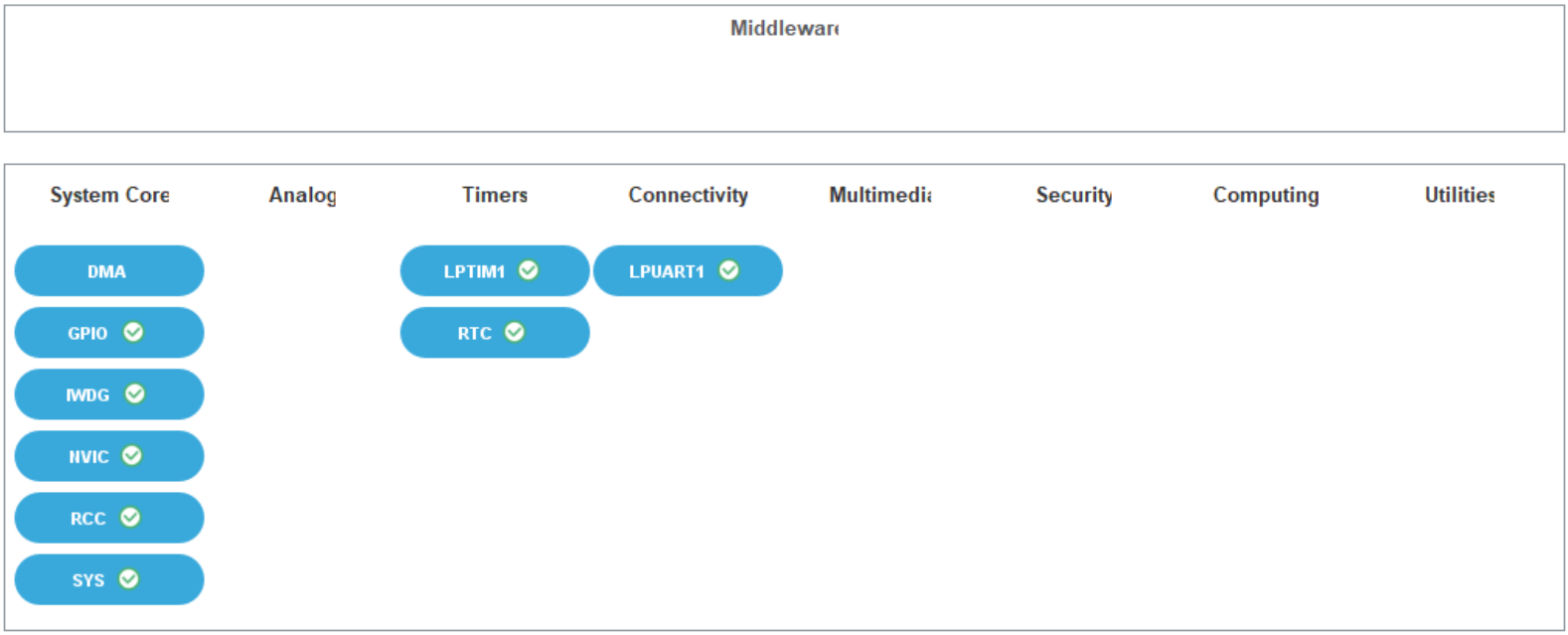
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
RTC wake-up interrupt through EXTI line 20	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link