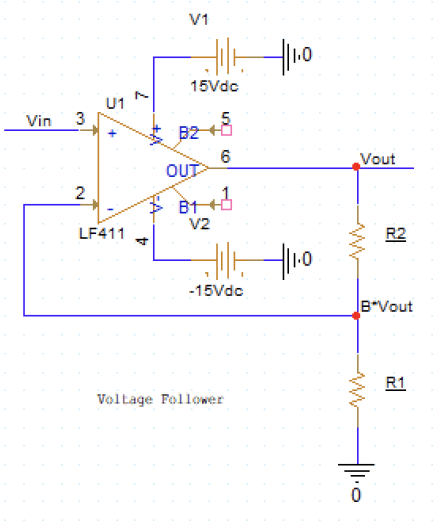
UC San Diego, ECE 100

Lab Project 3: Voltage Follower Circuit

This project aims to study the non-inverting voltage follower circuit when implemented with real op-amps. Ideal op-amps have infinite gain, infinite input impedance, and zero output impedance. In contrast, real op-amps are very complex, usually consisting of 10s of transistors and many passive elements. Despite this complexity, a first-order VCVS model captures much of the important behavior of a real op-amp. In this model, we define the gain as $A(s) = \frac{2\pi G}{S}$ where G is the unity-gain bandwidth. It is usually greater than 1 MHz, sometimes as high as 1 GHz. The input impedance is $R_i > 1M\Omega$, and the output impedance is $R_o < 100\Omega$.

Analysis

1. **Voltage Follower - Unloaded:** The normal follower-with-gain circuit is shown below. Here, we assume that $R_o \ll (R1 + R2)$ and $R_i \gg R1||R2$, where R_o and R_i are the output and input impedances of the op-amp, and $R1$ and $R2$ are the resistors in the feedback network. The assumptions will be valid if $R2$ and $R1$ are of the order of $10k\Omega$.



   (a) Derive rationalized polynomial expression for $A_{cl}(s)$, $Z_{IN}(s)$, $Z_{OUT}(s)$ in terms of G(Hz), B, R_i, R_o. Hint: Use $A(s) = \frac{2\pi G}{s}$.

(b) Show that $A_{cl}(s)$ is the transfer function of a low-pass filter with a dc gain of $\frac{1}{B}$ and a –3dB bandwidth of $G \times B$. Therefore, the product of the dc gain and the bandwidth is $\frac{1}{B} \times G \times B = G$. This is the origin of the useful rule "the gain-bandwidth product of a feedback amplifier is constant." One must remember that this "rule" only applies to the first-order model of the op-amp.

(c) Show that $Z_{IN}(s)$ can be modeled as a capacitor in series with R_i. So even when A is large, Z_{IN} is not resistive; it is capacitive.

(d) Show that Z_{OUT} can be modeled as an inductor in parallel with R_o. So even when A is large, Z_{OUT} is not resistive but inductive.

2. **Voltage Follower with Capacitive Load:** These results do not preclude the voltage follower from being used as a buffer but suggest that it may behave unexpectedly. For example, when loaded with a large capacitance, the buffer may behave like a resonant circuit rather than the ideal voltage source that one might have expected.

(a) Write the circuit's transfer function (closed-loop gain) when a capacitor C_L is connected from the output to ground. Here R_0 and C_L act like a low-pass filter. Put your expression in the general form. You will find that the denominator of the transfer function $(\frac{V_{out}(s)}{V_{in}(s)})$ looks exactly like an RLC resonant circuit. Find ω_0 and ζ in terms of G, B, and R_oC_L.

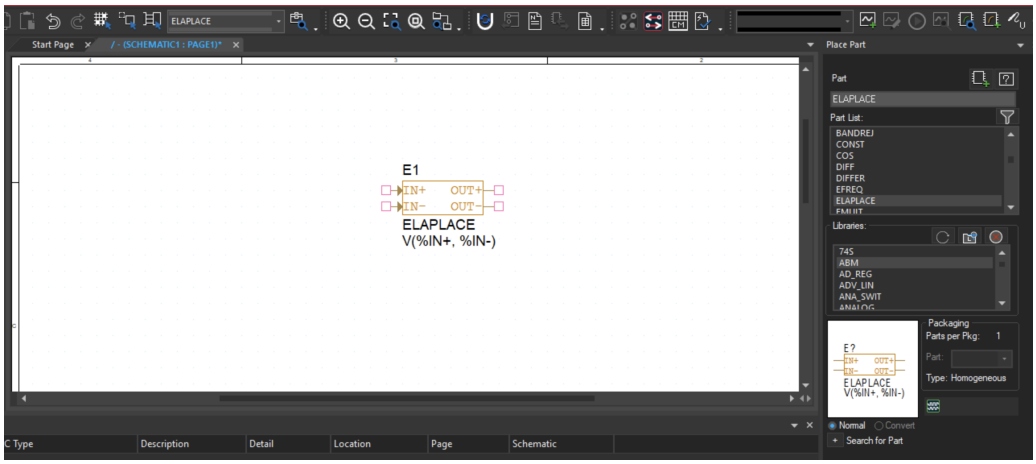
(b) If the C_L is large, for example, if the buffer is driving a long coaxial cable run, the damping factor can be quite small, and the step response will show a great deal of "ringing." This is a common problem in both analog and digital integrated circuits. In large-scale digital systems, it can occur in the buffers which drive the system clock to the various logic components. It can be reduced or eliminated by placing a "compensation" resistor R_C in series with C_L. The output will still be taken across C_L. Find the transfer function $(\frac{V_{out}(s)}{V_{in}(s)})$ of the modified circuit. Furthermore, show that ζ can be adjusted by choosing R_C without significantly changing the bandwidth ω_0.

Simulations

1. **Unloaded Gain-Bandwidth Product:**

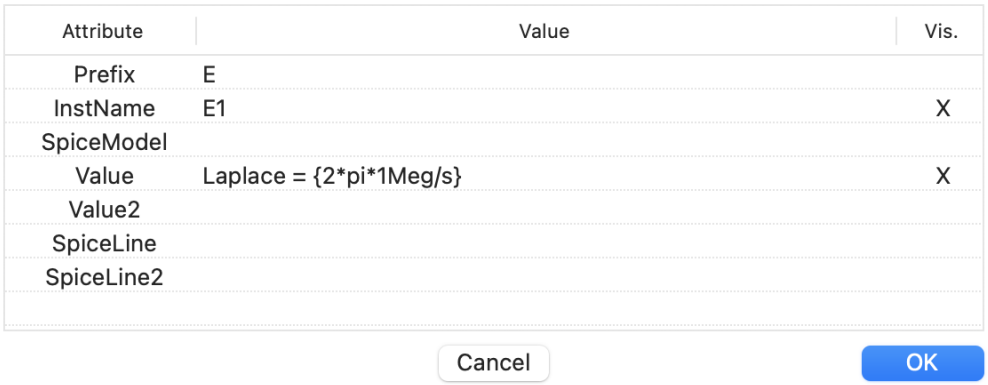
   (a) Simulate a voltage follower with a dc gain of 1, 3, 10, 30, and 100. Instead of an op-amp, use a VCVS with an open-loop gain $A(s) = \frac{2\pi G}{s}$, where $G = 10^6 Hz$. Measure the –3dB bandwidth in each case. Confirm that the Gain-Bandwidth product is constant. You can do all the simulations simultaneously using the Parameter property and a Parameter Sweep. Add a Parameter box to your schematic. Enter a parameter called "r" and give it a value of 1k. Then set R2 = 10k and R1 = {r}. In the analysis setup menu, add a Parameter Sweep with a value list. Enter the values of R1 required to give the gains listed above. PSpice will then do an AC Sweep for each value of r in the list and overlay them all. Make a copy of the plot and your schematic. You can measure the –3dB frequency manually with the cursor.

   Note1: In PSpice, use the ELAPLACE part as a model for a VCVS with a transfer function specified by A(s). The part is in PSpice\ABM library. Ground the terminal labeled OUT-.



   Note2: For the ELAPLACE component setup, add A(s) in the component parameter called XFORM. Use π to indicate pi and prefix Meg to indicate 10^6.

Note3: In LTspice, use a part named "e" for a VCVS. Apply the following edits.



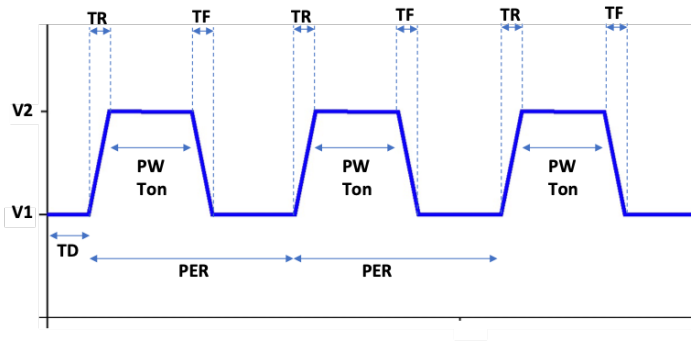
(b) Repeat the simulation for a voltage follower with a gain of 1, 3, 10, 30, and 100 using an LF411 op-amp. Remember to connect the power supplies. Note that the –3dB bandwidth is defined with respect to the dc gain, not the maximum gain. Make a copy of the plot. You will see that the gain-bandwidth product is constant for the higher gains but increases near unity gain. In fact, the LF411 op-amp has several poles and a right half-plane zero. The phase lag due to these high-frequency "features" causes the gain-bandwidth product to change. They also have other interesting effects - they can make the follower oscillate under certain conditions.

2. **Effect of Capacitive Load:** We can test this with a unity-gain follower.

(a) Use the LF411 op-amp in the unity gain voltage follower configuration to simulate the step response for load capacitances of 100pF, 300pF, 1nF, 2nF, 4nF, 6nF, and 10nF. Use the PARAM feature to get PSpice to run the entire list simultaneously and overlay the plots. A time range of 0 to $2\mu s$ should be sufficient. Make a copy of the plot. You will see that loads larger than 100pF can cause a lot of ringing. The typical capacitance of a coaxial cable is 30pF/ft. So, it is easy to get a lot of ringing driving a cable incautiously.

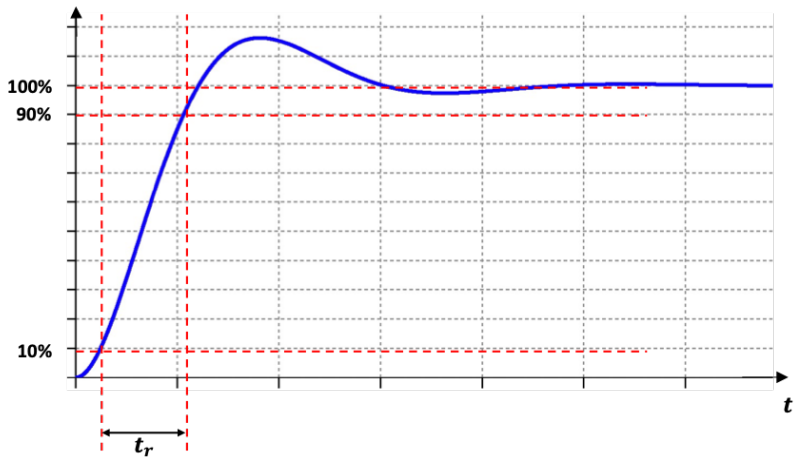
Note: Refer to the image below of the pulse waveform to understand the parameters.

(b) Put a 25Ω resistor in series with the load capacitance and rerun the simulation. Make a copy of this plot. You will see that it clearly mitigates the overshoot. In practice, you would adjust the compensation resistor to be as small as possible, consistent with the desired overshoot, because larger resistors will cause a slower rise time. Generally,



you would like the shortest feasible rise time. What is the smallest resistor to keep the overshoot $< 11\%$ for all loads?

(c) In a practical situation, you would have a certain load capacitance, say 3 nF, and you would want to compensate it to get the shortest rise-time consistent with some maximum overshoot, say 15%. Connect a 3 nF load and optimize the compensation resistor. What resistor works best? What was the optimal 10% to 90% rise time? Make a plot of the optimized step response.



Measurement:

1. **Unloaded Gain-Bandwidth Product:** In this section, you will measure the gain bandwidth product of the follower under the same conditions as the simulation in Part 1-(b). The measurements will require some care, and the circuit must be laid out neatly because the bandwidth is large. Bypass both dc supplies to the ground with a $0.1\mu F$ capacitor close to the chip. Special care is needed for the feedback when $B = 1$. You will not be able to use $R2 = 10K$ and $R1 =$ some large value because the capacitance on the breadboard is about 6 pF to ground and will cause enough phase shift to greatly increase the ringing (or even make it oscillate). **Set $R2 =$ short circuit and $R1 =$ open circuit instead**. The exact values of the gain are unimportant – use the closest convenient resistors.

   First, check the calibration of your scope probes and adjust them if necessary. The 10X probe setting must match the oscilloscope setting. It will be necessary to respect the "slew-rate limit." For the LF411 this is about 10 $\frac{v}{\mu s}$. This means that $|\frac{dV_o}{dt}| < 10\frac{v}{\mu s}$. If $v_o(t) = A\sin(2\pi ft)$ then $\frac{dv_o}{dt} = 2\pi fA\cos(2\pi ft)$. So we need $A < \frac{10^7}{2\pi f}$ or slew rate limiting will occur and mess up our measurements, e.g. at $f = 1Mhz$ the peak-to-peak $v_o < 3.18V$. If the gain = 100, the input voltage will be only $31.8mV$. This is low to measure or trigger from, and you may need to trigger from the output and use averaging to reduce the noise on the input. Using the 10X probe setting on the output will be necessary because the 1X probe has considerable capacitance. You can use the 1X probe setting on the input, though. Measure the gain-bandwidth product for each case you simulated in Simulation 1-(b). Remember that –$3dB$ is with respect to the dc gain, not the maximum gain.

   - Take a picture of your circuit setup and include it in your report.
   - For two of the gain values (select yourself), save the oscilloscope input and output voltage traces at the -3dB frequency. Ensure the peak-to-peak voltage amplitudes for channels 1 and 2 are shown on the oscilloscope screen.
   - In your report, explain how you found the –$3dB$ point or the bandwidth through your measurements.
   - Tabulate your measurement results.

2. **Capacitive Load:** In this section, you will measure the effect of a capacitive load on a unity-gain follower, as simulated in Simulation Part 2. The same precautions against slew rate

limiting apply. The input step must be $\ll 1V$, and you must use the $10X$ probe setting on the output. You might as well use it on both because both signals will be about the same amplitude. Remember to use $R2$ = short circuit and $R1$ = open circuit or you will see too much overshoot caused by the breadboard.

(a) Measure the overshoot for (roughly) the same capacitances that you used in the simulation. Here the exact values are not important. You may find that the follower actually oscillates with some values of CL. If it does oscillate, the amplitude will be limited by the slew rate, so you won't necessarily see a large signal. What you might see is a ringing that never dies away. If this happens, make a hard copy for your report.

(b) In a practical situation, you would have a certain load capacitance, say $3nF$, and you would want to compensate it to get the shortest rise-time consistent with some maximum overshoot, say 11%. Connect a $3nF$ load and optimize the compensation resistor. What resistor works best? What was the optimal 10% to 90% rise time?

- Tabulate your measurement results.
- Take a picture of your circuit setup with the optimized compensation resistor and the $3nF$ load capacitor and include it in your report.
- Save the oscilloscope trace of the optimized step response. Your report should include two pictures with the measurements of the overshoot and rise time using oscilloscope cursors.

Report:

Make sure to include the following in your lab report:

- Hand calculations from **Analysis** 1a-d
- Hand calculations for **Analysis** 2a-b
- -3dB points for **Simulations** in part 1a
- Plots of the simulation with ELAPLACE and with the LF411 op-amp for varying DC gains. (**Simulation** 1a-b)
- Plots of the simulation for the circuit with varying capacitive loads with and without a compensating resistor (**Simulation** 2a-b)

- Plot of the step response to the optimal resistor and the optimal resistor value (**Simulation** 2c)
- Experimental results, the requested oscilloscope traces, and circuit setups

This list is not all-encompassing, check with your TAs, but it serves as a helpful checklist.