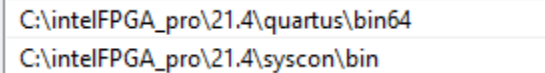


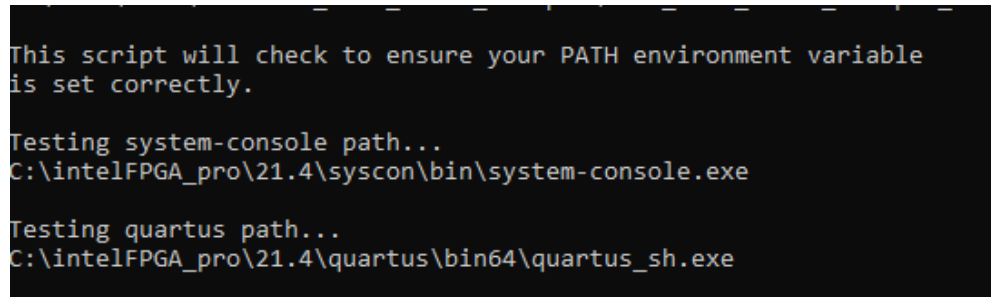
Tcl Read Write Example Instructions

1. Edit Windows PATH environment variable.
 - a. Open the Start Search, type in "env", and choose "Edit the system environment variables":
 - b. Click the "Environment Variables..." button near the bottom.
 - c. In the "User variables for <user>" frame highlight "Path" and then press "Edit..."
 - d. Use the "New" or "Edit" button to ensure the following paths have been added.



```
C:\intelFPGA_pro\21.4\quartus\bin64
C:\intelFPGA_pro\21.4\syscon\bin
```

2. Verify correctness of PATH environment variable
 - a. Double click the open_cmd_prompt.bat file to open a Windows Command Prompt in the present working directory.
 - b. From the Windows Command Prompt run path_env_check.bat. The output should look something like the following:

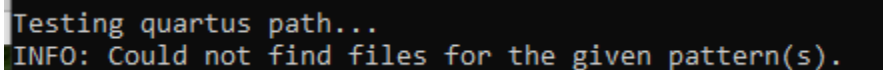


```
This script will check to ensure your PATH environment variable
is set correctly.

Testing system-console path...
C:\intelFPGA_pro\21.4\syscon\bin\system-console.exe

Testing quartus path...
C:\intelFPGA_pro\21.4\quartus\bin64\quartus_sh.exe
```

If you see a "Could not find files..." message you will need to correct your PATH environment variable prior to proceeding.








```
Testing quartus path...
INFO: Could not find files for the given pattern(s).
```

3. Unzip JTAG_Read_Write_Example_TCL.zip file
 - a. Below is a description of the files included in the JTAG_Read_Write_Example_TCL directory.

Filename	Description
cleanup.bat	Removes all restored and generated files.
compile_design.bat	Compiles the FPGA from a Windows Prompt.
JTAG_Read_Write_Example_Guide.pdf	Descriptions and instructions for the example design.
open_cmd_prompt.bat	Opens a Windows Command Prompt in the present working directory.
path_env_check.bat	Windows batch file to help check correctness of PATH environment variable.
program_fpga.bat	Windows batch file script to run the program_fpga.tcl and toggle_issp.tcl scripts from a Windows Prompt.
program_fpga.tcl	Tcl script to assist in the programming of the FPGA.
read_write_example.tcl	Software application file written in tcl.
restore_qar.bat	Windows batch file script to restore the Quartus project from the Quartus archive (.qar file)
run_app.bat	Windows batch file script to run the read_write_example.tcl application.
toggle_issp.tcl	Tcl script to toggle the internal reset register using In System Sources and Probes (ISSP).
top_21_4_0_67.qar	Quartus project archive file, including Platform Designer system and Verilog files.

4. Restore and View Quartus project

- a. From the command line type “restore_qar.bat”
- b. Open the Quartus project and the Platform Designer system (sys.qsys). The system consists of the following:
 - i. Clock and reset inputs
 - ii. Jtag2avalon_bridge - Used to provide a bridge between jtag and an Avalon Memory Mapped interface. Allowing Tcl API commands to communicate with agent/slave devices on the Avalon bus.
 - iii. pio_8bit - 8-bit Parallel I/O. Only bit 0 is used and connected to an LED on a development board. The application code blinks this LED.
 - iv. ram_32bit - 32-bit slave RAM connected to the Nios V CPU. The application code demonstrates how to read and write to this RAM.

Use	Co...	Name	Description
<input checked="" type="checkbox"/>		 clock_in	Clock Bridge Intel FPGA IP
<input checked="" type="checkbox"/>		 reset_in	Reset Bridge Intel FPGA IP
<input checked="" type="checkbox"/>		 jtag2avalon_bridge	JTAG to Avalon Master Bridge Intel FPGA IP
<input checked="" type="checkbox"/>		 ram_32bit	On-Chip Memory (RAM or ROM) Intel FPGA IP
<input checked="" type="checkbox"/>		 pio_8bit	PIO (Parallel I/O) Intel FPGA IP

5. Compile Project

- The project is currently targeted towards an Arria 10 development board. You will need to change the target to match your board and update the location of the "clk" and "led" pins to match your board. Connecting the "led" signal to an actual LED on a development board is optional, and only necessary if it is desirable to see the LED blink.
- You can compile the FPGA from within Quartus or from the command line by running the compile_design.bat file.

6. Program the FPGA

- Connect your computer to your board and run the "program_fpga.bat" from the command line. This script will program the FPGA and toggle the built-in reset register (using In System Sources and Probes).

7. Run the software application

- From the command line run the "run_app.bat" script. You should see the following output. Your selected LED on your development board should also be blinking.

```

Opening JTAG master service path...
I found the following masters:
0. /devices/10AT115S(1|2)@1#USB-1/(link)/JTAG/(110:132 v1 #0)/phy_0/master
1. /devices/5M(1270ZF324|2210Z)|EPM2210@2#USB-1/(link)/JTAG/(110:130 v3 #0)/jtagmem_0
Opening master: /devices/10AT115S(1|2)@1#USB-1/(link)/JTAG/(110:132 v1 #0)/phy_0/master

Read 0x01234567 at address 0x00000100
Read 0x89abcdef at address 0x00000104
Read 0x00 at address 0x00000000
Write a 0x1 to 0x00000000
Read 0x01 at address 0x00000000

Blinking LED for 10 seconds

```