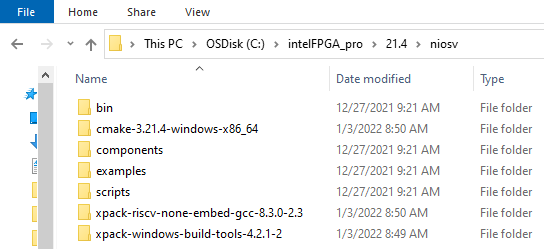
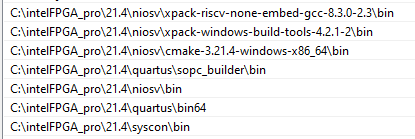
Nios V Read Write Example Instructions

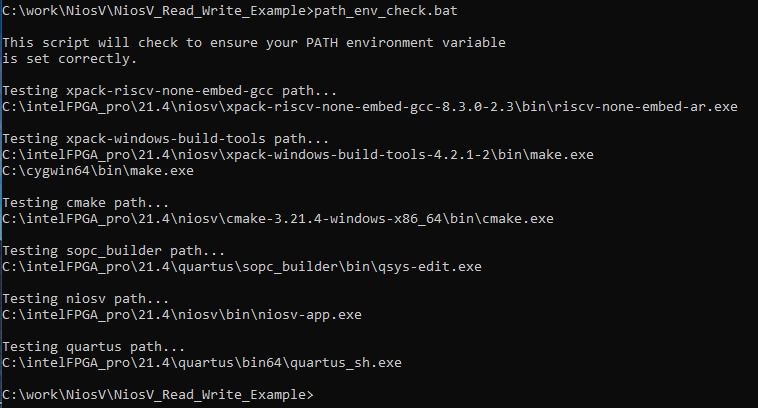
1. Quartus Prime Pro version 21.3 or newer is required for Nios V
2. Install required software
   1. GNU RISC-V Embedded GCC
      1. <https://github.com/xpack-dev-tools/riscv-none-embed-gcc-xpack/releases/tag/v8.3.0-2.3>
      2. Download file: [xpack-riscv-none-embed-gcc-8.3.0-2.3-win32-x64.zip](https://github.com/xpack-dev-tools/riscv-none-embed-gcc-xpack/releases/download/v8.3.0-2.3/xpack-riscv-none-embed-gcc-8.3.0-2.3-win32-x64.zip)
      3. Extract file in Quartus install directory
         1. C:\intelFPGA\_pro\21.4\niosv
   2. CMake packages for binary distributes
      1. <https://cmake.org/download/>
      2. Download file: [cmake-3.21.4-windows-x86\_64.zip](https://github.com/Kitware/CMake/releases/download/v3.21.4/cmake-3.21.4-windows-x86_64.zip)
      3. Extract file in Quartus install directory
         1. C:\intelFPGA\_pro\21.4\niosv
   3. xPack Windows Build Tools
      1. <https://github.com/xpack-dev-tools/windows-build-tools-xpack/releases/>
      2. Download file: [xpack-windows-build-tools-4.2.1-2-win32-x64.zip](https://github.com/xpack-dev-tools/windows-build-tools-xpack/releases/download/v4.2.1-2/xpack-windows-build-tools-4.2.1-2-win32-x64.zip)
      3. Extract file in Quartus install directory
         1. C:\intelFPGA\_pro\21.4\niosv
   4. Upon completion of steps a-c your niosv/ directory should look like the following.



1. Edit Windows PATH environment variable.
   1. Open the Start Search, type in “env”, and choose “Edit the system environment variables”:
   2. Click the “Environment Variables…” button near the bottom.
   3. In the “User variables for <user>” frame highlight “Path” and then press “Edit...”
   4. Use the “New” or “Edit” button to ensure the following paths have been added.



1. Verify correctness of PATH environment variable
   1. Double click the open\_cmd\_prompt.bat file to open a Windows Command Prompt in the present working directory.
   2. From the Windows Command Prompt run path\_env\_check.bat. The output should look something like the following:



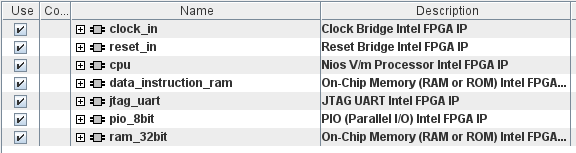
If you see a “Could not find files...” message you will need to correct your PATH environment variable prior to proceeding.



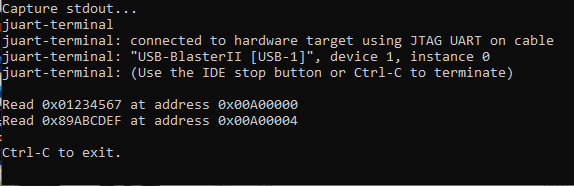
1. Unzip NiosV\_Read\_Write\_Example Design.zip file
   1. Below is a description of the files included in the NiosV\_Read\_Write\_Example\_C directory.

|  |  |
| --- | --- |
| **Filename** | **Description** |
| Makefile | Makefile to build and manage FPGA and software application projects. |
| NiosV\_Read\_Write\_Example\_Guilde.pdf | This document. |
| open\_cmd\_prompt.bat | Opens a Windows Command Prompt in the present working directory. |
| path\_env\_check.bat | Window batch file to help check correctness of PATH environment variable. |
| program\_fpga.tcl | Tcl script to assist in the programming of the FPGA. |
| read\_write\_example.c | Software application file written in C. |
| toggle\_issp.tcl | Tcl script to toggle the internal reset register using In System Sources and Probes (ISSP). |
| top\_21\_4\_0\_67.qar | Quartus project archive file. Including Platform Designer system and top-level System Verilog file. |

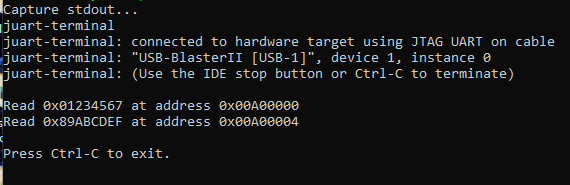
1. Restore and View Quartus project
   1. From the command line type “make restore”
   2. Open the Quartus project and the Platform Designer system (sys.qsys). The system consists of the following:
      1. Clock and reset inputs
      2. Nios V CPU
      3. data\_instruction\_ram - This RAM is used to hold the application code which the Nios V CPU will execute. During FPGA compilation the ./data\_instruction\_ram.hex file is located into this RAM.
      4. jtag\_uart - Used to capture STDIO from our application code.
      5. pio\_8bit - 8-bit Parallel I/O. Only bit 0 is used and connected to an LED on a development board. The application code blinks this LED.
      6. ram\_32bit - 32-bit slave RAM connected to the Nios V CPU. The application code demonstrates how to read and write to this RAM.



1. Compile Project
   1. The project is currently targeted towards an Arria 10 development board. You will need to change the target to match your board and update the location of the “clk” pin to match your board.
   2. To compile the FPGA, from the command line run “make fpga”. This will:
      1. Generate the Board Support Package
      2. Generate the software application (create the data\_instruction\_ram.hex file)
      3. Compile the FPGA
2. Program the FPGA
   1. Connect your computer to your board and run “make program” from the command line. This script will program the FPGA, toggle the built-in reset register (using In System Sources and Probes) and start the UART terminal. You should see the following output.



1. Update Application Code Without Recompiling the FPGA
   1. Open the read\_write\_example.c file and change the last printf statement to include the word “Press”:
      1. printf("\nPress Ctrl-C to exit.\n");
   2. Run “make app”. This script will regenerate the application code, creating an updated .elf file.
   3. run “make update”. The .elf file will be downloaded to the FPGA. The built-in reset register will be toggled, and the application code will execute. You should see the following output.



1. Application Code
   1. The application file read\_write\_example.c includes io.h. The io.h library provides the IOWR and IORD functions used to read and write the slave/agent RAMs attached to the Nios V.
   2. The included ./software/cpu\_hal\_bsb/system.h file is generated as part of the board support package. This file defines parameters associated with the components in the Platform Designer system including the base address location of the slave/agent RAM and PIO block which are used in the read\_write\_example.c file.