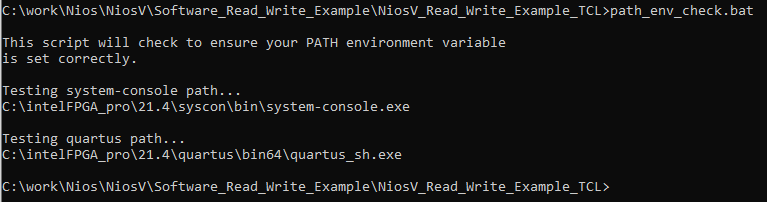
Nios V Read Write Example Instructions

1. Edit Windows PATH environment variable.
   1. Open the Start Search, type in “env”, and choose “Edit the system environment variables”:
   2. Click the “Environment Variables…” button near the bottom.
   3. In the “User variables for <user>” frame highlight “Path” and then press “Edit...”
   4. Use the “New” or “Edit” button to ensure the following paths have been added.



1. Verify correctness of PATH environment variable
   1. Double click the open\_cmd\_prompt.bat file to open a Windows Command Prompt in the present working directory.
   2. From the Windows Command Prompt run path\_env\_check.bat. The output should look something like the following:



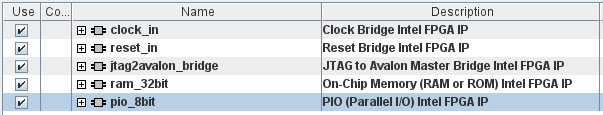
If you see a “Could not find files...” message you will need to correct your PATH environment variable prior to proceeding.



1. Unzip NiosV\_Read\_Write\_Example Design.zip file
   1. Below is a description of the files included in the NiosV\_Read\_Write\_Example\_TCL directory.

|  |  |
| --- | --- |
| **Filename** | **Description** |
| cleanup.bat | Removes all restored and generated files. |
| compile\_design.bat | Compiles the FPGA from a Windows Prompt. |
| NiosV\_Read\_Write\_Example\_Guilde.pdf | Descriptions and instructions for the example design. |
| open\_cmd\_prompt.bat | Opens a Windows Command Prompt in the present working directory. |
| path\_env\_check.bat | Windows batch file to help check correctness of PATH environment variable. |
| program\_fpga.bat | Windows batch file script to run the program\_fpga.tcl and toggle\_issp.tcl scripts from a Windows Prompt. |
| program\_fpga.tcl | Tcl script to assist in the programming of the FPGA. |
| read\_write\_example.tcl | Software application file written in tcl. |
| restore\_qar.bat | Windows batch file script to restore the Quartus project from the Quartus archive (.qar file) |
| run\_app.bat | Windows batch file script to run the read\_write\_example.tcl application. |
| toggle\_issp.tcl | Tcl script to toggle the internal reset register using In System Sources and Probes (ISSP). |
| top\_21\_4\_0\_67.qar | Quartus project archive file, including Platform Designer system and Verilog files. |

1. Restore and View Quartus project
   1. From the command line type “restore\_qar.bat”
   2. Open the Quartus project and the Platform Designer system (sys.qsys). The system consists of the following:
      1. Clock and reset inputs
      2. Jtag2avalon\_bridge - Used to provide a bridge between jtag and an Avalon Memory Mapped interface. Allowing Tcl API commands to communicate with agent/slave devices on the Avalon bus.
      3. pio\_8bit - 8-bit Parallel I/O. Only bit 0 is used and connected to an LED on a development board. The application code blinks this LED.
      4. ram\_32bit - 32-bit slave RAM connected to the Nios V CPU. The application code demonstrates how to read and write to this RAM.



1. Compile Project
   1. The project is currently targeted towards an Arria 10 development board. You will need to change the target to match your board and update the location of the “clk” and “led” pins to match your board. Optionally you can pin out the “led” pin to match your board in order to view the blinking LED.
   2. You can compile the FPGA from within Quartus or from the command line by running the compile\_design.bat file.
2. Program the FPGA
   1. Connect your computer to your board and run the “program\_fpga.bat” from the command line. This script will program the FPGA and toggle the built-in reset register (using In System Sources and Probes).
3. Run the software application
   1. From the command line run the “run\_app.bat” script. You should see the following output. Your selected LED on your development board should also be blinking.

