# READ：

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| reg. No. | variable | | function | fsmc\_add | number | Is used |
| 0 | CHA\_RUN\_REG | | 当前操作的那个通道 | 0 | 1 | N |
| 1 | CHA\_STA\_REG | | 通道状态存器 | 1 | =CN | Y |
| 2 | DAT\_LEN\_H | | 通道数据长度寄存器高字节 | 2 | =CN | Y |
| 3 | DAT\_LEN\_L | | 通道数据长度寄存器低字节 | 3 | =CN | Y |
| 4 | DAT\_MAX\_REG | | 上次采集的**峰值** | 4 | =CN | N |
| 5 | DAT\_AVR\_REG | | 上次采集的**均值** | 5 | =CN | N |
| 6 | SYN\_FRE\_REG | | 同步频率(同步方波频率) | 6 | =CN | N |
| 7 | CHA\_DAT\_ITR | | 读数据接口 | 7 | =CN | N |
| 8 | dw\_data\_start\_time[31:16] | | 局放原始波形开采时间-高位 | 8 |  |  |
| 9 | dw\_data\_start\_time[15:0] | | 局放原始波形开采时间-低位 | 9 |  |  |
| 10 | one\_second\_clk\_cnt[31:16] | | 1S时间的时钟计数的高16bit | 10 |  |  |
| 11 | one\_second\_clk\_cnt[15:0] | | 1S时间的时钟计数的低16bit | 11 |  |  |
| 12 | dw\_data\_start\_ utc [31:16] | | 局放原始波形时间高16bit |  |  |  |
| 13 | dw\_data\_start\_ utc [15:0] | | 局放原始波形时间低16bit |  |  |  |
| 14 | fpga\_version | | FPGA版本信息16bit\*32 |  |  |  |
| 15 | fpga\_ctrl0 | | Bit0来控制高频局放原始波形的产生机制  Bit1控制PRPD图的产生使能 |  |  |  |
|  |  | |  |  |  |  |
|  | | Channel number=CN | | | | |

Reg0: CHA\_RUN\_REG (16Bit) 显示操作那个通道【FPGA内部只有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| function | borad reset | Read begin | Run9 | Run8 | Run7 | Run6 | Run5 | Run4 | Channel code | | | | | | | |
|  |  | en |  | | | | | |  | | | | | | | |
|  |  | en | Channel Sample control bit | | | | | | Channel code | | | | | | | |

Bit0-bit7:通道译码

Bit8-bit13:RUN0-RUN9,ARM往该位写1命令0通道开始采集，FPGA开始采集后自动将该位清0。

Bit14:读数据前清零各寄存器标识位。

Bit15:BR:（Board\_Reset）B15:板级复位，ARM将该为写为1 则FPGA输出复位信号复位ARM和以太网芯片。

Reg1：CHA\_STA\_REG（16Bit）通道状态寄存器【FPGA内部针对每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| CRA\_NUM | | | | | | | | | | | |  | IDLE | INT | OVER |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 保留 | | | | | | | | | | | |  |  | 1/0 | 1/0 |

OVER:Bit0,表示上次ARM要求采集的数据是否采集完毕，新开启一次采集自动清除。

INT:Bit1,表示该通道是否处于中断状态，由ARM在中断服务程序中写寄存器清除。

IDLE:Bit2为1表示该通道处于空闲状态，可以进行下一次采集

CRA\_NUM:B15~B4:总的放电次数，如果放电次数不为0，则说明FPGA有记录放电的原始波形，单片机可以先通过写CHA\_RUN\_REG的bit0~bit4选择对应的通道，再配置SAM\_CTR\_REG的bit3,bit2写为2’b10来控制读模式，读取该通道缓存的AD原始波形。

Reg2：DAT\_LEN\_H (16Bit)通道数据长度寄存器高字节【FPGA内部针对每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| DAT\_LEN\_HIGH:数据长度高字节 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 该版本硬件缓存只有8M字节，所以数据长度高字节最大为0x80,后续版本可能突破该限制。 | | | | | | | | | | | | | | | |

Reg3：DAT\_LEN\_L (16Bit)通道数据长度寄存器低字节【FPGA内部针对每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| DAT\_LEN\_LOW:数据长度低字节 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| AD分辨率12Bit，每次最少存2个字节，所以B0应该永远为0。 | | | | | | | | | | | | | | | |

Reg4：DAT\_MAX\_REG（16Bit）上次采集的峰值(峰-峰值的峰值) 【FPGA内部针对每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| DAT\_MAX: 上次采集的峰值 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 该版本硬件AD分辨率最高为14位，所以B14、B15应该永远为0 | | | | | | | | | | | | | | | |

Reg5：DAT\_AVR\_REG（16Bit）上次采集的均值(峰-峰值的均值) 【FPGA内部针对每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| DAT\_MAX: 上次采集的均值 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 该版本硬件AD分辨率最高为14位，所以B14、B15应该永远为0 | | | | | | | | | | | | | | | |

Reg6：SYN\_FRE\_REG（16Bit）同步频率(同步方波频率) 及读取dataflash接口

|  |  |
| --- | --- |
| 同步方波频率：至于用外同步还是内同步由上层单片机控制 | |
| B15 | B14---B0 |
| input\_data\_from\_m25p64 | 同步方波频率，最小分辨率1HZ |
| 来之dataflash ST25V64的数据输出状态 |  |

Reg7: CHA\_DAT\_ITR（16Bit）读数据接口【FPGA内部针对每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读某个通道存放在FPGA外挂SDRAM中的数据 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Addition--------------------------------------------------------------------------------------------------------

Reg8: （16Bit） dw\_data\_start\_time[31:16]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读局放原始波形距离秒脉冲的时钟计数的高16bit | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg9: （16Bit） dw\_data\_start\_time[15:0]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读局放原始波形距离秒脉冲的时钟计数的低16bit | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg10: （16Bit） one\_second\_clk\_cnt[31:16]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读本机对1S时间的时钟计数的高16bit | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg11: （16Bit） one\_second\_clk\_cnt[15:0]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读本机对1S时间的时钟计数的低16bit | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg12: （16Bit） dw\_data\_start\_ utc [31:16]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读取局放原始波形时间高16bit | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg13: （16Bit） dw\_data\_start\_ utc [15:0]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该接口读取局放原始波形时间低16bit | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg14: （16Bit） fpga\_version

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 读数据接口：ARM通过该寄存器读取fpga程序版本，单片机连续读该寄存器32次，读到32个16bit数据，得到完整fpga程序版本信息 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

Reg15: (16Bit) fpga\_ctrl0

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 单片机通过写该寄存器的Bit0来控制高频局放原始波形的产生机制，和控制PRPD图的产生使能 | | | | | | | |
| B15 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 保留 |  |  |  |  | 1/0（默认为0） | 1/0（默认为1） | 1/0（默认为0） |

Bit0=0;FPGA工作在捕获模式，捕获到越限或变化率越限保存原始波形。

Bit0=1; FPGA工作在采集模式，FPGA在收到采集命令(reg8的bit0为1)则无条件采集一段局放原始波形。

Bit1=1;FPGA自动产生PRPD图使能。

Bit1=0; FPGA自动产生PRPD图关闭。

Bit2=0: 取峰值

Bit2=1: 取积分

Bit3-Bit6: 选择频带滤波器

# WRITE：

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| reg. No. | variable | function | Fsmc\_addr | Num. | used |
| 0 | CHA\_RUN\_REG | 决定操作那个通道 | 0000 | 1 | Y |
| 1 | DAT\_THR\_REG | 通道门限 |  | CN | Y |
| 2 | SAM\_CYC\_REG | 采集周期数 |  | CN | N |
| 3 | SAM\_CTR\_REG | 控制寄存器设置（噪声通道） |  | 1 | N |
| 4 | ONE\_PHA\_DATNUM\_REG | 设置一个相位对应多少个ＡＤ数据 |  | CN | N |
| 5 | AD\_BPS\_REG | 保留 |  |  | N |
| 6 | CHANGE\_RATE\_THR | 通道变化率门限 |  | CN | Y |
| 7 | RESET\_INT\_REG | 清中断标志 | 0111 |  |  |
| 8 | START\_SAMPLE\_REG |  | 1000 |  |  |
| 9 | write\_m25p64\_reg | conflict |  |  |  |
| 10 | FILTER\_START\_REQUENCY | 设置滤波器起始频率 |  |  |  |
| 11 | FILTER\_STOP\_REQUENCY | 设置滤波器结束频率 |  |  |  |
| 12 | utc [31:16] | 将utc时间高16bit写到FPGA |  |  |  |
| 13 | utc [15:0] | 将utc时间低16bit写到FPGA |  |  |  |
| 14 |  |  |  |  |  |
| 15 | fpga\_ctrl0 | Bit0来控制高频局放原始波形的产生机制  Bit1控制PRPD图的产生使能 |  |  |  |
|  |  |  |  |  |  |

Reg0: (16Bit) 决定操作那个通道【FPGA内部只有一个】CHA\_RUN\_REG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 功能 | BR | 开始读操作 | RUN5 | RUN4 | RUN3 | RUN2 | RUN1 | RUN0 | 决定操作那个通道，ARM要写某  个通道寄存器前，  一定要写该寄存器，例如ARM要  读/写通道2的reg2，则先将reg0  写为1，再执行读/  写reg2的操作。 | | | | | | | |
| 位数 | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |

RUN0:B8,ARM往该位写1命令0通道开始采集，FPGA开始采集后自动将该位清0。

RUN9:B13,ARM往该位写1命令9通道开始采集。FPGA开始采集后自动将该位清0。

BR:（Board\_Reset）B15:板级复位，ARM将该为写为1 则FPGA输出复位信号复位ARM和以太网芯片。

Reg1: (16Bit) 通道门限【FPGA内部针对每个通道都有一个】DAT\_THR\_REG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 通道门限，FPGA判决放电的门限。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  | | | | | | | | | | | | | | | |

Reg2: (16Bit) 采集周期数【FPGA内部针对每个通道都有一个】SAM\_CYC\_REG 保留

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 采集周期数，采集多少个周期的数据，周期是输入方波的周期。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  | | | | | | | | | | | | | | | |

Reg3: (16Bit) 指定噪声通道是哪个【FPGA只有一个】

SAM\_CTR\_REG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  | 保留 | | | | | | | | | | | |  |  |  |

Bit15:噪声通道开关：

Bit0-2:译码成6个通道

Reg4: (16Bit) 设置一个相位对应多少个ＡＤ数据【FPGA内部针对每个通道都有一个】ONE\_PHA\_DATNUM\_REG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 多少个AD数据拼为一个相位数据 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Default :10000 | | | | | | | | | | | | | | | |

Reg6: (16Bit) 通道变化率门限【FPGA内部针对每个通道都有一个】CHANGE\_RATE\_THR

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 通道门限，FPGA判决放电的变化率门限。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  | | | | | | | | | | | | | | | |

Reg7: (16Bit) 清中断标志【FPGA只有一个】

RESET\_INT\_REG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 清中断标志。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  | | | | | | | | | | | | | | | |

Reg8: (16Bit) START\_SAMPLE\_REG

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 单片机通过写该寄存器的Bit0为1来命令FPGA开始采集。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  | | | | | | | | | | | | | | | 1 |

Reg9: (16Bit) write\_m25p64\_reg

|  |  |  |  |
| --- | --- | --- | --- |
| 单片机通过写该寄存器的Bit0-Bit2为操作dataflash m25p64。 | | | |
| B15--B3 | B2 | B1 | B0 |
| 保留 | output\_ncso\_to\_m25p64 | output\_dclk\_to\_m25p64 | output\_data\_to\_m25p64 |

Reg10: (16Bit) 滤波器起始频率

FILTER\_START\_REQUENCY

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 写数据接口：ARM向该寄存器写入滤波器的起始频率。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reg11: (16Bit) 滤波器结束频率

FILTER\_STOP\_REQUENCY

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 写数据接口：ARM向该寄存器写入滤波器的结束频率。 | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reg12: （16Bit） utc [31:16]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 写数据接口：ARM向该寄存器写utc时间高16bit到FPGA | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reg13: （16Bit） utc [15:0]

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 写数据接口：ARM通过该寄存器将utc时间低16bit到FPGA | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reg14: （16Bit） 通道增益【每个通道都有一个】

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 写数据接口：ARM通过该寄存器将通道增益设置到FPGA | | | | | | | | | | | | | | | |
| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reg15: (16Bit) fpga\_ctrl0

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 单片机通过写该寄存器的Bit0来控制高频局放原始波形的产生机制，和控制PRPD图的产生使能 | | | | | | | |
| B15 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| 保留 |  |  |  |  | 1/0（默认为0） | 1/0（默认为1） | 1/0（默认为0） |

Bit0=0;FPGA工作在捕获模式，捕获到越限或变化率越限保存原始波形。

Bit0=1; FPGA工作在采集模式，FPGA在收到采集命令(reg8的bit0为1)则无条件采集一段局放原始波形。

Bit1=1;FPGA自动产生PRPD图使能。

Bit1=0; FPGA自动产生PRPD图关闭。

Bit2=0: 取峰值

Bit2=1: 取积分

Bit3-Bit6: 选择频带滤波器

Bit15:

0:外同步：由外部传入同步信号。

1:内同步，FPGA自己产生同步信号。