NIRMA UNIVERSITY

INSTITUTE OF TECHNOLOGY

Innovative Assignment Report

On

"PDP-8 COMPUTER"

B. Tech CSE 2022-23

SEMESTER III

2CS401 Computer Architecture

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PROJECT TITLE:

Logisim Implementation of the CPU of PDP-8 Computer

INTRODUCTION:

The PDP-8 family of minicomputers were built by Digital Equipment Corporation between 1965 and 1990, although it is worth noting that the term minicomputer first came into prominence after the machine was introduced.

By late 1973, the PDP-8 family was the best-selling computer in the world, and it is likely that it was only displaced from this honour by the Apple II (which was displaced by the IBM PC). Most models of the PDP-8 set new records as the least expensive computer on the market at the time of their introduction. The PDP-8 has been described as the model-T of the computer industry because it was the first computer to be mass produced at a cost that just about anyone could afford.

METHODOLOGY FOLLOWED:

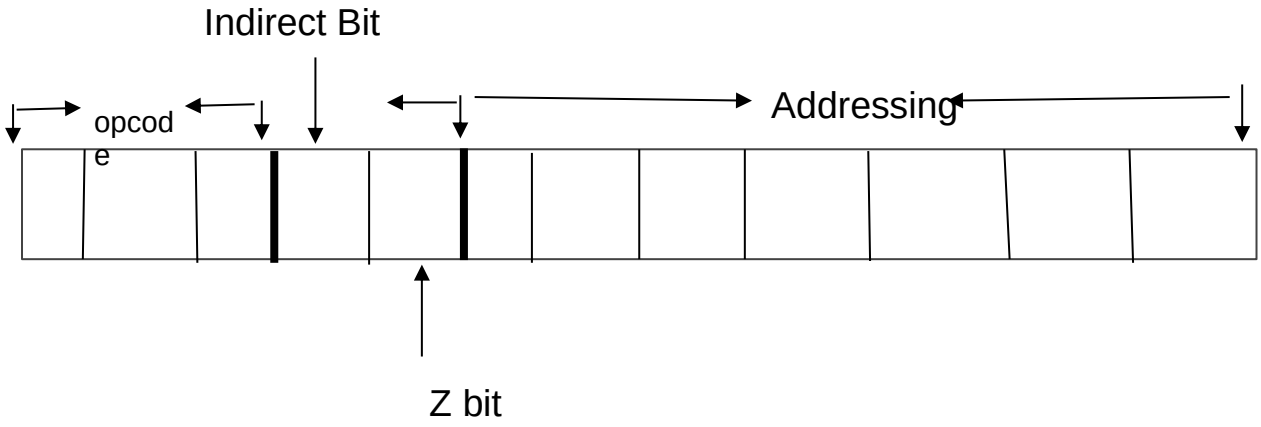
Instruction set:

The original PDP-8 had the word size of 12 bits and the memory size of 4 bits with the following registers:

- PC - the program counter, 12 bits.
- AC - the accumulator, 12 bits.
- L - the link register, 1 bit, commonly prefixed to AC

Instruction words are organized as follows:

The *original PDP-8* computer CPU instructions consists of the following format of the instruction word**.**



op - The Op-code.

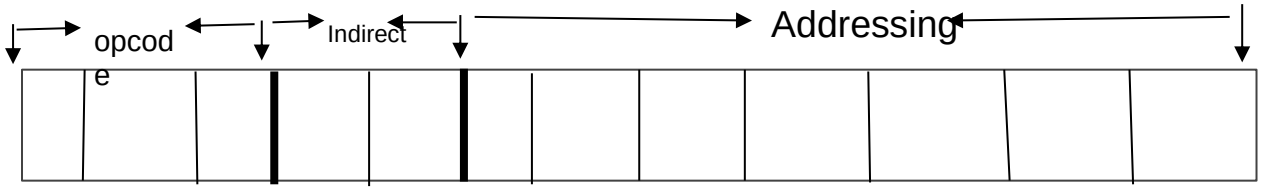
i - The Indirect Bit (0 = direct, 1 = indirect).

z - The Page Bit (0 = page zero, 1 = current page).

addr - The Word in Page.

The PDP-8 Computer CPU *<u>according to our project</u>* has the following structure: -

We decided to modify the original instruction set to have two indirect bits instead of the z bit.



op - The Op-Code (memory/register).

i - The Indirect Bit (00 = direct, 01= immediate,10=register direct,11= indirect).

addr - The Word in Page.

MICRO-INSTRUCTION SET:

This PDP-8 computer instruction set contains a 3 bit op-code. With three bit op-code, there are only eight primary instructions.

The basic instructions are:

- 000 - AND - and operand with AC.
- 001 - TAD - add operand to (a 13 bit value).
- 010 - ISZ - increment operand and skip if result is zero.
- 011 - DCA - deposit AC in memory and clear AC.
- 100 - JMS - jump to subroutine.
- 101 - JMP - jump.
- 110 - IOT - input/output transfer.
- 111 - OPR - microcoded operations.

Further, the OPR instructions i.e., op-code 7 consists of two groups of micro-instruction set. A single bit i.e., the 8th bit distinguishes the group 1 micro-instructions from the group 2 and the remaining eight bits of the word have mostly different functions depending upon which group is selected.

They are the following: -

Group 1

```
|1|1|1|0|_|_|_|_|_|_|_|_|
          1                 - CLA - clear AC
            1               - CLL - clear the L bit
              1             - CMA - ones complement AC
                1           - CML - complement L bit
                      1     - IAC - increment
                  1 0 0     - RAR - rotate  right
                  0 1 0     - RAL - rotate  left
                  1 0 1     - RTR - rotate  right twice
                  0 1 1     - RTL - rotate  left twice
```

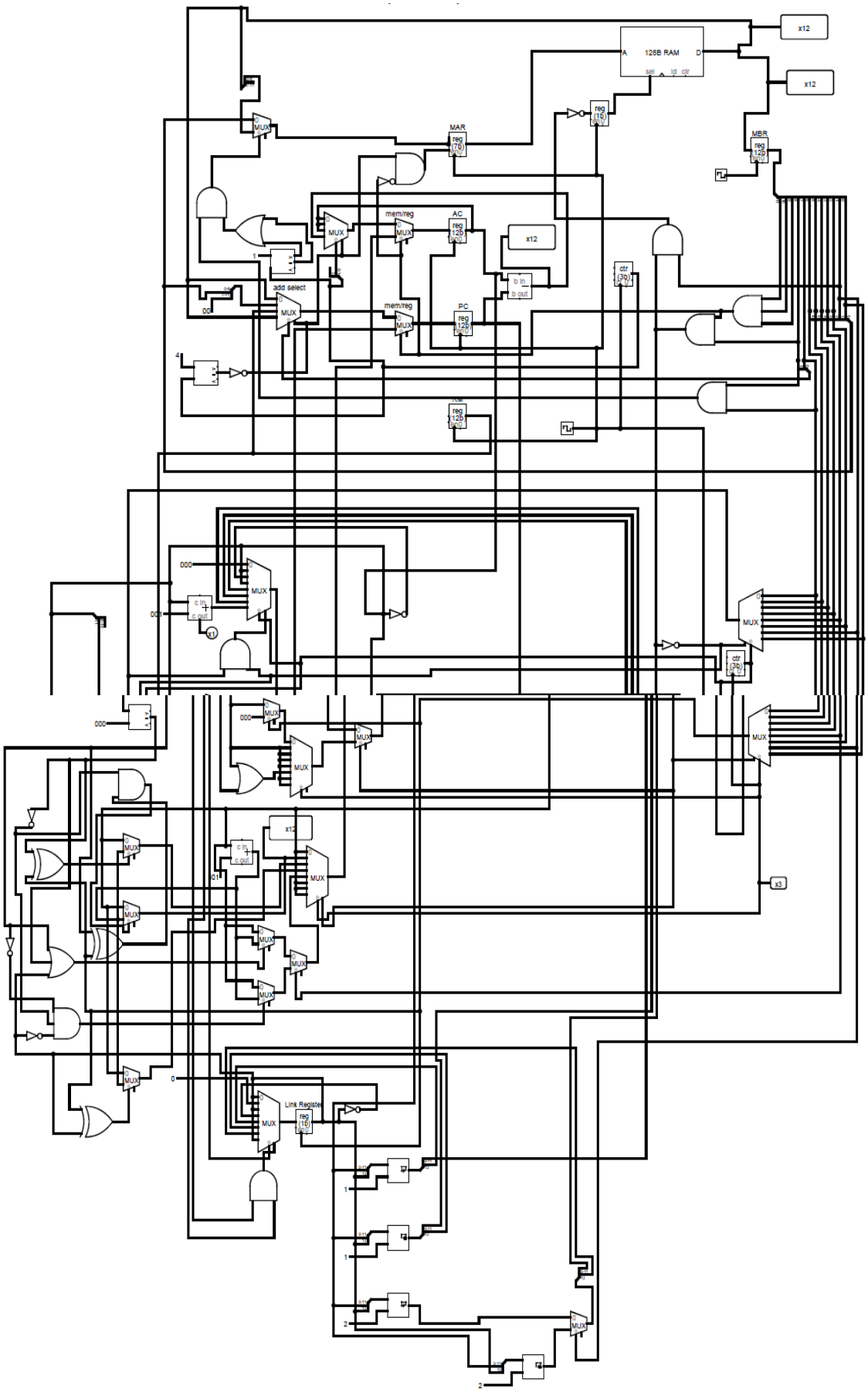
The group 1 micro-instructions are devoted to functions affecting the accumulate and link registers.

Group 2

```
|1|1|1|1|_|_|_|_|_|_|_|_|0|
            1     0         - SMA - skip on AC < 0  \
              1   0         - SZA - skip on AC = 0   > or group
                1 0         - SNL - skip on L /= 0  /
            0 0 0 1         - SKP - skip unconditionally
            1     1         - SPA - skip on AC >= 0 \
              1   1         - SNA - skip on AC /= 0  > and group
                1 1         - SZL - skip on L = 0   /
          1                 - CLA - clear AC
                    1       - OSR - or switches with AC
                      1     - HLT - halt
```

Group 2 micro-instructions primarily implement a number of extra skip instructions roughly corresponding to what would be tests on status bits in other processors.

Output:


x12
128B RAM
A
D
sel
ld
clr
x12
reg (16)
MAR
reg (16)
MBR
reg (128)
mem/reg
AC
reg (128)
x12
b in
b out
ctr (3b)
add select
mem/reg
PC
reg (128)
reg (128)
MUX
000
001
c in
c out
x1
x12
x3
Link Register
reg (16)

References

1. https://homepage.cs.uiowa.edu/~jones/pdp8/faqs/