

CURRENT MODE IMAGE SENSOR

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Department of Electrical Engineering in Partial Fulfilment of Requirements for
the degree of

Master of Science in Electrical and Computer Engineering

December 2023

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**SOUTHERN ILLINOIS UNIVERSITY
EDWARDSVILLE**

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1. INTRODUCTION

In the dynamic field of imaging technology, striving for unparalleled image quality is a constant pursuit. This project proposal introduces an ambitious initiative to develop an Enhanced Current Mode 3T APS (Active Pixel Sensor) Image Sensor. This venture is positioned at the cutting edge of image processing and sensor technology, aiming to transform traditional image sensors through the integration of advanced features and sophisticated techniques, thereby setting a new benchmark in image quality across various lighting environments.

The core of this project is not merely about advancing current sensor technologies but also about laying the groundwork for future breakthroughs. It involves the strategic integration of high-end components such as advanced current amplifiers, efficient Analog to Digital Converters (ADCs), and state-of-the-art noise reduction techniques. These elements are thoughtfully engineered to improve dynamic range, enhance linearity, minimize noise, and optimize for high-speed, low-power operation.

A critical and forward-looking aspect of this project is its emphasis on future ideas, which are central to its overarching vision. Innovations like pixel-level buffering aim to minimize readout times, enhancing the sensor's utility in high-speed imaging applications. The addition of on-chip temperature sensors is designed to ensure consistent image quality across temperature variations. Furthermore, the incorporation of sophisticated on-chip noise reduction methods (temporal noise reduction (TNR) and spatial noise reduction (SNR)) is expected to significantly refine image quality.

These future-focused enhancements are poised to elevate the sensor's capabilities, particularly in fields such as surveillance, medical imaging, satellite imaging, and real-time video streaming, where high-resolution, low-noise images and rapid frame rates are essential.

By centering on these innovative approaches, the project aims to address present technological needs while also spearheading future advancements. The potential integration of AI-driven ASICs for real-time image processing and the exploration of advanced on-chip AI-based image enhancement techniques demonstrate the project's commitment to remaining at the forefront of technological evolution.

1.1 BACKGROUND

The pursuit of exceptional image quality has been a driving force in the evolution of image sensor technology. This project proposal, centered around the development of an Enhanced Current Mode 2T APS Image Sensor, is rooted in a rich history of advancements and challenges in this domain. The background of this initiative is multifaceted, encompassing the development of image sensor technology, the integration of advanced circuitry, and the push toward incorporating AI and other cutting-edge techniques.

1. Evolution of Image Sensor Technology:

Image sensors have undergone significant transformations over the years, transitioning from traditional CCD (Charge-Coupled Device) sensors to the more versatile CMOS (Complementary Metal-Oxide-Semiconductor) sensors. Each step in this evolution has aimed at improving image quality, reducing power consumption, and enhancing the speed and sensitivity of the sensors. The Active Pixel Sensor (APS), particularly the CMOS APS, marked a pivotal advancement, offering integrated circuitry and on-chip processing capabilities, leading to improved noise reduction, dynamic range, and power efficiency.

2. Current Mode 2T APS:

The Current Mode 2T APS represents a further advancement in this lineage. Unlike traditional voltage-mode sensors, current mode sensors offer distinct advantages in terms of dynamic range and speed. However, they also pose unique challenges, particularly in noise management and signal processing, which this project aims to address.

3. Advanced Circuit Integration:

Central to the project is the integration of advanced circuits such as the Flipped Voltage Follower (FVF) and various forms of ADCs, each selected for their specific advantages. The FVF, for instance, is known for its low power consumption and high-speed operation, making it ideal for enhancing dynamic range and reducing noise.

The choice of ADC, whether Sigma-delta, SAR, or Time interleaved, hinges on the desired balance between resolution, speed, and power efficiency, each critical to the sensor's performance.

4. Noise Reduction and Image Quality Enhancement:

Noise reduction is a significant aspect of image sensor development. Techniques like Correlated Double Sampling (CDS) have been instrumental in reducing Fixed Pattern Noise (FPN), a common issue in image sensors. This project seeks to further enhance these techniques to achieve superior image quality.

5. Future-Oriented Innovations:

Looking ahead, the project includes forward-thinking features such as pixel-level buffering and on-chip temperature sensors. These innovations are not just about enhancing current capabilities but are geared toward ensuring the sensor's relevance and superiority in future applications.

The integration of AI, particularly in post-capture image processing, represents a leap toward a new era of smart image sensors. This aligns with the growing trend of embedding AI capabilities directly into hardware, opening up new possibilities in real-time image enhancement and analysis.

1.2 STATE-OF-THE-ART

The 3T APS design offers several advantages over its 2T predecessor. The source follower transistor in the 3T design acts as a buffer, providing a more stable voltage output and reducing the read noise, which is crucial for low-light imaging. Additionally, the 3T APS design allows for more efficient on-pixel conversion gain control, enhancing the dynamic range and improving the overall image quality.

State-of-the-art models for super-resolution primarily belong to the deep learning category, with Convolutional Neural Networks (CNN) being the most widely used. Models like the Super-Resolution Convolutional Neural Network (SRCNN), the Efficient Sub-Pixel Convolutional Neural Network (ESPCN), the Fast Super-Resolution Convolutional Neural Network (FSRCNN), and EDSR (Enhanced Deep Super-Resolution) have demonstrated good results. Generative adversarial networks (GANs), like SRGAN and ESRGAN, have also been used to produce high-resolution images that are perceptually closer to natural images.

1.3 GENERAL MOTIVATION

In the ever-evolving landscape of digital imaging technology, the impetus for innovation is driven by the perpetual quest to capture images of the highest possible quality. The development of the Enhanced 3T APS (Three-Transistor Active Pixel Sensor) Image Sensor is motivated by several key factors that highlight the necessity and significance of this advancement in the field.

1. Pursuit of Superior Image Quality:

At the core of this project's motivation is the aspiration to achieve unparalleled image quality. The Enhanced 3T APS aims to provide clearer, more detailed, and more accurate images, particularly in challenging lighting conditions. This improvement is not just a technical achievement but also enriches the user experience in various applications, from professional photography to everyday use in smartphones and other devices.

2. Overcoming Limitations of Current Technologies:

Despite significant advancements in image sensor technology, current sensors still face limitations in terms of noise levels, dynamic range, and low-light performance. The Enhanced 3T APS seeks to address these challenges, pushing the boundaries of what is currently achievable and setting new standards in the industry.

3. Adapting to Emerging Needs and Applications:

The demand for high-quality imaging is growing across various sectors, including surveillance, medical imaging, the automotive industry, and consumer electronics. The Enhanced 3T APS is motivated by the need to meet these diverse and increasingly sophisticated requirements, ensuring that the technology keeps pace with the evolving demands of these applications.

4. Leveraging Technological Advancements:

The motivation for this project is also fuelled by recent breakthroughs in semiconductor technology, advanced circuit designs, and AI. By integrating these advancements into the Enhanced 3T APS, the project aims to exploit the full potential of modern technology to revolutionize image-sensing capabilities.

5. Preparing for the Future of Imaging:

Looking ahead, there is a clear trend towards integrating smart capabilities directly into imaging sensors. The development of the Enhanced 3T APS is motivated by the desire to be at the forefront of this trend, paving the way for future innovations that could include AI-driven image processing, advanced real-time analytics, and adaptive imaging techniques.

1.4 TECHNICAL OBJECTIVE

The primary technical objective of this project is to develop an advanced 112×112 pixel Current Mode 3T-APS (Three-Transistor Active Pixel Sensor) image sensor capable of operating at 60 frames per second (FPS) with a dynamic range of 40 dB. This development aims to set a new benchmark in the realm of compact, high-performance image sensors tailored for applications demanding high-speed imaging with excellent dynamic range and noise performance.

Design the sensor with the flexibility to be adapted for specific applications. This includes ensuring that the sensor's form factor, power consumption, and output interfaces are compatible with a range of devices and systems.

By accomplishing these technical objectives, the project will deliver a 112×112 Current Mode 3T-APS image sensor, setting a new standard in high-speed, high-dynamic range current mode imaging technology. The successful development of this sensor will pave the way for far-reaching implications for various fields, offering enhanced capabilities for capturing high-quality images in fast-paced and diverse lighting environments.

2. Designs:

The design phase of the Enhanced Current Mode 3T-APS Image Sensor is meticulously structured to integrate state-of-the-art components and technologies. This section outlines the detailed design aspects, focusing on the implementation of an advanced current amplifier, trans-impedance amplifier (TIA), high-efficiency ADC, and dual sampling technique.

2.1 Standard 3T-APS Architecture

Design Framework: The 3T-APS will utilize the standard three-transistor configuration, comprising a photodiode, a reset transistor, a source-follower transistor, and a row-select transistor.

Advantages: This architecture provides a balance between image quality and pixel complexity. The source-follower transistor offers improved buffer capabilities, enhancing the readout stability and speed, while the reset and row-select transistors contribute to efficient pixel operation and readout control.

2.2 Transimpedance Amplifier (TIA)

Purpose: The TIA is essential in the current mode APS for converting the photocurrent generated by each pixel into a voltage signal, which can be processed by the ADC.

Design Details: The TIA will be designed to offer high linearity and bandwidth to convert the photocurrent accurately and efficiently to a voltage. It will be optimized for low noise and high sensitivity to ensure the fidelity of the image sensor's output.

Implementation: The TIA will be strategically placed in the signal path, immediately after the pixel array, to ensure minimal signal degradation. Its design will focus on balancing the requirements for speed, noise performance, and power efficiency.

2.3 High-Efficiency ADC

Options Considered:

Sigma-Delta ($\Sigma\Delta$) ADC: Known for its high resolution, making it suitable for applications requiring detailed image capture.

SAR ADC: Offers high-speed and low-power characteristics, ideal for fast-paced imaging with energy efficiency.

Time Interleaved ADC: Combines multiple ADCs to increase sampling rates, beneficial for extremely high-speed applications.

Design Decision: The choice of ADC will be based on a trade-off analysis considering resolution, speed, power consumption, and the specific requirements of the intended applications of the 3 T-APS

2.4. Dual Sampling Technique: Correlated Double Sampling (CDS)

Purpose: CDS is implemented to significantly reduce Fixed Pattern Noise (FPN), a common issue in image sensors, thereby enhancing image quality.

Design Details: The CDS technique will involve capturing two samples - one representing the reset level and the other representing the signal level. The difference between these two samples will be used to extract the true image signal, effectively eliminating the FPN.

Implementation: The CDS circuitry will be integrated at the pixel level or immediately after the pixel array, depending on the optimization for noise performance and circuit complexity.

2.5 Current Conveyor with Feedback

Purpose: The inclusion of a current conveyor with feedback is crucial for enhancing the sensor's resistance from FPN (Fixed Pattern Noise) and the response to varying light intensities and improving overall image fidelity.

Design Considerations: The current conveyor will be optimized for high linearity and responsiveness. The feedback mechanism will be tailored to stabilize the output, ensuring consistent performance across the sensor's operational range.

Implementation: Integrated within the pixel architecture, the current conveyor with feedback will work in conjunction with the TIA and the ADC, forming a cohesive system that maximizes dynamic range and minimizes noise.

In summary, the design phase of the Enhanced Current Mode 3T-APS Image Sensor is a harmonious integration of advanced components and techniques. Each element, from the design of the pixel to the ADC, is carefully chosen and engineered to complement each other, ensuring that the final product not only meets but surpasses the expectations in terms of image quality, speed, and efficiency. The implementation of these components will be a delicate balance of technical precision

and innovation, aimed at achieving a sensor that redefines the standards in image sensing technology.

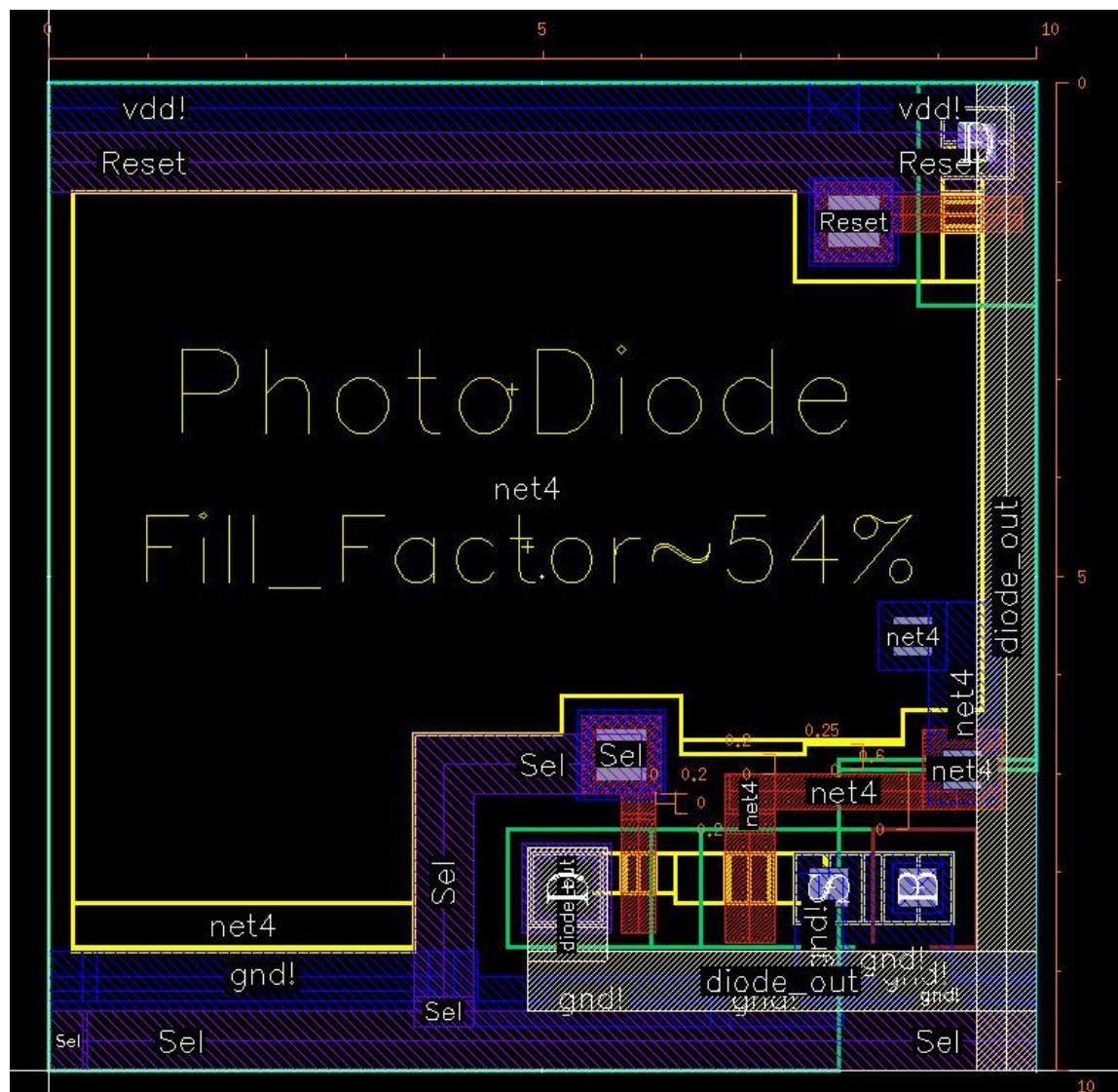
3. DETAILED DESIGN REPORTS:

3.1 3T Voltage Mode Active-Pixel-Sensor

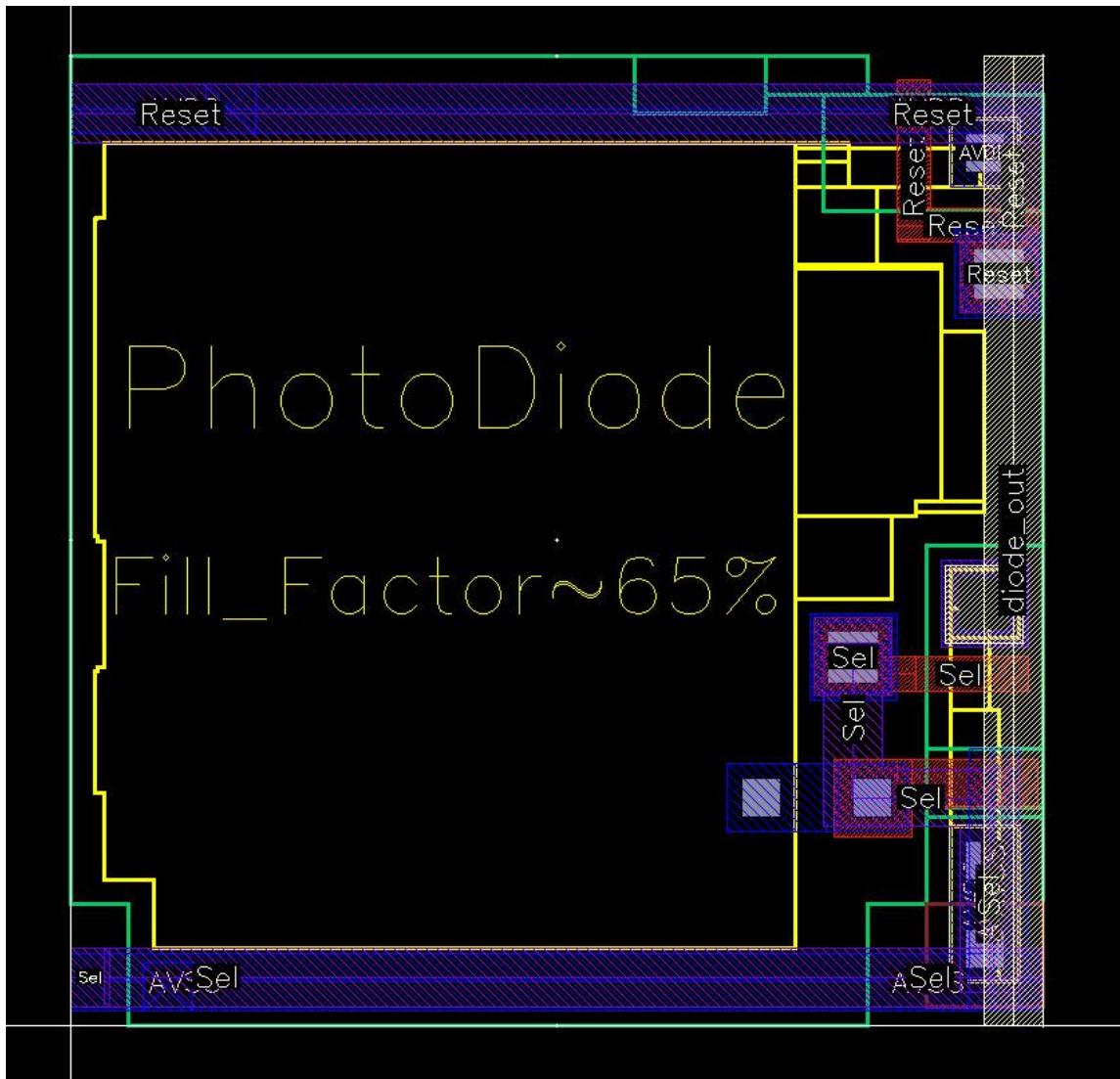
Abstract .

This report aims to explore the sizing and layout of a 3T Current mode active-pixel-sensor. The lab involves designing and laying out a $10\mu\text{m} \times 10\mu\text{m}$ 3T-APS pixel, with more than 50% fill factor. The report goes from theoretical/analytical calculations with explanations, simulations to laying out a pixel with those calculated values.

Photodiode Layout : (Version 1)



PhotoDiode Version 2 (awaiting approval)



Theory/calculations - The Transistor M1 is going to be used as a current source, the gate voltage is directly controlled by the intensity of the light and exposure time to light.

By the Saturation Current formula :

$$I_{ds} = \frac{1}{2} K_{pn} \cdot S \cdot (V_{eff})^2$$

We can study the relation between Current, V_{eff} and S .

When current increases either S or V_{eff} should increase as I is directly proportional to both S and V_{eff} . S and V_{eff} are indirectly proportional.

So here there are a number of trade offs....!

The **bias Current (I_{bias})** which is going to be the I_{ds} of M1. The first trade off and ballpark is with **I . If gate voltage increases** Current increase the V_{eff} should increase too ..! which implies V_d should decrease...!. So the **lower the I_{bias} the higher the Drain voltage the higher the current gets sucked in by the photo diode** which is good..!

This figure shows us the relation between I_{bias} in X-axis, and V_{out} in the Y-axis for a fixed shape factor. It's clear that while choosing Current the lower the better.

$$52\mu A = \frac{1}{2} \cdot 170 \times 10^{-6} \frac{\mu A}{V^2} \cdot \frac{s}{1.32} \cdot (0.90 V)^2, \text{ where } n = 1.32 \text{ (Subthreshold slope factor when } V_{sb} = 0 \text{)}$$

S = 1, Let L = 0.5μm (More the length less the impact of channel length modulation on the channel) and W = 0.5μm.

To find the voltage drop across the select transistor,

$$R_{\text{SEL}}, \text{ where } R_{\text{SEL}} = \frac{n}{Kpn.S.V_{\text{eff}}}$$

Since the select transistor is in triode region (low resistance) we can first find the inversion coefficient θ and the find V_{eff} using the "Saturation Voltage as a function of Inversion coefficient" graph or use the direct formula.

$$\theta = \frac{Id_s}{2.n.S.Kpn.V_{\text{eff}}^2} = \frac{3\mu A}{2.(1.17).(1.14).(170\mu A \frac{\mu A}{V^2}).(0.026)^2} = 9.78$$

$$V_{\text{eff}} = \frac{2.n.U_T}{\alpha} = \frac{2.1.17.(0.026)}{0.305}, \text{ Where } \alpha = \frac{1-e^{-\sqrt{9.78}}}{\sqrt{9.78}}$$

$$V_{\text{eff}} \simeq 0.2$$

$$R_{\text{SEL}} = \frac{1.17}{170.10^{-6}.(1.14).(0.2)} = 30K\Omega.$$

This value $n = 1.2$ is an estimation on the subthreshold slope factor as V_s will change a lot before coming to an approximate value as the Threshold depends on V_s and an approximate value for V_s is 1.3 V.

So this is the trade off here: the Area VS output current and gain.

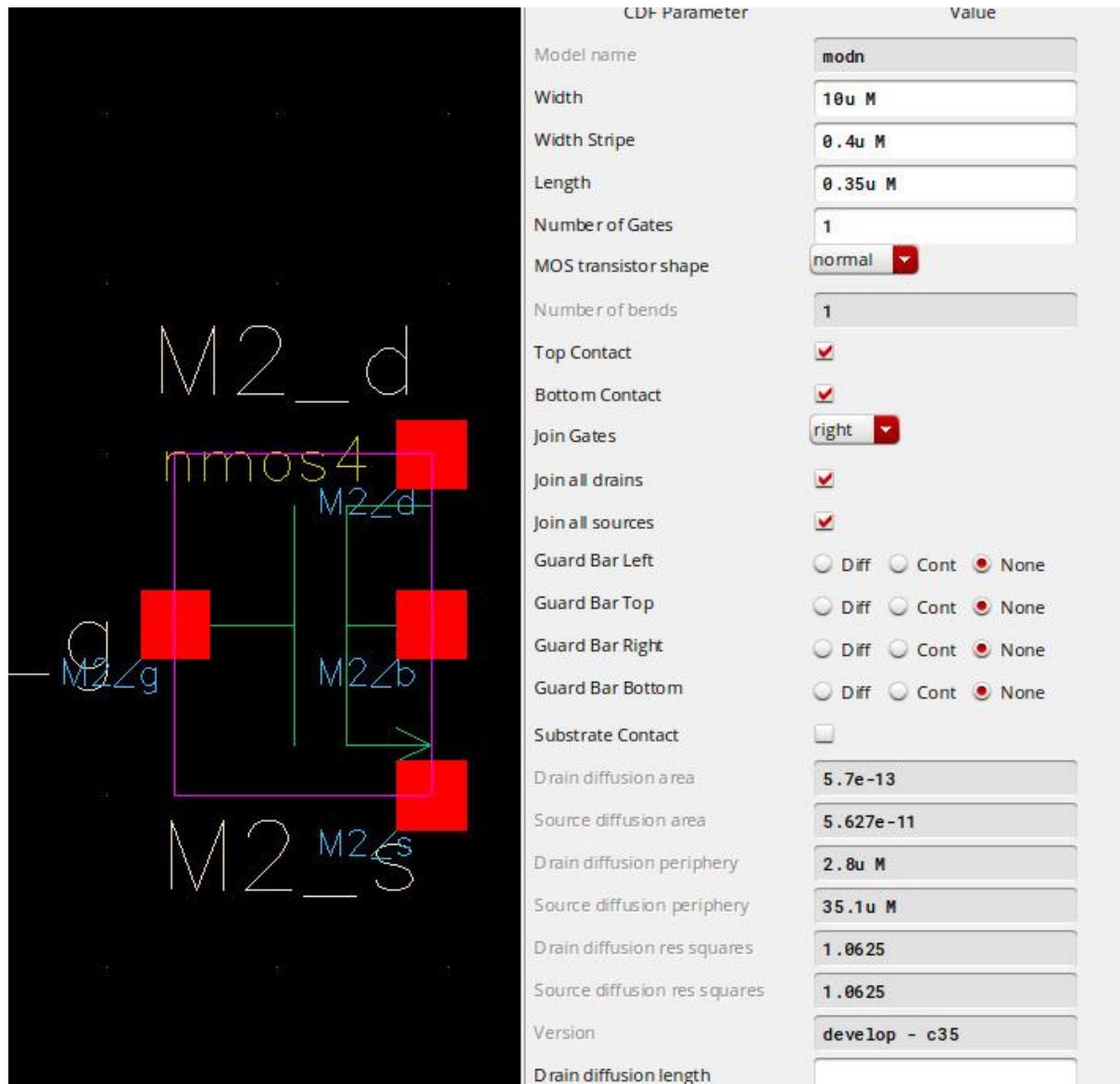


Fig 6- Parasitic Extraction output.

Total Area of the source Diffusion = $5.627 \times 10^{-11} m^2$

Total Source diffusion perimeter = 35.1 μm

The Well capacity of the source diffusion layer calculation:

$$Q_{photo} = C_{photo} \cdot (V_{dd} - V_{tn})$$

$$C_{photo} = C_\phi + C_{sw}$$

$$C_\phi = \frac{Cj.Area diff}{(1 + \frac{V_r}{V_\phi})^{mj}} = \frac{(8.4) \cdot 10^{-4} \cdot (5.627 \cdot 10^{-11})}{(1 + \frac{2.35}{0.69})^{0.34}} = 2.854 \times 10^{-14}$$

$$C_{sw} = \frac{C_{jsw} \cdot Perimeterdiff}{(1 + \frac{V_r}{V_\phi})^{msw}} = \frac{(2.5) \cdot 10^{-10} \cdot (35.1 \cdot 10^{-6})}{(1 + \frac{2.35}{0.69})^{0.23}} = 6.239 \times 10^{-15}$$

$$C_{photo} = C_\phi + C_{sw} = 3.4787 \times 10^{-14}$$

$$Q_{photo} = C_{photo} \cdot (V_{dd} - V_{tn}) = 3.4787 \times 10^{-14} \times (3.3 - 0.5) = 4.6018 \times 10^{-14}$$

We know $Q=nE$,

$$4.6018 \times 10^{-14} = n \cdot (1.602 \times 10^{-19})$$

$n \approx 28725.437$ (number of electrons the diffusion layer can accommodate or well capacity)

WELL CAPACITY = 28725. (Considering Quantum efficiency as 30%)

Resolution = $\log_2(\text{well capacity})$, not considering noise

Resolution = $\log_2(28725 \cdot 0.3)$.

Resolution ≈ 12 bits

Version 2:

Drain diffusion area	5.7e-13	off
Source diffusion area	6.60375e-11	off

Yields approximately same Resolution

3.2 Comparison Report of Current Conveyor Designs for 112x112 Current Mode Image Sensor

1. Introduction to Current-Mode Image Sensors

Current-mode image sensors rely on current conveyors to copy currents from the pixels to the periphery while providing a fixed reference voltage to the input node, that is, to the drain node of the pixel's readout transistor. The classic current conveyor design uses four transistors, two n-channel (NMOS), and two p-channel (PMOS) metals.

2. Applications and Range of Current Conveyors

The current conveyor can operate over a wide frequency range and therefore finds applications in the realization of broadband analog building blocks such as amplifiers, multipliers, oscillators, and active filters.

3. Challenges with Current Mode Image Sensors

A current mode image sensor enables simple implementation of focal plane algebraic functions but suffers from poor linearity and large fixed-pattern noise.

4. Linearity Improvement Methods

Previously reported linearity improvement methods are reviewed, while an architecture of a current mode image sensor with a voltage feedback loop between pixel output and the current conveyor for linearity enhancement is proposed. (Source: IEEE Xplore). And this is what we are going to use here.

5. Second-Generation Voltage and Current Conveyors

A review of second-generation voltage conveyor (VCII) and current conveyor (CCII) circuits for the conditioning of biosignals and sensors is presented. The CCII is the most known current-mode active block, able to overcome some of the limitations of the classical operational amplifier, which provides an output Voltage-Driven Nature: Traditional op-amps are voltage-driven devices, which means they respond to voltage differences at their inputs and output a voltage. This can be less efficient in certain applications, especially where current is a more natural or direct way to process or transmit information, as in many biosignal applications.

Bandwidth Limitations: Op-amps often have bandwidth limitations due to their internal compensation mechanisms, which are necessary to ensure stability in closed-loop configurations. CCIIIs, by their nature, can offer wider bandwidths, making them suitable for high-frequency applications.

Input Impedance: Op-amps typically have high input impedance at their non-inverting input and low impedance at the inverting input. This asymmetry can be problematic in some circuit designs. CCIIIs, on the other hand, offer high input impedance at both inputs, which can be advantageous in certain applications.

Output Impedance: Classical op-amps usually have low output impedance, which is beneficial for voltage buffering but can be limiting when a high output impedance is required, such as in current sourcing applications. CCIIIs provide an output current with high output impedance, which is more suitable for such scenarios.

Power Consumption: Op-amps can sometimes consume more power, especially in high-frequency or high-precision applications. CCIIIs can be designed to be more power-efficient, particularly in current-mode signal processing applications.

Linear Range: The linear operating range of op-amps can be limited, affecting their performance in applications requiring a wide linear range. CCIIIs can offer improved linearity over a broader range, which is crucial in precise signal-processing tasks.

Noise Performance: Op-amps can introduce significant noise, especially in low-signal applications like bio-signal processing. CCIIIs can be designed to have lower noise characteristics, which is essential in sensitive signal acquisition systems.

Overall, CCIIIs provide certain advantages over classical op-amps, particularly in applications that benefit from high impedance levels, wide bandwidths, efficient current-mode operation, and low noise characteristics. This makes them particularly suitable for bio signal conditioning and sensor interfacing where these characteristics are highly valued. current instead of a voltage.

6. Topologies and their Linearities:

As discussed above it is clear to have a CCII with a feedback loop.

Below three Topologies referred from IEEE research papers are considered here.

Calculation: (To be safe calculating widths that are capable of operating with 100u A)

$$I_{ds} = \frac{1}{2} K_{pn} \cdot S \cdot (V_{eff})^2$$

$$100 \times 10^{-6} = 0.5 \times 170 \times 10^{-6} \times S \times (1 - 0.5)^2$$

$$S = 6.2 \quad (W = 12.4 \mu m, L = 2 \mu m) \text{ For Nmos}$$

$$(W = 6.2 \mu m, L = 1 \mu m)$$

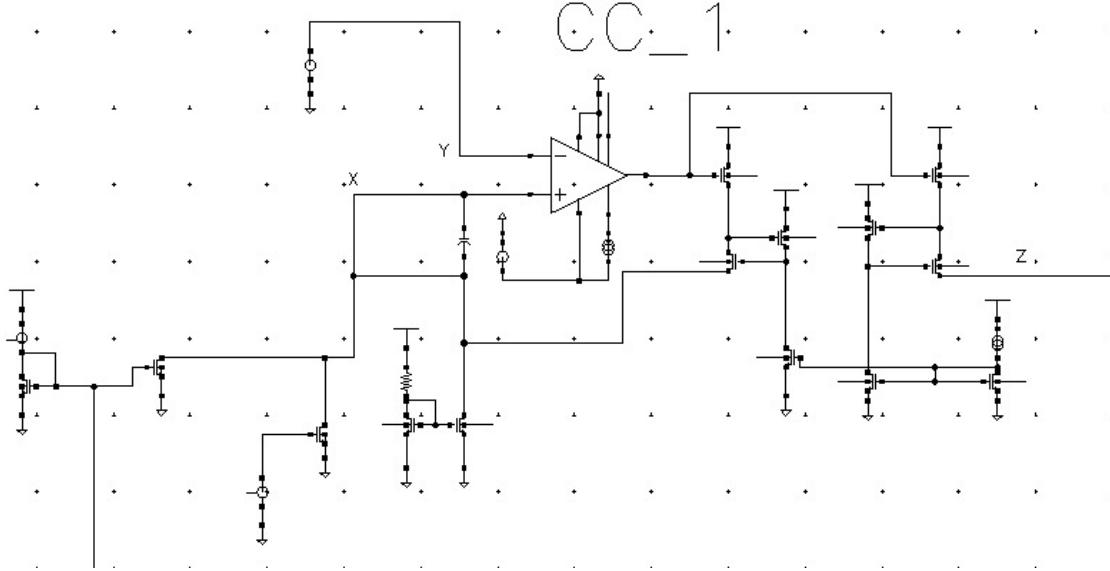
$$I_{ds} = \frac{1}{2} K_{pn} \cdot S \cdot (V_{eff})^2$$

$$100 \times 10^{-6} = 0.5 \times 60 \times 10^{-6} \times S \times (1 - 0.5)^2$$

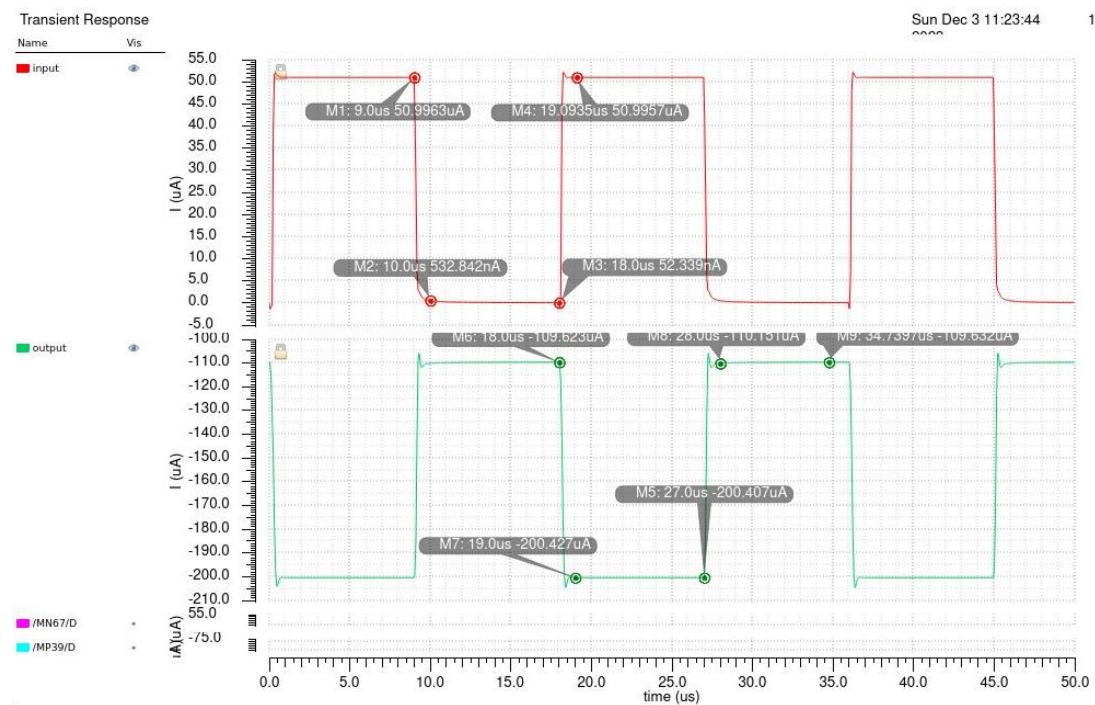
$$S = 2.6 \quad (W = 35.2 \mu m, L = 2 \mu m) \text{ For Pmos}$$

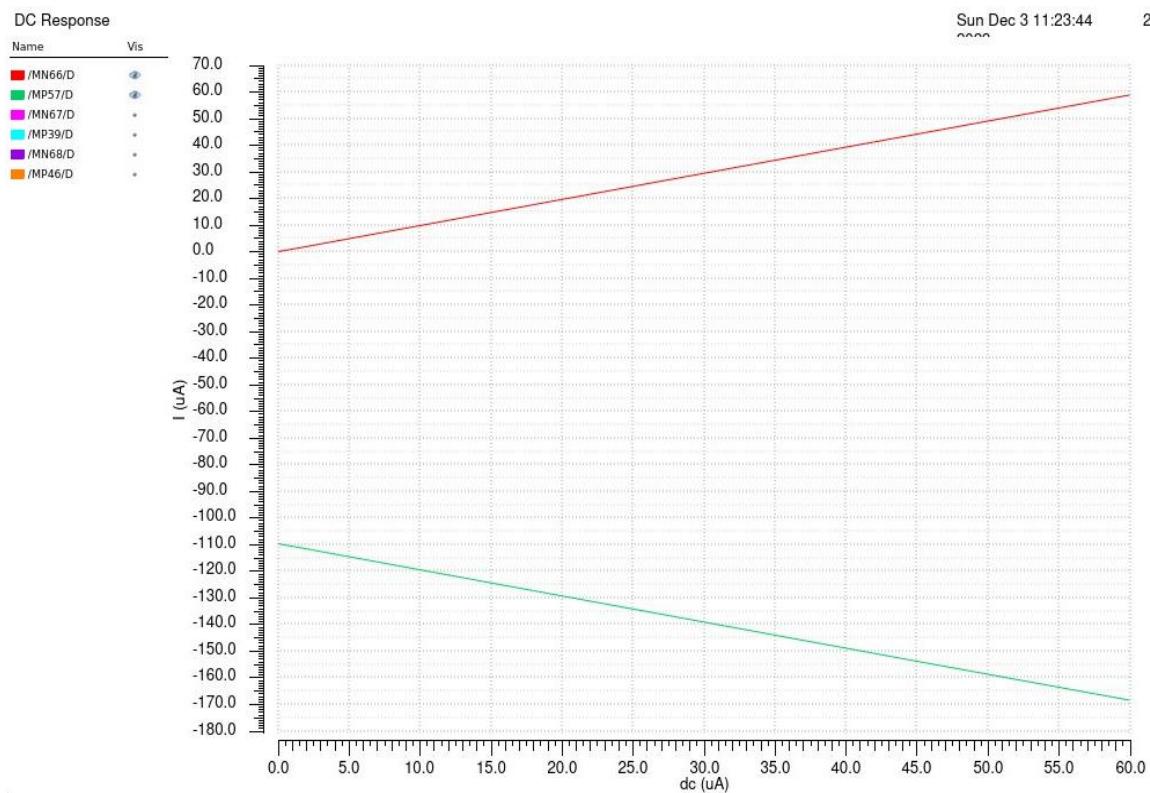
$$(W = 17.6 \mu m, L = 1 \mu m)$$

Topology 1:



Output :





Linearity

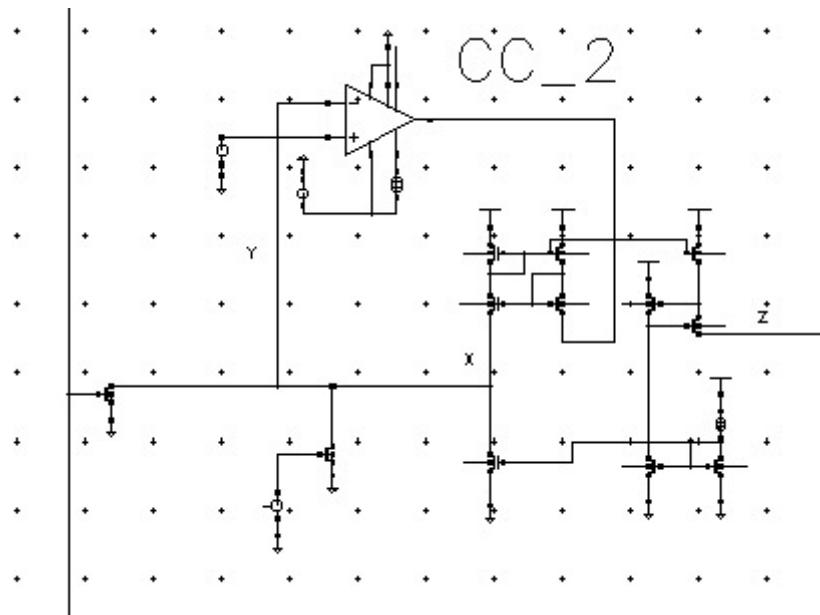
```
>> current_mode_bunch_version_4
/MN66/D X      /MP57/D Y
```

```
_____
0      -0.00010957
1.2e-06  -0.00011076
2.4e-06  -0.00011194
3.6e-06  -0.00011312
4.8e-06  -0.0001143
```

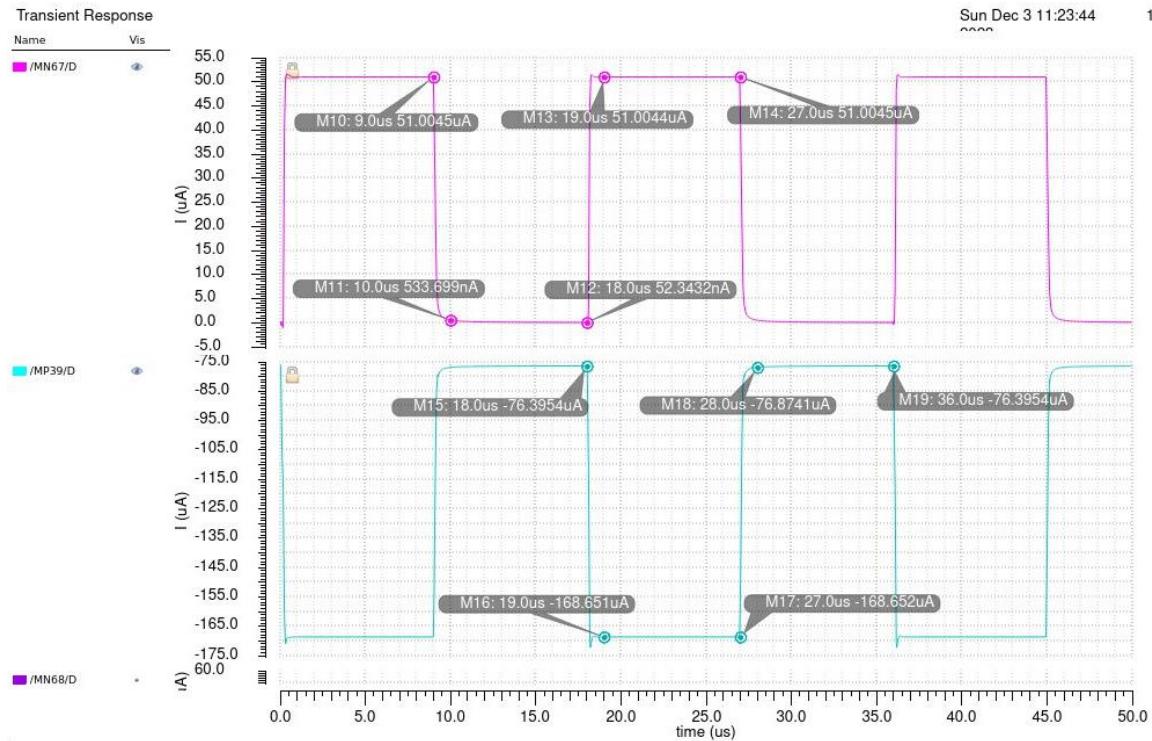
```
1.0000
```

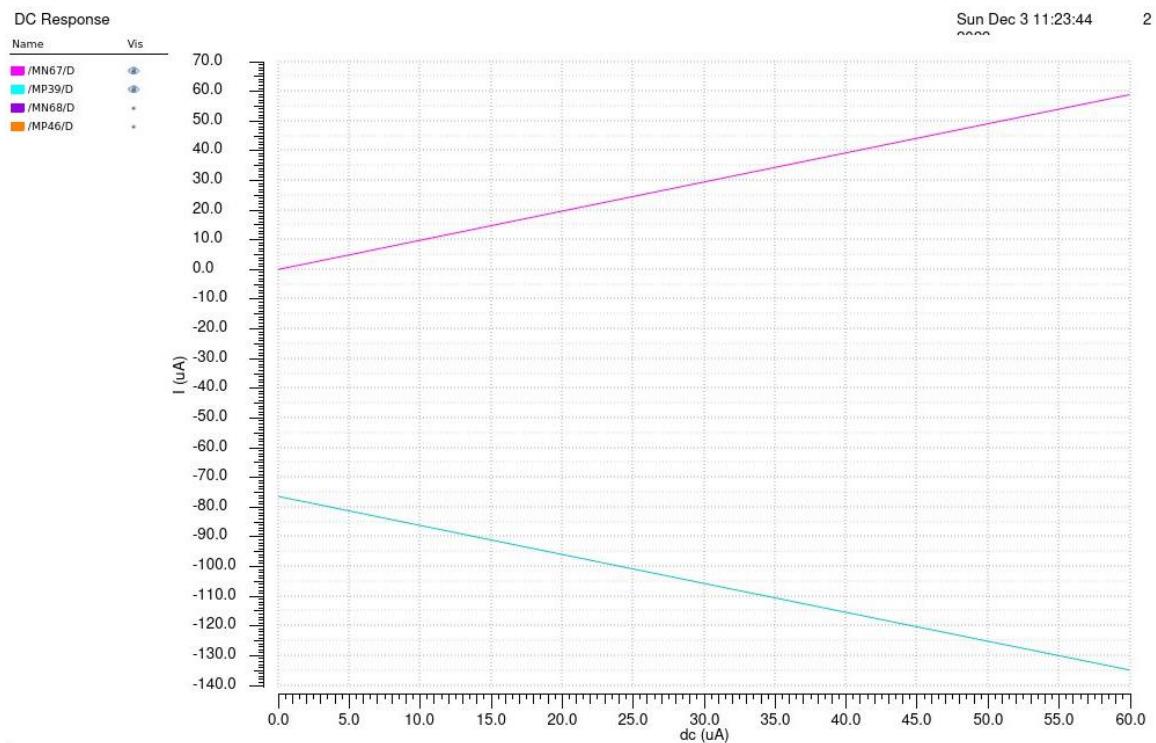
Rank 1: Linearity is 99.9999% for parameters /MP57/D X and /MP57/D Y
 Peak Current: -0.00010957 Lowest Current: -0.00016833

Topology 2:



Output:





Linearity :

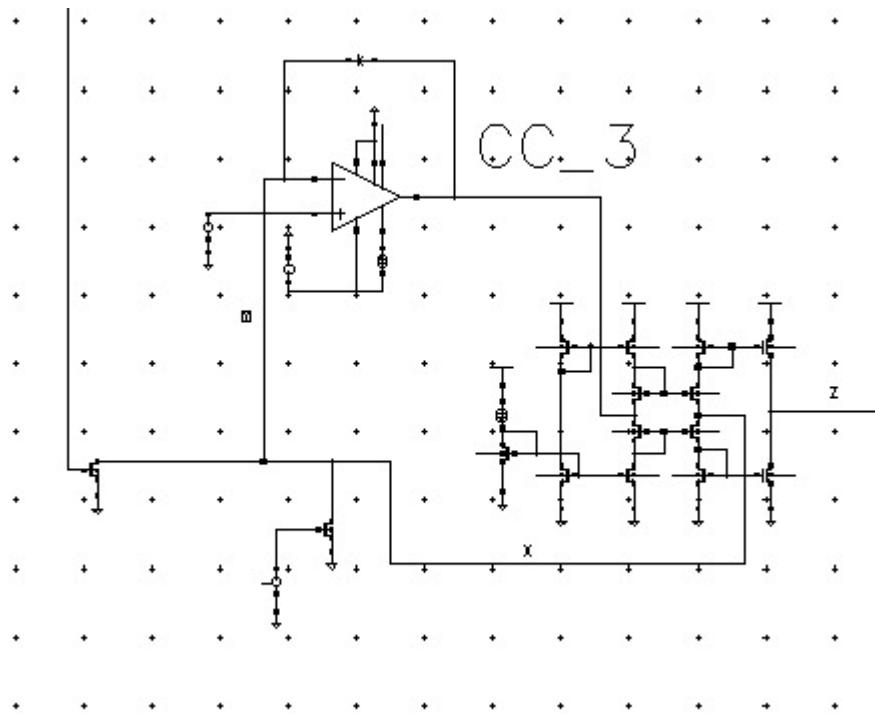
```
>> current_mode_bunch_version_4
    /MP39/D X      /MP39/D Y
```

```
_____
0      -7.6343e-05
1.2e-06   -7.7525e-05
2.4e-06   -7.8702e-05
3.6e-06   -7.9879e-05
4.8e-06   -8.1054e-05
```

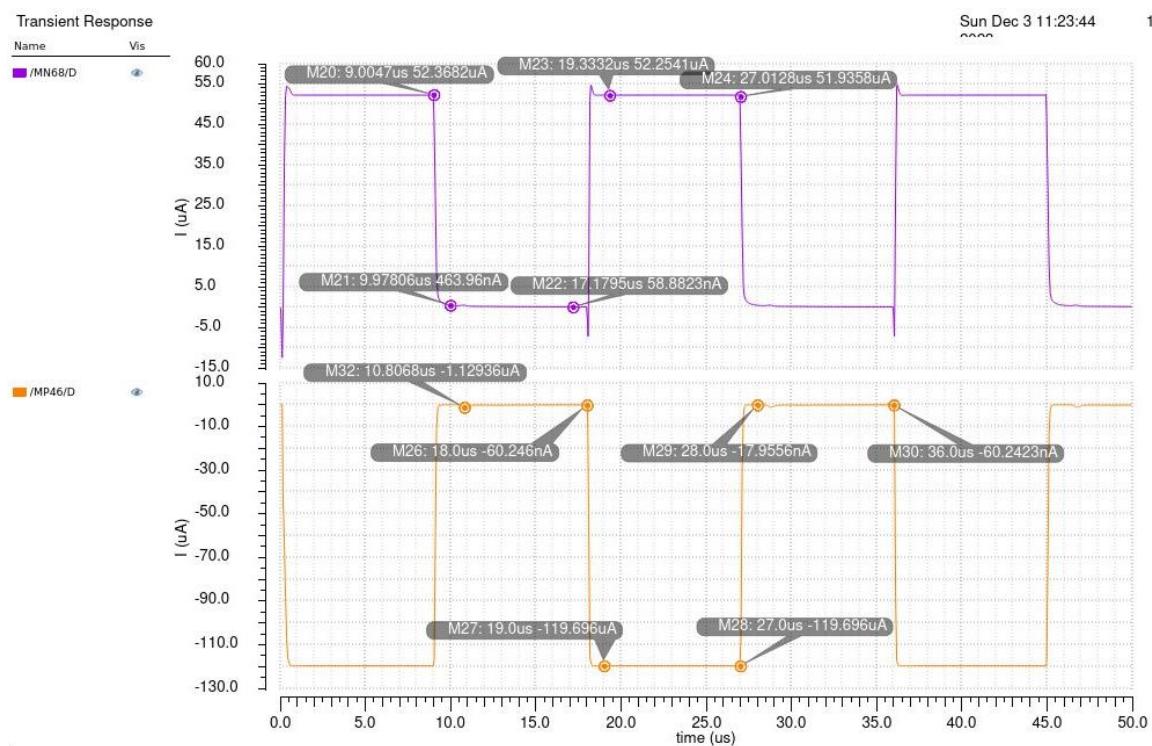
1.0000

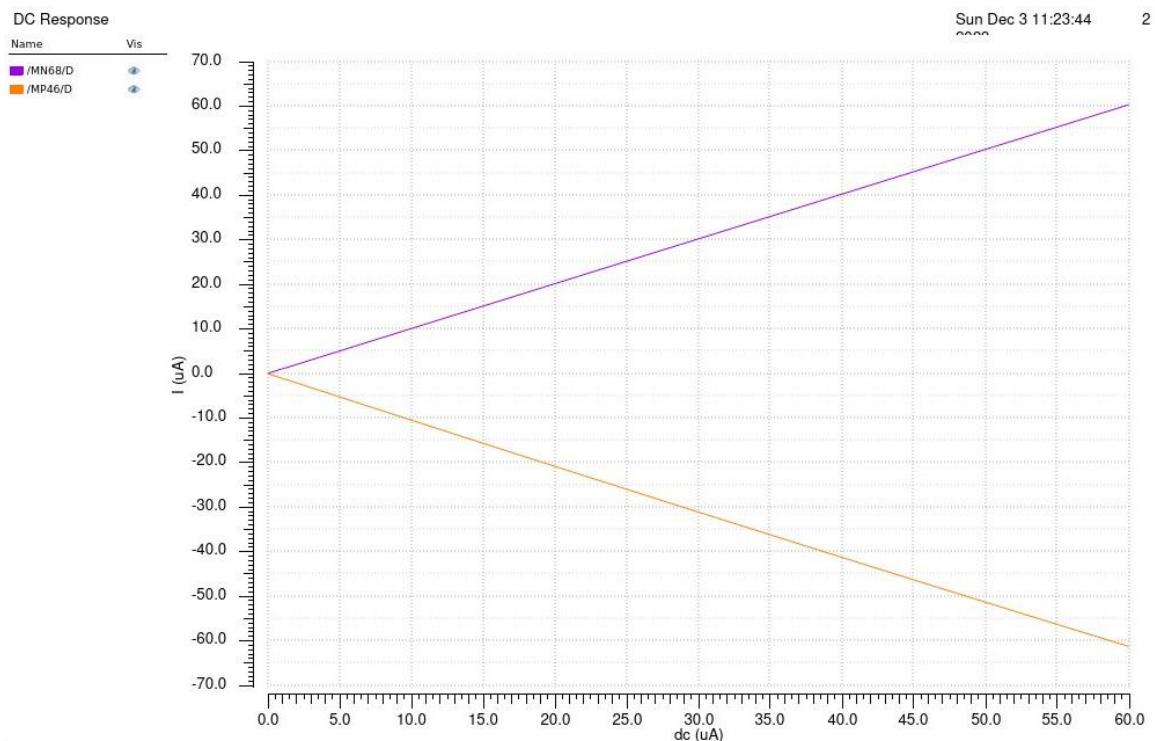
```
Rank 1: Linearity is 99.9998% for parameters /MP39/D X and /MP39/D Y
Peak Current: -7.6343e-05 Lowest Current: -0.00013479
```

Topology 3:



Output :





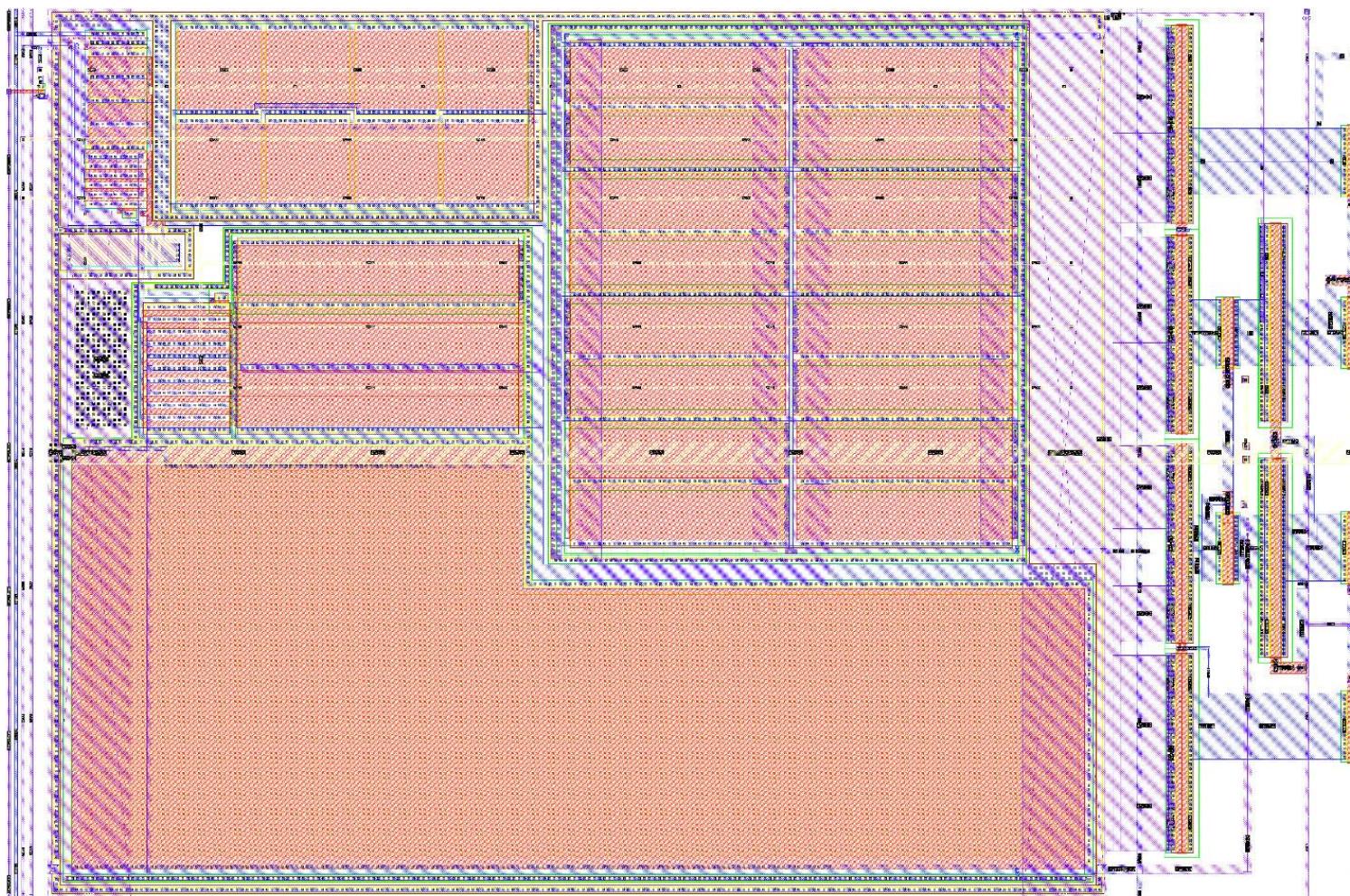
```
>> current_mode_bunch_version_4
/MR46/D X      /MR46/D Y
```

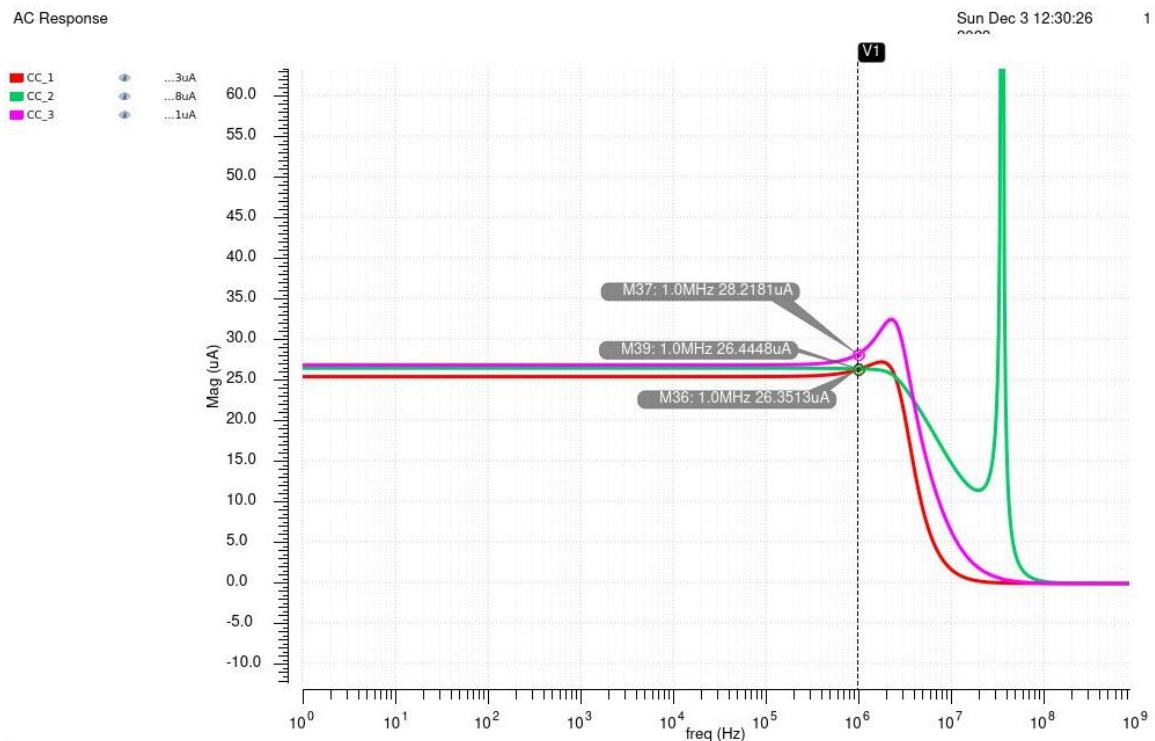
0	-4.0758e-11
1.2e-06	-1.268e-06
2.4e-06	-2.5293e-06
3.6e-06	-3.7876e-06
4.8e-06	-5.0435e-06

0.9999

Rank 1: Linearity is 99.9936% for parameters /MR46/D X and /MR46/D Y
 Peak Current: -4.0758e-11 Lowest Current: -6.1197e-05

Layout :





Even though current switches in 111K Hz it operates decently at 1MHz which tells us that CCII_1 can switch and stabilize around 1us.

By analyzing the output of these three configurations all designs give good linearity but now the trick lies with settling time as Design_3 showcases the best settling time which is around 1u s makes it the best choice among the three.

6. Conclusion

This report provided an overview of the current conveyor designs used in 112x112 current mode image sensors, highlighting the key features, applications, challenges, and improvements. The selection of the CC_1 topology is purely based on transition stability, Linearity, Power, and Design Complexity.

3.3 Design of a Transimpedance Amplifier Using OP_LN CMOS Operational Amplifier

1. Introduction

This report presents the design of a Transimpedance Amplifier (TIA) using the OP_LN CMOS Operational Amplifier. TIAs are essential in applications requiring the conversion of current signals to voltage signals, particularly in sensor interfaces and communication systems. The aim is to design a TIA that converts an input current range of 0 to 70 μ A into a corresponding voltage range of 1V to 2.5V without degrading signal integrity.

2. OP_LN CMOS Operational Amplifier Overview

The OP_LN CMOS Operational Amplifier is a low-noise, internally compensated operational amplifier suitable for low noise applications. Key features include a small area, low offset, and a wide temperature operating range, making it ideal for precision applications such as the TIA design.

3. Design Requirements

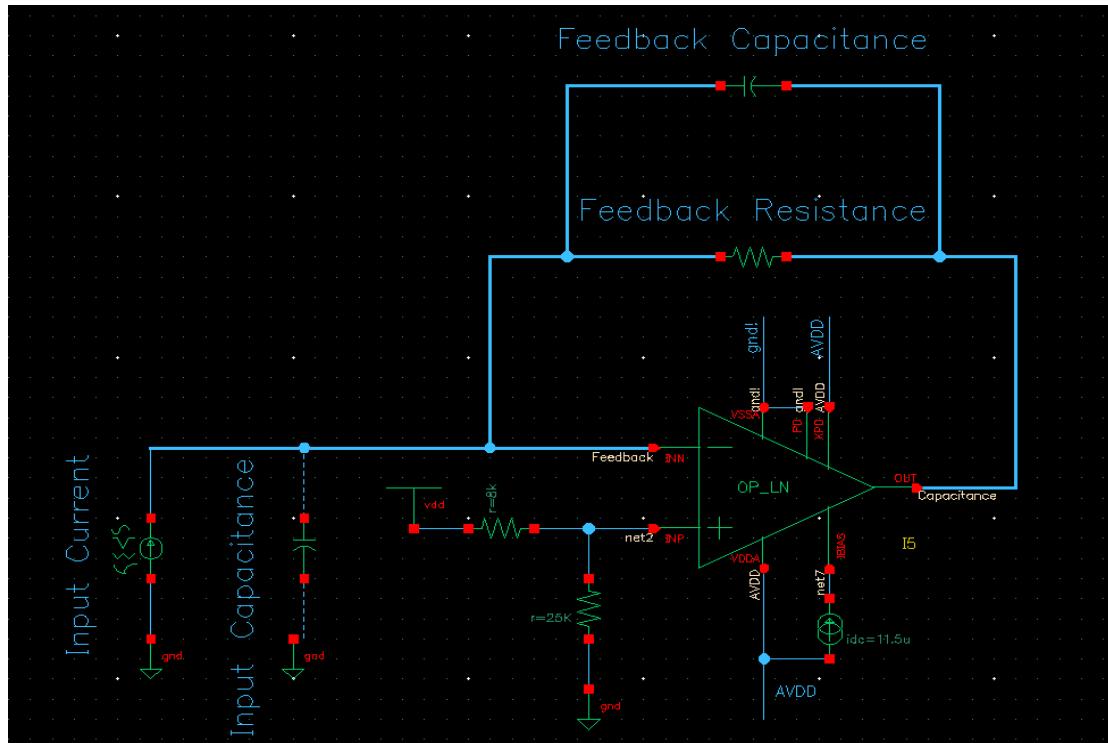
The TIA design focuses on achieving an input current range from 0 to $70 \mu\text{A}$ and an output voltage range from 1V to 2.5V. These specifications dictate the selection of components and the overall design approach.

4. TIA Design Methodology

The design methodology involves selecting an appropriate circuit topology, calculating feedback resistor and capacitor values, and ensuring optimal feedback network design. Component selection is critical for meeting the required input and output ranges while maintaining stability and low noise performance.

5. TIA Design & Calculations:

Input		Output		Bandwidth	Supply	
I_{MAX}	I_{MIN}	V_{MAX}	V_{MIN}	f_p	V_{DD}	V_{SS}
0A	$70\mu\text{A}$	1V	2.5V	1MHz	3.3V	0V



1.) Input Capacitance Calculation :

$$\text{Input Capacitance (Current Conveyor Output)} = C_{cc_pmos} + C_{cc_nmos}$$

$$C_{cc_pmos} = C_{gs} + C_{sb}$$

$$C_{cc_pmos} = \frac{2}{3} C_{ox} \cdot w \cdot l + 1.1fF \cdot w + 0.35fF$$

$$C_{cc_pmos} = \frac{2}{3} 4.5fF \cdot 5.2 \cdot 2 + 1.1fF \cdot 5.2 + 0.35fF$$

$$C_{cc_pmos} = 31.2fF + 6.07fF$$

$$C_{cc_pmos} = 37.27fF$$

$$C_{cc_nmos} = C_{gs} + C_{sb}$$

$$C_{cc_nmos} = \frac{2}{3} C_{ox} \cdot w \cdot l + 1.1fF \cdot w + 0.35fF$$

$$C_{cc_nmos} = \frac{2}{3} 4.5fF \cdot 1.8 \cdot 2 + 1.1fF \cdot 1.8 + 0.35fF$$

$$C_{cc_nmos} = 10.8fF + 2.33fF$$

$$C_{cc_nmos} = 13.13fF$$

$$C_{in} = 37.270fF + 13.13fF$$

$$C_{in} = 50.4fF$$

2.) Calculate R_{feedback}:

$$R_{\text{feedback}} = \frac{V_{MAX}-V_{MIN}}{I_{MAX}-I_{MIN}}$$

$$= \frac{2.5V-1V}{70\mu-0A}$$

$$R_{\text{feedback}} = 21.428K\Omega$$

3.) Calculation of C_{feedback}:

$$C_{\text{feedback}} = \frac{1}{2\pi \cdot 21.428K\Omega \cdot 1MHz}$$

$$= \frac{1}{42856000000\pi}$$

$$C_{\text{feedback}} = 7.4274\mu F$$

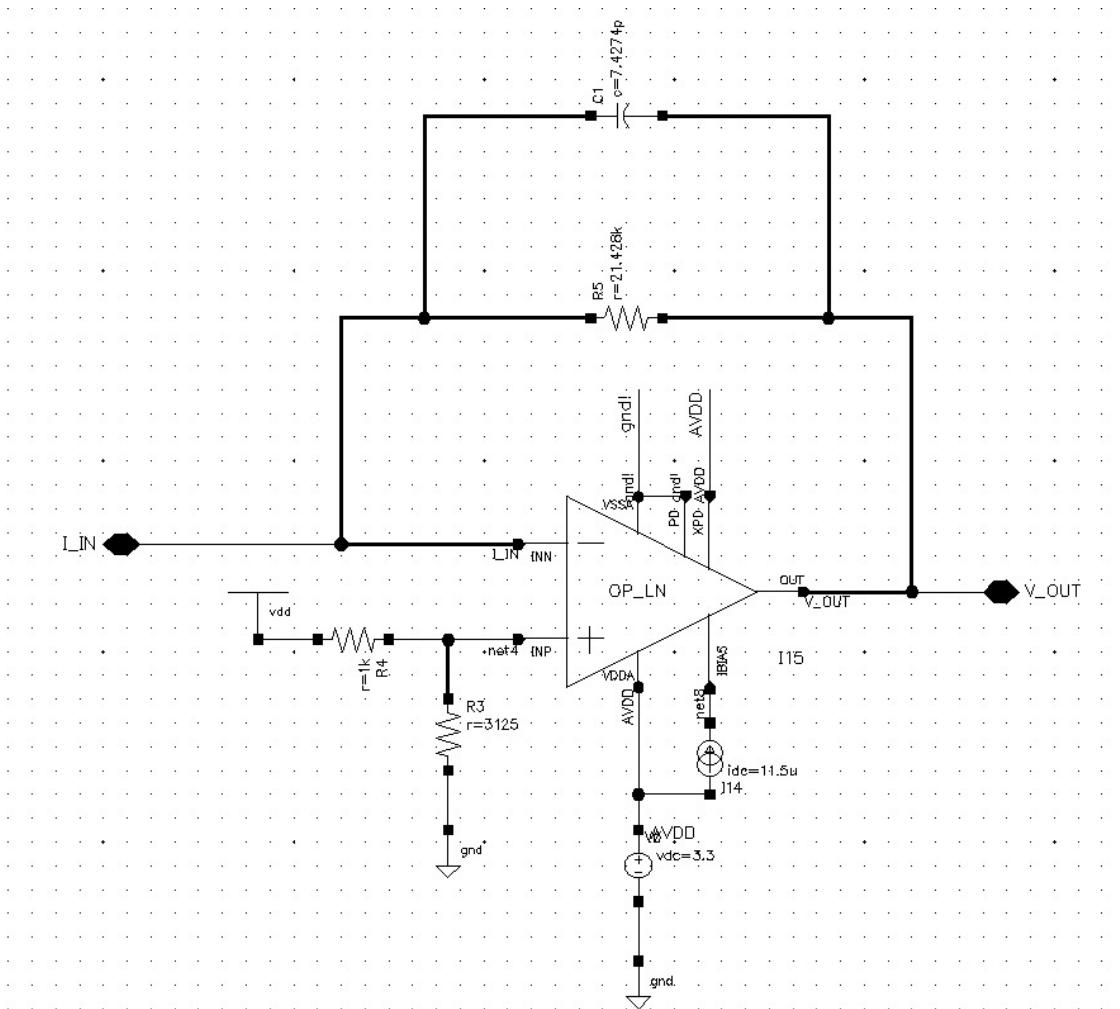
4.) Calculation of GBW :

$$GBW > \frac{2 - 22222 + 2 - 22222}{2 * 21.428 * (2 - 22222)^2}$$

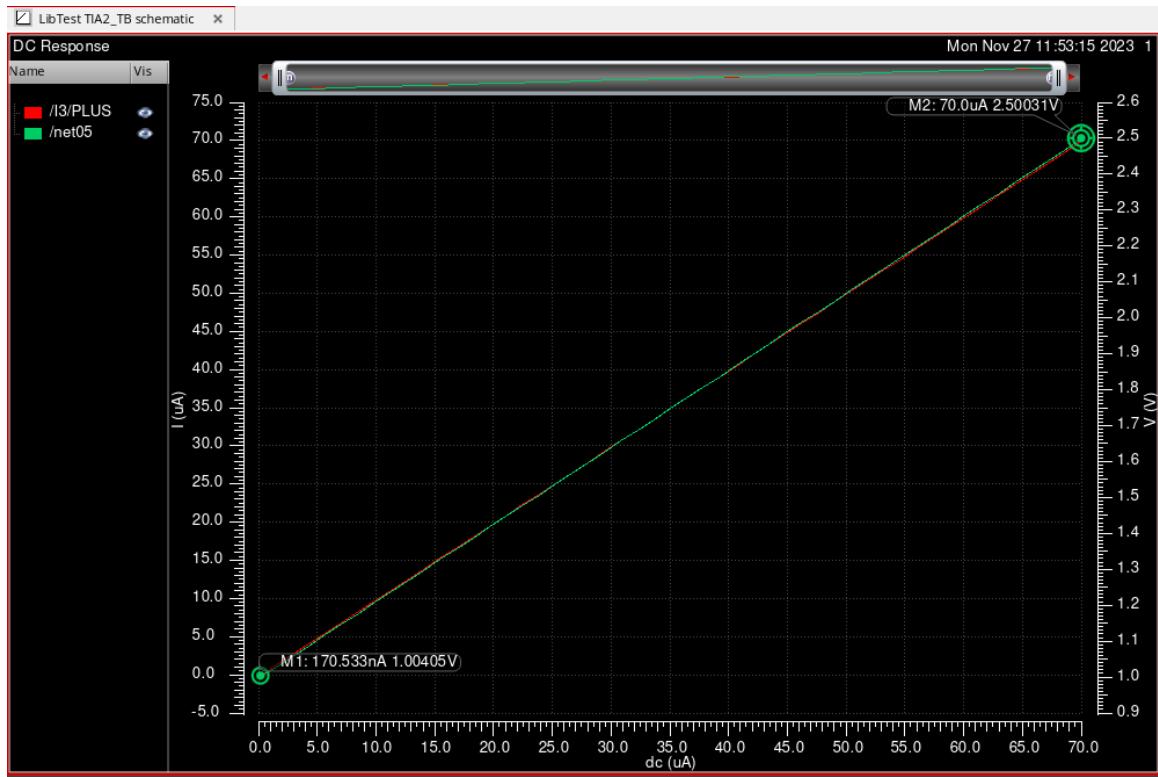
$$GBW > \frac{50.422 + 7.427322}{2 * 21428 * (7.427322)^2} > 1.006803 \text{MHz}$$

The minimum required gain Bandwidth is approximately 1 MHz . Our OP_LN's typical gain Bandwidth is 2.39 MHz which easily meets the requirement.

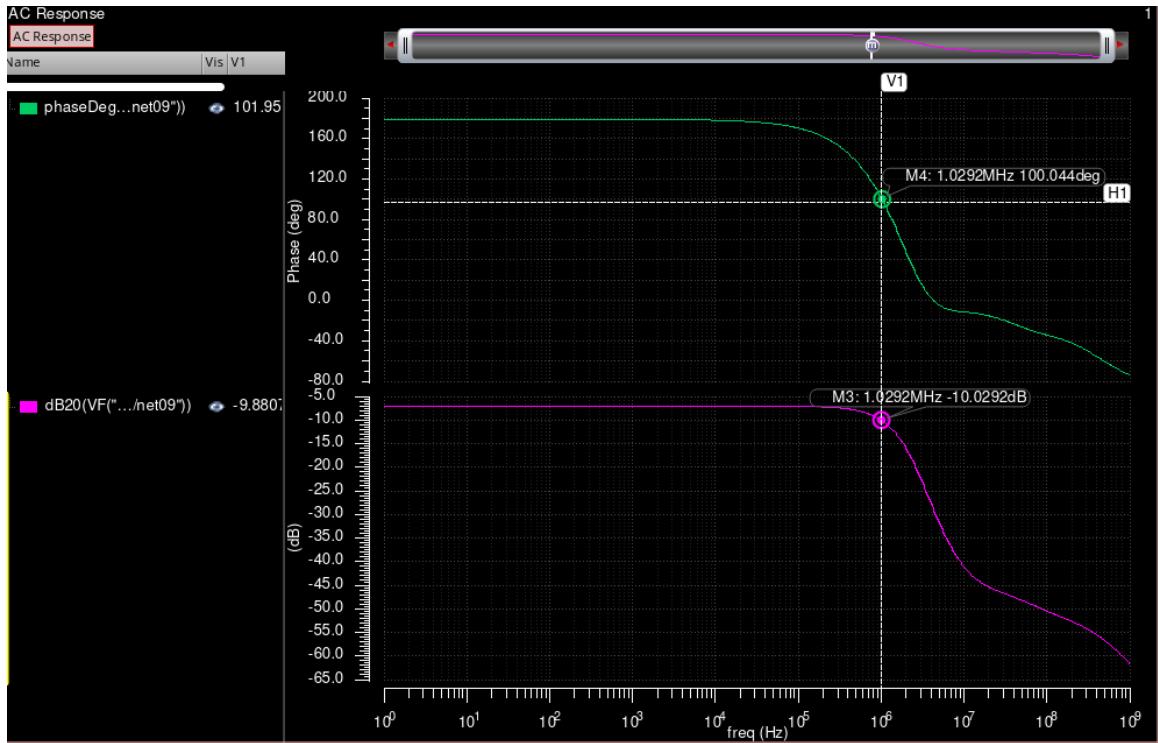
Final Schematic :



DC Sweep:

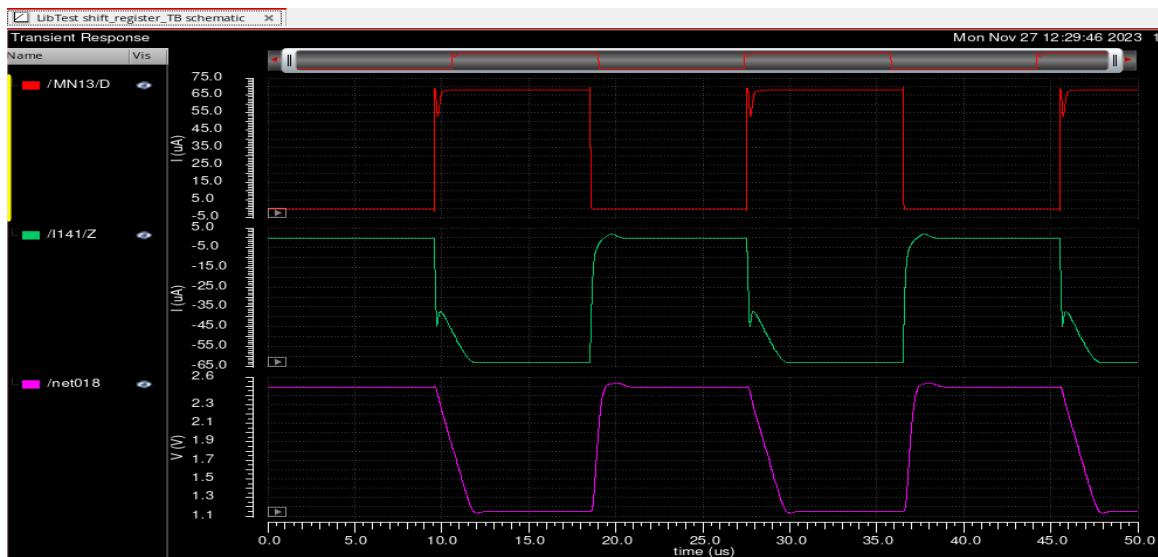


AC Sweep:



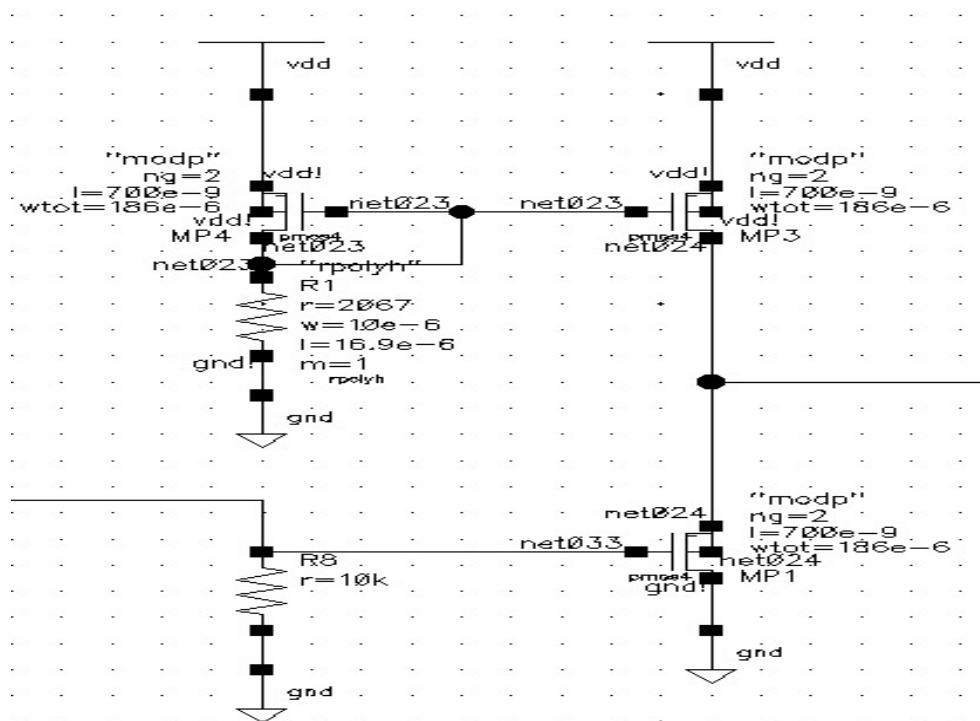
The Bandwidth of the Circuit is approximately 1MHz which meets the requirements.

When used in the actual circuit we get the following waveform.



The settling time isn't enough. Hence using a Voltage Buffer with resistor to ground changes the voltage according to the input current.

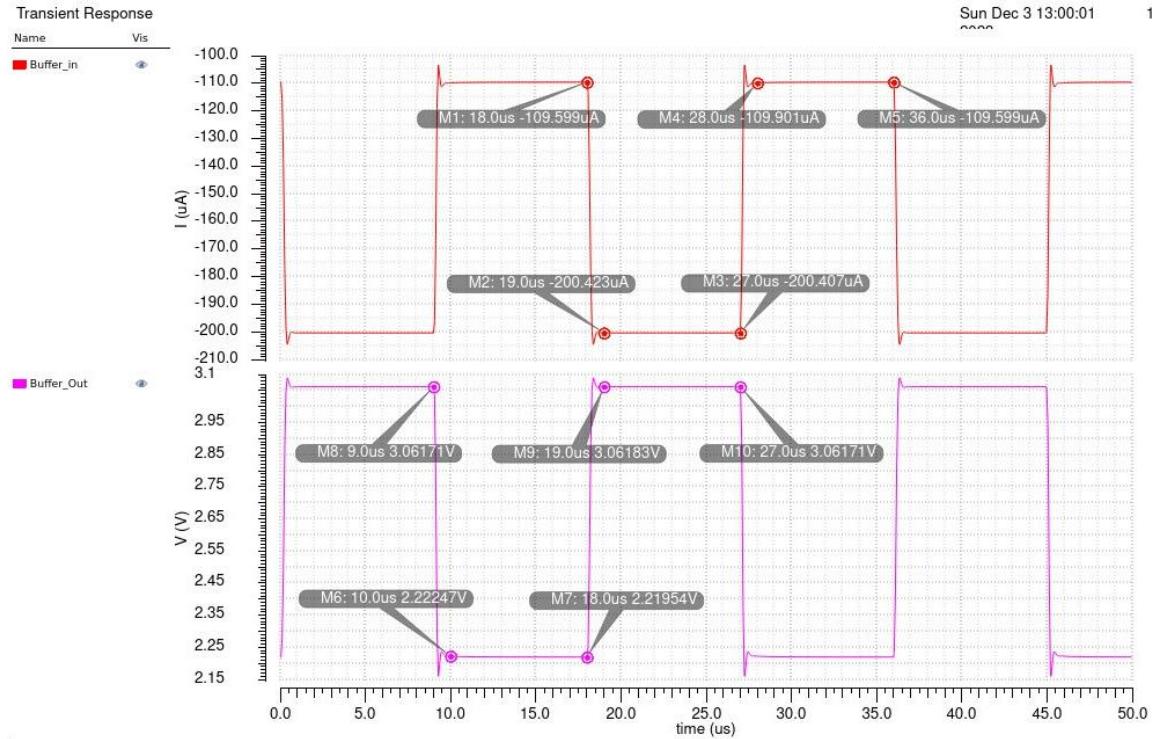
Alternate Circuit (The Buffer Circuit) :



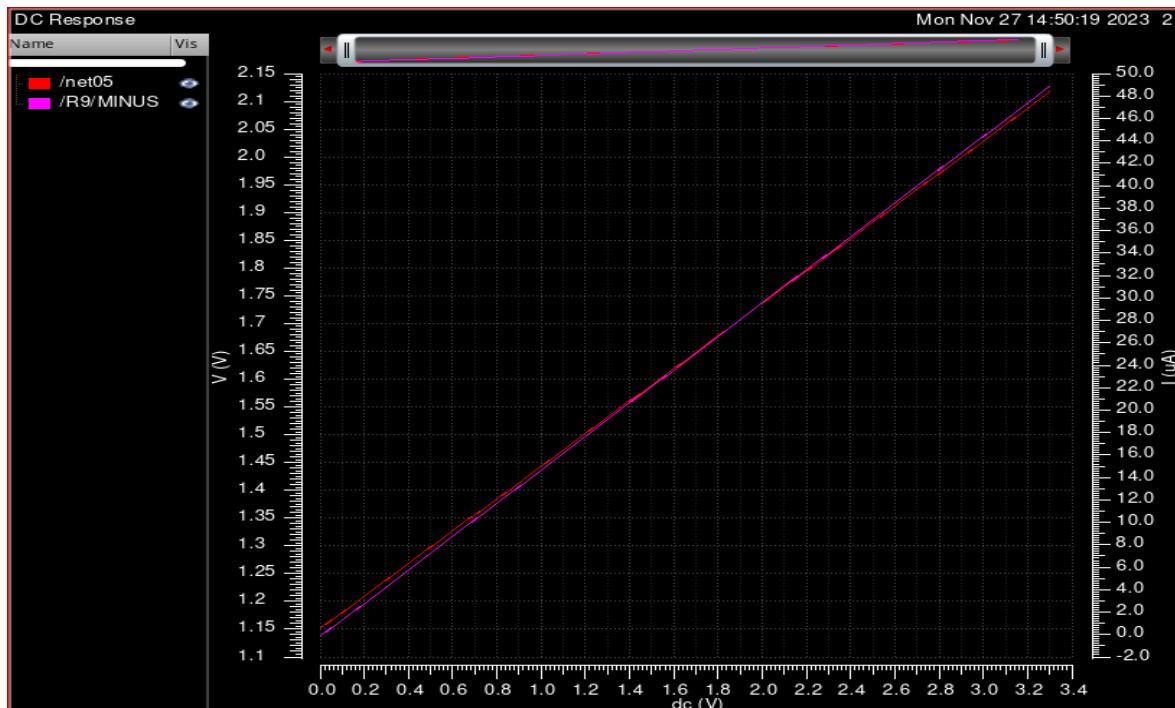
Input		Output		Bandwidth	Supply	
I _{MAX}	I _{MIN}	V _{MAX}	V _{MIN}	f _p	V _{DD}	V _{SS}

0A	52μA	1.678V	1.155V	1MHz	3.3V	0V
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Transient Analysis:



DC sweep :



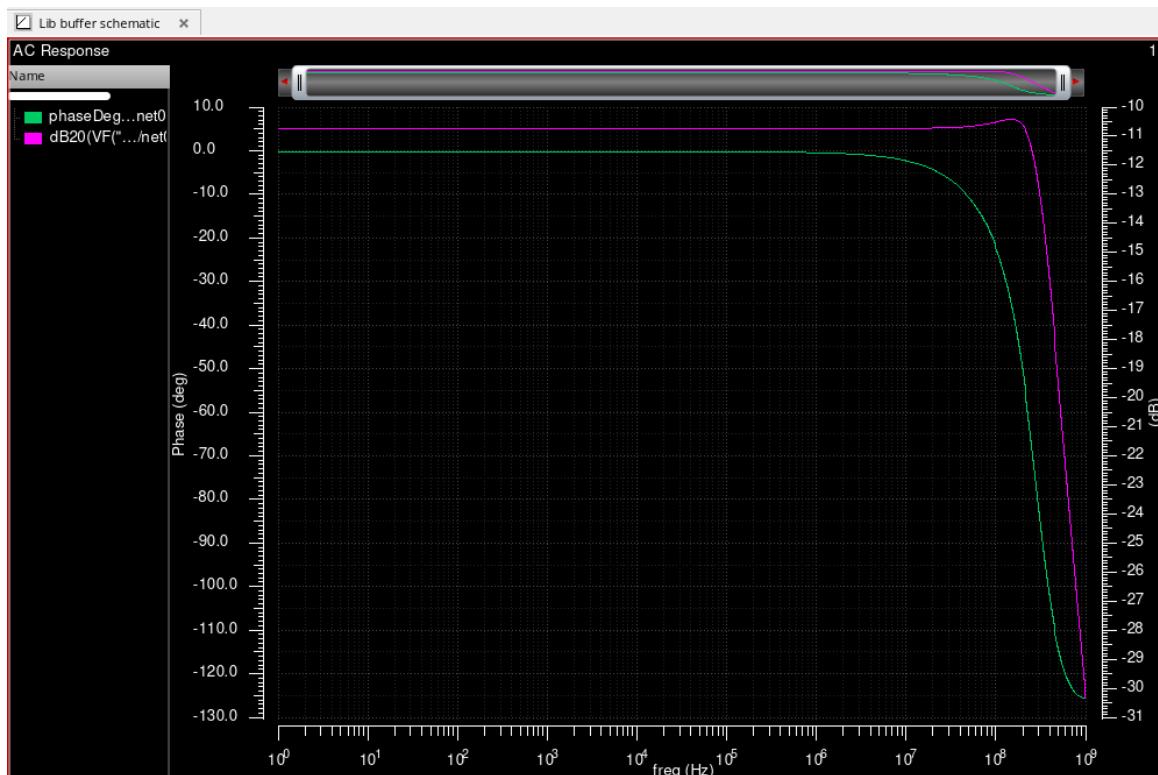
Linearity:

```
/net024 x      /net024 y
```

```
-----  
0      2.2193  
1.04e-06 2.2292  
2.08e-06 2.2392  
3.12e-06 2.2491  
4.16e-06 2.2591  
  
1.0000
```

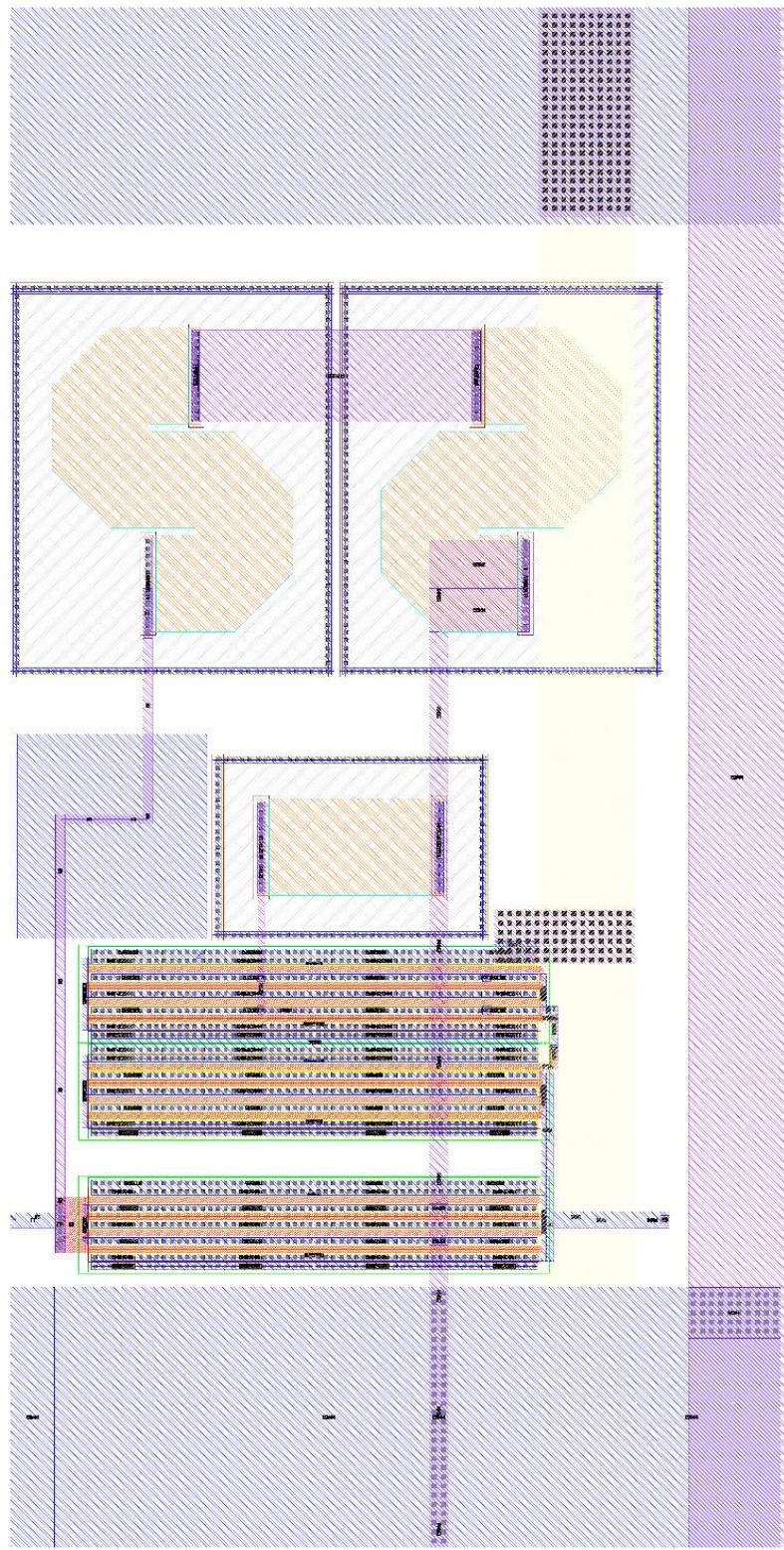
```
Rank 1: Linearity is 99.9998% for parameters /net024 X and /net024 Y  
Peak Voltage: 2.7134 Lowest Voltage: 2.2193
```

AC analysis:



This gives pretty good results. Good linearity and superior Frequency response.

Layout :



6. Conclusion

Hence to convert current to voltage i am going with a source follower ,the only thing am concerned is the Power consumption due to the heat generated by this 10k resistor. By referencing some industrial practices spreading (i.e) having 5 of a 2k resistors in series will have some improvement in the heat dissipation.

3.4 8-bit ADC with Serial Output via Shift Register

Abstract .

This report provides an overview of an 8-bit Analog-to-Digital Converter (ADC) and its integration with a serial output via a shift register. This is the system which we are going to integrate with our buffer. With attached outputs this report explains the linearity of the ADC.

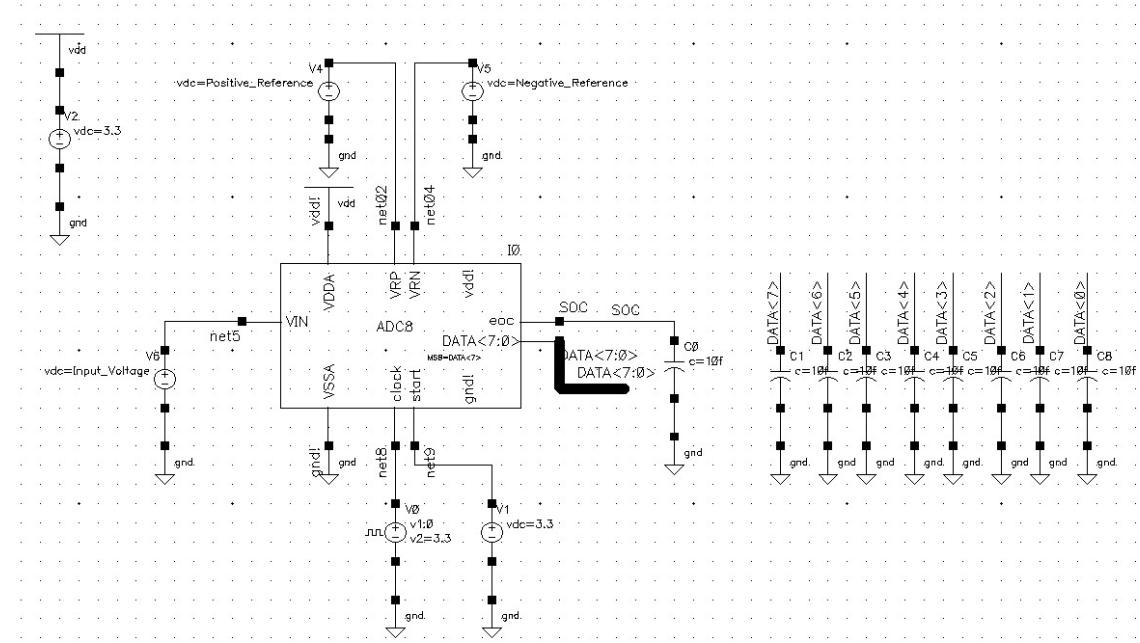
Introduction

Analog-to-digital converters (ADCs) are fundamental components in digital systems, converting analog signals to digital. This report focuses on 8-bit ADCs, offering high precision and suitability here. Understanding ADCs and their integration with shift registers for serial output is crucial in modern electronics.

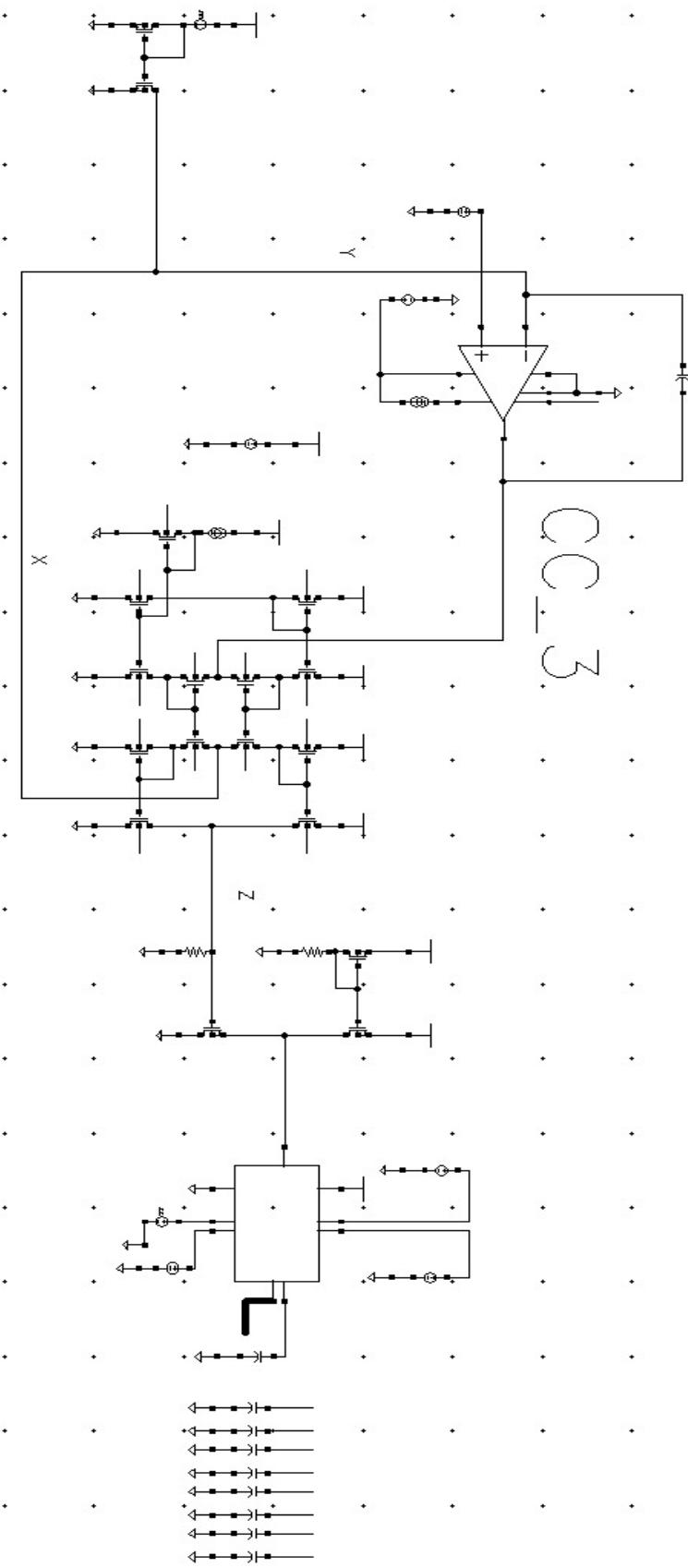
8-bit ADC

The 8-bit ADC converts analog signals into an 8-bit digital representation, providing 256 discrete levels.

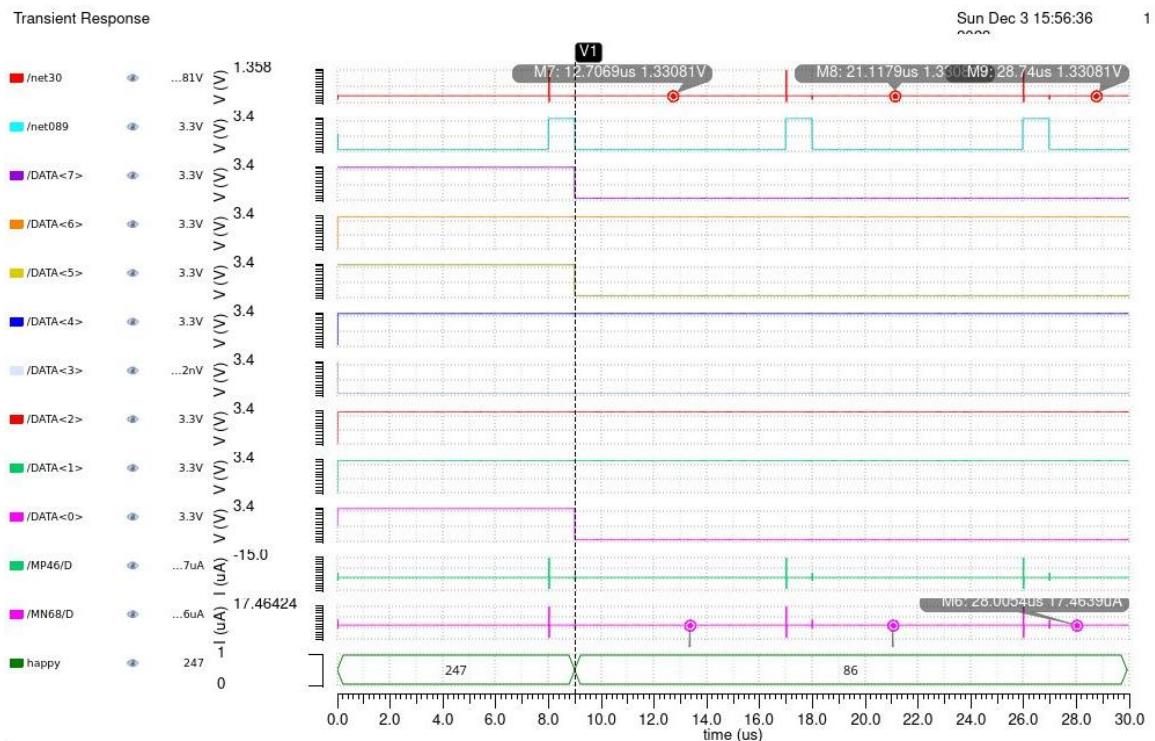
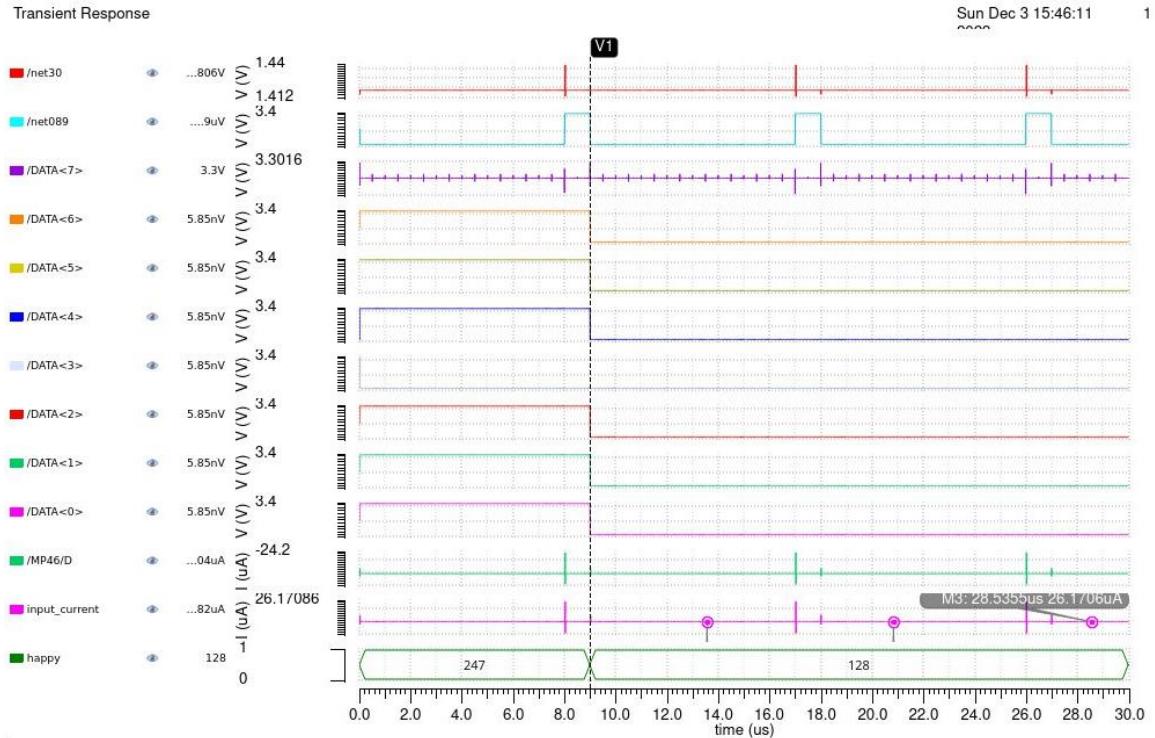
Configuration:

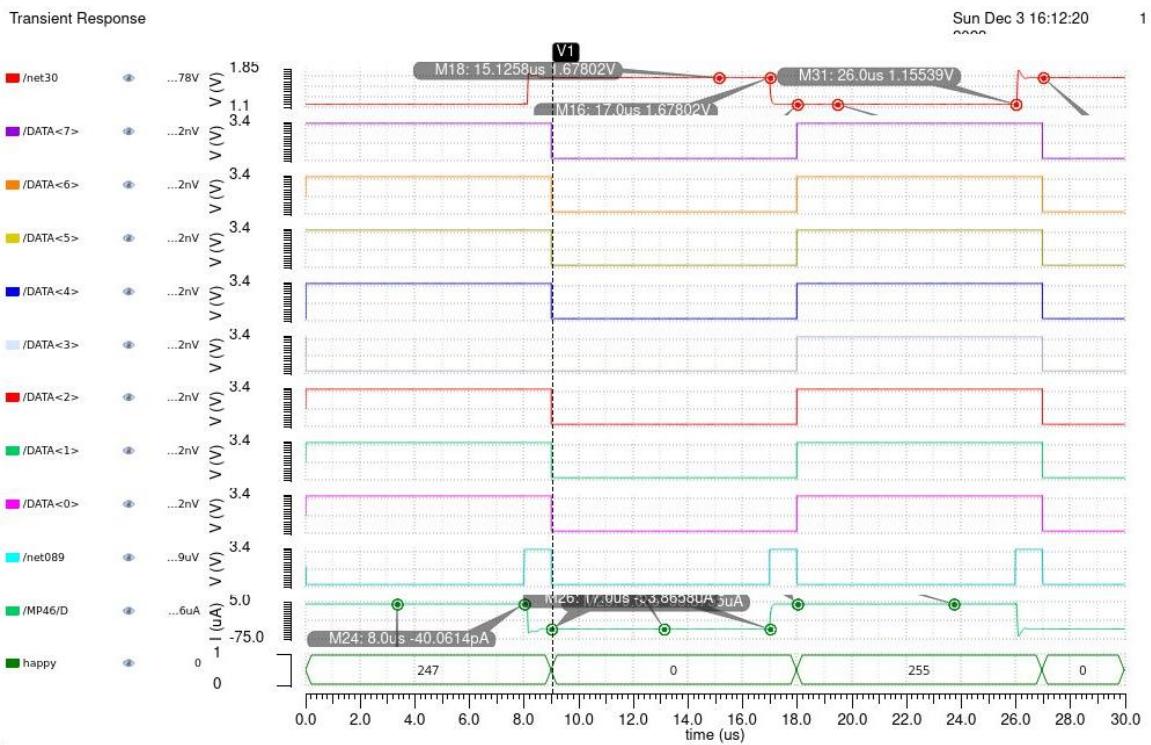
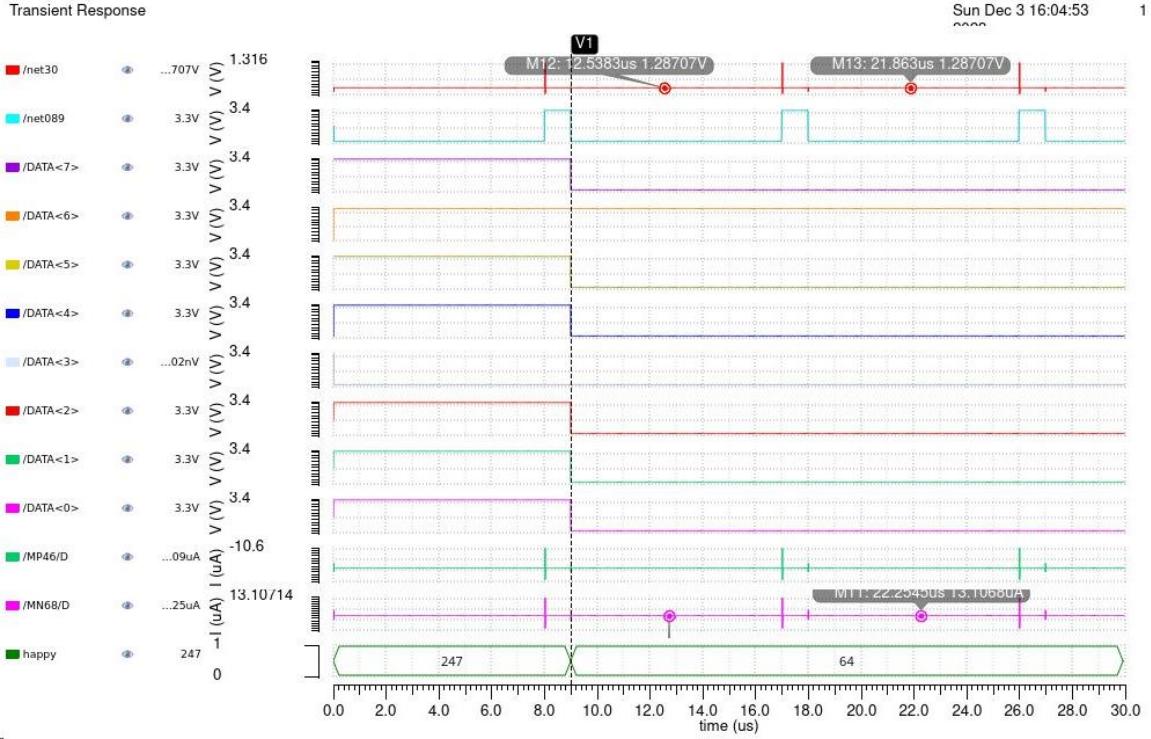


Based on Buffer Output (Input_Voltage = 1.678 V - 1.155 V) REFERENCE VOLTAGES for ADC is decided.



ADC Outputs:





The Transition For this instance where the highest to lowest (0- $52\mu\text{A}$) should be the worst case here however it proves us that its able to settle within $1\mu\text{s}$. Which puts us in a safe place.

These outputs gives us Perfect results :

$$0\mu\text{s} = 255,$$

$$255 \rightarrow 0 : 0 \rightarrow 52$$

$$52\mu\text{s} = 255,$$

$$0 = 255 : 52 = 0$$

$$26\mu\text{s} = 128,$$

$$26 \text{ is } 52/2 \text{ Hence } 256/2 = 128$$

$$13.00\mu\text{s} = 64,$$

$$13 \text{ is } 52/4 \text{ Hence } 256/4 = 64$$

$$17.333\mu\text{s} = 86$$

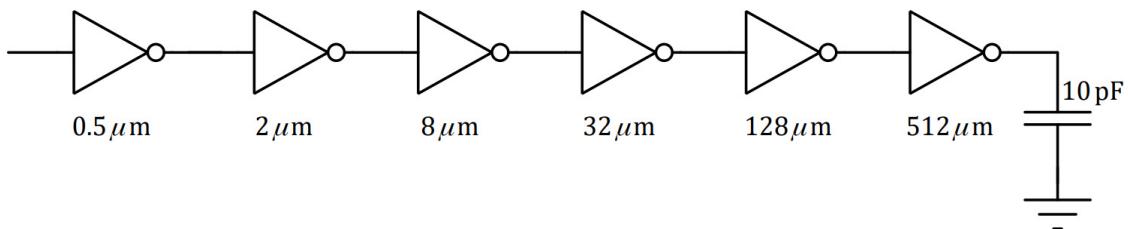
$$17.33 \text{ is } 52/3 \text{ Hence } 256/3 \approx 86$$

Which gives us really good results.

Shift Registers

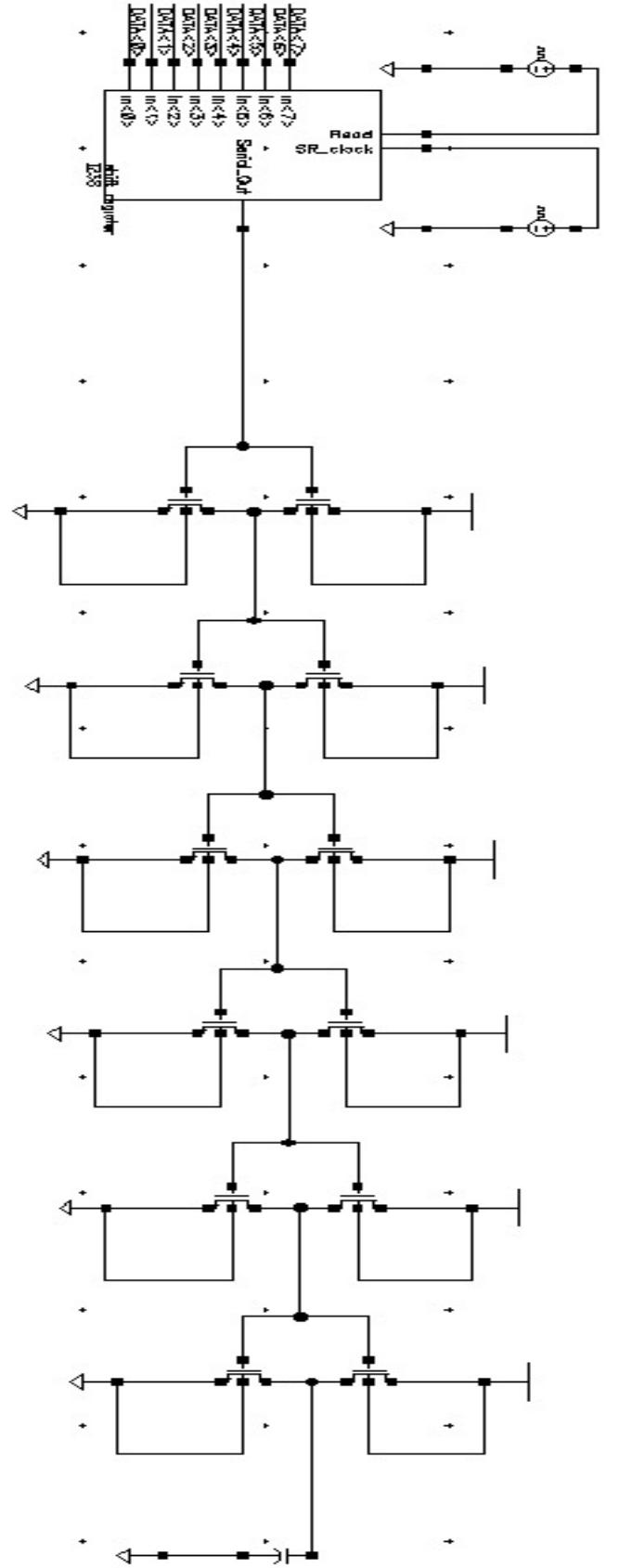
Shift registers are used for temporary data storage and transfer within digital circuits. They are particularly useful for converting parallel data from an ADC into a serial format.

Supper Buffer Calculation :

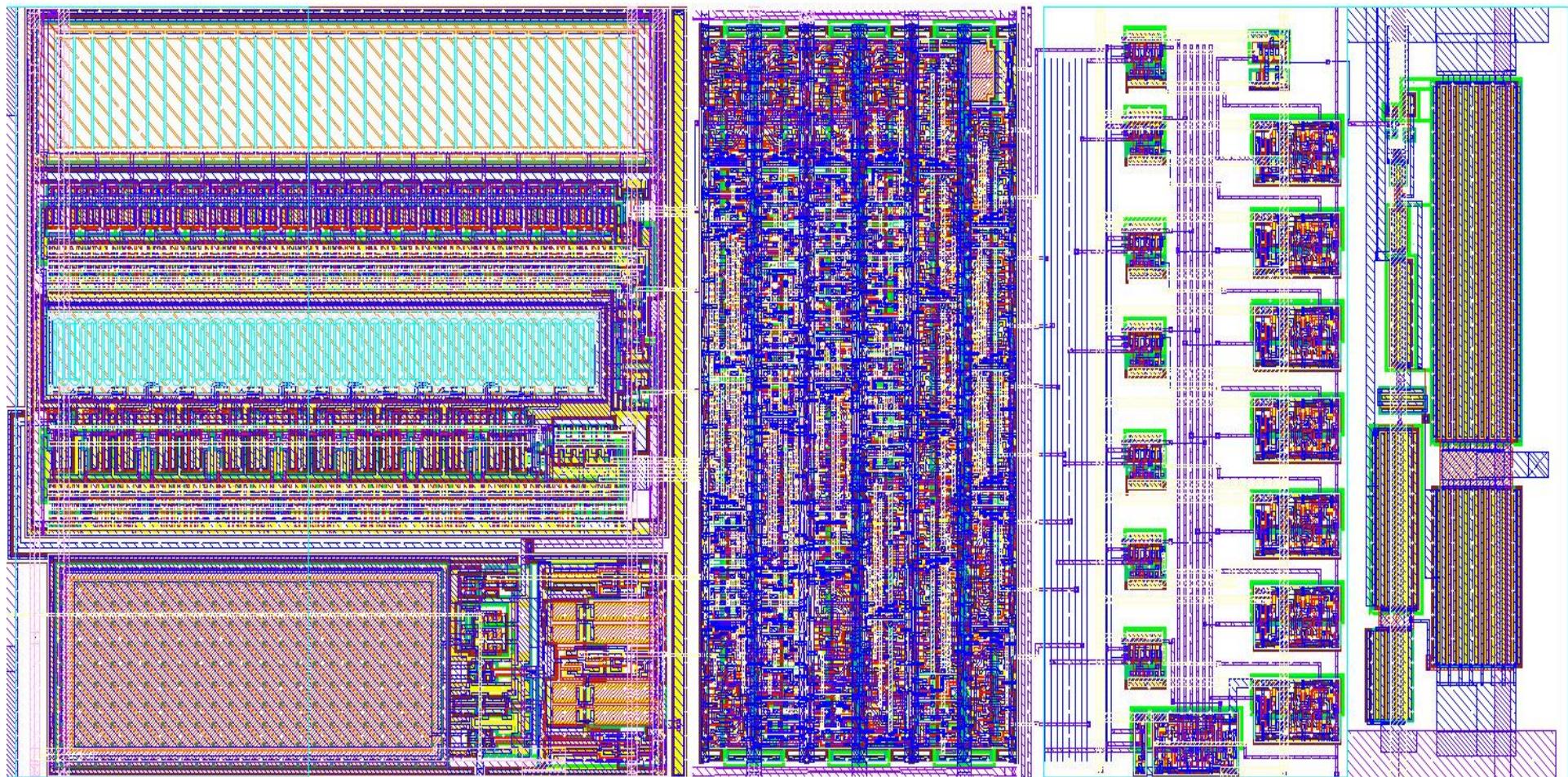


Delay:



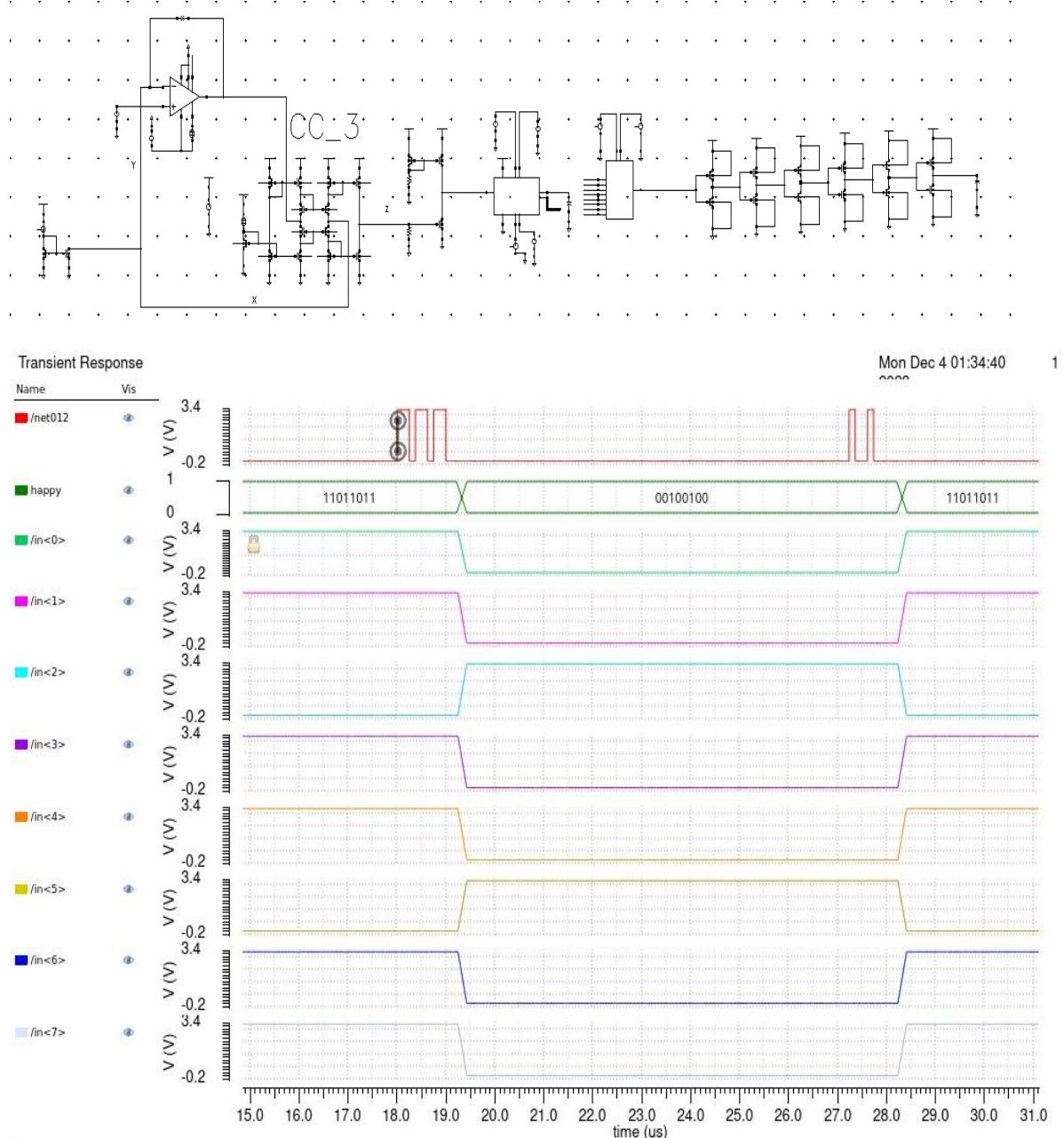


Layout :



System Overview

This section presents a block diagram of the 8-bit ADC system followed by a shift register, illustrating the flow of data from analog input to serial digital output.

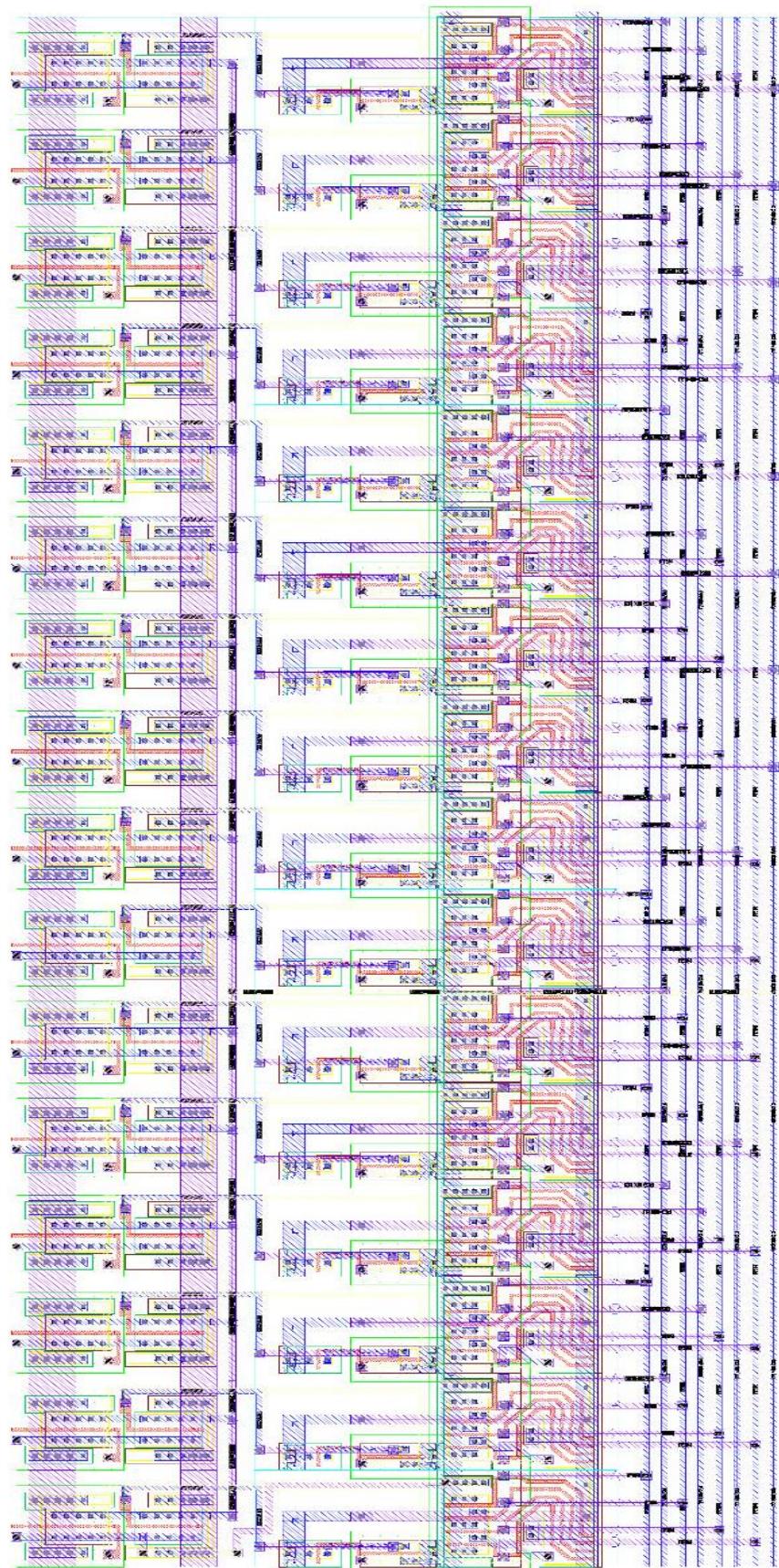


Rise Time : 157.3 ps.

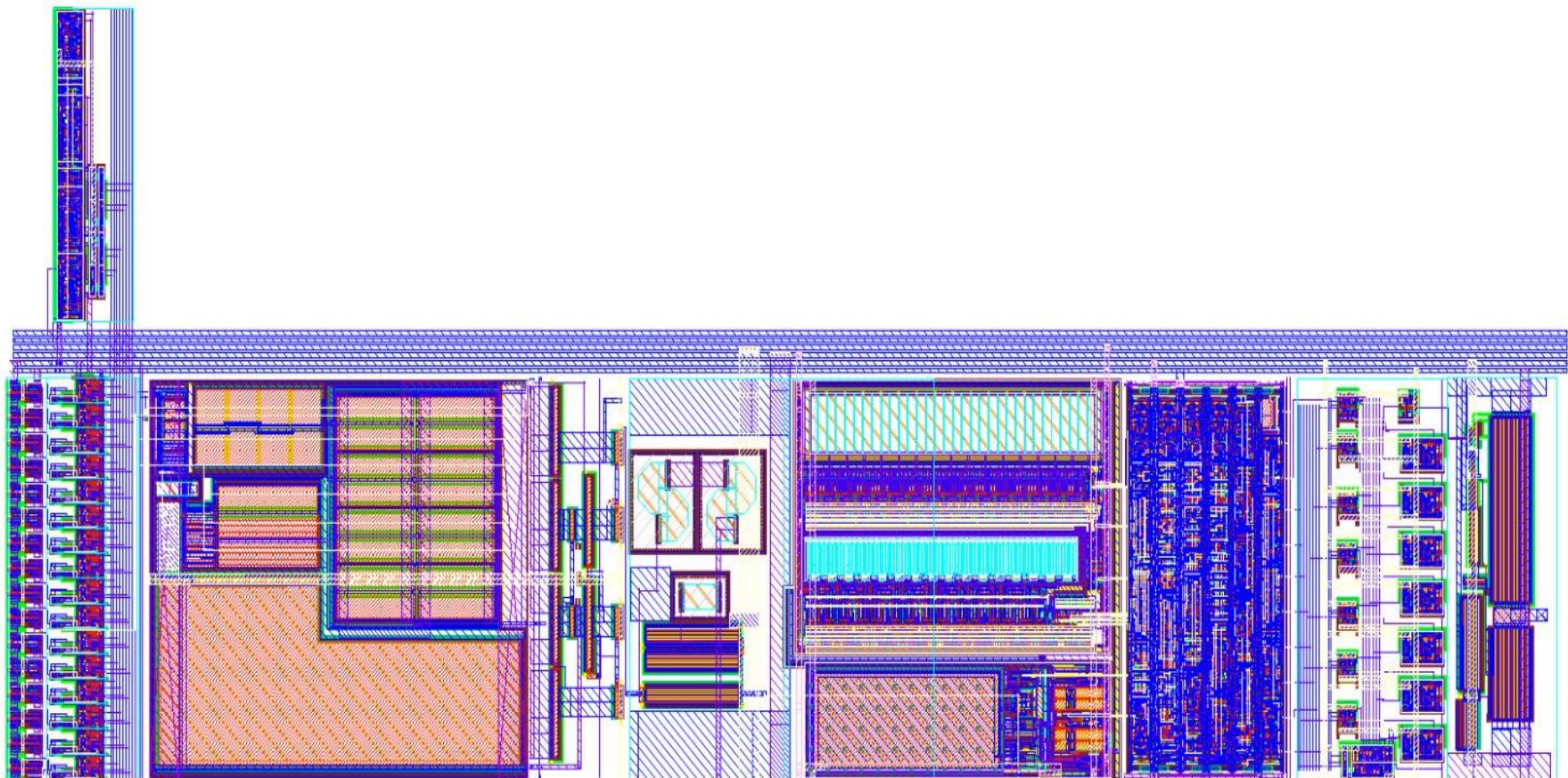
Conclusion

The integration of 8-bit ADCs with shift registers plays a crucial role in Analog to digital conversion part of the image sensor, enabling efficient data processing and transmission. And the attached output shows the linearity of the ADC.

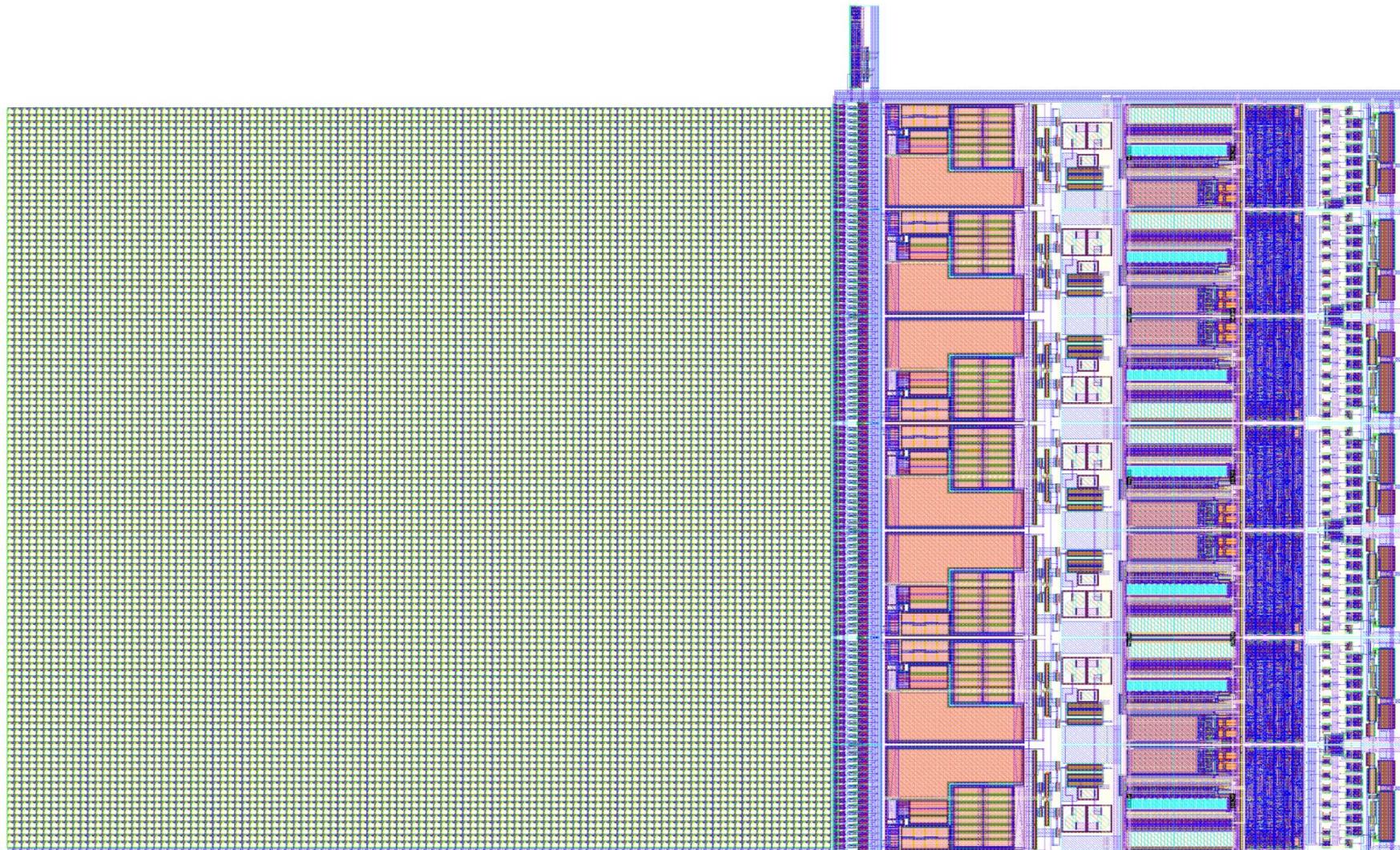
16 x 1 MUX (Transmission Gate):



Readout circuit :



Pixel Array with Readout circuit :



4. Conclusion:

The development of the Enhanced Current Mode 3T-APS Image Sensor, tailored with advanced specifications, marks a pivotal advancement in imaging technology, particularly in its integration with AI real-time processing hardware. This sensor's design and capabilities are not only suited for conventional imaging applications but also poised to play a crucial role in the burgeoning field of AI-driven image analysis.

Key Specifications and AI Integration:

- Resolution: $112 \times 112 = 12544$ pixels
- Pixel array: 1.12 mm x 1.12 mm
- Sensor Size: 1.90 mm x 1.27 mm
- FPS – 60
- Frame size: 0.012544 MB
- Well Capacity: 28,725
- SNR: 169.41
- Dynamic Range: 12.49 (Theoretical)
- SNR in decibels (dB): 44.58 dB.

Real-Time AI Processing: The integration of this sensor with AI hardware, specifically designed to mimic neuronal processing, allows for advanced real-time image processing. This includes capabilities like edge detection, pattern recognition, and adaptive learning directly on the sensor platform.

Efficiency in AI Computations: The compact size and efficient data handling of the sensor enable it to work seamlessly with AI hardware, ensuring that computational resources are optimally utilized for swift and accurate real-time processing.

Applications in Various Domains: This integration opens up a myriad of applications, ranging from advanced surveillance systems and autonomous vehicles to medical imaging and industrial automation, where real-time AI processing is crucial.

In conclusion, the Enhanced Current Mode 3T-APS Image Sensor, with its exceptional specifications, is not just an advanced imaging component but a key enabler in the realm of AI-driven real-time processing. Its integration with AI hardware, mimicking neuronal processing, sets a new standard in the synergy between imaging technology and artificial intelligence. This sensor is poised to revolutionize a wide array of applications, making significant contributions to the fields of AI and image processing technology.

5. FUTURE VISION:

Upon successful completion and testing of the enhanced Current Mode 2T APS, future work could focus on designing an AI-driven ASIC (Application-Specific Integrated Circuit) to further process the image data for features such as super-resolution, object detection, or noise reduction. The ASIC will feature a lightweight convolutional neural network (CNN) for real-time image enhancement tasks. Further research could also explore improving the design for greater power efficiency, incorporating more advanced AI-based image enhancement techniques on-chip, exploring the potential for scaling the design for multi-sensor applications, and developing advanced machine learning techniques for real-time image analysis.

Implementation of AI Models on Hardware Systems: AI models have been deployed on hardware systems using various methods, including the use of GPUs for parallel computation, dedicated ASICs, and FPGAs. Software libraries, such as TensorFlow Lite, ONNX Runtime, and TensorRT, have been used to optimize models for these platforms. In terms of super-resolution, much of the focus has been on optimizing the trade-off between resolution enhancement and computational and memory requirements, especially for real-time applications.

Current Status of the Field of VLSI Design for AI Applications: VLSI (Very Large Scale Integration) technology is evolving rapidly to meet the computational needs of AI workloads. This includes the development of specific AI accelerators, like Google's TPU, and startups like Graphcore and Cerebras Systems pushing the boundaries with novel architectures. There is also a move toward Edge AI, where AI processing is done on-device, necessitating efficient VLSI designs that balance performance, power, and area (PPA).

Challenges in Implementing AI Models on VLSI Chips: The primary challenge is the trade-off between model accuracy, computational resources, and power consumption. AI models, especially deep learning models, can have millions of parameters and require significant computational resources. Fitting this onto a VLSI chip that is power-efficient and within a reasonable size and cost is a significant challenge.

Furthermore, many AI models require high memory bandwidth, which can be a bottleneck in hardware designs.

Impact of AI on Super-Resolution in Image Sensors: AI has substantially improved the capabilities of super-resolution techniques, enabling the generation of high-resolution images from lower resolution inputs. This has applications in areas like surveillance, medical imaging, and satellite imaging, where high-resolution data is critical.

AI Models Suitable for VLSI Implementation: Simpler, less computationally intensive models, such as shallow neural networks, decision trees, or SVMs, are more straightforward to implement on VLSI chips. However, with sufficient optimization, it's also possible to implement more complex models like CNNs. The choice of model depends on the application and the available resources.

Future Trends for AI-Driven Super-Resolution Systems on VLSI Chips: We expect to see continued advancements in VLSI design for AI, with more efficient hardware accelerators, and increased edge computing capabilities. We may also see the development of new optimization techniques for deploying complex AI models on these platforms. In terms of super-resolution, we expect to see further improvements in image quality, real-time processing capabilities, and potentially new techniques that go beyond traditional deep learning.

Optimization of AI Models for Hardware Systems:

Quantization: Quantization is the process of reducing the precision of the numerical values in a model, such as weights and biases, from floating point numbers to lower precision numbers such as integers. This can lead to significant reductions in the computational resources required to perform inference with the model, and can also reduce memory footprint. The tradeoff is that there may be some loss of model accuracy due to the reduced numerical precision.

Pruning: Pruning is another technique for reducing model size and computational complexity. The basic idea is to remove connections in the model (for example, in a neural network) that contribute little to the model's output. By doing so, one can achieve a smaller, faster model with minimal loss in accuracy.

Knowledge Distillation: Knowledge distillation involves training a smaller, more computationally-efficient "student" model to mimic the behavior of a larger, more complex "teacher" model. This can result in a model with similar performance to the original, but which requires fewer computational resources to run.

Model Architecture Search: Model architecture search involves using techniques such as reinforcement learning or genetic algorithms to automatically discover optimized model architectures for a given task. This can include optimizing for hardware-specific constraints, such as memory footprint or computational throughput.

Hardware-Aware Neural Architecture Search (NAS): Traditional NAS often focuses on finding the optimal architecture to achieve the best performance without considering specific hardware properties. Hardware-Aware NAS considers hardware constraints, leading to models that are not only accurate but also efficient on specific hardware platforms.

Use of specialized hardware: Some AI models can be optimized by using specialized hardware accelerators such as GPUs (Graphical Processing Units), TPUs (Tensor Processing Units), and FPGAs (Field-Programmable Gate Arrays). These hardware platforms can greatly accelerate specific types of mathematical operations that are common in AI models.

Fusing Layers and Operations: Certain operations and layers in a neural network can be fused together to form a single operation, reducing the computational overhead and improving performance on specific hardware.

Software Optimization: Using libraries specifically designed to optimize AI models for particular hardware, like TensorRT for Nvidia GPUs, or oneDNN for Intel CPUs, can significantly improve performance.

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