DSP56301 Rev. 10, 7/2006

# **DSP56301**

#### 24-Bit Digital Signal Processor

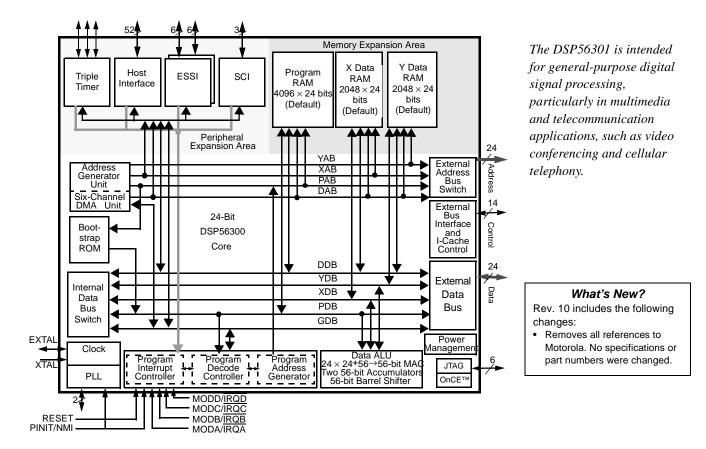


Figure 1. DSP56301 Block Diagram

The DSP56301 is a member of the DSP56300 core family of programmable CMOS Digital Signal Processors (DSPs). This family uses a high-performance, single clock cycle per instruction engine. Significant architectural features of the DSP56300 core family include a barrel shifter, 24-bit addressing, instruction cache, and DMA. The DSP56301 offers 80/100 MIPS using an internal 80/100 MHz clock at 3.0–3.6 volts. The DSP56300 core family offers a rich instruction set and low power dissipation, as well as increasing levels of speed and power, enabling wireless, telecommunications, and multimedia products.





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### **Data Sheet Conventions**

OVERBAR	Indicates a signal that is active when pulled low (For example, the RESET pin is active when low.)			
"asserted"	Means that a high true	e (active high) signal is	high or that a low true (acti	ve low) signal is low
"deasserted"	Means that a high true	e (active high) signal is	low or that a low true (activ	ve low) signal is high
Examples:	Signal/Symbol Logic State Signal State Voltage			
	PIN	True	Asserted	$V_{IL}/V_{OL}$
	PIN	False	Deasserted	$V_{IH}/V_{OH}$
	PIN	True	Asserted	$V_{IH}/V_{OH}$

False Note: Values for  $V_{IL}$ ,  $V_{OL}$ ,  $V_{IH}$ , and  $V_{OH}$  are defined by individual product specifications.

Deasserted

 $V_{IL}/V_{OL}$ 



#### **DSP56301 Features**

#### **High-Performance DSP56300 Core**

- 80/100 million instructions per second (MIPS) with a 80/100 MHz clock at 3.0-3.6 V
- Object code compatible with the DSP56000 core with highly parallel instruction set
- Data Arithmetic Logic Unit (Data ALU) with fully pipelined 24 × 24-bit parallel Multiplier-Accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control
- Program Control Unit (PCU) with Position Independent Code (PIC) support, addressing modes
  optimized for DSP applications (including immediate offsets), internal instruction cache
  controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast
  auto-return interrupts
- Direct Memory Access (DMA) with six DMA channels supporting internal and external accesses; one-, two-, and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals
- Phase Lock Loop (PLL) allows change of low-power Divide Factor (DF) without loss of lock and output clock with skew elimination
- Hardware debugging support including On-Chip Emulation (OnCE™) module, Joint Test Action Group (JTAG) Test Access Port (TAP)

#### **Internal Peripherals**

- 32-bit parallel PCI/Universal Host Interface (HI32), PCI Rev. 2.1 compliant with glueless interface to other DSP563xx buses or ISA interface requiring only 74LS45-style buffers
- Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)
- Serial communications interface (SCI) with baud rate generator
- Triple timer module
- Up to forty-two programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled

#### **Internal Memories**

- 3 K × 24-bit bootstrap ROM
- 8 K × 24-bit internal RAM total
- Program RAM, Instruction Cache, X data RAM, and Y data RAM sizes are programmable:

Program RAM Size	Instruction Cache Size	X Data RAM Size	Y Data RAM Size	Instruction Cache	Switch Mode
$4096 \times 24 \text{ bits}$	0	$2048 \times 24 \text{ bits}$	$2048 \times 24 \text{ bits}$	disabled	disabled
$3072 \times 24 \text{ bits}$	$1024 \times 24$ -bit	$2048 \times 24 \text{ bits}$	$2048 \times 24 \text{ bits}$	enabled	disabled
$2048 \times 24 \text{ bits}$	0	$3072 \times 24 \text{ bits}$	$3072 \times 24 \text{ bits}$	disabled	enabled
1024 × 24 bits	1024 × 24-bit	3072 × 24 bits	3072 × 24 bits	enabled	enabled



#### **External Memory Expansion**

- Data memory expansion to two 16 M × 24-bit word memory spaces in 24-Bit mode or two 64 K × 16-bit memory spaces in 16-Bit Compatibility mode
- Program memory expansion to one 16 M  $\times$  24-bit words memory space in 24-Bit mode or 64 K  $\times$  16-bit in 16-Bit Compatibility mode
- · External memory expansion port
- Chip Select Logic for glueless interface to SRAMs
- Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)

#### **Reduced Power Dissipation**

- Very low-power CMOS design
- Wait and Stop low-power standby modes
- Fully static design specified to operate down to 0 Hz (dc)
- Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)

#### **Packaging**

The DSP56301 is available in a 208-pin thin quad flat pack (TQFP) or a 252-pin molded array process-ball grid array (MAP-BGA) package. Both packages are available in lead-bearing and lead-free versions.

### **Target Applications**

Examples of target applications include:

- · Wireless and wireline infrastructure applications
- Multi-channel wireless local loop systems
- · DSP resource boards
- · High-speed modem banks
- · Packet telephony

#### **Product Documentation**

The three documents listed in the following table are required for a complete description of the DSP56301 and are necessary to design properly with the part. Documentation is available from the following sources. (See the back cover for detailed information.)

- A local Freescale distributor
- · A Freescale semiconductor sales office
- A Freescale Literature Distribution Center
- The World Wide Web (WWW)

Table 1. DSP56301 Documentation

Name	Description	Order Number	
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM/AD	
DSP56301 User's Manual	Detailed functional description of the DSP56301 memory configuration, operation, and register programming	DSP56301UM/D	
DSP56301 Technical Data	DSP56301 features list and physical, electrical, timing, and package specifications	DSP56301	

DSP56301 Technical Data, Rev. 10

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# Signals/Connections

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The DSP56301 input and output signals are organized into functional groups, as shown in **Table 1-1** and illustrated in **Figure 1-1**. The DSP56301 operates from a 3 V supply; however, some of the inputs can tolerate 5 V. A special notice for this feature is added to the signal descriptions of those inputs.

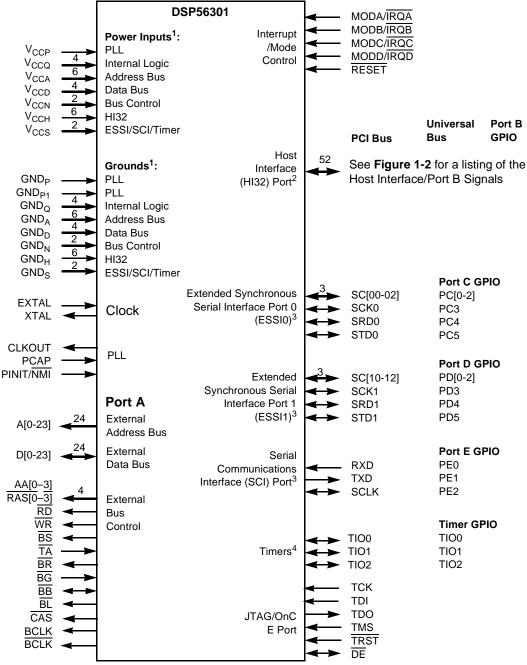
Table 1-1. DSP56301 Functional Signal Groupings

Functional Group	Sign	ber of als by ge Type	Detailed Description	
		TQFP	MAP- BGA	
Power (V <sub>CC</sub> ) <sup>1</sup>		25	45	Table 1-2
Ground (GND) <sup>1</sup>		26	38	Table 1-3
Clock		2	2	Table 1-4
PLL		3	3	Table 1-5
Address Bus	2	24	24	Table 1-6
Data Bus	Port A <sup>2</sup>	24	24	Table 1-7
Bus Control			15	Table 1-8
Interrupt and Mode Control		5	5	Table 1-9
Host Interface (HI32)	Port B <sup>3</sup>	52	52	Table 1-11
Enhanced Synchronous Serial Interface (ESSI)	Ports C and D <sup>4</sup>	12	12	Table 1-12 and Table 1-13
Serial Communication Interface (SCI)	Port E <sup>5</sup>	3	3	Table 1-14
Timer			3	Table 1-15
JTAG/OnCE Port			6	Table 1-16

#### Notes:

- The number of available power and ground signals is package-dependent. In the TQFP package specific pins are dedicated
  internally to device subsystems. In the MAP-BGA package, power and ground connections (except those providing PLL
  power) connect to internal power and ground planes, respectively.
- 2. Port A signals define the external memory interface port, including the external address bus, data bus, and control signals.
- 3. Port B signals are the HI32 port signals multiplexed with the GPIO signals.
- 4. Port C and D signals are the two ESSI port signals multiplexed with the GPIO signals.
- **5.** Port E signals are the SCI port signals multiplexed with the GPIO signals.
- **6.** Each device also includes several no connect (NC) pins. The number of NC connections is package-dependent: the TQFP has 9 NCs and the MAP-BGA has 20 NCs. Do not connect any line, component, trace, or via to these pins. See **Chapter 3** for details.

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Notes:

- Power and ground connections are shown for the TQFP package. The MAP-BGA package uses one V<sub>CCP</sub> for the PLL power input and 44 V<sub>CC</sub> pins that connect to an internal power plane. The MAP-BGA package uses two ground connections for the PLL (GND<sub>P</sub> and GND<sub>P1</sub>) and 36 GND pins that connect to an internal ground plane.
- 2. The HI32 port supports PCI and non-PCI bus configurations. Twenty-four HI32 signals can also be configured as GPIO signals (PB[0–23]).
- The ESSI0, ESSI1, and SCI signals are multiplexed with the Port C GPIO signals (PC[0-5]), Port D GPIO signals (PD[0-5]), and Port E GPIO signals (PE[0-2]), respectively.
- 4. TIO[0-2] can be configured as GPIO signals.

Figure 1-1. Signals Identified by Functional Group

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				Host Port (HP)
DSP56301	PCI Bus	Universal Bus	Port B GPIO	Reference
	HAD0	HA3	PB0	HP0
	HAD1	HA4	PB1	HP1
	HAD2	HA5	PB2	HP2
	HAD3	HA6	PB3	HP3
	HAD4	HA7	PB4	HP4
	HAD5	HA8	PB5	HP5
	HAD6	HA9	PB6	HP6
	HAD7	HA10	PB7	HP7
	HAD8	HD0	PB8	HP8
	HAD9	HD1	PB9	HP9
	HAD10	HD2	PB10	HP10
	HAD11	HD3	PB11	HP11
	HAD12	HD4	PB12	HP12
	HAD13	HD5	PB13	HP13
	HAD14	HD6	PB14	HP14
	HAD15	HD7	PB15	HP15
	HC0/HBE0	HA0	PB16	HP16
	HC1/HBE1	HA1	PB17	HP17
	HC2/HBE2	HA2	PB18	HP18
	HC3/HBE3	Tie to pull-up or V <sub>CC</sub>	PB19	HP19
Host Interface (HI32)/	HTRDY	HDBEN	PB20	HP20
	HIRDY	HDBDR	PB21	HP21
Port B Signals	HDEVSEL	HSAK	PB22	HP22
	HLOCK	HBS	PB23	HP23
	HPAR	HDAK	Internal disconnect	HP24
	HPERR	HDRQ	Internal disconnect	HP25
	HGNT	HAEN	Internal disconnect	HP26
	HREQ	HTA	Internal disconnect	HP27
	HSERR	HIRQ	Internal disconnect	HP28
	HSTOP	HWR/HRW	Internal disconnect	HP29
	HIDSEL	HRD/HDS	Internal disconnect	HP30
	HFRAME	Tie to pull-up or $V_{CC}$	Internal disconnect	HP31
	HCLK	Tie to pull-up or $V_{CC}$	Internal disconnect	HP32
	HAD16	HD8	Internal disconnect	HP33
	HAD17	HD9	Internal disconnect	HP34
	HAD18	HD10	Internal disconnect	HP35
	HAD19	HD11	Internal disconnect	HP36
	HAD20	HD12	Internal disconnect	HP37
	HAD21	HD13	Internal disconnect	HP38
	HAD22	HD14	Internal disconnect	HP39
	HAD23	HD15	Internal disconnect	HP40
	HAD24	HD16	Internal disconnect	HP41
	HAD25	HD17	Internal disconnect	HP42
	HAD26	HD18	Internal disconnect	HP43
	HAD27	HD19	Internal disconnect	HP44
	HAD28	HD20	Internal disconnect	HP45
	HAD29	HD21	Internal disconnect	HP46
	HAD30	HD22	Internal disconnect	HP47
	HAD31	HD23	Internal disconnect	HP48
	HRST	HRST	Internal disconnect	HP49
	HINTA	HINTA	Internal disconnect	HP50
	PVCL	Leave unconnected	Leave unconnected	PVCL

**Note:** HPxx is a reference only and is not a signal name. GPIO references formerly designated as HIOxx have been renamed PBxx for consistency with other Freescale DSPs.

Figure 1-2. Host Interface/Port B Detail Signal Diagram

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## 1.1 Power

Table 1-2. Power Inputs

Power Name	Description
V <sub>CCP</sub>	PLL Power Isolated power for the Phase Lock Loop (PLL). The voltage should be well-regulated and the input should be provided with an extremely low impedance path to the V <sub>CC</sub> power rail.
Vccq	Quiet Power Isolated power for the internal processing logic. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>CCA</sub>	Address Bus Power Isolated power for sections of the address bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>CCD</sub>	Data Bus Power Isolated power for sections of the data bus I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>CCN</sub>	Bus Control Power Isolated power for the bus control I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>ССН</sub>	Host Power Isolated power for the HI32 I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
V <sub>ccs</sub>	ESSI, SCI, and Timer Power Isolated power for the ESSI, SCI, and timer I/O drivers. This input must be tied externally to all other chip power inputs. The user must provide adequate external decoupling capacitors.
	lesignations are package-dependent. Some packages connect all $V_{CC}$ inputs except $V_{CCP}$ to each other internally. On ackages, all power input except $V_{CCP}$ are labeled $V_{CC}$ .

## 1.2 Ground

Table 1-3. Grounds

Ground Name	Description		
GND <sub>P</sub>	PLL Ground Ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground. $V_{CCP}$ should be bypassed to GND <sub>P</sub> by a 0.47 $\mu$ F capacitor located as close as possible to the chip package.		
GND <sub>P1</sub>	PLL Ground 1 Ground dedicated for PLL use. The connection should be provided with an extremely low-impedance path to ground.		
GND <sub>Q</sub>	Quiet Ground Isolated ground for the internal processing logic. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.		
GND <sub>A</sub>	Address Bus Ground Isolated ground for sections of the address bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.		
GND <sub>D</sub>	Data Bus Ground Isolated ground for sections of the data bus I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.		

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#### Table 1-3. Grounds

Ground Name	Description			
GND <sub>N</sub>	Bus Control Ground Isolated ground for the bus control I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.			
GND <sub>H</sub>	Host Ground Isolated ground for the HI32 I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.			
GND <sub>S</sub>	ESSI, SCI, and Timer Ground Isolated ground for the ESSI, SCI, and timer I/O drivers. This connection must be tied externally to all other chip ground connections. The user must provide adequate external decoupling capacitors.			
Note: These designations are package-dependent. Some packages connect all GND inputs except GND <sub>P</sub> and GND <sub>P1</sub> to each other internally. On those packages, all ground connections except GND <sub>P</sub> and GND <sub>P1</sub> are labeled GND.				

# 1.3 Clock

Table 1-4. Clock Signals

Signal Name	Туре	State During Reset	Signal Description
EXTAL	Input	Input	External Clock/Crystal Input Interfaces the internal crystal oscillator input to an external crystal or an external clock.
XTAL	Output	Chip-driven	Crystal Output Connects the internal crystal oscillator output to an external crystal. If an external clock is used, leave XTAL unconnected.

# 1.4 Phase Lock Loop (PLL)

 Table 1-5.
 Phase Lock Loop Signals

Signal Name	Туре	State During Reset	Signal Description
CLKOUT	Output	Chip-driven	Clock Output Provides an output clock synchronized to the internal core clock phase.  If the PLL is enabled and both the multiplication and division factors equal one, then CLKOUT is also synchronized to EXTAL.  If the PLL is disabled, the CLKOUT frequency is half the frequency of EXTAL.
PCAP	Input	Input	PLL Capacitor Connects an off-chip capacitor to the PLL filter. Connect one capacitor terminal to PCAP and the other terminal to $V_{CCP}$ .  If the PLL is not used, PCAP can be tied to $V_{CC}$ , GND, or left floating.

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 Table 1-5.
 Phase Lock Loop Signals (Continued)

Signal Name	Туре	State During Reset	Signal Description
PINIT/NMI	Input	Input	PLL Initial/Non-Maskable Interrupt During assertion of RESET, the value of PINIT/NMI is written into the PLL Enable (PEN) bit of the PLL control register, determining whether the PLL is enabled or disabled. After RESET deassertion and during normal instruction processing, the PINIT/NMI Schmitt-trigger input is a negative-edge-triggered Non-Maskable Interrupt (NMI) request internally synchronized to CLKOUT.  PINIT/NMI can tolerate 5 V.

## 1.5 External Memory Expansion Port (Port A)

Note: When the DSP56301 enters a low-power stand-by mode (Stop or Wait), it releases bus mastership and tristates the relevant Port A signals: A[0–23], D[0–23], AA0/RAS0–AA3/RAS3, RD, WR, BB, CAS, BCLK, and BCLK. If hardware refresh of external DRAM is enabled, Port A exits the Wait mode to allow the refresh to occur and then returns to the Wait mode.

#### 1.5.1 External Address Bus

Table 1-6. External Address Bus Signals

Signal Name	Туре	State During Reset	Signal Description
A[0-23]	Output	Tri-stated	Address Bus When the DSP is the bus master, A[0–23] specify the address for external program and data memory accesses. Otherwise, the signals are tri-stated. To minimize power dissipation, A[0–23] do not change state when external memory spaces are not being accessed.

#### 1.5.2 External Data Bus

Table 1-7. External Data Bus Signals

Signal Name	Туре	State During Reset	Signal Description
D[0-23]	Input/Output	Tri-stated	<b>Data Bus</b> When the DSP is the bus master, D[0–23] provide the bidirectional data bus for external program and data memory accesses. Otherwise, D[0–23] are tristated.

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### 1.5.3 External Bus Control

Table 1-8. External Bus Control Signals

			External bus control signals
Signal Name	Туре	State During Reset	Signal Description
AA0/RAS0- AA3/RAS3	Output	Tri-stated	Address Attribute or Row Address Strobe As AA, these signals function as chip selects or additional address lines. Unlike address lines, however, the AA lines do not hold their state after a read or write operation. As RAS, these signals can be used for Dynamic Random Access Memory (DRAM) interface. These signals have programmable polarity.
RD	Output	Tri-stated	Read Enable When the DSP is the bus master, RD is asserted to read external memory on the data bus (D[0–23]). Otherwise, RD is tri-stated.
WR	Output	Tri-stated	Write Enable When the DSP is the bus master, WR is asserted to write external memory on the data bus (D[0–23]). Otherwise, WR is tri-stated.
TA	Input	Ignored Input	Transfer Acknowledge  If the DSP56301 is the bus master and there is no external bus activity, or the DSP56301 is not the bus master, the TA input is ignored. The TA input is a Data Transfer Acknowledge (DTACK) function that can extern an external bus cycle indefinitely. Any number of wait states (1, 2,, infinity) can be added to the wait states inserted by the BCR by keeping TA deasserted. In typical operation, TA is deasserted at the start of a bus cycle, asserted to enable completion of the bus cycle, and deasserted before the next bus cycle. The current bus cycle completes one clock period after TA is asserted synchronous to CLKOUT. The number of wait states is determined by the TA input or by the Bus Control Register (BCR), whichever is longer. The BCR can set the minimum number of wait states in external bus cycles.  To use the TA functionality, the BCR must be programmed to at least one wait state. A zero wait state access cannot be extended by TA deassertion; otherwise improper operation may result. TA can operate synchronously or asynchronously, depending on the setting of the TAS bit in the Operating Mode Register (OMR).  TA functionality cannot be used during DRAM-type accesses; otherwise improper operation may result.
BR	Output	Output (deasserted)	Bus Request Asserted when the DSP requests bus mastership and deasserted when the DSP no longer needs the bus. BR can be asserted or deasserted independently of whether the DSP56301 is a bus master or a bus slave. Bus "parking" allows BR to be deasserted even though the DSP56301 is the bus master (see the description of bus "parking" in the BB signal description). The Bus Request Hole (BRH) bit in the BCR allows BR to be asserted under software control, even though the DSP does not need the bus. BR is typically sent to an external bus arbitrator that controls the priority, parking and tenure of each master on the same external bus. BR is affected only by DSP requests for the external bus, never for the internal bus. During hardware reset, BR is deasserted and the arbitration is reset to the bus slave state.
BG	Input	Ignored Input	Bus Grant  Must be asserted/deasserted synchronous to CLKOUT for proper operation.  An external bus arbitration circuit asserts BG when the DSP56301 becomes the next bus master. When BG is asserted, the DSP56301 must wait until BB is deasserted before taking bus mastership. When BG is deasserted, bus mastership is typically given up at the end of the current bus cycle. This may occur in the middle of an instruction that requires more than one external bus cycle for execution.

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 Table 1-8.
 External Bus Control Signals (Continued)

Signal Name	Туре	State During Reset	Signal Description
BB	Input/ Output	Input	Bus Busy Indicates that the bus is active and must be asserted and deasserted synchronous to CLKOUT. Only after \$\overline{BB}\$ is deasserted can the pending bus master become the bus master (and then assert the signal again). The bus master can keep \$\overline{BB}\$ asserted after ceasing bus activity, regardless of whether \$\overline{BR}\$ is asserted or deasserted. This is called "bus parking" and allows the current bus master to reuse the bus without re-arbitration until another device requires the bus. \$\overline{BB}\$ is deasserted by an "active pull-up" method (that is, \$\overline{BB}\$ is driven high and then released and held high by an external pull-up resistor).  \$\overline{BB}\$ requires an external pull-up resistor.
BL	Output	Driven high (deasserted)	Bus Lock—BL is asserted at the start of an external divisible Read-Modify-Write (RMW) bus cycle, remains asserted between the read and write cycles, and is deasserted at the end of the write bus cycle. This provides an "early bus start" signal for the bus controller. BL may be used to "resource lock" an external multi-port memory for secure semaphore updates. Early deassertion provides an "early bus end" signal useful for external bus control. If the external bus is not used during an instruction cycle, BL remains deasserted until the next external indivisible RMW cycle. The only instructions that assert BL automatically are the BSET, CLR, and BCHG instructions when they are used to modify external memory. An operation can also assert BL by setting the BLH bit in the Bus Control Register.
CAS	Output	Tri-stated	Column Address Strobe When the DSP is the bus master, DRAM uses CAS to strobe the column address. Otherwise, if the Bus Mastership Enable (BME) bit in the DRAM Control Register is cleared, the signal is tri-stated.
BCLK	Output	Tri-stated	Bus Clock When the DSP is the bus master, BCLK is active when the OMR[ATE] is set. When BCLK is active and synchronized to CLKOUT by the internal PLL, BCLK precedes CLKOUT by one-fourth of a clock cycle.
BCLK	Output	Tri-stated	Bus Clock Not When the DSP is the bus master, BCLK is the inverse of the BCLK signal. Otherwise, the signal is tri-stated.

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# 1.6 Interrupt and Mode Control

The interrupt and mode control signals select the chip's operating mode as it comes out of hardware reset. After RESET is deasserted, these inputs are hardware interrupt request lines.

Table 1-9. Interrupt and Mode Control

Signal Name	Туре	State During Reset	Signal Description
MODA	Input	Input	Mode Select A Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQA during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
ĪRQĀ	Input		External Interrupt Request A Internally synchronized to CLKOUT. If IRQA is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQA to exit the Wait state. If the processor is in the Stop stand-by state and IRQA is asserted, the processor exits the Stop state.  These inputs are 5 V tolerant.
MODB	Input	Input	Mode Select B
MODB	при	при	Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQB during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
ĪRQB	Input		External Interrupt Request B Internally synchronized to CLKOUT. If IRQB is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQB to exit the Wait state. If the processor is in the Stop stand-by state and IRQC is asserted, the processor will exit the Stop state.
			These inputs are 5 V tolerant.
MODC	Input	Input	Mode Select C Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQC during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
ĪRQC	Input		External Interrupt Request C Internally synchronized to CLKOUT. If IRQC is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQC to exit the Wait state. If the processor is in the Stop stand-by state and IRQC is asserted, the processor exits the Stop state.
			These inputs are 5 V tolerant.

Table 1-9. Interrupt and Mode Control (Continued)

Signal Name	Туре	State During Reset	Signal Description
MODD	Input	Input	Mode Select D Selects the initial chip operating mode during hardware reset and becomes a level-sensitive or negative-edge-triggered, maskable interrupt request input IRQD during normal instruction processing. MODA, MODB, MODC, and MODD select one of sixteen initial chip operating modes, latched into the OMR when the RESET signal is deasserted.
ĪRQD	Input		External Interrupt Request D Internally synchronized to CLKOUT. If IRQD is asserted synchronous to CLKOUT, multiple processors can be re-synchronized using the WAIT instruction and asserting IRQD to exit the Wait state. If the processor is in the Stop stand-by state and IRQD is asserted, the processor exits the Stop state.  These inputs are 5 V tolerant.
RESET	Input	Input	Reset  Deassertion of RESET is internally synchronized to the clock out (CLKOUT). When asserted, the chip is placed in the Reset state and the internal phase generator is reset. The Schmitt-trigger input allows a slowly rising input (such as a capacitor charging) to reset the chip reliably. If RESET is deasserted synchronous to CLKOUT, exact start-up timing is guaranteed, allowing multiple processors to start synchronously and operate together in "lock-step." When the RESET signal is deasserted, the initial chip operating mode is latched from the MODA, MODB, MODC, and MODD inputs. The RESET signal must be asserted after power-up.  This input is 5 V tolerant.

# 1.7 Host Interface (HI32)

The Host Interface (HI32) provides fast parallel data to a 32-bit port directly connected to the host bus. The HI32 supports a variety of standard buses and directly connects to a PCI bus and a number of industry-standard microcomputers, microprocessors, DSPs, and DMA hardware.

### 1.7.1 Host Port Usage Considerations

Careful synchronization is required when the system reads multiple-bit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected (as they are in the Host port). The considerations for proper operation are discussed in **Table 1-10**.

Table 1-10. Host Port Usage Considerations

Action	Description
Asynchronous read of receive byte registers	When reading the receive byte registers, Receive register High (RXH), Receive register Middle (RXM), or Receive register Low (RXL), use interrupts or poll the Receive register Data Full (RXDF) flag that indicates data is available. This assures that the data in the receive byte registers is valid.
Asynchronous write to transmit byte registers	Do not write to the transmit byte registers, Transmit register High (TXH), Transmit register Middle (TXM), or Transmit register Low (TXL), unless the Transmit register Data Empty (TXDE) bit is set, indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers transfer valid data to the Host Receive (HRX) register.

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Table 1-10. Host Port Usage Considerations (Continued)

Action	Description
Asynchronous write to host vector	Change the Host Vector (HV) register only when the Host Command bit (HC) is clear. This practice guarantees that the DSP interrupt control logic receives a stable vector.

## 1.7.2 Host Port Configuration

HI32 signal functions vary according to the programmed configuration of the interface as determined by the 24-bit DSP Control Register (DCTR). Refer to the DSP56301 User's Manual for details on HI32 configuration registers.

Table 1-11. Host Interface

Signal Name	Туре	State During Reset	Signal Description
HAD[0-7]	Input/Output	Tri-stated	Host Address/Data 0–7 When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 0–7 of the Address/Data bus.
HA[3–10]	Input		Host Address 3–10 When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 3–10 of the Address bus.
PB[0-7]	Input or Output		Port B 0–7 When the Hl32 is configured as GPIO through the DCTR, these signals are individually programmed through the Hl32 Data Direction Register (DIRH).
1			These inputs are 5 V tolerant.
HAD[8–15]	Input/Output	Tri-stated	Host Address/Data 8–15 When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 8–15 of the Address/Data bus.
HD[0-7]	Input/Output		Host Data 0–7 When HI32 is programmed to interface with a universal non-PCI bus and the HI function is selected, these signals are lines 0–7 of the Data bus.
PB[8–15]	Input or Output		Port B 8–15 When the Hl32 is configured as GPIO through the DCTR, these signals are individually programmed through the Hl32 DIRH.
			These inputs are 5 V tolerant.
HC[0-3]/ HBE[0-3]	Input/Output	Tri-stated	Command 0-3/Byte Enable 0-3  When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 0-7 of the Address/Data bus.
HA[0-2]	Input		Host Address 0–2 When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 0–2 of the Address bus.
			The fourth signal in this set should connect to a pull-up resistor or directly to $V_{CC}$ when a non-PCI bus is used.
PB[16–19]	Input or Output		Port B 16–19 When the Hl32 is configured as GPIO through the DCTR, these signals are individually programmed through the Hl32 DIRH.
			These inputs are 5 V tolerant.



Table 1-11. Host Interface (Continued)

Signal Name	Туре	State During Reset	Signal Description
HTRDY	Input/ Output	Tri-stated	Host Target Ready When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Target Ready signal.
HDBEN	Output		Host Data Bus Enable When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Enable signal.
PB20	Input or Output		Port B 20 When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH.
			This input is 5 V tolerant.
HIRDY	Input/ Output	Tri-stated	Host Initiator Ready When the Hl32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Initiator Ready signal.
HDBDR	Output		Host Data Bus Direction When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Direction signal.
PB21	Input or Output		Port B 21 When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH.
			This input is 5 V tolerant.
HDEVSEL	Input/ Output	Tri-stated	Host Device Select When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Device Select signal.
HSAK	Output		Host Select Acknowledge When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Select Acknowledge signal.
PB22	Input or Output		Port B 22  When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH.
			This input is 5 V tolerant.
HLOCK	Input	Tri-stated	Host Lock When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Lock signal.
HBS	Input		Host Bus Strobe When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Bus Strobe Schmitt-trigger signal.
PB23	Input or Output		Port B 23  When the HI32 is configured as GPIO through the DCTR, this signal is individually programmed through the HI32 DIRH.
			This input is 5 V tolerant.

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Table 1-11. Host Interface (Continued)

Signal Name	Туре	State During Reset	Signal Description
HPAR	Input/ Output	Tri-stated	Host Parity When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Parity signal.
HDAK	Input		Host DMA Acknowledge When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host DMA Acknowledge Schmitt-trigger signal.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HPERR	Input/ Output	Tri-stated	Host Parity Error When the Hl32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Parity Error signal.
HDRQ	Output		Host DMA Request When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host DMA Request output.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HGNT	Input	Input	Host Bus Grant When the Hl32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Grant signal.
HAEN	Input		Host Address Enable When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Address Enable output signal.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HREQ	Output	Tri-stated	Host Bus Request When the Hl32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Request signal.
НТА	Output		Host Transfer Acknowledge—When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Bus Enable signal. HTA can be programmed as active high or active low.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.



Table 1-11. Host Interface (Continued)

Signal Name	Туре	State During Reset	Signal Description
HSERR	Output, open drain	Tri-stated	Host System Error When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host System Error signal.
HIRQ	Output, open drain		Host Interrupt Request When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Interrupt Request signal.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HSTOP	Input/ Output	Tri-stated	Host Stop When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Stop signal.
HWR/HRW	Input		Host Write/Host Read-Write When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Write/Host Read-Write Schmitt-trigger signal.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HIDSEL	Input	Input	Host Initialization Device Select When the Hl32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Initialization Device Select signal.
HRD/HDS	Input		Host Read/Host Data Strobe When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Host Data Read/Host Data Strobe Schmitt-trigger signal.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HFRAME	Input/ Output	Tri-stated	Host Frame When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host cycle Frame signal.
			Non-PCI bus When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to $V_{\rm CC}$ .
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.

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Table 1-11. Host Interface (Continued)

Signal Name	Туре	State During Reset	Signal Description
HCLK	Input	Input	Host Clock When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Host Bus Clock input.
			Non-PCI bus When HI32 is programmed to interface a universal non-PCI bus and the HI function is selected, this signal must be connected to a pull-up resistor or directly to V <sub>CC</sub> .
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HAD[16-31]	Input/Output	Tri-stated	Host Address/Data 16–31 When the HI32 is programmed to interface with a PCI bus and the HI function is selected, these signals are lines 16–31 of the Address/Data bus.
HD[8-23]	Input/Output		Host Data 8–23 When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, these signals are lines 8–23 of the Data bus.
			Port B When the HI32 is configured as GPIO through the DCTR, these signals are internally disconnected.
			These inputs are 5 V tolerant.
HRST	Input	Tri-stated	Hardware Reset When the HI32 is programmed to interface with a PCI bus and the HI function is selected, this is the Hardware Reset input.
HRST	Input		Hardware Reset When HI32 is programmed to interface with a universal, non-PCI bus and the HI function is selected, this is the Hardware Reset Schmitt-trigger signal.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
HINTA	Output, open drain	Tri-stated	Host Interrupt A When the HI function is selected, this signal is the Interrupt A open-drain output.
			Port B When the HI32 is configured as GPIO through the DCTR, this signal is internally disconnected.
			This input is 5 V tolerant.
PVCL	Input	Input	PCI Voltage Clamp When the HI32 is programmed to interface with a PCI bus and the HI function is selected and the PCI bus uses a 3 V signal environment, connect this pin to $V_{CC}$ (3.3 V) to enable the high voltage clamping required by the PCI specifications. In all other cases, including a 5 V PCI signal environment, leave the input unconnected.



# 1.8 Enhanced Synchronous Serial Interface 0 (ESSI0)

Two synchronous serial interfaces (ESSI0 and ESSI1) provide a full-duplex serial port for serial communication with a variety of serial devices, including one or more industry-standard codecs, other DSPs, microprocessors, and peripherals that implement the Serial Peripheral Interface (SPI).

 Table 1-12.
 Enhanced Synchronous Serial Interface 0 (ESSI0)

Signal Name	Туре	State During Reset	Signal Description
SC00	Input or Output	Input	Serial Control 0 Functions in either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is either for Transmitter 1 output or Serial I/O Flag 0.
PC0			Port C 0 The default configuration following reset is GPIO. For PC0, signal direction is controlled through the Port Directions Register (PRR0). The signal can be configured as ESSI signal SC00 through the Port Control Register (PCR0).  This input is 5 V tolerant.
SC01	Input/Output	Input	Serial Control 1 Functions in either Synchronous or Asynchronous mode. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is either Transmitter 2 output or Serial I/O Flag 1.
PC1	Input or Output		Port C 1 The default configuration following reset is GPIO. For PC1, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC01 through PCR0.  This input is 5 V tolerant.
SC02	Input/Output	Input	Serial Control Signal 2  The frame sync for both the transmitter and receiver in Synchronous mode, and for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in synchronous operation).
PC2	Input or Output		Port C 2 The default configuration following reset is GPIO. For PC2, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SC02 through PCR0.
			This input is 5 V tolerant.





 Table 1-12.
 Enhanced Synchronous Serial Interface 0 (ESSI0) (Continued)

Signal Name	Туре	State During Reset	Signal Description
SCK0	Input/Output	Input	Serial Clock Provides the serial bit rate clock for the ESSI interface for both the transmitter and receiver in Synchronous modes, or the transmitter only in Asynchronous modes.
			Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6 T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.
PC3	Input or Output		Port C 3 The default configuration following reset is GPIO. For PC3, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SCK0 through PCR0.
			This input is 5 V tolerant.
SRD0	Input/Output	Input	Serial Receive Data Receives serial data and transfers the data to the ESSI receive shift register. SRD0 is an input when data is being received.
PC4	Input or Output		Port C 4 The default configuration following reset is GPIO. For PC4, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal SRD0 through PCR0.
			This input is 5 V tolerant.
STD0	Input/Output	Input	Serial Transmit Data Transmits data from the serial transmit shift register. STD0 is an output when data is being transmitted.
PC5	Input or Output		Port C 5 The default configuration following reset is GPIO. For PC5, signal direction is controlled through PRR0. The signal can be configured as an ESSI signal STD0 through PCR0.
			This input is 5 V tolerant.



# 1.9 Enhanced Synchronous Serial Interface 1 (ESSI1)

Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1)

Signal Name	Туре	State During Reset	Signal Description			
SC10	Input or Output	Input	Serial Control 0 Selection of Synchronous or Asynchronous mode determines function. For Asynchronous mode, this signal is the receive clock I/O (Schmitt-trigger input). For Synchronous mode, this signal is either Transmitter 1 output or Serial I/O Flag 0.			
PD0			Port D 0  The default configuration following reset is GPIO. For PD0, signal direction is controlled through the Port Directions Register (PRR1). The signal can be configured as an ESSI signal SC10 through the Port Control Register (PCR1).			
			This input is 5 V tolerant.			
SC11	Input/Output	Input	Serial Control 1 Selection of Synchronous or Asynchronous mode determines function. For Asynchronous mode, this signal is the receiver frame sync I/O. For Synchronous mode, this signal is either Transmitter 2 output or Serial I/O Flag 1.			
PD1	Input or Output		Port D 1  The default configuration following reset is GPIO. For PD1, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC11 through PCR1.			
			This input is 5 V tolerant.			
SC12	Input/Output	Input	Serial Control Signal 2 Frame sync for both the transmitter and receiver in Synchronous mode, for the transmitter only in Asynchronous mode. When configured as an output, this signal is the internally generated frame sync signal. When configured as an input, this signal receives an external frame sync signal for the transmitter (and the receiver in Synchronous operation).			
PD2	Input or Output		Port D 2 The default configuration following reset is GPIO. For PD2, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SC12 through PCR1.  This input is 5 V tolerant.			
SCK1	Input/Output	Input	Serial Clock Provides the serial bit rate clock for the ESSI interface. Clock input or output can be used by the transmitter and receiver in Synchronous modes, by the transmitter only in Asynchronous modes.			
			Although an external serial clock can be independent of and asynchronous to the DSP system clock, it must exceed the minimum clock cycle time of 6T (that is, the system clock frequency must be at least three times the external ESSI clock frequency). The ESSI needs at least three DSP phases inside each half of the serial clock.			
PD3	Input or Output		Port D 3 The default configuration following reset is GPIO. For PD3, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SCK1 through PCR1.			
			This input is 5 V tolerant.			

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Table 1-13. Enhanced Synchronous Serial Interface 1 (ESSI1) (Continued)

Signal Name	Туре	State During Reset	Signal Description
SRD1	Input/Output	Input	Serial Receive Data Receives serial data and transfers it to the ESSI receive shift register. SRD1 is an input when data is being received.
PD4	Input or Output		Port D 4 The default configuration following reset is GPIO. For PD4, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal SRD1 through PCR1.  This input is 5 V tolerant.
STD1	Input/Output	Input	Serial Transmit Data Transmits data from the serial transmit shift register. STD1 is an output when data is being transmitted.
PD5	Input or Output		Port D 5 The default configuration following reset is GPIO. For PD5, signal direction is controlled through PRR1. The signal can be configured as an ESSI signal STD1 through PCR1.
			This input is 5 V tolerant.

# 1.10 Serial Communication Interface (SCI)

The Serial Communication interface (SCI) provides a full duplex port for serial communication with other DSPs, microprocessors, or peripherals such as modems.

Table 1-14. Serial Communication Interface (SCI)

Signal Name	Туре	State During Reset	Signal Description
RXD	Input	Input	Serial Receive Data Receives byte-oriented serial data and transfers it to the SCI receive shift register.
PE0	Input or Output		Port E 0 The default configuration following reset is GPIO. When configured as PE0, signal direction is controlled through the SCI Port Directions Register (PRR). The signal can be configured as an SCI signal RXD through the SCI Port Control Register (PCR).  This input is 5 V tolerant.
TXD	Output	Input	Serial Transmit Data Transmits data from SCI transmit data register.
PE1	Input or Output		Port E 1  The default configuration following reset is GPIO. When configured as PE1, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal TXD through the SCI PCR.  This input is 5 V tolerant.

Table 1-14. Serial Communication Interface (SCI) (Continued)

Signal Name	Туре	State During Reset	Signal Description	
SCLK	Input/Output	Input	Serial Clock Provides the input or output clock used by the transmitter and/or the receiver.	
PE2	Input or Output		Port E 2 The default configuration following reset is GPIO. For PE2, signal direction is controlled through the SCI PRR. The signal can be configured as an SCI signal SCLK through the SCI PCR.  This input is 5 V tolerant.	

### 1.11 Timers

The DSP56301 has three identical and independent timers. Each can use internal or external clocking, interrupt the DSP56301 after a specified number of events (clocks), or signal an external device after counting a specific number of internal events.

 Table 1-15.
 Triple Timer Signals

Signal Name	Туре	State During Reset	Signal Description
TIO0	Input or Output	Input	Timer 0 Schmitt-Trigger Input/Output As an external event counter or in Measurement mode, TIO0 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO0 is output.  The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 0 Control/Status Register (TCSR0).  This input is 5 V tolerant.
TIO1	Input or Output	Input	Timer 1 Schmitt-Trigger Input/Output As an external event counter or in Measurement mode, TIO1 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO1 is output.  The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 1 Control/Status Register (TCSR1).  This input is 5 V tolerant.
TIO2	Input or Output	Input	Timer 2 Schmitt-Trigger Input/Output As an external event counter or in Measurement mode, TIO2 is input. In Watchdog, Timer, or Pulse Modulation mode, TIO2 is output.  The default mode after reset is GPIO input. This can be changed to output or configured as a Timer Input/Output through the Timer 2 Control/Status Register (TCSR2).  This input is 5 V tolerant.

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# 1.12 JTAG/OnCE Interface

Table 1-16. JTAG/OnCE Interface

Signal Name	Туре	State During Reset	Signal Description				
тск	Input	Input	Test Clock A test clock signal for synchronizing JTAG test logic. This input is 5 V tolerant.				
TDI	Input	Input	Test Data Input A test data serial signal for test instructions and data. TDI is sampled on the rising edge of TCK and has an internal pull-up resistor.  This input is 5 V tolerant.				
TDO	Output	Tri-stated	Test Data Output A test data serial signal for test instructions and data. TDO can be tri-stated. The signal is actively driven in the shift-IR and shift-DR controller states and changes on the falling edge of TCK.  This input is 5 V tolerant.				
TMS	Input	Input	Test Mode Select Sequences the test controller's state machine, is sampled on the rising edge of TCK, and has an internal pull-up resistor.  This input is 5 V tolerant.				
TRST	Input	Input	Test Reset Asynchronously initializes the test controller, has an internal pull-up resistor, and must be asserted after power up. This input is 5 V tolerant.				
DE	Input/Output	Input	Debug Event Provides a way to enter Debug mode from an external command controller (as input) or to acknowledge that the chip has entered Debug mode (as output). When asserted as an input, DE causes the DSP56300 core to finish the current instruction, save the instruction pipeline information, enter Debug mode, and wait for commands from the debug serial input line. When a debug request or a breakpoint condition causes the chip to enter Debug mode, DE is asserted as an output for three clock cycles. DE has an internal pull-up resistor.				
			DE is not a standard part of the JTAG Test Access Port (TAP) Controller. It connects to the OnCE module to initiate Debug mode directly or to provide a direct external indication that the chip has entered the Debug mode. All other interface with the OnCE module must occur through the JTAG port.				
			This input is 5 V tolerant.				



# **Specifications**

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The DSP56301 is fabricated in high-density CMOS with Transistor-Transistor Logic (TTL) compatible inputs and outputs.

## 2.1 Maximum Ratings

#### **CAUTION**

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, normal precautions should be taken to avoid exceeding maximum voltage ratings. Reliability is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V<sub>CC</sub>).

**Note:** In the calculation of timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device that has a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.



## 2.2 Absolute Maximum Ratings

Table 2-1. Maximum Ratings

Rating <sup>1</sup>	Symbol	Value <sup>1, 2</sup>	Unit
Supply Voltage	V <sub>CC</sub>	-0.3 to +4.0	V
All input voltages excluding "5 V tolerant" inputs <sup>3</sup>	V <sub>IN</sub>	GND - 0.3 to V <sub>CC</sub> + 0.3	V
All "5 V tolerant" input voltages <sup>3</sup>	V <sub>IN5</sub>	GND – 0.3 to V <sub>CC</sub> + 3.95	V
Current drain per pin excluding V <sub>CC</sub> and GND	I	10	mA
Operating temperature range	T <sub>J</sub>	-40 to +100	°C
Storage temperature	T <sub>STG</sub>	-55 to +150	°C

Notes:

- 1. GND = 0 V,  $V_{CC}$  = 3.3 V ± 0.3 V,  $T_{J}$  = -40°C to +100°C, CL = 50 pF
- 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the maximum rating may affect device reliability or cause permanent damage to the device.
- 3. CAUTION: All "5 V Tolerant" input voltages cannot be more than 3.95 V greater than the supply voltage; this restriction applies to "power on," as well as during normal operation. In any case, the input voltages must not be higher than 5.75 V. "5 V Tolerant" inputs are inputs that tolerate 5 V.

#### 2.3 Thermal Characteristics

Table 2-2. Thermal Characteristics

Characteristic	Symbol	TQFP Value	PBGA <sup>3</sup> Value	PBGA <sup>4</sup> Value	Unit
Junction-to-ambient thermal resistance <sup>1</sup>	$R_{\theta JA}$ or $\theta_{JA}$	49.5	48.4	25.2	°C/W
Junction-to-case thermal resistance <sup>2</sup>	$R_{\theta JC}$ or $\theta_{JC}$	7.2	9	_	°C/W
Thermal characterization parameter	$\Psi_{JT}$	4.7	5	_	°C/W

Notes:

- Junction-to-ambient thermal resistance is based on measurements on a horizontal single-sided printed circuit board per JEDEC Specification JESD51-3.
- 2. Junction-to-case thermal resistance is based on measurements using a cold plate per SEMI G30-88, with the exception that the cold plate temperature is used for the case temperature.
- 3. These are simulated values. See note 1 for test board conditions.
- 4. These are simulated values. The test board has two 2-ounce signal layers and two 1-ounce solid ground planes internal to the test board.

# 2.4 DC Electrical Characteristics

**Table 2-3.** DC Electrical Characteristics<sup>6</sup>

Characteristics	Symbol	Min	Тур	Max	Unit
Supply voltage	V <sub>CC</sub>	3.0	3.3	3.6	V

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**Table 2-3.** DC Electrical Characteristics<sup>6</sup> (Continued)

Characteristics	Symbol	Min	Т	ур	Max	Unit								
Input high voltage  • D[0–23], BG, BB, TA  • MOD¹/IRQ¹, RESET, PINIT/NMI and all JTAG/ESSI/SCI/Timer/HI32 pins  • EXTAL <sup>8</sup>	V <sub>IH</sub> V <sub>IHP</sub> V <sub>IHX</sub>	2.0 2.0 0.8 × V <sub>CC</sub>	_ _ _		_ _ _		_ _ _		_ _ _		_ _ _		V <sub>CC</sub> 5.25 V <sub>CC</sub>	V V
Input low voltage  • D[0–23], BG, BB, TA, MOD¹/IRQ¹, RESET, PINIT  • All JTAG/ESSI/SCI/Timer/HI32 pins  • EXTAL <sup>8</sup>	V <sub>IL</sub> V <sub>ILP</sub> V <sub>ILX</sub>	-0.3 -0.3 -0.3	_ _ _ _		_ _ _		_ _ _ _		_ _ _ _		_ _ _		0.8 0.8 0.2 × V <sub>CC</sub>	V V V
Input leakage current	I <sub>IN</sub>	-10	_		10	μΑ								
High impedance (off-state) input current (@ 2.4 V / 0.4 V)	I <sub>TSI</sub>	-10	_		10	μΑ								
Output high voltage • TTL (I <sub>OH</sub> = -0.4 mA) <sup>5,7</sup> • CMOS (I <sub>OH</sub> = -10 μA) <sup>5</sup>	V <sub>ОН</sub>	2.4 V <sub>CC</sub> – 0.01	=		_ _	V V								
Output low voltage • TTL (I <sub>OL</sub> = 1.6 mA, open-drain pins I <sub>OL</sub> = 6.7 mA) <sup>5,7</sup> • CMOS (I <sub>OL</sub> = 10 μA) <sup>5</sup>	V <sub>OL</sub>	_ _	_ _		0.4 0.01	V V								
Internal supply current <sup>2</sup> :  In Normal mode  In Wait mode <sup>3</sup> In Stop mode <sup>4</sup>	I <sub>CCI</sub> I <sub>CCW</sub> I <sub>CCS</sub>	_ _ _	80 MHz         100 MHz           102         127           6         7.5           100         100		_ _ _	mA mA μA								
PLL supply current		_	1		2.5	mA								
Input capacitance <sup>5</sup>	C <sub>IN</sub>	_	_		10	pF								

#### Notes:

- 1. Refers to MODA/IRQA, MODB/IRQB, MODC/IRQC, and MODD/IRQD pins.
- 2. Power Consumption Considerations on page 4-3 provides a formula to compute the estimated current requirements in Normal mode. To obtain these results, all inputs must be terminated (that is, not allowed to float). Measurements are based on synthetic intensive DSP benchmarks (see Appendix A). The power consumption numbers in this specification are 90 percent of the measured results of this benchmark. This reflects typical DSP applications. Typical internal supply current is measured with V<sub>CC</sub> = 3.0 V at T<sub>J</sub> = 100°C.
- 3. To obtain these results, all inputs must be terminated (that is, not allowed to float).
- 4. To obtain these results, all inputs that are not disconnected at Stop mode must be terminated (that is, not allowed to float). PLL and XTAL signals are disabled during Stop state.
- 5. Periodically sampled and not 100 percent tested.
- **6.**  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $T_{J} = -40 ^{\circ}\text{C}$  to +100  $^{\circ}\text{C}$ ,  $C_{L} = 50 \text{ pF}$
- 7. This characteristic does not apply to XTAL and PCAP.
- 8. Driving EXTAL to the low  $V_{IHX}$  or the high  $V_{ILX}$  value may cause additional power consumption (DC current). To minimize power consumption, the minimum  $V_{IHX}$  should be no lower than  $0.9 \times V_{CC}$  and the maximum  $V_{ILX}$  should be no higher than  $0.1 \times V_{CC}$ .



### 2.5 AC Electrical Characteristics

The timing waveforms shown in the AC electrical characteristics section are tested with a  $V_{IL}$  maximum of 0.3 V and a  $V_{IH}$  minimum of 2.4 V for all pins except EXTAL, which is tested using the input levels shown in Note 6 of **Table 2-3**. AC timing specifications, which are referenced to a device input signal, are measured in production with respect to the 50 percent point of the respective input signal's transition.

**Note:** Although the minimum value for the frequency of EXTAL is 0 MHz, the device AC test conditions are 15 MHz and rated speed.

All specifications for the high impedance state are guaranteed by design.

#### 2.5.1 Internal Clocks

Table 2-4. Internal Clocks, CLKOUT

Characteristics	Symbol	Expression <sup>1, 2</sup>				
Gilaracteristics	Symbol	Min	Тур	Max		
Internal operation frequency and CLKOUT with PLL enabled	f	_	$(Ef \times MF)/$ $(PDF \times DF)$	1		
Internal operation frequency and CLKOUT with PLL disabled	f	_	Ef/2	_		
Internal clock and CLKOUT high period  • With PLL disabled  • With PLL enabled and MF ≤ 4	T <sub>H</sub>	 0.49 × ET <sub>C</sub> × PDF × DF/MF	ET <sub>C</sub>	 0.51 × ET <sub>C</sub> × PDF × DF/MF		
With PLL enabled and MF > 4		$0.47 \times \text{ET}_{\text{C}} \times \text{PDF} \times \text{DF/MF}$	_	$0.53 \times \text{ET}_{\text{C}} \times \text{PDF} \times \text{DF/MF}$		
Internal clock and CLKOUT low period  • With PLL disabled  • With PLL enabled and MF ≤ 4	TL	 0.49 × ET <sub>C</sub> × PDF × DF/MF	ET <sub>C</sub>	 0.51 × ET <sub>C</sub> × PDF × DF/MF		
With PLL enabled and MF > 4		$0.47 \times \text{ET}_{\text{C}} \times \text{PDF} \times \text{DF/MF}$	_	$0.53 \times \text{ET}_{\text{C}} \times \text{PDF} \times \text{DF/MF}$		
Internal clock and CLKOUT cycle time with PLL enabled	T <sub>C</sub>	_	ET <sub>C</sub> × PDF × DF/MF	_		
Internal clock and CLKOUT cycle time with PLL disabled	T <sub>C</sub>	_	2 × ET <sub>C</sub>	_		
Instruction cycle time	I <sub>CYC</sub>	_	T <sub>C</sub>	_		

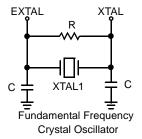
Notes: 1. DF = Division Factor; Ef = External frequency; ET<sub>C</sub> = External clock cycle = 1/Ef; MF = Multiplication Factor; PDF = Predivision Factor; T<sub>C</sub> = Internal clock cycle

2. See the PLL and Clock Generator section in the DSP56300 Family Manual for details on the PLL.



#### 2.5.2 External Clock Operation

The DSP56301 system clock is derived from the on-chip oscillator or it is externally supplied. To use the on-chip oscillator, connect a crystal and associated resistor/capacitor components to EXTAL and XTAL; examples are shown in **Figure 2-1**.



**Note:** Make sure that in the PCTL Register:

- XTLD (bit 16) = 0
- If f<sub>OSC</sub> > 200 kHz, XTLR (bit 15) = 0

#### **Suggested Component Values:**

$$\begin{split} f_{OSC} &= 4 \text{ MHz} \\ R &= 680 \text{ } k\Omega \pm 10\% \\ C &= 56 \text{ pF} \pm 20\% \end{split} \qquad \begin{aligned} f_{OSC} &= 20 \text{ MHz} \\ R &= 680 \text{ } k\Omega \pm 10\% \\ C &= 22 \text{ pF} \pm 20\% \end{aligned}$$

Calculations were done for a 4/20 MHz crystal with the following parameters:

- C<sub>L</sub>of 30/20 pF,
- C<sub>0</sub> of 7/6 pF,
- series resistance of 100/20  $\Omega$ , and
- drive level of 2 mW.

Figure 2-1. Crystal Oscillator Circuits

If an externally supplied square wave voltage source is used, disable the internal oscillator circuit during boot-up by setting XTLD (PCTL Register bit 16 = 1—see the *DSP56301 User's Manual*). The external square wave source connects to EXTAL; XTAL is not physically connected to the board or socket. **Figure 2-2** shows the relationship between the EXTAL input and the internal clock and CLKOUT.

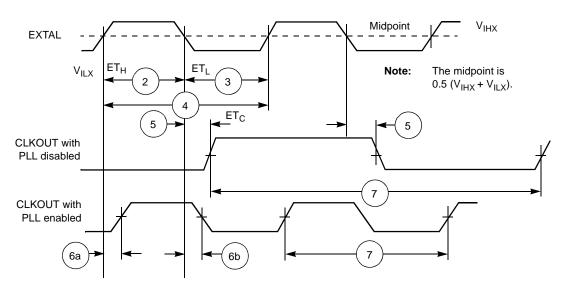


Figure 2-2. External Clock Timing

**Table 2-5.** Clock Operation

No.	Characteristics	Cumbal	80 1	ИHz	100 MHz		
NO.	Characteristics	Symbol	Min	Max	Min	Max	
1	Frequency of EXTAL (EXTAL Pin Frequency) The rise and fall time of this external clock should be 3 ns maximum.	Ef	0	80.0 MHz	0	100.0 MHz	
2	<ul> <li>EXTAL input high<sup>1, 2</sup></li> <li>With PLL disabled (46.7%–53.3% duty cycle<sup>6</sup>)</li> <li>With PLL enabled (42.5%–57.5% duty cycle<sup>6</sup>)</li> </ul>	ET <sub>H</sub>	5.84 ns 5.31 ns	∞ 157.0 μs	4.67 ns 4.25 ns	∞ 157.0 μs	
3	<ul> <li>EXTAL input low<sup>1, 2</sup></li> <li>With PLL disabled (46.7%–53.3% duty cycle<sup>6</sup>)</li> <li>With PLL enabled (42.5%–57.5% duty cycle<sup>6</sup>)</li> </ul>	ET <sub>L</sub>	5.84 ns 5.31 ns	∞ 157.0 μs	4.67 ns 4.25 ns	∞ 157.0 μs	
4	EXTAL cycle time <sup>2</sup> • With PLL disabled • With PLL enabled	ET <sub>C</sub>	12.50 ns 12.50 ns	∞ 273.1 μs	10.00 ns 10.00 ns	∞ 273.1 μs	
5	CLKOUT change from EXTAL fall with PLL disabled		4.3 ns	11.0 ns	4.3 ns	11.0 ns	
6	a. CLKOUT rising edge from EXTAL rising edge with PLL enabled (MF = 1 or 2 or 4, PDF = 1, Ef > 15 MHz) $^{3,5}$		0.0 ns	1.8 ns	0.0 ns	1.8 ns	
	b. CLKOUT falling edge from EXTAL falling edge with PLL enabled (MF $\leq$ 4, PDF $\neq$ 1, Ef / PDF $>$ 15 MHz) $^{3,5}$		0.0 ns	1.8 ns	0.0 ns	1.8 ns	
7	Instruction cycle time = I <sub>CYC</sub> = T <sub>C</sub> <sup>4</sup> (see <b>Table 2-4</b> ) (46.7%–53.3% duty cycle)  • With PLL disabled		25.0 ns		20.0 ns		
	With PLL disabled     With PLL enabled	Icyc	25.0 ns 12.50 ns	∞ 8.53 μs	20.0 ns 10.00 ns	<sub>∞</sub> 8.53 μs	

Notes:

- 1. Measured at 50 percent of the input transition
- 2. The maximum value for PLL enabled is given for minimum VCO frequency (see Table 2-6) and maximum MF.
- 3. Periodically sampled and not 100 percent tested
- 4. The maximum value for PLL enabled is given for minimum VCO frequency and maximum DF.
- **5.** The skew is not guaranteed for any other MF value.
- 6. The indicated duty cycle is for the specified maximum frequency for which a part is rated. The minimum clock high or low time required for correction operation, however, remains the same at lower operating frequencies; therefore, when a lower clock frequency is used, the signal symmetry may vary from the specified duty cycle as long as the minimum high time and low time requirements are met.

## 2.5.3 Phase Lock Loop (PLL) Characteristics

Table 2-6. PLL Characteristics

Observatoristics	80 1	ИHz	100	1111	
Characteristics	Min	Max	Min	Max	Unit
Voltage Controlled Oscillator (VCO) frequency when PLL enabled (MF $\times$ E $_{\rm f} \times$ 2/PDF)	30	160	30	200	MHz
PLL external capacitor (PCAP pin to $V_{CCP}$ ) ( $C_{PCAP}$ ) • @ MF $\leq$ 4	(MF × 580) – 100	(MF × 780) – 140	(MF × 580) – 100	(MF × 780) – 140	pF
• @ MF > 4	MF × 830	MF × 1470	MF × 830	MF × 1470	pF

**Note:** C<sub>PCAP</sub> is the value of the PLL capacitor (connected between the PCAP pin and V<sub>CCP</sub>). The recommended value in pF for C<sub>PCAP</sub> can be computed from one of the following equations:

 $(680 \times MF) - 120$ , for MF  $\leq 4$ , or  $1100 \times MF$ , for MF > 4.



# 2.5.4 Reset, Stop, Mode Select, and Interrupt Timing

**Table 2-7.** Reset, Stop, Mode Select, and Interrupt Timing<sup>6</sup>

No.	Characteristics	Fyggessien	80 MHz		100 MHz		11-:4
No.	Characteristics	Expression	Min	Max	Min	Max	Unit
8	Delay from RESET assertion to all pins at reset value <sup>3</sup>	_	_	26.0	_	26.0	ns
9	Required RESET duration <sup>4</sup> Power on, external clock generator, PLL disabled  Power on, external clock generator, PLL enabled  Power on, internal oscillator  During STOP, XTAL disabled (PCTL Bit 16 = 0)  During STOP, XTAL enabled (PCTL Bit 16 = 1)  During normal operation	$50 \times \text{ET}_{\text{C}} \\ 1000 \times \text{ET}_{\text{C}} \\ 75000 \times \text{ET}_{\text{C}} \\ 75000 \times \text{ET}_{\text{C}} \\ 2.5 \times \text{T}_{\text{C}} \\ 2.5 \times \text{T}_{\text{C}}$	625.0 12.5 1.0 1.0 31.3 31.3	_ _ _ _ _	500.0 10.0 0.75 0.75 25.0 25.0	- - - -	ns µs ms ms ns ns
10	Delay from asynchronous RESET deassertion to first external address output (internal reset deassertion) <sup>5</sup> • Minimum  • Maximum	3.25 × T <sub>C</sub> + 2.0 20.25 T <sub>C</sub> + 10.0	42.6 —	 263.1	34.5 —	 212.5	ns ns
11	Synchronous reset setup time from RESET deassertion to CLKOUT Transition 1  Minimum  Maximum	T <sub>C</sub>	7.4 —	<u> </u>	5.9 —	<u> </u>	ns ns
12	Synchronous reset deasserted, delay time from the CLKOUT Transition 1 to the first external address output  Minimum  Maximum	3.25 × T <sub>C</sub> + 1.0 20.25 × T <sub>C</sub> + 1.0	41.6 —	 258.1	33.5	 207.5	ns ns
13	Mode select setup time		30.0	_	30.0	_	ns
14	Mode select hold time		0.0	_	0.0	_	ns
15	Minimum edge-triggered interrupt request assertion width		8.25	_	6.6	_	ns
16	Minimum edge-triggered interrupt request deassertion width		8.25	_	7.1	_	ns
17	Delay from IRQA, IRQB, IRQC, IRQD, NMI assertion to external memory access address out valid  Caused by first interrupt instruction fetch  Caused by first interrupt instruction execution	$4.25 \times T_{C} + 2.0$ $7.25 \times T_{C} + 2.0$	55.1 92.6	_	44.5 74.5	_	ns ns
18	Delay from IRQA, IRQB, IRQC, IRQD, NMI assertion to general-purpose transfer output valid caused by first interrupt instruction execution	10 × T <sub>C</sub> + 5.0	130.0	_	105.0	_	ns
19	Delay from address output valid caused by first interrupt instruction execute to interrupt request deassertion for level sensitive fast interrupts <sup>1</sup>	$\begin{array}{c} \textbf{80 MHz:} \\ 3.75 \times T_{C} + \text{WS} \times T_{C} - 12.4 \\ \textbf{100 MHz:} \\ 3.75 \times T_{C} + \text{WS} \times T_{C} - 10.94 \end{array}$	_	Note 8	_	Note 8	ns ns
20	Delay from RD assertion to interrupt request deassertion for level sensitive fast interrupts <sup>1</sup>	<b>80 MHz</b> : $3.25 \times T_C + WS \times T_C - 12.4$ <b>100 MHz</b> : $3.25 \times T_C + WS \times T_C - 10.94$	_	Note 8	_	Note 8	ns ns



 Table 2-7.
 Reset, Stop, Mode Select, and Interrupt Timing<sup>6</sup> (Continued)

N'a	Characteristic -	Fyggessien	80 1	ИНz	100 MHz		lle!4
No.	Characteristics	Expression	Min	Max	Min	Max	Unit
21	Delay from WR assertion to interrupt request deassertion for level sensitive fast interrupts <sup>1</sup> • DRAM for all WS <sup>7</sup>	<b>80 MHz</b> : (WS + 3.5) × T <sub>C</sub> – 12.4 <b>100 MHz</b> :	_	Note 8	_	Note 8	ns ns
	• SRAM WS = 1	$(WS + 3.5) \times T_C - 10.94$ <b>80 MHz</b> : $(WS + 3.5) \times T_C - 12.4$ <b>100 MHz</b> :	_	Note 8	_	Note 8	ns ns
	• SRAM WS = 2, 3	(WS + 3.5) × T <sub>C</sub> - 10.94 <b>80 MHz</b> : (WS + 3) × T <sub>C</sub> - 12.4 <b>100 MHz</b> :	_	Note 8		Note 8	ns
	• SRAM WS ≥ 4	$(WS + 3) \times T_C - 10.94$ <b>80 MHz</b> : $(WS + 2.5) \times T_C - 12.4$	_	Note 8	_		ns ns
		<b>100 MHz</b> : (WS + 2.5) × T <sub>C</sub> – 10.94			_	Note 8	ns
22	Synchronous interrupt setup time from IRQA, IRQB, IRQC, IRQD, NMI assertion to the CLKOUT Transition 2		7.4	T <sub>C</sub>	5.9	T <sub>C</sub>	ns
23	Synchronous interrupt delay time from the CLKOUT Transition 2 to the first external address output valid caused by the first instruction fetch after coming out of Wait Processing state  Minimum  Maximum	8.25 × T <sub>C</sub> + 1.0 24.75 × T <sub>C</sub> + 5.0	116.6 —	— 314.4	83.5	 252.5	ns ns
24	Duration for IRQA assertion to recover from Stop state		7.4	_	5.9	_	ns
25	Delay from IRQA assertion to fetch of first instruction (when exiting Stop) <sup>2, 3</sup> • PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0)	$PLC \times ET_{C} \times PDF + (128 \text{ K} - PLC/2) \times T_{C}$	1.6	17.0	1.3	13.6	ms
	<ul> <li>PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1)</li> </ul>	PLC × ET <sub>C</sub> × PDF + $(23.75 \pm 0.5) \times$ T <sub>C</sub> $(9.25 \pm 0.5) \times$ TC	290.6 ns	15.4 ms 121.9	232.5 ns 87.5	12.3 ms 97.5	ns
	<ul> <li>PLL is active during Stop (PCTL Bit 17 = 1) (Implies No Stop Delay)</li> </ul>						
26	Duration of level sensitive IRQA assertion to ensure interrupt service (when exiting Stop) <sup>2, 3</sup> PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is enabled (Operating Mode Register Bit 6 = 0)	$\begin{array}{c} PLC \times ET_{C} \times PDF + (128K - \\ PLC/2) \times T_{C} \end{array}$	17.0	_	13.6	_	ms
	<ul> <li>PLL is not active during Stop (PCTL Bit 17 = 0) and Stop delay is not enabled (Operating Mode Register Bit 6 = 1)</li> </ul>	$PLC \times ET_C \times PDF + (20.5 \pm 0.5) \times T_C$ $5.5 \times T_C$	15.4 68.8	_	12.3 55.0	_	ms ns
	<ul> <li>PLL is active during Stop (PCTL Bit 17 = 1) (implies no Stop delay)</li> </ul>						
27	Interrupt Request Rate  HI32, ESSI, SCI, Timer  DMA  IRQ, NMI (edge trigger)  IRQ, NMI (level trigger)	$\begin{array}{c} 12 \times T_C \\ 8 \times T_C \\ 8 \times T_C \\ 12 \times T_C \end{array}$	_ _ _ _	150.0 100.0 100.0 150.0	_ _ _	120.0 80.0 80.0 120.0	ns ns ns

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2-8 Freescale Semiconductor



<b>Table 2-7.</b> Reset, Stop, Mode Select, and Interrupt Timing <sup>6</sup> (Contin
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No.	Characteristics	Expression	80 MHz		100 MHz		I I m i 4
			Min	Max	Min	Max	Unit
28	DMA Request Rate  Data read from HI32, ESSI, SCI  Data write to HI32, ESSI, SCI  Timer  IRQ, NMI (edge trigger)	$\begin{array}{c} 6\times T_{C} \\ 7\times T_{C} \\ 2\times T_{C} \\ 3\times T_{C} \end{array}$	_ _ _ _	75.0 87.5 25.0 37.5	_ _ _ _	60.0 70.0 20.0 30.0	ns ns ns
29	Delay from IRQA, IRQB, IRQC, IRQD, NMI assertion to external memory (DMA source) access address out valid	$4.25 \times T_{C} + 2.0$	55.1	_	44.5	_	ns

Notes:

- 1. When using fast interrupts and  $\overline{IRQB}$ ,  $\overline{IRQB}$ ,  $\overline{IRQC}$ , and  $\overline{IRQD}$  are defined as level-sensitive, timings 19 through 21 apply to prevent multiple interrupt service. To avoid these timing restrictions, the deasserted Edge-triggered mode is recommended when using fast interrupts. Long interrupts are recommended when using Level-sensitive mode.
- **2.** This timing depends on several settings:
  - For PLL disable, using internal oscillator (PLL Control Register (PCTL) Bit 16 = 0) and oscillator disabled during Stop (PCTL Bit 17 = 0), a stabilization delay is required to assure that the oscillator is stable before programs are executed. Resetting the Stop delay (Operating Mode Register Bit 6 = 0) provides the proper delay. While Operating Mode Register Bit 6 = 1 can be set, it is not recommended, and these specifications do not guarantee timings for that case.
  - For PLL disable, using internal oscillator (PCTL Bit 16 = 0) and oscillator enabled during Stop (PCTL Bit 17=1), no stabilization delay is required and recovery is minimal (Operating Mode Register Bit 6 setting is ignored).
  - For PLL disable, using external clock (PCTL Bit 16 = 1), no stabilization delay is required and recovery time is defined by the PCTL Bit 17 and Operating Mode Register Bit 6 settings.
  - For PLL enable, if PCTL Bit 17 is 0, the PLL is shutdown during Stop. Recovering from Stop requires the PLL to get locked. The PLL lock procedure duration, PLL Lock Cycles (PLC), may be in the range of 0 to 1000 cycles. This procedure occurs in parallel with the stop delay counter, and stop recovery ends when the last of these two events occurs. The stop delay counter completes count or PLL lock procedure completion.
  - PLC value for PLL disable is 0.
  - The maximum value for ET<sub>C</sub> is 4096 (maximum MF) divided by the desired internal frequency (that is, for 66 MHz it is 4096/66 MHz = 62  $\mu$ s). During the stabilization period, T<sub>C</sub>, T<sub>H</sub>, and T<sub>L</sub> is not constant, and their width may vary, so timing may vary as well.
- 3. Periodically sampled and not 100 percent tested.
- 4. Value depends on clock source:
  - For an external clock generator, RESET duration is measured while RESET is asserted, V<sub>CC</sub> is valid, and the EXTAL input is active and valid.
  - For an internal oscillator, RESET duration is measured while RESET is asserted and V<sub>CC</sub> is valid. The specified timing reflects the crystal oscillator stabilization time after power-up. This number is affected both by the specifications of the crystal and other components connected to the oscillator and reflects worst case conditions.
  - When the V<sub>CC</sub> is valid, but the other "required RESET duration" conditions (as specified above) have not been yet met, the device circuitry is in an uninitialized state that can result in significant power consumption and heat-up. Designs should minimize this state to the shortest possible duration.
- 5. If PLL does not lose lock.
- **6.**  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $T_{J} = -40 ^{\circ}\text{C}$  to +100  $^{\circ}\text{C}$ ,  $C_{L} = 50 \text{ pF}$ .
- 7. WS = number of wait states (measured in clock cycles, number of  $T_C$ ).
- 8. Use the expression to compute a maximum value.

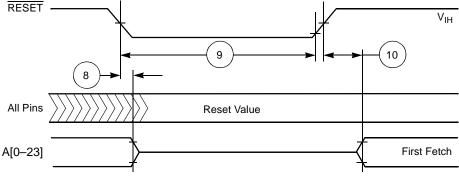


Figure 2-3. Reset Timing

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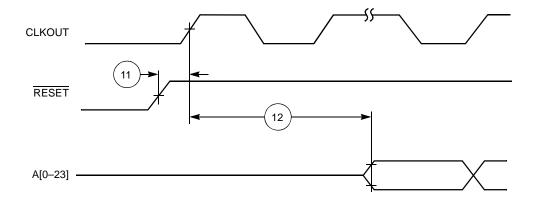
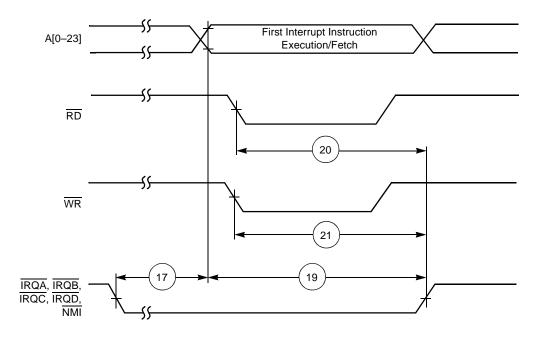
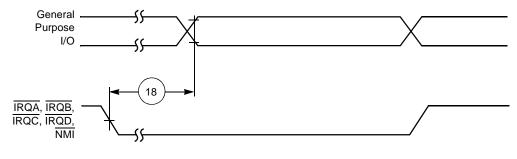


Figure 2-4. Synchronous Reset Timing



#### a) First Interrupt Instruction Execution



b) General-Purpose I/O

Figure 2-5. External Fast Interrupt Timing

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2-10 Freescale Semiconductor



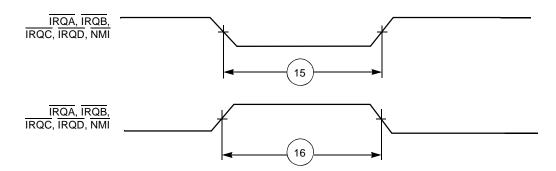


Figure 2-6. External Interrupt Timing (Negative Edge-Triggered)

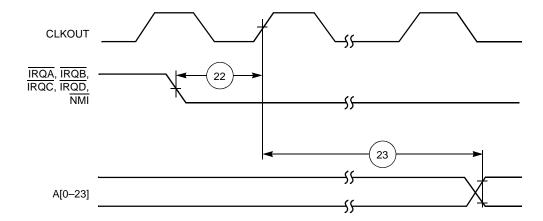


Figure 2-7. Synchronous Interrupt from Wait State Timing

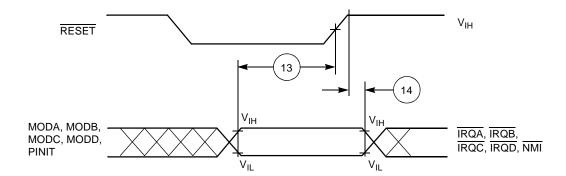


Figure 2-8. Operating Mode Select Timing

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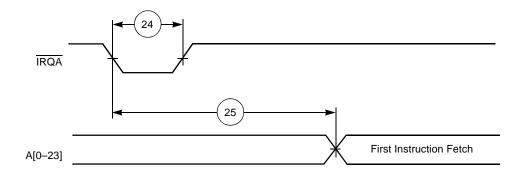


Figure 2-9. Recovery from Stop State Using IRQA

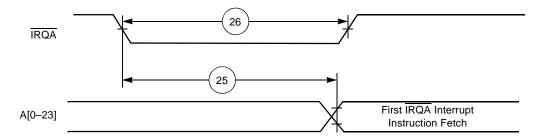


Figure 2-10. Recovery from Stop State Using IRQA Interrupt Service

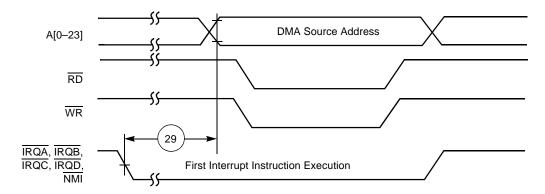


Figure 2-11. External Memory Access (DMA Source) Timing

# 2.5.5 External Memory Expansion Port (Port A)



## 2.5.5.1 SRAM Timing

**Table 2-8.** SRAM Read and Write Accesses<sup>3,6</sup>

NI	Oh amari a tati a	0	F 1	80 1	ИНz	100	MHz	1124
No.	Characteristics	Symbol	Expression <sup>1</sup>	Min	Max	Min	Max	Unit
100	Address valid and AA assertion pulse width <sup>2</sup>	t <sub>RC</sub> , t <sub>WC</sub>	$ \begin{array}{c} (\text{WS} + 1) \times \text{T}_{\text{C}} - 4.0 \ [1 \leq \text{WS} \leq 3] \\ (\text{WS} + 2) \times \text{T}_{\text{C}} - 4.0 \ [4 \leq \text{WS} \leq 7] \\ (\text{WS} + 3) \times \text{T}_{\text{C}} - 4.0 \ [\text{WS} \geq 8] \end{array} $	21.0 71.0 133.5	_ _ _	16.0 56.0 106.0	_ _ _	ns ns ns
101	Address and AA valid to WR assertion	t <sub>AS</sub>	$\begin{array}{c} 0.25 \times T_{C} - 2.0 \; [WS = 1] \\ 0.75 \times T_{C} - 2.0 \; [2 \leq WS \leq 3] \\ 1.25 \times T_{C} - 2.0 \; [WS \geq 4] \end{array}$	1.1 7.4 13.6	 _ _	0.5 5.5 10.5	_ _ _	ns ns ns
102	WR assertion pulse width	t <sub>WP</sub>	$\begin{array}{c} 1.5 \times T_{C} - 4.0 \; [WS = 1] \\ WS \times T_{C} - 4.0 \; [2 \leq WS \leq 3] \\ (WS - 0.5) \times T_{C} - 4.0 \; [WS \geq 4] \end{array}$	14.8 21.0 39.8	_ _ _	11.0 16.0 31.0	_ _ _	ns ns ns
103	WR deassertion to address not valid	t <sub>WR</sub>	$\begin{array}{c} 0.25 \times T_{C} - 2.0 \; [1 \leq WS \leq 3] \\ 1.25 \times T_{C} - 4.0 \; [4 \leq WS \leq 7] \\ 2.25 \times T_{C} - 4.0 \; [WS \geq 8] \end{array}$	1.1 11.6 24.1	_ _ _	0.5 8.5 18.5	_ _ _	ns ns ns
104	Address and AA valid to input data valid	t <sub>AA</sub> , t <sub>AC</sub>	$(WS + 0.75) \times T_C - 5.0 [WS \ge 1]$	_	16.9	_	12.5	ns
105	RD assertion to input data valid	t <sub>OE</sub>	$(WS + 0.25) \times T_{C} - 5.0 \text{ [WS } \ge 1]$	_	10.6	_	7.5	ns
106	RD deassertion to data not valid (data hold time)	t <sub>OHZ</sub>		0.0	_	0.0	_	ns
107	Address valid to WR deassertion <sup>2</sup>	t <sub>AW</sub>	$(WS + 0.75) \times T_C - 4.0 \ [WS \ge 1]$	17.9	_	13.5	_	ns
108	Data valid to WR deassertion (data setup time)	t <sub>DS</sub> (t <sub>DW</sub> )	$(WS - 0.25) \times T_C - 3.0 \ [WS \ge 1]$	6.4	_	4.5	_	ns
109	Data hold time from WR deassertion	t <sub>DH</sub>	$\begin{array}{c} 0.25 \times T_{C} - 2.0 \; [1 \leq WS \leq 3] \\ 1.25 \times T_{C} - 2.0 \; [4 \leq WS \leq 7] \\ 2.25 \times T_{C} - 2.0 \; [WS \geq 8] \end{array}$	1.1 13.6 26.1	_ _ _	0.5 10.5 20.5	_ _ _	ns ns ns
110	WR assertion to data active		$\begin{array}{c} 0.75 \times T_{C} - 3.7 \; [WS = 1] \\ 0.25 \times T_{C} - 3.7 \; [2 \leq WS \leq 3] \\ -0.25 \times T_{C} - 3.7 \; [WS \geq 4] \end{array}$	5.7 -0.6 -6.8	_ _ _	3.8 -1.2 -6.2	_ _ _	ns ns ns
111	WR deassertion to data high impedance		$\begin{array}{c} 0.25 \times T_{C} + 0.2 \; [1 \leq WS \leq 3] \\ 1.25 \times T_{C} + 0.2 \; [4 \leq WS \leq 7] \\ 2.25 \times T_{C} + 0.2 \; [WS \geq 8] \end{array}$	_ _ _	3.3 15.8 28.3	_ _ _	2.7 12.7 22.7	ns ns ns
112	Previous RD deassertion to data active (write)		$\begin{array}{l} 1.25 \times T_{C} - 4.0 \; [1 \leq WS \leq 3] \\ 2.25 \times T_{C} - 4.0 \; [4 \leq WS \leq 7] \\ 3.25 \times T_{C} - 4.0 \; [WS \geq 8] \end{array}$	11.6 24.1 36.6	_ _ _	8.5 18.5 28.5	_ _ _	ns ns ns
113	RD deassertion time		$\begin{array}{c} 0.75 \times T_C - 4.0 \; [1 \leq WS \leq 3] \\ 1.75 \times T_C - 4.0 \; [4 \leq WS \leq 7] \\ 2.75 \times T_C - 4.0 \; [WS \geq 8] \end{array}$	5.4 17.9 30.4	_ _ _	3.5 13.5 23.5	_ _ _	ns ns ns
114	WR deassertion time		$0.5 \times T_{C} - 4.0 \text{ [WS = 1]}$ $T_{C} - 4.0 \text{ [2 \le WS \le 3]}$ $2.5 \times T_{C} - 4.0 \text{ [4 \le WS \le 7]}$ $3.5 \times T_{C} - 4.0 \text{ [WS \ge 8]}$	2.3 8.5 27.3 39.8	_ _ _ _	1.0 6.0 21.0 31.0	_ _ _ _	ns ns ns

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**Table 2-8.** SRAM Read and Write Accesses<sup>3,6</sup> (Continued)

No.	Characteristics	Symbol	Expression <sup>1</sup>	1 08	ИНz	100	MHz	Unit
140.	Onaracteristics	Oymboi	Expression	Min	Max	Min	Max	Onit
115	Address valid to RD assertion		0.5 × T <sub>C</sub> – 4.0	2.3	_	1.0	_	ns
116	RD assertion pulse width		$(WS + 0.25) \times T_C - 4.0$	11.6	_	8.5	_	ns
117	RD deassertion to address not valid		$\begin{array}{c} 0.25 \times T_{C} - 2.0 \ [1 \leq WS \leq 3] \\ 1.25 \times T_{C} - 2.0 \ [4 \leq WS \leq 7] \\ 2.25 \times T_{C} - 2.0 \ [WS \geq 8] \end{array}$	1.1 13.6 26.1	_ _ _	0.5 10.5 20.5	_ _ _	ns ns ns
118	TA setup before RD or WR deassertion <sup>4</sup>		$0.25 \times T_{C} + 2.0$	5.1	_	4.5	_	ns
119	TA hold after RD or WR deassertion			0	_	0	_	ns

- 1. WS is the number of wait states specified in the BCR.
- 2. Timings 100, 107 are guaranteed by design, not tested.
- 3. All timings for 100 MHz are measured from 0.5 · Vcc to 0.5 · Vcc
- **4.** Timing 118 is relative to the deassertion edge of  $\overline{RD}$  or  $\overline{WR}$  even if  $\overline{TA}$  remains active.
- 5. Timings 110, 111, and 112, are not helpful and are not specified for 100 MHz.
- **6.**  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $T_{J} = -40^{\circ}\text{C}$  to  $+100^{\circ}\text{C}$ ,  $C_{L} = 50 \text{ pF}$

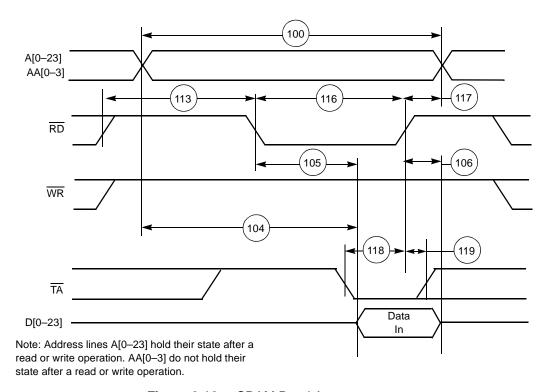
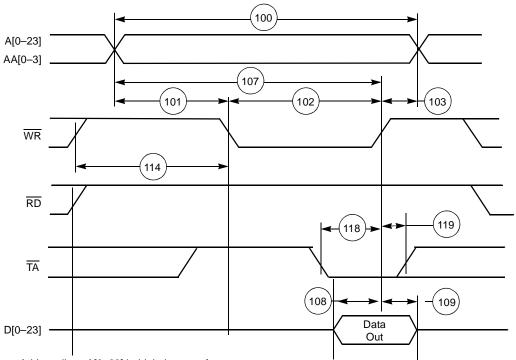


Figure 2-12. SRAM Read Access

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Note: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-13. SRAM Write Access

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### 2.5.5.2 DRAM Timing

The selection guides in **Figure 2-14** and **Figure 2-17** are for primary selection only. Final selection should be based on the timing in the following tables. For example, the selection guide suggests that four wait states must be used for 100 MHz operation in Page Mode DRAM. However, using the information in the appropriate table, a designer could choose to evaluate whether fewer wait states might be used by determining which timing prevents operation at 100 MHz, by running the chip at a slightly lower frequency (for example, 95 MHz), by using faster DRAM (if it becomes available), and by manipulating control factors such as capacitive and resistive load to improve overall system performance.

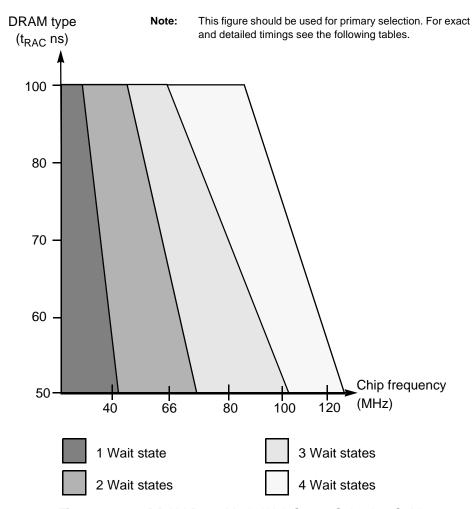


Figure 2-14. DRAM Page Mode Wait States Selection Guide

2-16 Freescale Semiconductor



**Table 2-9.** DRAM Page Mode Timings, Two Wait States<sup>1, 2, 3, 7</sup>

N-	Observatoristica	0	F	80 1	ИНz	1121
No.	Characteristics	Symbol	Expression	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction		3×T <sub>C</sub>	37.5	_	ns
	Page mode cycle time for mixed (read and write) accesses	t <sub>PC</sub>	$2.75\times T_{\hbox{\scriptsize C}}$	34.4	_	ns
132	CAS assertion to data valid (read)	t <sub>CAC</sub>	$1.5 \times T_C - 6.5$	_	12.3	ns
133	Column address valid to data valid (read)	t <sub>AA</sub>	$2.5 \times T_C - 6.5$	_	24.8	ns
134	CAS deassertion to data not valid (read hold time)	t <sub>OFF</sub>		0.0	_	ns
135	Last CAS assertion to RAS deassertion	t <sub>RSH</sub>	$1.75 \times T_{C} - 4.0$	17.9	_	ns
136	Previous CAS deassertion to RAS deassertion	t <sub>RHCP</sub>	$3.25 \times T_{C} - 4.0$	36.6	_	ns
137	CAS assertion pulse width	t <sub>CAS</sub>	$1.5 \times T_{C} - 4.0$	14.8	_	ns
138	Last $\overline{\text{CAS}}$ deassertion to $\overline{\text{RAS}}$ deassertion <sup>5</sup> BRW[1-0] = 00  BRW[1-0] = 01  BRW[1-0] = 10  BRW[1-0] = 11	t <sub>CRP</sub>	Not supported $3.5 \times T_C - 6.0$ $4.5 \times T_C - 6.0$ $6.5 \times T_C - 6.0$	 37.8 50.3 75.3	_ _ _ _	ns ns ns
139	CAS deassertion pulse width	t <sub>CP</sub>	1.25 × T <sub>C</sub> – 4.0	11.6	_	ns
140	Column address valid to CAS assertion	t <sub>ASC</sub>	T <sub>C</sub> – 4.0	8.5	_	ns
141	CAS assertion to column address not valid	t <sub>CAH</sub>	$1.75 \times T_{C} - 4.0$	17.9	_	ns
142	Last column address valid to RAS deassertion	t <sub>RAL</sub>	$3 \times T_C - 4.0$	33.5	_	ns
143	WR deassertion to CAS assertion	t <sub>RCS</sub>	1.25 × T <sub>C</sub> – 4	11.6	_	ns
144	CAS deassertion to WR assertion	t <sub>RCH</sub>	$0.5 \times T_{C} - 3.7$	2.6	_	ns
145	CAS assertion to WR deassertion	t <sub>WCH</sub>	1.5 × T <sub>C</sub> – 4.2	14.6	_	ns
146	WR assertion pulse width	t <sub>WP</sub>	$2.5 \times T_{C} - 4.5$	26.8	_	ns
147	Last WR assertion to RAS deassertion	t <sub>RWL</sub>	$2.75 \times T_{C} - 4.3$	30.1	_	ns
148	WR assertion to CAS deassertion	t <sub>CWL</sub>	$2.5 \times T_{C} - 4.3$	27.0	_	ns
149	Data valid to CAS assertion (write)	t <sub>DS</sub>	$0.25 \times T_C - 3.0$	0.1	_	ns
150	CAS assertion to data not valid (write)	t <sub>DH</sub>	$1.75 \times T_{C} - 4.0$	17.9	_	ns
151	WR assertion to CAS assertion	t <sub>WCS</sub>	T <sub>C</sub> – 4.3	8.2	_	ns
152	Last RD assertion to RAS deassertion	t <sub>ROH</sub>	$2.5\times T_C-4.0$	27.3	_	ns
153	RD assertion to data valid	t <sub>GA</sub>	$1.75 \times T_{C} - 6.5$	<u> </u>	15.4	ns
154	RD deassertion to data not valid <sup>6</sup>	t <sub>GZ</sub>		0.0	_	ns
155	WR assertion to data active		$0.75 \times T_{C} - 1.5$	7.9	_	ns
156	WR deassertion to data high impedance		$0.25 \times T_C$	_	3.1	ns
1	· · · · · · · · · · · · · · · · · · ·					

- 1. The number of wait states for Page mode access is specified in the DCR.
- 2. The refresh period is specified in the DCR.
- 3. The asynchronous delays specified in the expressions are valid for the DSP56301.
- 4. All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example,  $t_{PC}$  equals  $3 \times T_{C}$  for read-after-read or write-after-write sequences).
- 5. BRW[1–0] (DRAM Control Register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access.
- **6.** RD deassertion always occurs after  $\overline{\text{CAS}}$  deassertion; therefore, the restricted timing is  $t_{\text{OFF}}$  and not  $t_{\text{GZ}}$ .
- 7. At this time, there are no DRAMs fast enough to fit with two wait states Page mode @ 100MHz (see **Table 2-14**). However, DRAM speeds are approaching two-wait-state compatibility.



DRAM Page Mode Timings, Three Wait States<sup>1, 2, 3</sup> Table 2-10.

				80 1	MHz	100	MHz	
No.	Characteristics	Symbol	Expression	Min	Max	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction		4×T <sub>C</sub>	50.0	_	40.0	_	ns
	Page mode cycle time for mixed (read and write) accesses	t <sub>PC</sub>	$3.5 \times T_C$	43.7	_	35.0	_	ns
132	CAS assertion to data valid (read)	t <sub>CAC</sub>	$2 \times T_C - 5.7$	_	19.3	_	14.3	ns
133	Column address valid to data valid (read)	t <sub>AA</sub>	$3 \times T_C - 5.7$	_	31.8	_	24.3	ns
134	CAS deassertion to data not valid (read hold time)	t <sub>OFF</sub>		0.0	_	0.0	_	ns
135	Last CAS assertion to RAS deassertion	t <sub>RSH</sub>	$2.5\times T_C-4.0$	27.3	_	21.0	_	ns
136	Previous CAS deassertion to RAS deassertion	t <sub>RHCP</sub>	$4.5\times T_C-4.0$	52.3	_	41.0	_	ns
137	CAS assertion pulse width	t <sub>CAS</sub>	$2 \times T_C - 4.0$	21.0	_	16.0	_	ns
138	Last CAS deassertion to RAS assertion <sup>5</sup> BRW[1-0] = 00  BRW[1-0] = 01  BRW[1-0] = 10  BRW[1-0] = 11	t <sub>CRP</sub>	Not supported $3.75 \times T_C - 6.0$ $4.75 \times T_C - 6.0$ $6.75 \times T_C - 6.0$	40.9 53.4 78.4	_ _ _ _	— 31.5 41.5 61.5	_ _ _ _	ns ns ns
139	CAS deassertion pulse width	t <sub>CP</sub>	$1.5 \times T_{C} - 4.0$	14.8	_	11.0	_	ns
140	Column address valid to CAS assertion	t <sub>ASC</sub>	T <sub>C</sub> – 4.0	8.5	_	6.0	_	ns
141	TAS assertion to column address not valid	t <sub>CAH</sub>	$2.5 \times T_{C} - 4.0$	27.3	_	21.0	_	ns
142	Last column address valid to RAS deassertion	t <sub>RAL</sub>	$4 \times T_C - 4.0$	46.0	_	36.0	_	ns
143	WR deassertion to CAS assertion	t <sub>RCS</sub>	$1.25\times T_C-4.0$	11.6	_	8.5	_	ns
144	CAS deassertion to WR assertion	t <sub>RCH</sub>	$0.75 \times TC - 4.0$	5.4	_	3.5	_	ns
145	CAS assertion to WR deassertion	t <sub>WCH</sub>	$2.25\times T_C-4.2$	23.9	_	18.3	_	ns
146	WR assertion pulse width	t <sub>WP</sub>	$3.5\times T_C-4.5$	39.3	_	30.5	_	ns
147	Last WR assertion to RAS deassertion	t <sub>RWL</sub>	$3.75\times T_C-4.3$	42.6	_	33.2	_	ns
148	WR assertion to CAS deassertion	t <sub>CWL</sub>	$3.25\times T_C-4.3$	36.3	_	28.2	_	ns
149	Data valid to CAS assertion (write)	t <sub>DS</sub>	$0.5\times T_C-4.8$	2.0	_	0.2	_	ns
150	CAS assertion to data not valid (write)	t <sub>DH</sub>	$2.5\times T_C-4.0$	27.3	_	21.0	_	ns
151	WR assertion to CAS assertion	t <sub>WCS</sub>	$1.25\times T_C-4.3$	11.3	_	8.2	_	ns
152	Last RD assertion to RAS deassertion	t <sub>ROH</sub>	$3.5\times T_C-4.0$	39.8	_	31.0	_	ns
153	RD assertion to data valid	t <sub>GA</sub>	$2.5 \times T_C - 5.7$	_	25.6	_	19.3	ns
154	RD deassertion to data not valid <sup>6</sup>	t <sub>GZ</sub>		0.0	_	0.0	_	ns
155	WR assertion to data active		$0.75 \times T_{C} - 1.5$	7.9	_	6.0		ns
156	WR deassertion to data high impedance		$0.25 \times T_{\mathbb{C}}$	_	3.1	_	2.5	ns

- 1. The number of wait states for Page mode access is specified in the DCR.
- 2. The refresh period is specified in the DCR.
- The asynchronous delays specified in the expressions are valid for DSP56301.
- All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example,  $t_{PC}$  equals  $4 \times 10^{-2}$ T<sub>C</sub> for read-after-read or write-after-write sequences).
- BRW[1-0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of pageaccess.
- $\overline{\text{RD}}$  deassertion always occurs after  $\overline{\text{CAS}}$  deassertion; therefore, the restricted timing is  $t_{\text{OFF}}$  and not  $t_{\text{GZ}}$ .



**Table 2-11.** DRAM Page Mode Timings, Four Wait States<sup>1, 2, 3</sup>

Na	Ch avantovinting	Comple el	Funnasian	1 08	ИНz	100	MHz	l l m !t
No.	Characteristics	Symbol	Expression	Min	Max	Min	Max	Unit
131	Page mode cycle time for two consecutive accesses of the same direction		5×T <sub>C</sub>	62.5	_	50.0		ns
	Page mode cycle time for mixed (read and write) accesses	t <sub>PC</sub>	$4.5 \times T_{C}$	56.2	_	45.0	-	ns
132	CAS assertion to data valid (read)	t <sub>CAC</sub>	$2.75\times T_C-5.7$	_	28.7	_	21.8	ns
133	Column address valid to data valid (read)	t <sub>AA</sub>	$3.75\times T_C-5.7$	_	41.2	_	31.8	ns
134	CAS deassertion to data not valid (read hold time)	t <sub>OFF</sub>		0.0	_	0.0	1	ns
135	Last CAS assertion to RAS deassertion	t <sub>RSH</sub>	$3.5 \times T_C - 4.0$	39.8	_	31.0	_	ns
136	Previous CAS deassertion to RAS deassertion	t <sub>RHCP</sub>	6 × T <sub>C</sub> – 4.0	71.0	_	56.0	_	ns
137	CAS assertion pulse width	t <sub>CAS</sub>	$2.5 \times T_{C} - 4.0$	27.3	_	21.0	_	ns
138	Last CAS deassertion to RAS assertion <sup>5</sup> BRW[1-0] = 00  BRW[1-0] = 01  BRW[1-0] = 10  BRW[1-0] = 11	<sup>t</sup> CRP	Not supported $4.25 \times T_C - 6.0$ $5.25 \times T_C - 6.0$ $7.25 \times T_C - 6.0$	 47.2 59.6 84.6	_ _ _ _	— 36.5 46.5 66.5		ns ns ns
139	CAS deassertion pulse width	t <sub>CP</sub>	2 × T <sub>C</sub> - 4.0	21.0	_	16.0		ns
140	Column address valid to CAS assertion	t <sub>ASC</sub>	T <sub>C</sub> – 4.0	8.5	_	6.0	_	ns
141	CAS assertion to column address not valid	t <sub>CAH</sub>	$3.5 \times T_C - 4.0$	39.8	_	31.0	_	ns
142	Last column address valid to RAS deassertion	t <sub>RAL</sub>	5 × T <sub>C</sub> – 4.0	58.5	_	46.0	_	ns
143	WR deassertion to CAS assertion	t <sub>RCS</sub>	$1.25 \times T_{C} - 4.0$	11.8	_	8.5	_	ns
144	CAS deassertion to WR assertion	t <sub>RCH</sub>	$1.25 \times T_{C} - 3.7$	11.9	_	8.8	_	ns
145	CAS assertion to WR deassertion	t <sub>WCH</sub>	$3.25 \times T_{C} - 4.2$	36.4	_	28.3	_	ns
146	WR assertion pulse width	t <sub>WP</sub>	$4.5 \times T_C - 4.5$	51.8	_	40.5	_	ns
147	Last WR assertion to RAS deassertion	t <sub>RWL</sub>	$4.75\times T_{C}-4.3$	55.1	_	43.2	_	ns
148	WR assertion to CAS deassertion	t <sub>CWL</sub>	$3.75 \times T_{C} - 4.3$	42.6	_	33.2	_	ns
149	Data valid to CAS assertion (write)	t <sub>DS</sub>	$0.5 \times T_{C} - 4.8$	1.5	_	0.2	_	ns
150	CAS assertion to data not valid (write)	t <sub>DH</sub>	$3.5 \times T_C - 4.0$	39.8	_	31.0	_	ns
151	WR assertion to CAS assertion	t <sub>wcs</sub>	$1.25 \times T_{C} - 4.3$	11.3	_	8.2	_	ns
152	Last RD assertion to RAS deassertion	t <sub>ROH</sub>	$4.5 \times T_C - 4.0$	52.3	_	41.0	_	ns
153	RD assertion to data valid	t <sub>GA</sub>	$3.25 \times T_C - 5.7$	_	34.9	_	26.8	ns
154	RD deassertion to data not valid <sup>6</sup>	t <sub>GZ</sub>		0.0	_	0.0	_	ns
155	WR assertion to data active		$0.75 \times T_{C} - 1.5$	7.9	_	6.0	_	ns
156	WR deassertion to data high impedance		0.25 × T <sub>C</sub>	_	3.1		2.5	ns

- 1. The number of wait states for Page mode access is specified in the DCR.
- **2.** The refresh period is specified in the DCR.
- 3. The asynchronous delays specified in the expressions are valid for DSP56301.
- **4.** All the timings are calculated for the worst case. Some of the timings are better for specific cases (for example, t<sub>PC</sub> equals  $3 \times T_C$  for read-after-read or write-after-write sequences).
- 5. BRW[1–0] (DRAM control register bits) defines the number of wait states that should be inserted in each DRAM out-of-page access. N/A = does not apply because 100 MHz requires a minimum of three wait states.
- 6. RD deassertion always occurs after CAS deassertion; therefore, the restricted timing is t<sub>OFF</sub> and not t<sub>GZ</sub>.



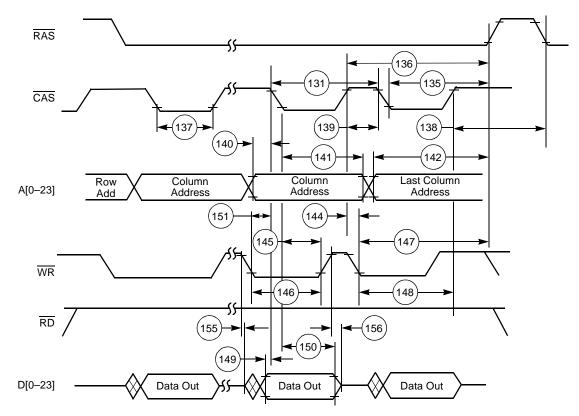


Figure 2-15. DRAM Page Mode Write Accesses

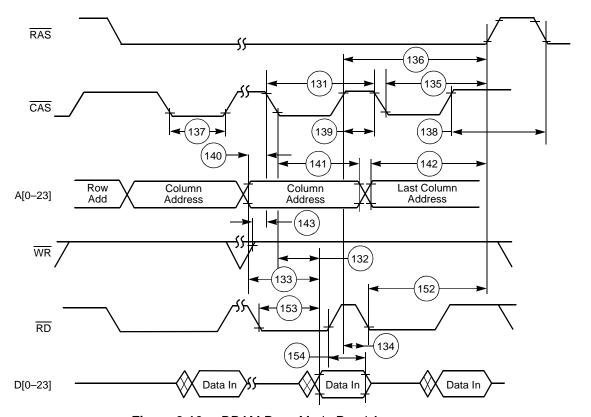


Figure 2-16. DRAM Page Mode Read Accesses

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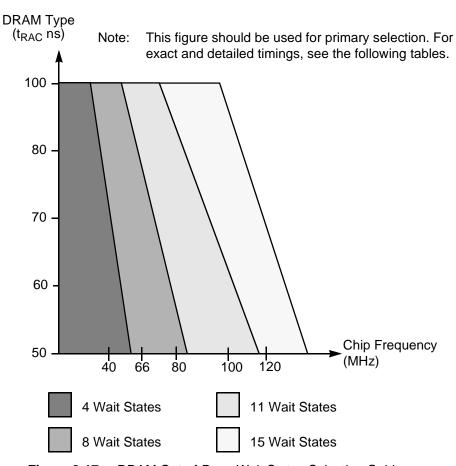


Figure 2-17. DRAM Out-of-Page Wait States Selection Guide

**Table 2-12.** DRAM Out-of-Page and Refresh Timings, Eight Wait States<sup>1, 2</sup>

N.	3	Comple of	Fygunasian	80 1	ИНz	I I mit
No.	Characteristics <sup>3</sup>	Symbol	Expression	Min	Max	Unit
157	Random read or write cycle time	t <sub>RC</sub>	9×T <sub>C</sub>	112.5	_	ns
158	RAS assertion to data valid (read)	t <sub>RAC</sub>	$4.75 \times T_{C} - 6.5$	_	52.9	ns
159	CAS assertion to data valid (read)	t <sub>CAC</sub>	$2.25 \times T_{C} - 6.5$	_	21.6	ns
160	Column address valid to data valid (read)	t <sub>AA</sub>	$3 \times T_C - 6.5$		31.0	ns
161	CAS deassertion to data not valid (read hold time)	t <sub>OFF</sub>		0.0	_	ns
162	RAS deassertion to RAS assertion	t <sub>RP</sub>	$3.25 \times T_{C} - 4.0$	36.6	_	ns
163	RAS assertion pulse width	t <sub>RAS</sub>	$5.75 \times T_C - 4.0$	67.9	_	ns
164	CAS assertion to RAS deassertion	t <sub>RSH</sub>	$3.25 \times T_{C} - 4.0$	36.6	_	ns
165	RAS assertion to CAS deassertion	t <sub>CSH</sub>	$4.75 \times T_{C} - 4.0$	55.4	_	ns
166	CAS assertion pulse width	t <sub>CAS</sub>	$2.25 \times T_{C} - 4.0$	24.1	_	ns
167	RAS assertion to CAS assertion	t <sub>RCD</sub>	$2.5 \times T_C \pm 2$	29.3	33.3	ns
168	RAS assertion to column address valid	t <sub>RAD</sub>	1.75 × T <sub>C</sub> ± 2	19.9	23.9	ns
169	CAS deassertion to RAS assertion	t <sub>CRP</sub>	$4.25 \times T_{C} - 4.0$	49.1	_	ns
170	CAS deassertion pulse width	t <sub>CP</sub>	$2.75 \times T_{C} - 6.0$	28.4	_	ns
171	Row address valid to RAS assertion	t <sub>ASR</sub>	$3.25 \times T_C - 4.0$	36.6	_	ns

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**Table 2-12.** DRAM Out-of-Page and Refresh Timings, Eight Wait States<sup>1, 2</sup> (Continued)

	2	0 1 1	_	80 1	ИНz	
No.	Characteristics <sup>3</sup>	Symbol	Expression	Min	Max	Unit
172	RAS assertion to row address not valid	t <sub>RAH</sub>	1.75 × T <sub>C</sub> – 4.0	17.9	_	ns
173	Column address valid to CAS assertion	t <sub>ASC</sub>	$0.75 \times T_{C} - 4.0$	5.4	_	ns
174	CAS assertion to column address not valid	t <sub>CAH</sub>	$3.25 \times T_{C} - 4.0$	36.6	_	ns
175	RAS assertion to column address not valid	t <sub>AR</sub>	$5.75\times T_C-4.0$	67.9	_	ns
176	Column address valid to RAS deassertion	t <sub>RAL</sub>	$4 \times T_C - 4.0$	46.0	_	ns
177	WR deassertion to CAS assertion	t <sub>RCS</sub>	$2 \times T_C - 3.8$	21.2	_	ns
178	CAS deassertion to WR <sup>4</sup> assertion	t <sub>RCH</sub>	$1.25\times T_C-3.7$	11.9	_	ns
179	RAS deassertion to WR <sup>4</sup> assertion	t <sub>RRH</sub>	$0.25\times T_C-2.6$	0.5	_	ns
180	CAS assertion to WR deassertion	t <sub>WCH</sub>	$3 \times T_C - 4.2$	33.3	_	ns
181	RAS assertion to WR deassertion	t <sub>WCR</sub>	$5.5 \times T_C - 4.2$	64.6	_	ns
182	WR assertion pulse width	t <sub>WP</sub>	$8.5 \times T_C - 4.5$	101.8	_	ns
183	WR assertion to RAS deassertion	t <sub>RWL</sub>	$8.75 \times T_{C} - 4.3$	105.1	_	ns
184	WR assertion to CAS deassertion	t <sub>CWL</sub>	$7.75 \times T_{C} - 4.3$	92.6	_	ns
185	Data valid to CAS assertion (write)	t <sub>DS</sub>	$4.75\times T_C-4.0$	55.4	_	ns
186	CAS assertion to data not valid (write)	t <sub>DH</sub>	$3.25 \times T_{C} - 4.0$	36.6	_	ns
187	RAS assertion to data not valid (write)	t <sub>DHR</sub>	$5.75\times T_C-4.0$	67.9	_	ns
188	WR assertion to CAS assertion	t <sub>WCS</sub>	5.5 × T <sub>C</sub> – 4.3	64.5	_	ns
189	CAS assertion to RAS assertion (refresh)	t <sub>CSR</sub>	$1.5 \times T_{C} - 4.0$	14.8	_	ns
190	RAS deassertion to CAS assertion (refresh)	t <sub>RPC</sub>	1.75 × T <sub>C</sub> – 4.0	17.9	_	ns
191	RD assertion to RAS deassertion	t <sub>ROH</sub>	$8.5 \times T_C - 4.0$	102.3	_	ns
192	RD assertion to data valid	t <sub>GA</sub>	7.5 × T <sub>C</sub> – 6.5	_	87.3	ns
193	RD deassertion to data not valid <sup>3</sup>	t <sub>GZ</sub>		0.0	_	ns
194	WR assertion to data active		$0.75 \times T_{C} - 1.5$	7.9	_	ns
195	WR deassertion to data high impedance		0.25 × T <sub>C</sub>		3.1	ns

- 1. The number of wait states for an out-of-page access is specified in the DCR.
- 2. The refresh period is specified in the DCR.
- 3.  $\overline{RD}$  deassertion always occurs after  $\overline{CAS}$  deassertion; therefore, the restricted timing is  $t_{OFF}$  and not  $t_{GZ}$ .
- **4.** Either t<sub>RCH</sub> or t<sub>RRH</sub> must be satisfied for read cycles.



 Table 2-13.
 DRAM Out-of-Page and Refresh Timings, Eleven Wait States<sup>1, 2</sup>

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	lax	Min	MHz 100 MHz	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		IVIIII	Max	Unit
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	_	120.0	_	ns
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	1.6	_	 55.5	ns ns
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	0.4	_	30.5	ns ns
161 $\overline{\text{CAS}}$ deassertion to data not valid (read hold time) $t_{\text{OFF}}$ 0.0-162 $\overline{\text{RAS}}$ deassertion to $\overline{\text{RAS}}$ assertion $t_{\text{RP}}$ $4.25 \times T_{\text{C}} - 4.0$ 49.1-163 $\overline{\text{RAS}}$ assertion pulse width $t_{\text{RAS}}$ $7.75 \times T_{\text{C}} - 4.0$ 92.9-164 $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion $t_{\text{RSH}}$ $5.25 \times T_{\text{C}} - 4.0$ 61.6-165 $\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion $t_{\text{CSH}}$ $6.25 \times T_{\text{C}} - 4.0$ 74.1-166 $\overline{\text{CAS}}$ assertion pulse width $t_{\text{CAS}}$ $3.75 \times T_{\text{C}} - 4.0$ 42.9-	9.8	_	_ 38.0	ns ns
162 $\overline{RAS}$ deassertion to $\overline{RAS}$ assertion $t_{RP}$ $4.25 \times T_C - 4.0$ $49.1$ -163 $\overline{RAS}$ assertion pulse width $t_{RAS}$ $7.75 \times T_C - 4.0$ $92.9$ -164 $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion $t_{RSH}$ $5.25 \times T_C - 4.0$ $61.6$ -165 $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion $t_{CSH}$ $6.25 \times T_C - 4.0$ $74.1$ -166 $\overline{CAS}$ assertion pulse width $t_{CAS}$ $3.75 \times T_C - 4.0$ $42.9$ -	_ +	0.0	_	ns
163 $\overline{RAS}$ assertion pulse width $t_{RAS}$ $7.75 \times T_C - 4.0$ $92.9$ -164 $\overline{CAS}$ assertion to $\overline{RAS}$ deassertion $t_{RSH}$ $5.25 \times T_C - 4.0$ $61.6$ -165 $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion $t_{CSH}$ $6.25 \times T_C - 4.0$ $74.1$ -166 $\overline{CAS}$ assertion pulse width $t_{CAS}$ $3.75 \times T_C - 4.0$ $42.9$ -	_ †	38.5	_	ns
164 $\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion $t_{\text{RSH}}$ $5.25 \times T_{\text{C}} - 4.0$ $61.6$ $-1.6$ 165 $\overline{\text{RAS}}$ assertion to $\overline{\text{CAS}}$ deassertion $t_{\text{CSH}}$ $6.25 \times T_{\text{C}} - 4.0$ $74.1$ $-1.6$ 166 $\overline{\text{CAS}}$ assertion pulse width $t_{\text{CAS}}$ $3.75 \times T_{\text{C}} - 4.0$ $42.9$ $-1.6$	_ †	73.5	_	ns
165 $\overline{RAS}$ assertion to $\overline{CAS}$ deassertion $t_{CSH}$ $6.25 \times T_C - 4.0$ $74.1$ $-166$ 166 $\overline{CAS}$ assertion pulse width $t_{CAS}$ $3.75 \times T_C - 4.0$ $42.9$	_	48.5	_	ns
166 CAS assertion pulse width t <sub>CAS</sub> 3.75 × T <sub>C</sub> - 4.0 42.9 -	_	58.5	_	ns
		33.5	_	ns
	5.3	21.0	29.0	ns
	5.9	13.5	21.5	ns
	_	53.5	_	ns
170 $\overline{\text{CAS}}$ deassertion pulse width $t_{\text{CP}}$ 4.25 × $T_{\text{C}}$ – 6.0 49.1 -	_	36.5	_	ns
171 Row address valid to $\overline{RAS}$ assertion $t_{ASR}$ 4.25 × $T_{C}$ - 4.0 49.1 -	_	38.5	_	ns
172 $\overline{RAS}$ assertion to row address not valid $t_{RAH}$ 1.75 × $T_{C}$ - 4.0 17.9 -	_	13.5	_	ns
173 Column address valid to $\overline{\text{CAS}}$ assertion $t_{\text{ASC}} = 0.75 \times T_{\text{C}} - 4.0 = 5.4$	_	3.5	_	ns
174 $\overline{\text{CAS}}$ assertion to column address not valid $t_{\text{CAH}}$ 5.25 $\times$ T <sub>C</sub> $-$ 4.0 61.6 -	_	48.5	_	ns
	_ [	73.5	_	ns
176 Column address valid to $\overline{RAS}$ deassertion $t_{RAL}$ $6 \times T_{C} - 4.0$ 71.0 -	_	56.0	_	ns
177 $\overline{\text{WR}}$ deassertion to $\overline{\text{CAS}}$ assertion $t_{\text{RCS}}$ $3.0 \times T_{\text{C}} - 4.0$ 33.5	_	26.0	_	ns
	_ [	13.8	_	ns
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	_	— 0.5	_	ns ns
180 $\overline{\text{CAS}}$ assertion to $\overline{\text{WR}}$ deassertion $t_{\text{WCH}}$ $5 \times T_{\text{C}} - 4.2$ 58.3 -		45.8	_	ns
	_	70.8	_	ns
		110.5	_	ns
		113.2	_	ns
	_	98.2	_	ns
	_	53.5	_	ns
186 $\overline{\text{CAS}}$ assertion to data not valid (write) $t_{\text{DH}}$ 5.25 × $T_{\text{C}}$ - 4.0 61.6 -				

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**Table 2-13.** DRAM Out-of-Page and Refresh Timings, Eleven Wait States<sup>1, 2</sup> (Continued)

Na	Characteristics <sup>3</sup>	Comple ed	Funnasian	1 08	ИНz	100	MHz	11:4
No.	Characteristics	Symbol	Expression	Min	Max	Min	Max	Unit
187	RAS assertion to data not valid (write)	t <sub>DHR</sub>	$7.75\times T_C-4.0$	92.9	_	73.5	_	ns
188	WR assertion to CAS assertion	t <sub>WCS</sub>	$6.5\times T_C-4.3$	77.0	_	60.7		ns
189	CAS assertion to RAS assertion (refresh)	t <sub>CSR</sub>	$1.5 \times T_C - 4.0$	14.8	_	11.0	_	ns
190	RAS deassertion to CAS assertion (refresh)	t <sub>RPC</sub>	$2.75\times T_C-4.0$	30.4	_	23.5	_	ns
191	RD assertion to RAS deassertion	t <sub>ROH</sub>	$11.5 \times T_{C} - 4.0$	139.8	_	111.0	_	ns
192	RD assertion to data valid	t <sub>GA</sub>	$\begin{array}{c} \textbf{80 MHz:} \\ \textbf{10} \times \textbf{T}_{C} - \textbf{6.5} \\ \textbf{100 MHz:} \\ \textbf{10} \times \textbf{T}_{C} - \textbf{7.0} \end{array}$	_	118.5	1 1	93.0	ns ns
193	RD deassertion to data not valid <sup>3</sup>	t <sub>GZ</sub>		0.0	_	0.0	-	ns
194	WR assertion to data active		$0.75 \times T_{C} - 1.5$	9.1	_	6.0		ns
195	WR deassertion to data high impedance		0.25 × T <sub>C</sub>	_	3.1		2.5	ns

- 1. The number of wait states for an out-of-page access is specified in the DCR.
  - 2. The refresh period is specified in the DCR.
  - 3.  $\overline{RD}$  deassertion always occurs after  $\overline{CAS}$  deassertion; therefore, the restricted timing is  $t_{OFF}$  and not  $t_{GZ}$ .
  - 4. Either t<sub>RCH</sub> or t<sub>RRH</sub> must be satisfied for read cycles.

**Table 2-14.** DRAM Out-of-Page and Refresh Timings, Fifteen Wait States<sup>1, 2</sup>

N	Characteristics <sup>3</sup>	Comple of	Funnasian	80 1	ИHz	100	MHz	Unit
No.	Characteristics	Symbol	Expression	Min	Max	Min	Max	Unit
157	Random read or write cycle time	t <sub>RC</sub>	$16 \times T_C$	200.0	_	160.0	_	ns
158	RAS assertion to data valid (read)	t <sub>RAC</sub>	80 MHz: $8.25\times T_C-6.5$ 100 MHz:	_	96.6	_	_	ns
			$8.25 \times T_{C} - 5.7$	_	_	_	76.8	ns
159	CAS assertion to data valid (read)	<sup>t</sup> CAC	<b>80 MHz</b> : $4.75 \times T_C - 6.5$ <b>100 MHz</b> :	_	52.9	_	_	ns
			$4.75\times T_{C}-5.7$	_	_	_	41.8	ns
160	Column address valid to data valid (read)	t <sub>AA</sub>	<b>80 MHz</b> : 5.5 × T <sub>C</sub> – 6.5 <b>100 MHz</b> :		62.3	_	_	ns
			$5.5 \times T_C - 5.7$	_	_	_	49.3	ns
161	CAS deassertion to data not valid (read hold time)	t <sub>OFF</sub>	0.0	0.0	_	0.0	_	ns
162	RAS deassertion to RAS assertion	t <sub>RP</sub>	$6.25 \times T_{C} - 4.0$	74.1	_	58.5	_	ns
163	RAS assertion pulse width	t <sub>RAS</sub>	$9.75\times T_C-4.0$	117.9	_	93.5	_	ns
164	$\overline{\text{CAS}}$ assertion to $\overline{\text{RAS}}$ deassertion	t <sub>RSH</sub>	$6.25\times T_C-4.0$	74.1	1	58.5	_	ns
165	RAS assertion to CAS deassertion	t <sub>CSH</sub>	$8.25\times T_C-4.0$	99.1		78.5	_	ns
166	CAS assertion pulse width	t <sub>CAS</sub>	$4.75\times T_C-4.0$	55.4	_	43.5	_	ns
167	RAS assertion to CAS assertion	t <sub>RCD</sub>	$3.5 \times T_C \pm 2$	41.8	45.8	33.0	37.0	ns
168	RAS assertion to column address valid	t <sub>RAD</sub>	$2.75\times T_{\hbox{\scriptsize C}}\pm 2.0$	32.4	36.4	25.5	29.5	ns
169	CAS deassertion to RAS assertion	t <sub>CRP</sub>	$7.75\times T_C-4.0$	92.9	-	73.5	_	ns

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**Table 2-14.** DRAM Out-of-Page and Refresh Timings, Fifteen Wait States<sup>1, 2</sup> (Continued)

	Observation of the state of the	0	F	80 1	ИНz	100	MHz	1111
No.	Characteristics <sup>3</sup>	Symbol	Expression	Min	Max	Min	Max	Unit
170	CAS deassertion pulse width	t <sub>CP</sub>	$6.25 \times T_C - 6.0$	74.1	_	56.5	_	ns
171	Row address valid to RAS assertion	t <sub>ASR</sub>	$6.25 \times T_{C} - 4.0$	74.1	_	58.5	_	ns
172	RAS assertion to row address not valid	t <sub>RAH</sub>	$2.75 \times T_{C} - 4.0$	30.4	_	23.5	_	ns
173	Column address valid to CAS assertion	t <sub>ASC</sub>	$0.75 \times T_{C} - 4.0$	5.4	_	3.5	_	ns
174	CAS assertion to column address not valid	t <sub>CAH</sub>	$6.25 \times T_{C} - 4.0$	74.1	_	58.5	_	ns
175	RAS assertion to column address not valid	t <sub>AR</sub>	$9.75 \times T_{C} - 4.0$	117.9	_	93.5	_	ns
176	Column address valid to RAS deassertion	t <sub>RAL</sub>	$7 \times T_C - 4.0$	83.5	_	66.0	_	ns
177	WR deassertion to CAS assertion	t <sub>RCS</sub>	5 × T <sub>C</sub> – 3.8	58.7	_	46.2	_	ns
178	CAS deassertion to WR <sup>4</sup> assertion	t <sub>RCH</sub>	$1.75 \times T_{C} - 3.7$	18.2	_	13.8	_	ns
179	RAS deassertion to WR <sup>4</sup> assertion	t <sub>RRH</sub>	<b>80 MHz</b> : 0.25 × T <sub>C</sub> – 2.6 <b>100 MHz</b> :	0.5	_	_	_	ns
			$0.25 \times T_{C} - 2.0$	_		0.5		ns
180	CAS assertion to WR deassertion	t <sub>WCH</sub>	$6 \times T_C - 4.2$	70.8	_	55.8	_	ns
181	RAS assertion to WR deassertion	t <sub>WCR</sub>	$9.5\times T_{C}-4.2$	114.6	_	90.8	_	ns
182	WR assertion pulse width	t <sub>WP</sub>	$15.5\times T_C-4.5$	189.3	_	150.5	_	ns
183	WR assertion to RAS deassertion	t <sub>RWL</sub>	$15.75 \times T_{C} - 4.3$	192.6	_	153.2	_	ns
184	WR assertion to CAS deassertion	t <sub>CWL</sub>	$14.25 \times T_{C} - 4.3$	173.8	_	138.2	_	ns
185	Data valid to CAS assertion (write)	t <sub>DS</sub>	$8.75\times T_C-4.0$	105.4	_	83.5	_	ns
186	CAS assertion to data not valid (write)	t <sub>DH</sub>	$6.25\times T_C-4.0$	74.1	_	58.5	_	ns
187	RAS assertion to data not valid (write)	t <sub>DHR</sub>	$9.75\times T_{C}-4.0$	117.9	_	93.5	_	ns
188	WR assertion to CAS assertion	t <sub>WCS</sub>	$9.5\times T_C-4.3$	114.5	_	90.7	_	ns
189	CAS assertion to RAS assertion (refresh)	t <sub>CSR</sub>	$1.5 \times T_C - 4.0$	14.8	_	11.0	_	ns
190	RAS deassertion to CAS assertion (refresh)	t <sub>RPC</sub>	$4.75\times T_C-4.0$	55.4	_	43.5	_	ns
191	RD assertion to RAS deassertion	t <sub>ROH</sub>	$15.5 \times T_{C} - 4.0$	189.8	_	151.0	_	ns
192	RD assertion to data valid	t <sub>GA</sub>	<b>80 MHz</b> : 14 × T <sub>C</sub> - 6.5 <b>100 MHz</b> :	_	168.5	_	_	ns
			$14 \times T_{C} - 5.7$	_	_	_	134.3	ns
193	RD deassertion to data not valid <sup>3</sup>	t <sub>GZ</sub>		0.0	_	0.0	_	ns
194	WR assertion to data active		$0.75 \times T_{C} - 1.5$	9.1	_	6.0	_	ns
195	WR deassertion to data high impedance		0.25 × T <sub>C</sub>	_	3.1	_	2.5	ns

- 1. The number of wait states for an out-of-page access is specified in the DCR.
- 2. The refresh period is specified in the DCR.
- 3. RD deassertion always occurs after CAS deassertion; therefore, the restricted timing is t<sub>OFF</sub> and not t<sub>GZ</sub>.
- **4.** Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for read cycles.



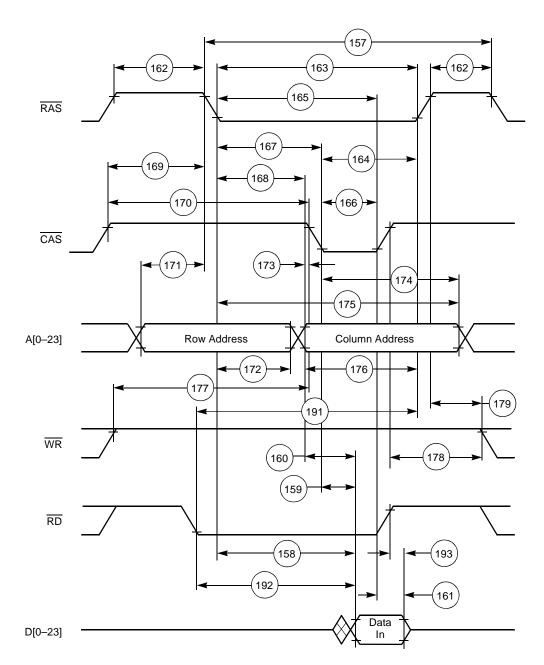


Figure 2-18. DRAM Out-of-Page Read Access

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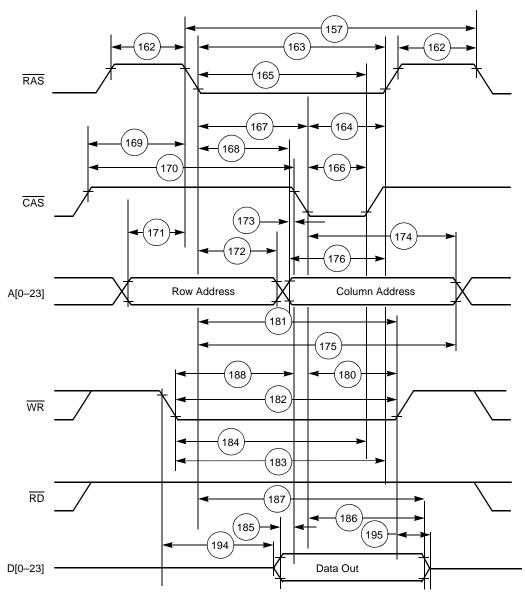


Figure 2-19. DRAM Out-of-Page Write Access

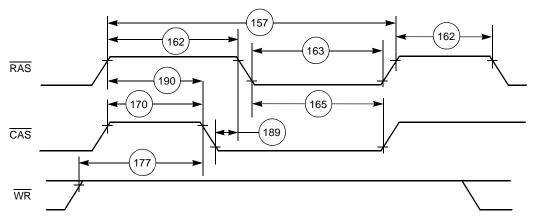


Figure 2-20. DRAM Refresh Access

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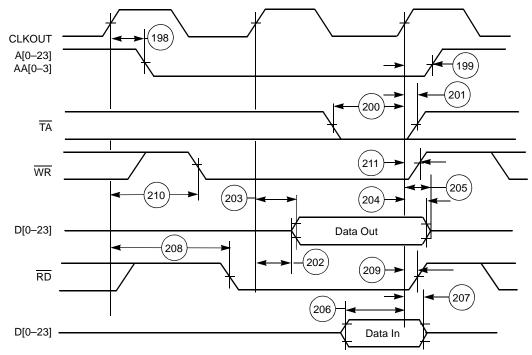
## 2.5.5.3 Synchronous Timings (SRAM)

**Table 2-15.** External Bus Synchronous Timings (SRAM Access)<sup>3</sup>

	21	F 12	80 1	MHz	100	MHz	
No.	Characteristics	Expression <sup>1,2</sup>	Min	Max	Min	Max	Unit
196	CLKOUT high to BS assertion	$0.25 \times T_{C} + 5.2 / -0.5$	2.6	8.3	2.0	7.7	ns
197	CLKOUT high to BS deassertion	$0.75 \times T_{C} + 4.2 / -1.0$	8.4	13.6	6.5	11.7	ns
198	CLKOUT high to address, and AA valid <sup>4</sup>	$0.25 \times T_{C} + 2.5$	_	5.6	_	5.0	ns
199	CLKOUT high to address, and AA invalid <sup>4</sup>	$0.25 \times T_{C} - 0.7$	2.4	_	1.8	_	ns
200	TA valid to CLKOUT high (setup time)		5.8	_	4.0	_	ns
201	CLKOUT high to TA invalid (hold time)		0.0	_	0.0	_	ns
202	CLKOUT high to data out active	0.25 × T <sub>C</sub>	3.1	_	2.5	_	ns
203	CLKOUT high to data out valid	$\begin{array}{c} \textbf{80 MHz}:\\ 0.25\times T_{\text{C}} + 4.5\\ \textbf{100 MHz}:\\ 0.25\times T_{\text{C}} + 4.0 \end{array}$	-	7.6	_	— 6.5	ns ns
204	CLKOUT high to data out invalid	0.25 × T <sub>C</sub>	3.1	_	2.5	_	ns
205	CLKOUT high to data out high impedance	$\begin{array}{c} \textbf{80 MHz}:\\ 0.25\times T_{\text{C}} + 0.5\\ \textbf{100 MHz}:\\ 0.25\times T_{\text{C}} \end{array}$	  -  -	3.6	_ _	_ 2.5	ns ns
206	Data in valid to CLKOUT high (setup)		5.0	_	4.0	_	ns
207	CLKOUT high to data in invalid (hold)		0.0	_	0.0	_	ns
208	CLKOUT high to RD assertion	maximum: 0.75 × T <sub>C</sub> + 2.5	10.4	11.9	6.7	10.0	ns ns
209	CLKOUT high to RD deassertion		0.0	4.5	0.0	4.0	ns
210	CLKOUT high to WR assertion <sup>2</sup>	$0.5 \times T_C + 4.3$ [WS = 1 or WS $\geq$ 4] [2 $\leq$ WS $\leq$ 3]	7.6 1.3	10.6 4.8	4.5 0.0	9.3 4.3	ns ns
211	CLKOUT high to WR deassertion	[2 3 880 3 0]	0.0	4.3	0.0	3.8	ns

- 1. WS is the number of wait states specified in the BCR.
- 2. If WS > 1,  $\overline{\text{WR}}$  assertion refers to the next rising edge of CLKOUT.
- 3. External bus synchronous timings should be used only for reference to the clock and *not* for relative timings.
- 4. T198 and T199 are valid for Address Trace mode if the ATE bit in the Operating Mode Register is set. Use the status of BR (See T212) to determine whether the access referenced by A[0–23] is internal or external in this mode.





**Note**: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

CLKOUT A[0-23] **\_**199 AA[0-3] 201 201 200 TA 211 WR 205 203 D[0-23] Data Out 202 208 (209 RD (207 (206 Data In D[0-23]

Figure 2-21. Synchronous Bus Timings 1 WS (BCR Controlled)

**Note**: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-22. Synchronous Bus Timings 2 WS (TA Controlled)

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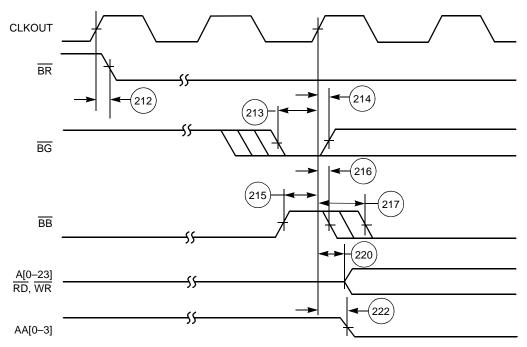
## 2.5.5.4 Arbitration Timings

**Table 2-16.** Arbitration Bus Timings<sup>1</sup>.

No.	Characteristics	Expression <sup>2</sup>	80 1	MHz	100	MHz	Unit
140.	Characteristics	Lxpression	Min	Max	Min	Max	Onit
212	CLKOUT high to BR assertion/deassertion <sup>3</sup>		1.0	4.5	0.0	4.0	ns
213	BG asserted/deasserted to CLKOUT high (setup)		5.0	_	4.0	_	ns
214	CLKOUT high to BG deasserted/asserted (hold)		0.0	_	0.0	_	ns
215	BB deassertion to CLKOUT high (input setup)		5.0	_	4.0	_	ns
216	CLKOUT high to BB assertion (input hold)		0.0	_	0.0	_	ns
217	CLKOUT high to BB assertion (output)		1.0	4.5	0.0	4.0	ns
218	CLKOUT high to BB deassertion (output)		1.0	4.5	0.0	4.0	ns
219	BB high to BB high impedance (output)		_	5.6	_	4.5	ns
220	CLKOUT high to address and controls active	0.25 × T <sub>C</sub>	3.1	_	2.5	_	ns
221	CLKOUT high to address and controls high impedance	0.75 × T <sub>C</sub>	_	9.4	_	7.5	ns
222	CLKOUT high to AA active	0.25 × T <sub>C</sub>	3.1	_	2.5	_	ns
223	CLKOUT high to AA deassertion	maximum: $0.25 \times T_C + 4.0$	4.1	7.1	2.0	6.5	ns
224	CLKOUT high to AA high impedance	0.75 × T <sub>C</sub>	_	9.4	_	7.5	ns

- 1. Synchronous Bus Arbitration is not recommended. Use Asynchronous mode whenever possible.
- 2. An expression is used to compute the maximum or minimum value listed, as appropriate. For timing 223, the minimum is an absolute value.
- 3. T212 is valid for Address Trace mode when the ATE bit in the Operating Mode Register is set. BR is deasserted for internal accesses and asserted for external accesses.





**Note**: Address lines A[0–23] hold their state after a read or write operation. AA[0–3] do not hold their state after a read or write operation.

Figure 2-23. Bus Acquisition Timings

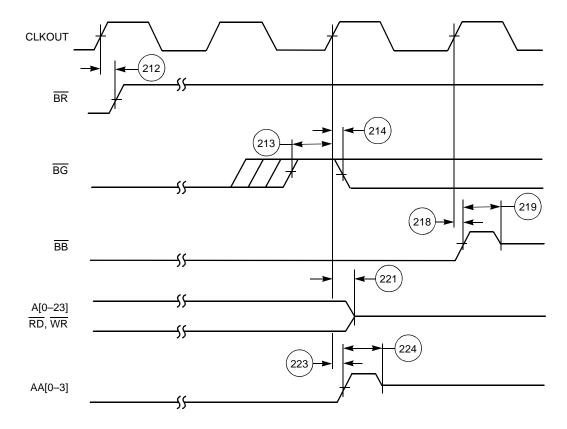
Note: Address lines A[0-23] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

Figure 2-24. Bus Release Timings Case 1 (BRT Bit in Operating Mode Register Cleared)

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Note: Address lines A[0-23] hold their state after a read or write operation. AA[0-3] do not hold their state after a read or write operation.

Figure 2-25. Bus Release Timings Case 2 (BRT Bit in Operating Mode Register Set)

### 2.5.5.5 Asynchronous Bus Arbitrations Timings

**Table 2-17.** Asynchronous Bus Arbitration Timing<sup>1,3</sup>

No.	Characteristics	Expression	80 MHz		100 I	Unit	
	Onaracteristics	Expression	Min	Max	Min	Max	
250	BB assertion window from BG input deassertion <sup>4</sup>	2.5 × Tc + 5	_	25	_	30	ns
251	Delay from BB assertion to BG assertion <sup>4</sup>	2 × Tc + 5	25		25	1	ns

- Bit 13 in the Operating Mode Register must be set to enter Asynchronous Arbitration mode.
- Asynchronous Arbitration mode is recommended for operation at 100 MHz.
- If Asynchronous Arbitration mode is active, none of the timings in Table 2-16 is required.
- In order to guarantee timings 250, and 251, BG inputs must be asserted to different DSP56300 devices on the same bus in the non-overlap manner shown in Figure 2-26.



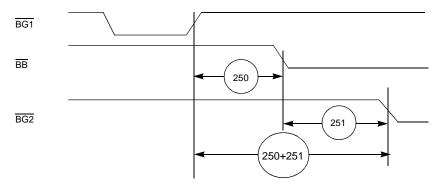


Figure 2-26. Asynchronous Bus Arbitration Timing

The asynchronous bus arbitration is enabled by internal BB inputs and synchronization circuits on BG. These synchronization circuits add delay from the external signal until it is exposed to internal logic. As a result of this delay, a DSP56300 part can assume mastership and assert BB, for some time after BG is deasserted. Timing 250 defines when  $\overline{BB}$  can be asserted.

Once BB is asserted, there is a synchronization delay from BB assertion to the time this assertion is exposed to other DSP56300 components which are potential masters on the same bus. If BG input is asserted before that time, a situation of BG asserted, and BB deasserted, can cause another DSP56300 component to assume mastership at the same time. Therefore, a non-overlap period between one  $\overline{BG}$  input active to another  $\overline{BG}$  input active is required. Timing 251 ensures that such a situation is avoided.

Universal Bus Mode Timing Parameters

#### **Host Interface Timing** 2.5.6

Table 2-18.

		8
Characteristic	Everencies	

	Observatoristis	<b>F</b>	80 1	ИНz	100	MHz	11!
No.	Characteristic	Expression	Min	Max	Min	Max	Unit
300	Access Cycle Time	3×T <sub>C</sub>	37.5	_	30.0	_	ns
301	HA[10–0], HAEN Setup to Data Strobe Assertion <sup>1</sup>		5.8	_	4.6	_	ns
302	HA[10–0], HAEN Valid Hold from Data Strobe Deassertion <sup>1</sup>		0.0	_	0.0	_	ns
303	HRW Setup to HDS Assertion <sup>2</sup>		5.8	_	4.6	_	ns
304	HRW Valid Hold from HDS Deassertion <sup>2</sup>		0.0	_	0.0	_	ns
305	Data Strobe Deasserted Width <sup>1</sup>		4.1	_	3.3	_	ns
306	Data Strobe Asserted Pulse Width <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 1.7 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 1.3	32.9	_	26.3	_	ns ns
307	HBS Asserted Pulse Width		2.5	_	2.0	_	ns
308	HBS Assertion to Data Strobe Assertion <sup>1</sup>	<b>80 MHz</b> : T <sub>C</sub> – 4.9 <b>100 MHz</b> : T <sub>C</sub> – 4.0	_	7.6	_	6.0	ns ns
309	HBS Assertion to Data Strobe Deassertion <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 2.9 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 2.3	34.1	_	27.3	_	ns ns
310	HBS Deassertion to Data Strobe Deassertion <sup>1</sup>	<b>80 MHz:</b> 1.5 × T <sub>C</sub> + 3.3 <b>100 MHz:</b> 1.5 × T <sub>C</sub> + 2.6	22.1	_	17.6	_	ns ns
311	Data Out Valid to TA Assertion (HBS Not Used—Tied to V <sub>CC</sub> ) <sup>2</sup>	<b>80 MHz:</b> 2 × T <sub>C</sub> - 11.6 <b>100 MHz:</b> 2 × T <sub>C</sub> - 9.2	13.4	_	10.8	_	ns ns
312	Data Out Active from Read Data Strobe Assertion <sup>3</sup>		1.7	_	1.3	_	ns

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 Table 2-18.
 Universal Bus Mode Timing Parameters (Continued)

No.	Characteristic	Expression	80 I	ИНz	100	MHz	Unit
NO.	Characteristic	Expression	Min	Max	Min	Max	Unit
313	Data Out Valid from Read <u>Data</u> Strobe Assertion (No Wait States Inserted—HTA Asserted) <sup>3</sup>		_	18.9	_	16.9	ns
314	Data Out Valid Hold from Read Data Strobe Deassertion <sub>3</sub>		1.7	_	1.3	_	ns
315	Data Out High Impedance from Read Data Strobe Deassertion <sup>3</sup>		_	12.0	_	9.6	ns
316	Data In Valid Setup to Write Data Strobe Deassertion <sup>4</sup>		8.3	_	6.6	_	ns
317	Data In Valid Hold from Write Data Strobe Deassertion <sup>4</sup>		0.0	_	0.0	_	ns
318	HSAK Assertion from Data Strobe Assertion <sup>1</sup>		_	30.0	_	30.0	ns
319	HSAK Asserted Hold from Data Strobe Deassertion <sup>1</sup>		2.0	_	2.0	_	ns
320	HTA Active from Data Strobe Assertion <sup>1,2,5</sup>		3.1	_	2.5	_	ns
321	$\overline{\text{HTA}}$ Assertion from Data Strobe Assertion (HBS Not Used—Tied to $\text{V}_{\text{CC}}$ ) <sup>1,2,5</sup>	<b>80 MHz:</b> 2.0 × T <sub>C</sub> + 13.0 <b>100 MHz:</b> 2.0 × T <sub>C</sub> + 12.2	38.0	_	32.2	_	ns ns
322	HTA Assertion from HBS Assertion <sup>2,5</sup>	<b>80 MHz:</b> 2.0 × T <sub>C</sub> + 13.0 <b>100 MHz:</b> 2.0 × T <sub>C</sub> + 12.2	38.0	_	32.2	_	ns ns
323	HTA Deasserted from Data Strobe Assertion <sup>1,2,5</sup>		_	17.1	_	15.0	ns
324	HTA Assertion to Data Strobe Deassertion <sup>1,2</sup>		0.0	_	0.0	_	ns
325	HTA High Impedance from Data Strobe Deassertion <sup>1,2</sup>		_	15.3	_	12.2	ns
326	HIRQ Asserted Pulse Width (HIRH = 0, HIRD = 1)	$(LT + 1) \times T_C - 6.0^7$	19.0	_	14.0	_	ns
327	Data Strobe Deasserted Hold from HIRQ Deassertion (HIRH = 0) <sup>1</sup>		0.0	_	0.0	_	ns
328	HIRQ Asserted Hold from Data Strobe Assertion (HIRH = 1) <sup>1</sup>	1.5 × T <sub>C</sub>	18.8	_	15.0	_	ns
329	HIRQ Deassertion from Data Strobe Assertion (HIRH = 1, HIRD = 1) <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 24.7 100 MHz: 2.5 × T <sub>C</sub> + 21.5	_	55.9	_	46.5	ns ns
330	HIRQ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0) <sup>1,6</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 24.7 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 21.5	_	55.9	_	46.5	ns ns
331	HIRQ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0) <sup>1</sup>	2.5 × T <sub>C</sub>	31.3	_	25.0	_	ns
332	HIRQ Deasserted Hold from Data Strobe Deassertion <sup>1</sup>	2.5 × T <sub>C</sub>	31.3	_	25.0	_	ns
333	HDRQ <sup>2</sup> Asserted Hold from Data Strobe Assertion <sup>1</sup>	1.5 × T <sub>C</sub>	18.8	_	15.0	_	ns
334	HDRQ <sup>2</sup> Deassertion from Data Strobe Assertion <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 24.7 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 21.5	_	55.9	_	46.5	ns ns
335	HDRQ <sup>2</sup> Deasserted Hold from Data Strobe Deassertion <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 3.7 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 3.0	35.0	_	28.0	_	ns ns
336	HDAK Assertion to Data Strobe Assertion <sup>1</sup>		5.8	_	4.6	_	ns
337	HDAK Asserted Hold from Data Strobe Deassertion <sup>1</sup>		0.0	_	0.0	_	ns
338	HDBEN Deasserted Hold from Data Strobe Assertion <sup>1</sup>		2.5	_	2.0	_	ns
339	HDBEN Assertion from Data Strobe Assertion <sup>1</sup>		_	22.2	_	19.6	ns
340	HDBEN Asserted Hold from Data Strobe Deassertion <sup>1</sup>		2.5		2.0	_	ns
341	HDBEN Deassertion from Data Strobe Deassertion <sup>1</sup>		_	22.2	_	19.6	ns
342	HDBDR High Hold from Read Data Strobe Assertion <sup>3</sup>		2.5		2.0		ns
343	HDBDR Low from Read Data Strobe Assertion <sup>3</sup>			22.2	_	19.6	ns
344	HDBDR Low Hold from Read Data Strobe Deassertion <sup>3</sup>		2.5	_	2.0	_	ns

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**Table 2-18.** Universal Bus Mode Timing Parameters (Continued)

No. Characteristic	Characteristic	Everacion	80 MHz		100 MHz		Unit
	Expression	Min	Max	Min	Max	Ullit	
345	HDBDR High from Read Data Strobe Deassertion <sup>3</sup>		_	22.2		19.6	ns
346	HRST Assertion to Host Port Pins High Impedance <sup>2</sup>		_	22.2	_	19.6	ns

- 1. The Data Strobe is  $\overline{\text{HRD}}$  or  $\overline{\text{HWR}}$  in the Dual Data Strobe mode and  $\overline{\text{HDS}}$  in the Single Data Strobe mode.
- 2. HTA, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and HTA is shown as active low.
- 3. The Read Data Strobe is HRD in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
- 4. The Write Data Strobe is  $\overline{HWR}$  in the Dual Data Strobe mode and  $\overline{HDS}$  in the Single Data Strobe mode.
- 5. HTA requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
- **6.** HIRQ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
- 7. "LT" is the value of the latency timer register (CLAT) as programmed by the user during self configuration.  $LT \ge 1$ .
- **8.** Values are valid for  $V_{CC} = 3.3 \pm 0.3 V$

**Table 2-19.** Universal Bus Mode, Synchronous Port A Type Host Timing

NI -	Oh avantaviatie	<b>5</b>	80 I	MHz	100 MHz		11!1
No.	Characteristic	Expression	Min	Max	Min	Max	Unit
300	Access Cycle Time	$3 \times T_{C}$	37.5	_	30.0	_	ns
301	HA[10–0], HAEN Setup to Data Strobe Assertion <sup>1</sup>		5.8	_	4.6	_	ns
302	HA[10–0], HAEN Valid Hold from Data Strobe Deassertion <sup>1</sup>		0.0	_	0.0	_	ns
305	Data Strobe Deasserted Width <sup>1</sup>		4.1	_	3.3	_	ns
307	HBS Asserted Pulse Width		2.5	_	2.0	_	ns
308	HBS Assertion to Data Strobe Assertion <sup>1</sup>	<b>80 MHz:</b> T <sub>C</sub> – 4.9 <b>100 MHz:</b> T <sub>C</sub> – 4.0	_	7.6	_	6.0	ns ns
309	HBS Assertion to Data Strobe Deassertion <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 2.9 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 2.3	34.1	_	27.3	_	ns ns
310	HBS Deassertion to Data Strobe Deassertion <sup>1</sup>	<b>80 MHz:</b> 1.5 × T <sub>C</sub> + 3.3 <b>100 MHz:</b> 1.5 × T <sub>C</sub> + 2.6	22.1	_	17.6	_	ns ns
312	Data Out Active from Read Data Strobe Assertion <sup>3</sup>		1.7	_	1.3	_	ns
313	Data Out Valid from Read <u>Data</u> Strobe Assertion (No Wait States Inserted—HTA Asserted) <sup>3</sup>		_	18.9	_	16.9	ns
314	Data Out Valid Hold from Read Data Strobe Deassertion <sub>3</sub>		1.7	_	1.3	_	ns
315	Data Out High Impedance from Read Data Strobe Deassertion <sup>3</sup>		_	12.0	_	9.6	ns
316	Data In Valid Setup to Write Data Strobe Deassertion <sup>4</sup>		8.3	_	6.6	_	ns
317	Data In Valid Hold from Write Data Strobe Deassertion <sup>4</sup>		0.0	_	0.0	_	ns
324	HTA Assertion to Data Strobe Deassertion <sup>1,2</sup>		0.0	_	0.0	_	ns
325	HTA High Impedance from Data Strobe Deassertion <sup>1,2</sup>		_	15.3	_	12.2	ns
326	HIRQ Asserted Pulse Width (HIRH = 0, HIRD = 1)	$(LT + 1) \times T_C - 6.0^7$	6.5	_	4.0	_	ns
327	Data Strobe Deasserted Hold from HIRQ Deassertion (HIRH = 0) <sup>1</sup>		0.0	_	0.0	_	ns
328	HIRQ Asserted Hold from Data Strobe Assertion (HIRH = 1) <sup>1</sup>	1.5 × T <sub>C</sub>	18.8	_	15.0	_	ns
329	HIRQ Deassertion from Data Strobe Assertion (HIRH = 1, HIRD = 1) <sup>1</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 24.7 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 21.5	—	55.9	_	46.5	ns ns

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Table 2-19. Universal Bus Mode, Synchronous Port A Type Host Timing (Continued)

No.	Characteristic	Evpression	80 MHz		100	MHz	- Unit
NO.	Characteristic	Expression	Min	Max	Min	Max	Onit
330	HIRQ High Impedance from Data Strobe Assertion (HIRH = 1, HIRD = 0) <sup>1,6</sup>	<b>80 MHz:</b> 2.5 × T <sub>C</sub> + 24.7 <b>100 MHz:</b> 2.5 × T <sub>C</sub> + 21.5		55.9	_	46.5	ns ns
331	$\overline{\text{HIRQ}}$ Active from Data Strobe Deassertion (HIRH = 1, HIRD = 0) <sup>1</sup>	$2.5 \times T_{C}$	31.3	_	25.0		ns
332	HIRQ Deasserted Hold from Data Strobe Deassertion <sup>1</sup>	2.5 × T <sub>C</sub>	31.3	_	25.0	_	ns
346	HRST Assertion to Host Port Pins High Impedance <sup>2</sup>		_	22.2	_	19.6	ns
347	HBS Assertion to CLKOUT Rising Edge		4.3	_	3.4	_	ns
348	Data Strobe Deassertion to CLKOUT Rising Edge <sup>1</sup>		7.4	_	5.9		ns

- 1. The Data Strobe is  $\overline{\mathsf{HRD}}$  or  $\overline{\mathsf{HWR}}$  in the Dual Data Strobe mode and  $\overline{\mathsf{HDS}}$  in the Single Data Strobe mode.
- 2. HTA, HDRQ, and HRST may be programmed as active-high or active-low. In the example timing diagrams, HDRQ and HRST are shown as active-high and HTA is shown as active low.
- 3. The Read Data Strobe is  $\overline{HRD}$  in the Dual Data Strobe mode and  $\overline{HDS}$  in the Single Data Strobe mode.
- 4. The Write Data Strobe is HWR in the Dual Data Strobe mode and HDS in the Single Data Strobe mode.
- 5. HTA requires an external pull-down resistor if programmed as active high (HTAP = 0); or an external pull-up resistor if programmed as active low (HTAP = 1). The resistor value should be consistent with the DC specifications.
- **6.** HIRQ requires an external pull-up resistor if programmed as open drain (HIRD = 0). The resistor value should be consistent with the DC specifications.
- 7. "LT" is the value of the latency timer register (CLAT) as programmed by the user during self configuration.
- **8.** Values are valid for  $V_{CC} = 3.3 \pm 0.3 V$

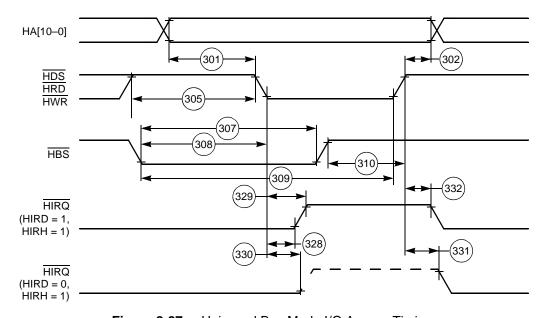


Figure 2-27. Universal Bus Mode I/O Access Timing



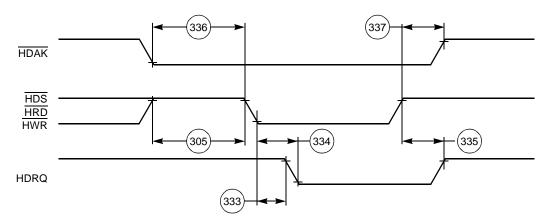


Figure 2-28. Universal Bus Mode DMA Access Timing

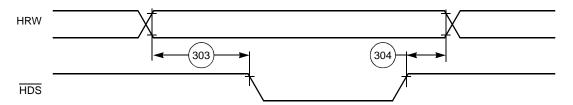
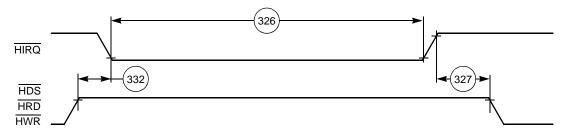


Figure 2-29. HRW to HDS Timing



**Figure 2-30.**  $\overline{HIRQ}$  Pulse Width (HIRH = 0)

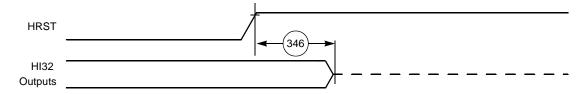


Figure 2-31. HRST Timing

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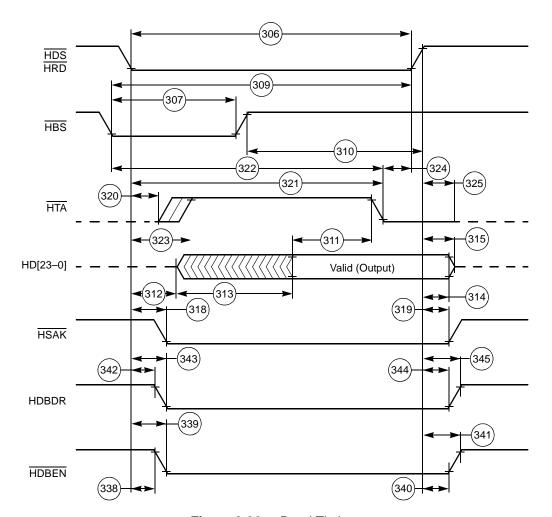


Figure 2-32. Read Timing

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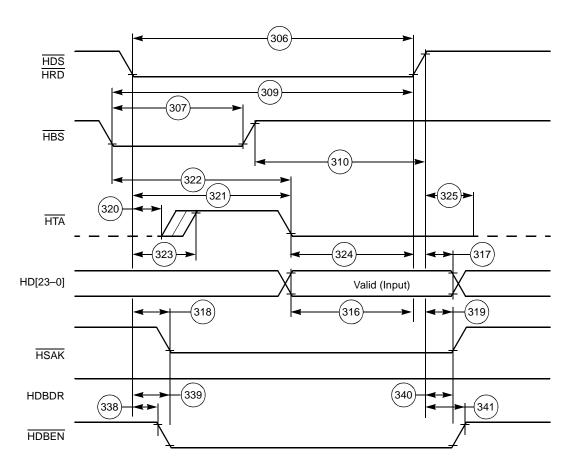


Figure 2-33. Write Timing

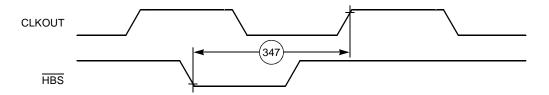


Figure 2-34. HBS Synchronous Timing

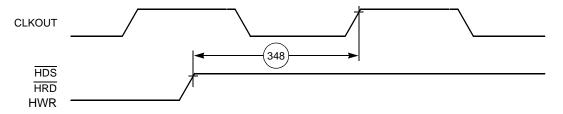


Figure 2-35. Data Strobe Synchronous Timing



**Table 2-20.** PCI Mode Timing Parameters<sup>1</sup>

No	Characteristic <sup>10</sup>	Counch of	80 MHz		100	MHz	Unit
No.	Characteristic	Symbol	Min	Max	Min	Max	Unit
349	HCLK to Signal Valid Delay—Bussed Signals	t <sub>VAL</sub>	2.0	11.0	2.0	11.0	ns
350	HCLK to Signal Valid Delay—Point to Point	t <sub>VAL(ptp)</sub>	2.0	12.0	2.0	12.0	ns
351	Float to Active Delay	t <sub>ON</sub>	2.0	1	2.0		ns
352	Active to Float Delay	t <sub>OFF</sub>		28.0		28.0	ns
353	Input Set Up Time to HCLK—Bussed Signals	t <sub>SU</sub>	7.0	_	7.0	_	ns
354	Input Set Up Time to HCLK—Point to Point	t <sub>SU(ptp)</sub>	10.0, 12.0	1	10.0, 12.0		ns
355	Input Hold Time from HCLK	t <sub>H</sub>	0.0	ı	0.0	ı	ns
356	Reset Active Time After Power Stable	t <sub>RST</sub>	1.0	_	1.0	_	ms
357	Reset Active Time After HCLK Stable	t <sub>RST-CLK</sub>	100.0	1	100.0		μs
358	Reset Active to Output Float Delay	t <sub>RST-OFF</sub>	_	40.0	_	40.0	ns
359	HCLK Cycle Time	t <sub>CYC</sub>	30.0	_	30.0	_	ns
360	HCLK High Time	t <sub>HIGH</sub>	11.0	1	11.0	_	ns
361	HCLK Low Time	t <sub>LOW</sub>	11.0	_	11.0	_	ns

Notes: 1. For standard PCI timing, see the PCI Local Bus Specification, Rev. 2.0, especially Chapters 3 and 4.

2. The HI32 supports these timings for a PCI bus operating at 33 MHz for a DSP clock frequency of 56 MHz and above. The DSP core operating frequency should be greater than 5/3 of the PCI bus frequency to maintain proper PCI operation.

3. HGNT has a setup time of 10 ns. HREQ has a setup time of 12 ns.

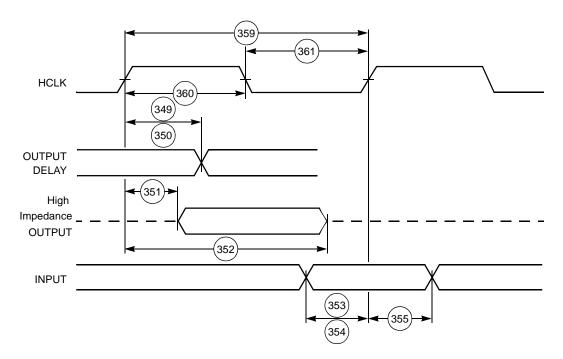


Figure 2-36. PCI Timing

2-40 Freescale Semiconductor



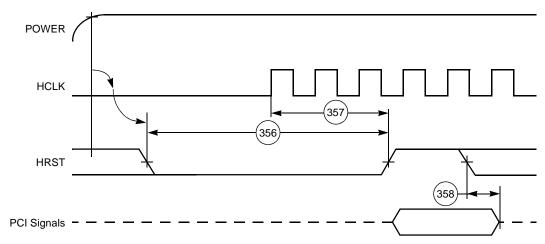


Figure 2-37. PCI Reset Timing

# 2.5.7 SCI Timing

Table 2-21. SCI Timing

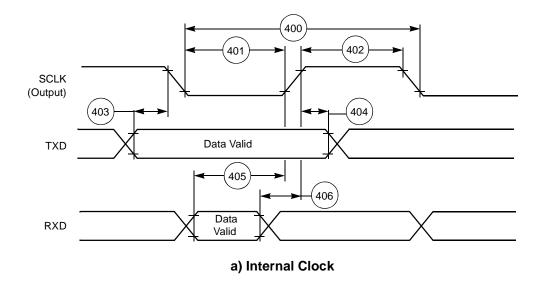
				80 I	MHz	100	MHz	
No.	Characteristics <sup>1</sup>	Symbol	Expression	Min	Max	Min	Max	Unit
400	Synchronous clock cycle	t <sub>SCC</sub> <sup>2</sup>	8×T <sub>C</sub>	100.0	_	80.0	_	ns
401	Clock low period		t <sub>SCC</sub> /2 – 10.0	40.0	_	30.0	_	ns
402	Clock high period		t <sub>SCC</sub> /2 - 10.0	40.0	_	30.0	_	ns
403	Output data setup to clock falling edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C - 17.0$	14.3	_	8.0	_	ns
404	Output data hold after clock rising edge (internal clock)		$t_{SCC}/4 - 0.5 \times T_{C}$	18.8	_	15.0	_	ns
405	Input data setup time before clock rising edge (internal clock)		$t_{SCC}/4 + 0.5 \times T_C + 25.0$	56.3	_	50.0	_	ns
406	Input data not valid before clock rising edge (internal clock)		t <sub>SCC</sub> /4 + 0.5 × T <sub>C</sub> - 5.5	_	25.8	_	19.5	ns
407	Clock falling edge to output data valid (external clock)			_	32.0	_	32.0	ns
408	Output data hold after clock rising edge (external clock)		T <sub>C</sub> + 8.0	20.5	_	18.0	_	ns
409	Input data setup time before clock rising edge (external clock)			0.0	_	0.0	_	ns
410	Input data hold time after clock rising edge (external clock)			9.0	_	9.0	_	ns
411	Asynchronous clock cycle	t <sub>ACC</sub> <sup>3</sup>	64 × T <sub>C</sub>	800.0	_	640.0	_	ns
412	Clock low period		t <sub>ACC</sub> /2 - 10.0	390.0	_	310.0	_	ns
413	Clock high period		t <sub>ACC</sub> /2 – 10.0	390.0	_	310.0	_	ns
414	Output data setup to clock rising edge (internal clock)		t <sub>ACC</sub> /2 - 30.0	370.0	_	290.0	_	ns
415	Output data hold after clock rising edge (internal clock)		t <sub>ACC</sub> /2 - 30.0	370.0	_	290.0	_	ns



**Table 2-21.** SCI Timing (Continued)

No.	Characteristics1	Symbol	Evarencies	80 1	ИНz	100	MHz	l lmi4
NO.	Characteristics <sup>1</sup>	Symbol	Expression	Min	Max	Min	Max	Unit

- $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}; T_J = -40 ^{\circ}\text{C}$  to +100  $^{\circ}\text{C}$ ,  $C_L = 50 \text{ pF}$   $t_{SCC} = \text{synchronous clock cycle time}$  (For internal clock,  $t_{SCC}$  is determined by the SCI clock control register and  $T_{C.}$ )  $t_{ACC} = \text{asynchronous clock cycle time};$  value given for 1X Clock mode (For internal clock,  $t_{ACC}$  is determined by the SCI clock control register and T<sub>C</sub>)



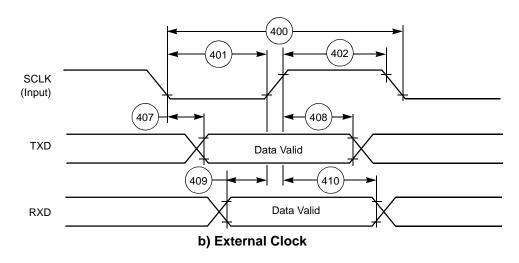


Figure 2-38. SCI Synchronous Mode Timing



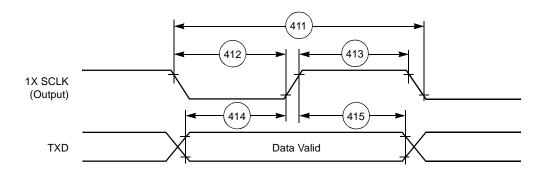


Figure 2-39. SCI Asynchronous Mode Timing

## 2.5.8 ESSI0/ESSI1 Timing

Table 2-22. ESSI Timings

	0 457			80 1	ИНz	100	MHz	Cond-	
No.	Characteristics <sup>4, 5, 7</sup>	Symbol	Expression	Min	Max	Min	Max	ition <sup>6</sup>	Unit
430	Clock cycle <sup>1</sup>	t <sub>SSICC</sub>	$\begin{array}{c} 3\times T_C \\ 4\times T_C \end{array}$	50.0 37.5	_ _	30.0 40.0	_ _	x ck i ck	ns
431	Clock high period For internal clock For external clock		$2 \times T_{C} - 10.0$ $1.5 \times T_{C}$	15.0 18.8	_	10.0 15.0	_		ns ns
432	Clock low period For internal clock For external clock		2 × T <sub>C</sub> - 10.0 1.5 × T <sub>C</sub>	15.0 18.8	_	10.0 15.0	_		ns ns
433	RXC rising edge to FSR out (bl) high			_ _	37.0 22.0	_	37.0 22.0	x ck i ck a	ns
434	RXC rising edge to FSR out (bl) low			_	37.0 22.0	_	37.0 22.0	x ck i ck a	ns
435	RXC rising edge to FSR out (wr) high <sup>2</sup>			_	39.0 24.0	_	39.0 24.0	x ck i ck a	ns
436	RXC rising edge to FSR out (wr) low <sup>2</sup>			_	39.0 24.0	_	39.0 24.0	x ck i ck a	ns
437	RXC rising edge to FSR out (wl) high			_ _	36.0 21.0	_	36.0 21.0	x ck i ck a	ns
438	RXC rising edge to FSR out (wl) low			_	37.0 22.0	_	37.0 22.0	x ck i ck a	ns
439	Data in setup time before RXC (SCK in Synchronous mode) falling edge			10.0 19.0	_	10.0 19.0	_	x ck i ck	ns
440	Data in hold time after RXC falling edge			5.0 3.0	_	5.0 3.0	_	x ck i ck	ns
441	FSR input (bl, wr) high before RXC falling edge <sup>2</sup>			1.0 23.0	_	1.0 23.0	_	x ck i ck a	ns
442	FSR input (wl) high before RXC falling edge			3.5 23.0	_	3.5 23.0	_	x ck i ck a	ns
443	FSR input hold time after RXC falling edge			3.0 0.0	_	3.0 0.0		x ck i ck a	ns
444	Flags input setup before RXC falling edge			5.5 19.0		5.5 19.0		x ck i ck s	ns

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 Table 2-22.
 ESSI Timings (Continued)

	Characteristics <sup>4, 5, 7</sup>	Symbol	Expression	80 MHz		100 MHz		Cond-	
No.				Min	Max	Min	Max	ition <sup>6</sup>	Unit
445	Flags input hold time after RXC falling edge			6.0 0.0	_	6.0 0.0	_	x ck i ck s	ns
446	TXC rising edge to FST out (bl) high			_ _	29.0 15.0	_ _	29.0 15.0	x ck i ck	ns
447	TXC rising edge to FST out (bl) low			_	31.0 17.0	_ _	31.0 17.0	x ck i ck	ns
448	TXC rising edge to FST out (wr) high <sup>2</sup>			_	31.0 17.0	_	31.0 17.0	x ck i ck	ns
449	TXC rising edge to FST out (wr) low <sup>2</sup>			_	33.0 19.0	_	33.0 19.0	x ck i ck	ns
450	TXC rising edge to FST out (wl) high			_	30.0 16.0	_	30.0 16.0	x ck i ck	ns
451	TXC rising edge to FST out (wl) low			_	31.0 17.0	_	31.0 17.0	x ck i ck	ns
452	TXC rising edge to data out enable from high impedance			_	31.0 17.0	_	31.0 17.0	x ck i ck	ns
453	TXC rising edge to Transmitter #0 drive enable assertion			_	34.0 20.0	_	34.0 20.0	x ck i ck	ns
454	TXC rising edge to data out valid <sup>8</sup>			_	20.0 10.0	_	20.0 10.0	x ck i ck	ns
455	TXC rising edge to data out high impedance <sup>3</sup>			_	31.0 16.0	_	31.0 16.0	x ck i ck	ns
456	TXC rising edge to Transmitter #0 drive enable deassertion <sup>3</sup>			_	34.0 20.0	_	34.0 20.0	x ck i ck	ns
457	FST input (bl, wr) setup time before TXC falling edge <sup>2</sup>			2.0 21.0	_	2.0 21.0	_	x ck i ck	ns
458	FST input (wl) to data out enable from high impedance			_	27.0	_	27.0	_	ns
459	FST input (wl) to Transmitter #0 drive enable assertion			_	31.0	_	31.0	_	ns
460	FST input (wl) setup time before TXC falling edge			2.5 21.0	_	2.5 21.0	_	x ck i ck	ns
461	FST input hold time after TXC falling edge			4.0 0.0	_	4.0 0.0	_	x ck i ck	ns
462	Flag output valid after TXC rising edge			_	32.0 18.0	_	32.0 18.0	x ck i ck	ns

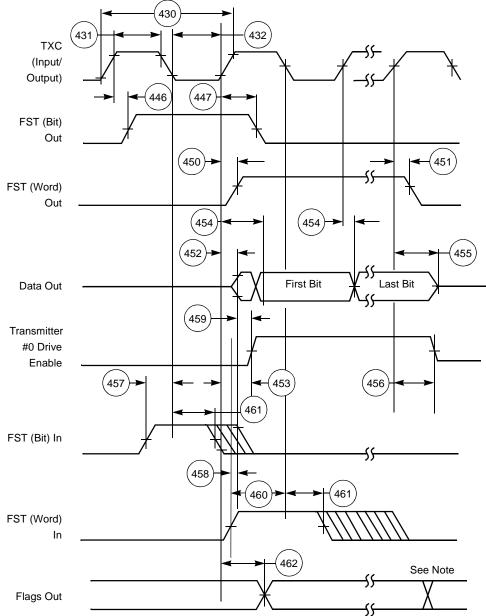


 $T_C$ ).

### Table 2-22. ESSI Timings (Continued)

	Characteristics <sup>4, 5, 7</sup>	01	0		80 MHz		100 MHz		Cond-	
No.		Symbol	Expression	Min	Max	Min	Max	ition <sup>6</sup>	Unit	
Notes:	1.									
	2.	the ESSI control register.  The word-relative frame sync signal waveform relative to the clock operates the same way as the bit-length frame sync signal waveform, but spreads from one serial clock before the first bit clock (same as Bit Length Frame Sync signal), until the one before the last bit clock of the first word in frame.								
	3.									
	4.									
	5.									
		RXC (SC0 or SCK Pin) = Receive Clock FST (SC2 Pin) = Transmit Frame Sync FSR (SC1 or SC2 Pin) Receive Frame Sync								
	6.	i ck = Internal Clock								
		x ck = External Clock								
	i ck a = Internal Clock, Asynchronous Mode									
		(Asynchronous implies that TXC and RXC are two different clocks)								
		i ck s = Internal Clock, Synchronous Mode								
		(Synchronous implies that TXC and RXC are the same clock)								
		(Synchronous implies that TXC and R		same clock)						
	7.	(Synchronous implies that TXC and R bl = bit length		same clock)						
	7.			same clock)						
	7.	bl = bit length		same clock)						





**Note:** In Network mode, output flag transitions can occur at the start of each time slot within the frame. In Normal mode, the output flag state is asserted for the entire frame period.

Figure 2-40. ESSI Transmitter Timing

2-46 Freescale Semiconductor



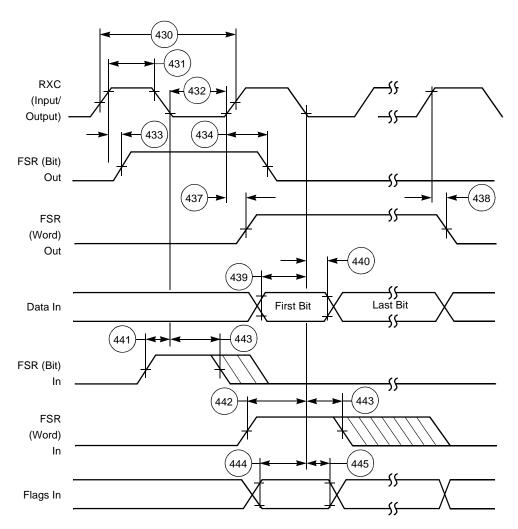


Figure 2-41. ESSI Receiver Timing

## 2.5.9 Timer Timing

Table 2-23. Timer Timing

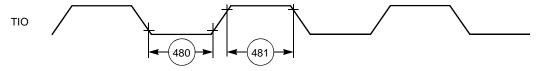
NI -		F	80 1	ИНz	100 MHz		11
No.	Characteristics	Expression	Min	Max	Min	Max	Unit
480	TIO Low	$2 \times T_C + 2.0$	27.0	_	22.0	_	ns
481	TIO High	$2 \times T_C + 2.0$	27.0	_	22.0	_	ns
482	Timer setup time from TIO (Input) assertion to CLKOUT rising edge		9.0	12.5	9.0	10.0	ns
483	Synchronous timer delay time from CLKOUT rising edge to the external memory access address out valid caused by first interrupt instruction execution	10.25 × T <sub>C</sub> + 1.0	129.1	_	103.5	_	ns
484	CLKOUT rising edge to TIO (Output) assertion  Minimum  Maximum	$0.5 \times T_{C} + 0.5$ $0.5 \times T_{C} + 19.8$	9.8 —	 26.1	5.5 —	 24.8	ns ns

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Timer Timing (Continued) Table 2-23.

No.	Characteristics	Everossion	80 MHz		100 MHz		Unit
NO.		Expression	Min	Max	Min	Max	Onit
485	CLKOUT rising edge to TIO (Output) deassertion  Minimum  Maximum	$0.5 \times T_{C} + 0.5$ $0.5 \times T_{C} + 19.8$	9.8	 26.1	5.5 —	 24.8	ns ns
Note:	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}; T_J = -40^{\circ}\text{C to } +100 \text{ °C}, C_L = 50 \text{ pF}$						



TIO Timer Event Input Restrictions Figure 2-42.

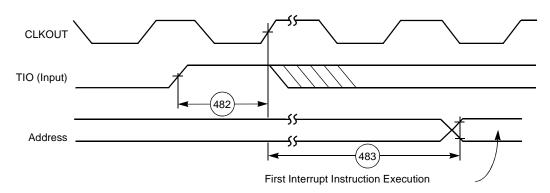


Figure 2-43. Timer Interrupt Generation

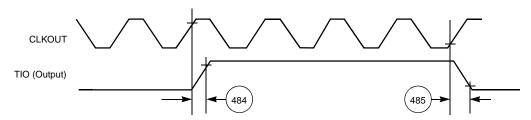


Figure 2-44. External Pulse Generation

### 2.5.10 GPIO Timing

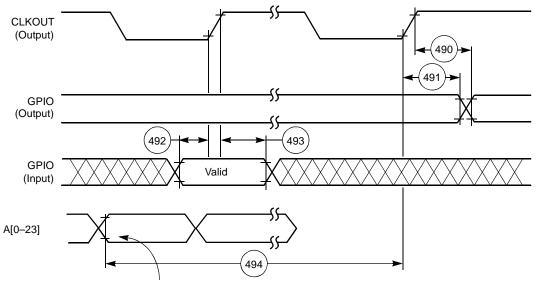
Table 2-24. **GPIO Timing** 

No.	Characteristics	Evarossion	1 08	ИНz	100 MHz		Unit
NO.	Cridiacteristics	Expression	Min	Max	Min	Max	Ullit
490	CLKOUT edge to GPIO out valid (GPIO out delay time)		_	31.0	_	8.5	ns
491	CLKOUT edge to GPIO out not valid (GPIO out hold time)		0.0	_	0.0	_	ns
492	GPIO In valid to CLKOUT edge (GPIO in set-up time)		8.5	_	8.5	_	ns
493	CLKOUT edge to GPIO in not valid (GPIO in hold time)		0.0	_	0.0	_	ns
494	Fetch to CLKOUT edge before GPIO change	$6.75 \times T_C$	84.4	_	67.5	_	ns
Note:	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}; T_{J} = -40^{\circ}\text{C} \text{ to } +100 ^{\circ}\text{C}, C_{L} = 50 \text{ pF}$						

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2-48 Freescale Semiconductor





Fetch the instruction MOVE X0,X:(R0); X0 contains the new value of GPIO and R0 contains the address of GPIO data register.

Figure 2-45. GPIO Timing

### 2.5.11 JTAG Timing

Table 2-25. JTAG Timing

N1 -	Characteristics <sup>1,2</sup>	All freq	uencies	Hois
No.	Characteristics	Min	Max	Unit
500	TCK frequency of operation (1/( $T_C \times 3$ ); maximum 22 MHz)	0.0	22.0	MHz
501	TCK cycle time in Crystal mode	45.0	_	ns
502	TCK clock pulse width measured at 1.5 V	20.0	_	ns
503	TCK rise and fall times	0.0	3.0	ns
504	Boundary scan input data setup time	5.0	_	ns
505	Boundary scan input data hold time	24.0	_	ns
506	TCK low to output data valid	0.0	40.0	ns
507	TCK low to output high impedance	0.0	40.0	ns
508	TMS, TDI data setup time	5.0	_	ns
509	TMS, TDI data hold time	25.0	_	ns
510	TCK low to TDO data valid	0.0	44.0	ns
511	TCK low to TDO high impedance	0.0	44.0	ns
512	TRST assert time	100.0	_	ns
513	TRST setup time to TCK low	40.0	_	ns

**Notes:** 1.  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ;  $T_J = -40 ^{\circ}\text{C}$  to +100  $^{\circ}\text{C}$ ,  $C_L = 50 \text{ pF}$ 

2. All timings apply to OnCE module data transfers because it uses the JTAG port as an interface.



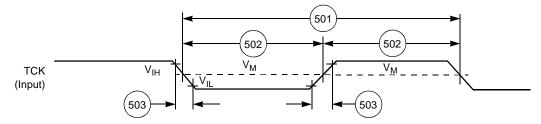


Figure 2-46. Test Clock Input Timing Diagram

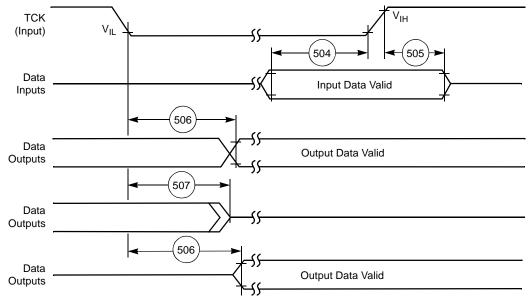


Figure 2-47. Boundary Scan (JTAG) Timing Diagram

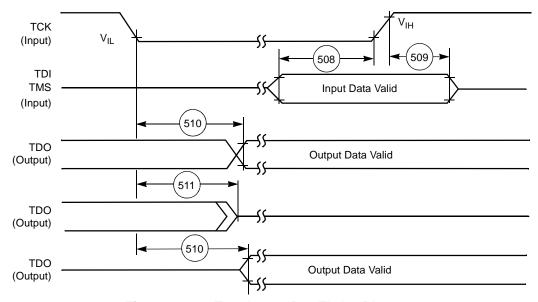


Figure 2-48. Test Access Port Timing Diagram

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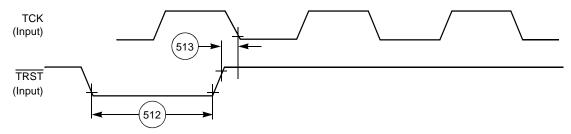


Figure 2-49. TRST Timing Diagram

### 2.5.12 OnCE Module TimIng

Table 2-26. OnCE Module Timing

NI -	Characteristics	F	80 1	80 MHz		100 MHz	
No.	Cnaracteristics	Expression	Min	Max	Min	Max	Unit
500	TCK frequency of operation	1/(T <sub>C</sub> × 3), max: 22.0 MHz	0.0	22.0	0.0	22.0	MHz
514	DE assertion time in order to enter Debug mode	$1.5 \times T_{C} + 10.0$	28.8	_	25.0	_	ns
515	Response time when DSP56301 is executing NOP instructions from internal memory	$5.5 \times T_{C} + 30.0$	_	98.8	_	85.0	ns
516	Debug acknowledge assertion time	$3 \times T_C - 5.0$	47.5	_	25.0	_	ns
Note:	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ : $T_1 = -40^{\circ}\text{C}$ to $+100^{\circ}\text{C}$ . $C_1 = 50 \text{ pF}$						

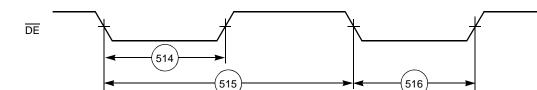


Figure 2-50. OnCE—Debug Request

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ifications



Packaging 3

This section provides information on the available packages for the DSP56301, including diagrams of the package pinouts and tables showing how the signals discussed in **Section 1** are allocated for each package. The DSP56301 is available in two package types:

- 208-pin Thin Quad Flat Pack (TQFP)
- 252-pin Molded Array Process-Ball Grid Array (MAP-BGA)

**Note:** Both packages are available in lead-bearing and lead-free versions. Switching a design from a lead-bearing package device to a lead-free package device may require a change in the board manufacturing process. The lead-free package requires a higher solder flow temperature than the lead-bearing device. Refer to *Lead-Free BGA Solder Joint Assembly Evaluation* (EB635) for manufacturing considerations when incorporating lead-free package devices into a design.



## 3.1 TQFP Package Description

Top and bottom views of the TQFP package are shown in Figure 3-1 and Figure 3-2 with their pin-outs.

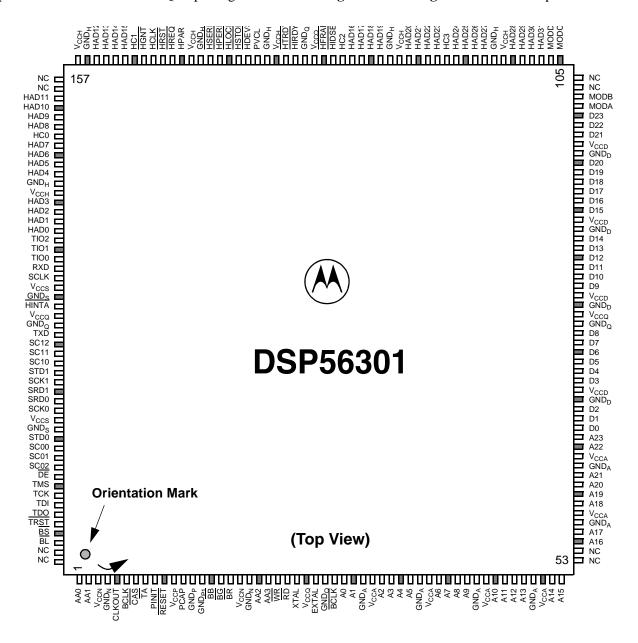


Figure 3-1. DSP56301 Thin Quad Flat Pack (TQFP), Top View

3-2 Freescale Semiconductor



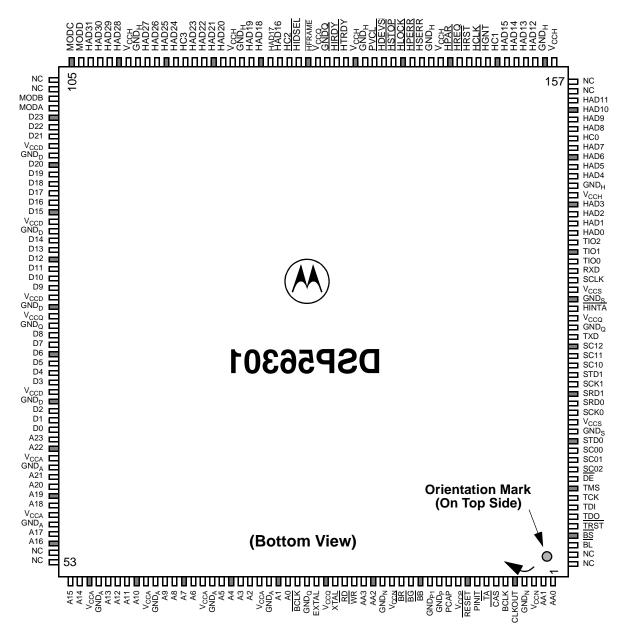


Figure 3-2. DSP56301 Thin Quad Flat Pack (TQFP), Bottom View

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 Table 3-1.
 DSP56301 TQFP Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	AA0/RAS0	26	EXTAL	51	A14
2	AA1/RAS1	27	GND <sub>Q</sub>	52	A15
3	V <sub>CCN</sub>	28	BCLK	53	NC
4	GND <sub>N</sub>	29	A0	54	NC
5	CLKOUT	30	A1	55	A16
6	BCLK	31	GND <sub>A</sub>	56	A17
7	CAS	32	V <sub>CCA</sub>	57	GND <sub>A</sub>
8	TA	33	A2	58	V <sub>CCA</sub>
9	PINIT/NMI	34	А3	59	A18
10	RESET	35	A4	60	A19
11	V <sub>CCP</sub>	36	A5	61	A20
12	PCAP	37	GND <sub>A</sub>	62	A21
13	GND <sub>P</sub>	38	V <sub>CCA</sub>	63	GND <sub>A</sub>
14	GND <sub>P1</sub>	39	A6	64	V <sub>CCA</sub>
15	BB	40	A7	65	A22
16	BG	41	A8	66	A23
17	BR	42	A9	67	D0
18	V <sub>CCN</sub>	43	GND <sub>A</sub>	68	D1
19	GND <sub>N</sub>	44	V <sub>CCA</sub>	69	D2
20	AA2/RAS2	45	A10	70	GND <sub>D</sub>
21	AA3/RAS3	46	A11	71	V <sub>CCD</sub>
22	WR	47	A12	72	D3
23	RD	48	A13	73	D4
24	XTAL	49	GND <sub>A</sub>	74	D5
25	V <sub>CCQ</sub>	50	V <sub>CCA</sub>	75	D6

3-4 Freescale Semiconductor



 Table 3-1.
 DSP56301 TQFP Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
76	D7	101	MODA/IRQA	126	HAD17 or HD9
77	D8	102	MODB/IRQB	127	HAD16 or HD8
78	$GND_Q$	103	NC	128	HC2/HBE2, HA2, or PB18
79	V <sub>CCQ</sub>	104	NC	129	HIDSEL or HRD/HDS
80	GND <sub>D</sub>	105	MODC/IRQC	130	HFRAME
81	V <sub>CCD</sub>	106	MODD/IRQD	131	V <sub>CCQ</sub>
82	D9	107	HAD31 or HD23	132	$GND_Q$
83	D10	108	HAD30 or HD22	133	HIRDY, HDBDR, or PB21
84	D11	109	HAD29 or HD21	134	HTRDY, HDBEN, or PB20
85	D12	110	HAD28 or HD20	135	V <sub>CCH</sub>
86	D13	111	V <sub>CCH</sub>	136	GND <sub>H</sub>
87	D14	112	GND <sub>H</sub>	137	PVCL
88	GND <sub>D</sub>	113	HAD27 or HD19	138	HDEVSEL, HSAK, or PB22
89	V <sub>CCD</sub>	114	HAD26 or HD18	139	HSTOP or HWR/HRW
90	D15	115	HAD25 or HD17	140	HLOCK, HBS, or PB23
91	D16	116	HAD24 or HD16	141	HPERR or HDRQ
92	D17	117	HC3/HBE3 or PB19	142	HSERR or HIRQ
93	D18	118	HAD23 or HD15	143	GND <sub>H</sub>
94	D19	119	HAD22 or HD14	144	V <sub>CCH</sub>
95	D20	120	HAD21 or HD13	145	HPAR or HDAK
96	GND <sub>D</sub>	121	HAD20 or HD12	146	HREQ or HTA
97	V <sub>CCD</sub>	122	V <sub>CCH</sub>	147	HRST or HRST
98	D21	123	GND <sub>H</sub>	148	HCLK
99	D22	124	HAD19 or HD11	149	HGNT or HAEN
100	D23	125	HAD18 or HD10	150	HC1/HBE1, HA1, or PB17



 Table 3-1.
 DSP56301 TQFP Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
151	HAD15, HD7, or PB15	171	HAD2, HA5, or PB2	191	SRD0 or PC4
152	HAD14, HD6, or PB14	172	HAD1, HA4, or PB1	192	SCK0 or PC3
153	HAD13, HD5, or PB13	173	HAD0, HA3, or PB0	193	V <sub>CCS</sub>
154	HAD12, HD4, or PB12	174	TIO2	194	GND <sub>S</sub>
155	GND <sub>H</sub>	175	TIO1	195	STD0 or PC5
156	V <sub>CCH</sub>	176	TIO0	196	SC00 or PC0
157	NC	177	RXD or PE0	197	SC01 or PC1
158	NC	178	SCLK or PE2	198	SC02 or PC2
159	HAD11, HD3, or PB11	179	V <sub>CCS</sub>	199	DE
160	HAD10, HD2, or PB10	180	GND <sub>S</sub>	200	TMS
161	HAD9, HD1, or PB9	181	HINTA	201	TCK
162	HAD8, HD0, or PB8	182	V <sub>CCQ</sub>	202	TDI
163	HC0/HBE0, HA0, or PB16	183	$GND_Q$	203	TDO
164	HAD7, HA10, or PB7	184	TXD or PE1	204	TRST
165	HAD6, HA9, or PB6	185	SC12 or PD2	205	BS
166	HAD5, HA8, or PB5	186	SC11 or PD1	206	BL
167	HAD4, HA7, or PB4	187	SC10 or PD0	207	NC
168	GND <sub>H</sub>	188	STD1 or PD5	208	NC
169	V <sub>CCH</sub>	189	SCK1 or PD3		
170	HAD3, HA6, or PB3	190	SRD1 or PD4	1	

#### Notes:

- 1. Signal names are based on configured functionality. Most pins supply a single signal. Some pins provide a signal with dual functionality, such as the MODx/IRQx pins that select an operating mode after RESET is deasserted, but act as interrupt lines during operation. Some pins have two or more configurable functions; names assigned to these pins indicate the function for a specific configuration. For example, Pin 165 is address/data line HAD6 in PCI bus mode, address line HA9 in non-PCI bus mode, or GPIO line PB6 when the GPIO function is enabled for this pin.
- 2. NC stands for Not Connected. These pins are reserved for future development. Do not connect any line, component, trace, or via to these pins.

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 Table 3-2.
 DSP56301 TQFP Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	29	AA3	21	D3	72
A1	30	BB	15	D4	73
A10	45	BCLK	6	D5	74
A11	46	BCLK	28	D6	75
A12	47	BG	16	D7	76
A13	48	BL	206	D8	77
A14	51	BR	17	D9	82
A15	52	BS	205	DE	199
A16	55	CAS	7	EXTAL	26
A17	56	CLKOUT	5	GND <sub>P1</sub>	14
A18	59	D0	67	GND <sub>A</sub>	31
A19	60	D1	68	GND <sub>A</sub>	37
A2	33	D10	83	GND <sub>A</sub>	43
A20	61	D11	84	GND <sub>A</sub>	49
A21	62	D12	85	GND <sub>A</sub>	57
A22	65	D13	86	GND <sub>A</sub>	63
A23	66	D14	87	GND <sub>D</sub>	70
A3	34	D15	90	GND <sub>D</sub>	80
A4	35	D16	91	GND <sub>D</sub>	88
A5	36	D17	92	GND <sub>D</sub>	96
A6	39	D18	93	GND <sub>H</sub>	112
A7	40	D19	94	GND <sub>H</sub>	123
A8	41	D2	69	GND <sub>H</sub>	136
A9	42	D20	95	GND <sub>H</sub>	143
AA0	1	D21	98	GND <sub>H</sub>	155
AA1	2	D22	99	GND <sub>H</sub>	168
AA2	20	D23	100	GND <sub>N</sub>	4



DSP56301 TQFP Signal Identification by Name (Continued) **Table 3-2.** 

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND <sub>N</sub>	19	HAD14	152	HAEN	149
GND <sub>P</sub>	13	HAD15	151	HBE0	163
GND <sub>Q</sub>	27	HAD16	127	HBE1	150
GND <sub>Q</sub>	78	HAD17	126	HBE2	128
GND <sub>Q</sub>	132	HAD18	125	HBE3	117
GND <sub>Q</sub>	183	HAD19	124	HBS	140
GND <sub>Q</sub>	183	HAD2	171	HC0	163
GND <sub>S</sub>	180	HAD20	121	HC1	150
GND <sub>S</sub>	194	HAD21	120	HC2	128
HA0	163	HAD22	119	HC3	117
HA1	150	HAD23	118	HCLK	148
HA10	164	HAD24	116	HD0	162
HA2	128	HAD25	115	HD1	161
HA3	173	HAD26	114	HD10	125
HA4	172	HAD27	113	HD11	124
HA5	171	HAD28	110	HD12	121
HA6	170	HAD29	109	HD13	120
HA7	167	HAD3	170	HD14	119
HA8	166	HAD30	108	HD15	118
HA9	165	HAD31	107	HD16	116
HAD0	173	HAD4	167	HD17	115
HAD1	172	HAD5	166	HD18	114
HAD10	160	HAD6	165	HD19	113
HAD11	159	HAD7	164	HD2	160
HAD12	154	HAD8	162	HD20	110
HAD13	153	HAD9	161	HD21	109



 Table 3-2.
 DSP56301 TQFP Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HD22	108	HRST/HRST	147	PB0	173
HD23	107	HRW	139	PB1	172
HD3	159	HSAK	138	PB10	160
HD4	154	HSERR	142	PB11	159
HD5	153	HSTOP	139	PB12	154
HD6	152	HTA	146	PB13	153
HD7	151	HTRDY	134	PB14	152
HD8	127	HWR	139	PB15	151
HD9	126	ĪRQĀ	101	PB16	163
HDAK	145	ĪRQB	102	PB17	150
HDBDR	133	ĪRQC	105	PB18	128
HDBEN	134	ĪRQD	106	PB19	117
HDEVSEL	138	MODA	101	PB2	171
HDRQ	141	MODB	102	PB20	134
HDS	129	MODC	105	PB21	133
HFRAME	130	MODD	106	PB22	138
HGNT	149	NC	28	PB23	140
HIDSEL	129	NC	53	PB3	170
HINTA	181	NC	54	PB4	167
HIRDY	133	NC	103	PB5	166
HIRQ	142	NC	104	PB6	165
HLOCK	140	NC	157	PB7	164
HPAR	145	NC	158	PB8	162
HPERR	141	NC	207	PB9	161
HRD	129	NC	208	PC0	196
HREQ	146	NMI	9	PC1	197



DSP56301 TQFP Signal Identification by Name (Continued) **Table 3-2.** 

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
PC2	198	SC02	198	V <sub>CCA</sub>	58
PC3	192	SC10	187	V <sub>CCA</sub>	64
PC4	191	SC11	186	V <sub>CCD</sub>	71
PC5	195	SC12	185	V <sub>CCD</sub>	81
PCAP	12	SCK0	192	V <sub>CCD</sub>	89
PD0	187	SCK1	189	V <sub>CCD</sub>	97
PD1	186	SCLK	178	V <sub>CCH</sub>	111
PD2	185	SRD0	191	V <sub>CCH</sub>	122
PD3	189	SRD1	190	V <sub>CCH</sub>	135
PD4	190	STD0	195	V <sub>CCH</sub>	144
PD5	188	STD1	188	V <sub>CCH</sub>	156
PE0	177	TA	8	V <sub>CCH</sub>	169
PE1	184	TCK	201	V <sub>CCN</sub>	3
PE2	178	TDI	202	V <sub>CCN</sub>	18
PINIT	9	TDO	203	V <sub>CCP</sub>	11
PVCL	137	TIO0	176	V <sub>CCQ</sub>	25
RAS0	1	TIO1	175	V <sub>CCQ</sub>	79
RAS1	2	TIO2	174	V <sub>CCQ</sub>	131
RAS2	20	TMS	200	V <sub>CCQ</sub>	182
RAS3	21	TRST	204	V <sub>ccs</sub>	179
RD	23	TXD	184	V <sub>ccs</sub>	193
RESET	10	V <sub>CCA</sub>	32	WR	22
RXD	177	$V_{CCA}$	38	XTAL	24
SC00	196	V <sub>CCA</sub>	44		
SC01	197	V <sub>CCA</sub>	50		

Note: NC stands for Not Connected. These pins are reserved for future development. Do not connect any line, component, or trace to these pins.

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## 3.2 TQFP Package Mechanical Drawing

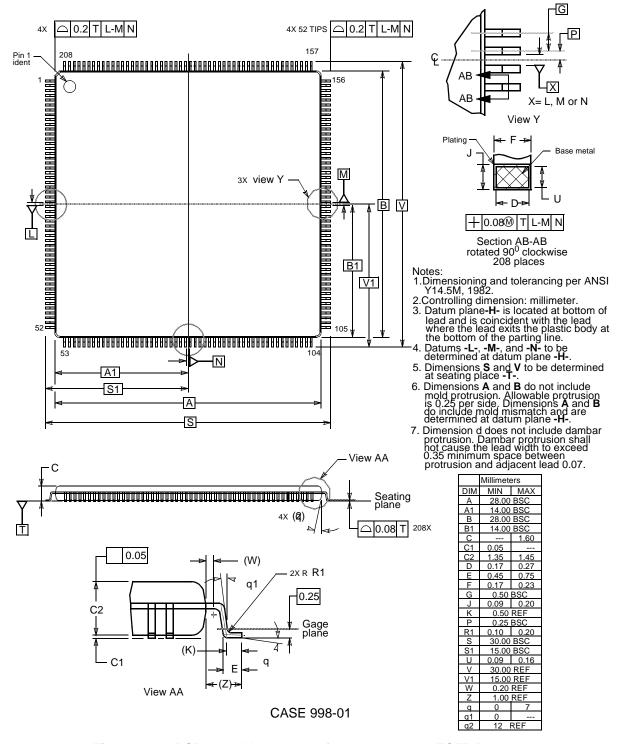


Figure 3-3. DSP56301 Mechanical Information, 208-pin TQFP Package



# 3.3 MAP-BGA Package Description

Top and bottom views of the MAP-BGA package are shown in Figure 3-4 and Figure 3-5 with their pin-outs.

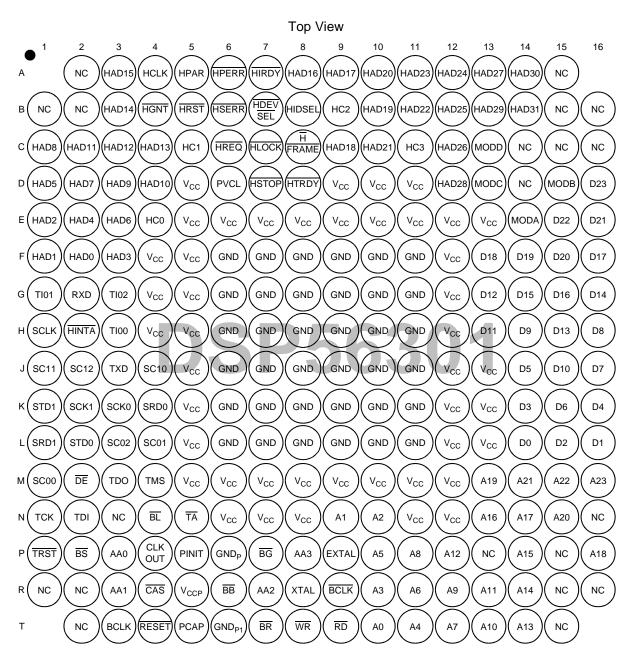


Figure 3-4. DSP56301 Molded Array Process-Ball Grid Array (MAP-BGA), Top View

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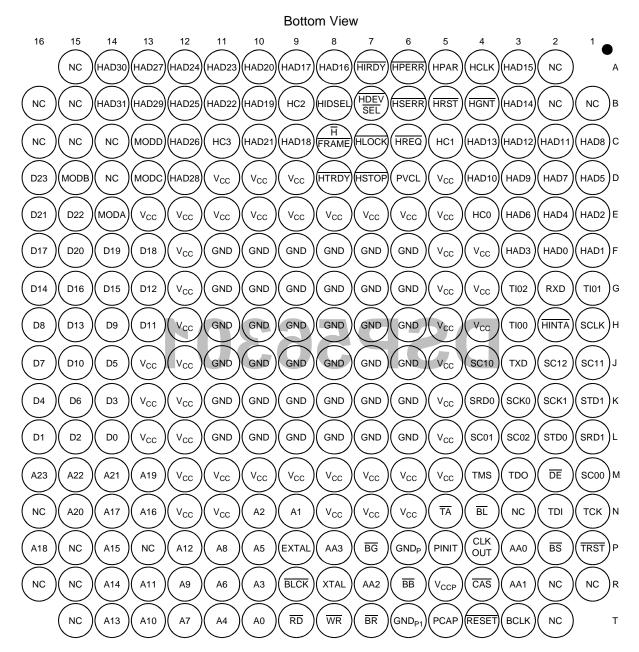


Figure 3-5. DSP56301 Molded Array Process-Ball Grid Array (MAP-BGA), Bottom View



 Table 3-3.
 DSP56301 MAP-BGA Signal Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A2	NC	B12	HAD25 or HD17	D5	V <sub>CC</sub>
А3	HAD15, HD7, or PB15	B13	HAD29 or HD21	D6	PVCL
A4	HCLK	B14	HAD31 or HD23	D7	HSTOP or HWR/HRW
A5	HPAR or HDAK	B15	NC	D8	HTRDY, HDBEN, or PB20
A6	HPERR or HDRQ	B16	NC	D9	V <sub>CC</sub>
A7	HIRDY, HDBDR, or PB21	C1	HAD8, HD0, or PB8	D10	V <sub>CC</sub>
A8	HAD16 or HD8	C2	HAD11, HD3, or PB11	D11	V <sub>CC</sub>
A9	HAD17 or HD9	C3	HAD12, HD4, or PB12	D12	HAD28 or HD20
A10	HAD20 or HD12	C4	HAD13, HD5, or PB13	D13	MODC/IRQC
A11	HAD23 or HD15	C5	HC1/HBE1, HA1, or PB17	D14	NC
A12	HAD24 or HD16	C6	HREQ or HTA	D15	MODB/IRQB
A13	HAD27 or HD19	C7	HLOCK, HBS, or PB23	D16	D23
A14	HAD30 or HD22	C8	HFRAME	E1	HAD2, HA5, or PB2
A15	NC	C9	HAD18 or HD10	E2	HAD4, HA7, or PB4
B1	NC	C10	HAD21 or HD13	E3	HAD6, HA9, or PB6
B2	NC	C11	HC3/HBE3 or PB19	E4	HC0/HBE0, HA0, or PB16
В3	HAD14, HD6, or PB14	C12	HAD26 or HD18	E5	V <sub>CC</sub>
B4	HGNT or HAEN	C13	MODD/IRQD	E6	V <sub>CC</sub>
B5	HRST/HRST	C14	NC	E7	V <sub>CC</sub>
В6	HSERR or HIRQ	C15	NC	E8	V <sub>CC</sub>
В7	HDEVSEL, HSAK, or PB22	C16	NC	E9	V <sub>CC</sub>
B8	HIDSEL or HRD/HDS	D1	HAD5, HA8, or PB5	E10	V <sub>CC</sub>
В9	HC2/HBE2, HA2, or PB18	D2	HAD7, HA10, or PB7	E11	V <sub>CC</sub>
B10	HAD19 or HD11	D3	HAD9, HD1, or PB9	E12	V <sub>CC</sub>
B11	HAD22 or HD14	D4	HAD10, HD2, or PB10	E13	V <sub>CC</sub>

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 Table 3-3.
 DSP56301 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
E14	MODA/IRQA	G7	GND	H16	D8
E15	D22	G8	GND	J1	SC11 or PD1
E16	D21	G9	GND	J2	SC12 or PD2
F1	HAD1, HA4, or PB1	G10	GND	J3	TXD or PE1
F2	HAD0, HA3, or PB0	G11	GND	J4	SC10 or PD0
F3	HAD3, HA6, or PB3	G12	V <sub>CC</sub>	J5	V <sub>CC</sub>
F4	V <sub>CC</sub>	G13	D12	J6	GND
F5	V <sub>CC</sub>	G14	D15	J7	GND
F6	GND	G15	D16	J8	GND
F7	GND	G16	D14	J9	GND
F8	GND	H1	SCLK or PE2	J10	GND
F9	GND	H2	HINTA	J11	GND
F10	GND	НЗ	TIO0	J12	V <sub>CC</sub>
F11	GND	H4	V <sub>CC</sub>	J13	V <sub>CC</sub>
F12	V <sub>CC</sub>	H5	V <sub>CC</sub>	J14	D5
F13	D18	H6	GND	J15	D10
F14	D19	H7	GND	J16	D7
F15	D20	H8	GND	K1	STD1 or PD5
F16	D17	H9	GND	K2	SCK1 or PD3
G1	TIO1	H10	GND	КЗ	SCK0 or PC3
G2	RXD or PE0	H11	GND	K4	SRD0 or PC4
G3	TIO2	H12	V <sub>CC</sub>	K5	V <sub>CC</sub>
G4	V <sub>CC</sub>	H13	D11	K6	GND
G5	V <sub>CC</sub>	H14	D9	K7	GND
G6	GND	H15	D13	K8	GND



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 Table 3-3.
 DSP56301 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
K9	GND	M2	DE	N11	V <sub>CC</sub>
K10	GND	М3	TDO	N12	V <sub>CC</sub>
K11	GND	M4	TMS	N13	A16
K12	V <sub>CC</sub>	M5	V <sub>CC</sub>	N14	A17
K13	V <sub>CC</sub>	M6	V <sub>CC</sub>	N15	A20
K14	D3	M7	V <sub>CC</sub>	N16	NC
K15	D6	M8	V <sub>CC</sub>	P1	TRST
K16	D4	M9	V <sub>CC</sub>	P2	BS
L1	SRD1 or PD4	M10	V <sub>CC</sub>	P3	AA0/RAS0
L2	STD0 or PC5	M11	V <sub>CC</sub>	P4	CLKOUT
L3	SC02 or PC2	M12	V <sub>CC</sub>	P5	PINIT/NMI
L4	SC01 or PC1	M13	A19	P6	GND <sub>P</sub>
L5	V <sub>CC</sub>	M14	A21	P7	BG
L6	GND	M15	A22	P8	AA3/RAS3
L7	GND	M16	A23	P9	EXTAL
L8	GND	N1	TCK	P10	A5
L9	GND	N2	TDI	P11	A8
L10	GND	N3	NC	P12	A12
L11	GND	N4	BL	P13	NC
L12	V <sub>CC</sub>	N5	TA	P14	A15
L13	V <sub>CC</sub>	N6	V <sub>CC</sub>	P15	NC
L14	D0	N7	V <sub>CC</sub>	P16	A18
L15	D2	N8	V <sub>CC</sub>	R1	NC
L16	D1	N9	A1	R2	NC
M1	SC00 or PC0	N10	A2	R3	AA1/RAS1

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Table 3-3. DSP56301 MAP-BGA Signal Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
R4	CAS	R13	A11	T7	BR
R5	V <sub>CCP</sub>	R14	A14	Т8	WR
R6	BB	R15	NC	Т9	RD
R7	AA2/RAS2	R16	NC	T10	A0
R8	XTAL	T2	NC	T11	A4
R9	BCLK	Т3	BCLK	T12	A7
R10	А3	T4	RESET	T13	A10
R11	A6	T5	PCAP	T14	A13
R12	A9	Т6	GND <sub>P1</sub>	T15	NC

#### Notes:

- Signal names are based on configured functionality. Most connections supply a single signal. Some connections provide a signal with dual functionality, such as the MODx/IRQx pins that select an operating mode after RESET is deasserted, but act as interrupt lines during operation. Some signals have configurable polarity; these names are shown with and without overbars, such as HAS/HAS. Some connections have two or more configurable functions; names assigned to these connections indicate the function for a specific configuration. For example, connection N2 is data line H7 in non-multiplexed bus mode, data/address line HAD7 in multiplexed bus mode, or GPIO line PB7 when the GPIO function is enabled for this pin. Unlike the TQFP package, most of the GND pins are connected internally in the center of the connection array and act as heat sink for the chip. Therefore, except for GND<sub>P</sub> and GND<sub>P1</sub> that support the PLL, other GND signals do not support individual subsystems in the chip.
- 2. NC stands for Not Connected. The following pin groups are shorted to each other:
  - pins A2, B1, and B2
  - pins A15, B15, B16, C14, C15, C16, and D14
  - pins N3, R1, R2, and T2
  - pins N16, P13, P15, R15, R16, and T15

Do not connect any line, component, trace, or via to these pins.



 Table 3-4.
 DSP56301 MAP-BGA Signal Identification by Name

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
A0	T10	AA2	R7	D22	E15
A1	N9	AA3	P8	D23	D16
A10	T13	BB	R6	D3	K14
A11	R13	BCLK	Т3	D4	K16
A12	P12	BCLK	R9	D5	J14
A13	T14	BG	P7	D6	K15
A14	R14	BL	N4	D7	J16
A15	P14	BR	T7	D8	H16
A16	N13	BS	P2	D9	H14
A17	N14	CAS	R4	DE	M2
A18	P16	CLKOUT	P4	EXTAL	P9
A19	M13	D0	L14	GND	F10
A2	N10	D1	L16	GND	F11
A20	N15	D10	J15	GND	F6
A21	M14	D11	H13	GND	F7
A22	M15	D12	G13	GND	F8
A23	M16	D13	H15	GND	F9
A3	R10	D14	G16	GND	G10
A4	T11	D15	G14	GND	G11
A5	P10	D16	G15	GND	G6
A6	R11	D17	F16	GND	G7
A7	T12	D18	F13	GND	G8
A8	P11	D19	F14	GND	G9
A9	R12	D2	L15	GND	H10
AA0	P3	D20	F15	GND	H11
AA1	R3	D21	E16	GND	H6

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 Table 3-4.
 DSP56301 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	H7	HA10	D2	HAD23	A11
GND	H8	HA2	В9	HAD24	A12
GND	H9	HA3	F2	HAD25	B12
GND	J10	HA4	F1	HAD26	C12
GND	J11	HA5	E1	HAD27	A13
GND	J6	HA6	F3	HAD28	D12
GND	J7	HA7	E2	HAD29	B13
GND	J8	HA8	D1	HAD3	F3
GND	J9	HA9	E3	HAD30	A14
GND	K10	HAD0	F2	HAD31	B14
GND	K11	HAD1	F1	HAD4	E2
GND	K6	HAD10	D4	HAD5	D1
GND	K7	HAD11	C2	HAD6	E3
GND	K8	HAD12	C3	HAD7	D2
GND	K9	HAD13	C4	HAD8	C1
GND	L10	HAD14	В3	HAD9	D3
GND	L11	HAD15	А3	HAEN	B4
GND	L6	HAD16	A8	HBE0	E4
GND	L7	HAD17	A9	HBE1	C5
GND	L8	HAD18	C9	HBE2	В9
GND	L9	HAD19	B10	HBE3	C11
GND <sub>P1</sub>	Т6	HAD2	E1	HBS	C7
GND <sub>P</sub>	P6	HAD20	A10	HC0	E4
HA0	E4	HAD21	C10	HC1	C5
HA1	C5	HAD22	B11	HC2	В9



 Table 3-4.
 DSP56301 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
HC3	C11	HD9	A9	HWR	D7
HCLK	A4	HDAK	A5	ĪRQĀ	E14
HD0	C1	HDBDR	A7	ĪRQB	D15
HD1	D3	HDBEN	D8	ĪRQC	D13
HD10	C9	HDEVSEL	B7	ĪRQD	C13
HD11	B10	HDRQ	A6	MODA	E14
HD12	A10	HDS	B8	MODB	D15
HD13	C10	HFRAME	C8	MODC	D13
HD14	B11	HGNT	B4	MODD	C13
HD15	A11	HIDSEL	B8	NC	A15
HD16	A12	HINTA	H2	NC	A2
HD17	B12	HIRDY	A7	NC	B1
HD18	C12	HIRQ	В6	NC	B15
HD19	A13	HLOCK	C7	NC	B16
HD2	D4	HPAR	A5	NC	B2
HD20	D12	HPERR	A6	NC	C14
HD21	B13	HRD	B8	NC	C15
HD22	A14	HREQ	C6	NC	C16
HD23	B14	HRST/HRST	B5	NC	D14
HD3	C2	HRW	D7	NC	N16
HD4	C3	HSAK	В7	NC	N3
HD5	C4	HSERR	B6	NC	P13
HD6	В3	HSTOP	D7	NC	P15
HD7	A3	HTA	C6	NC	R1
HD8	A8	HTRDY	D8	NC	R2

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 Table 3-4.
 DSP56301 MAP-BGA Signal Identification by Name (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
NC	R15	PB6	E3	RAS3	P8
NC	R16	PB7	D2	RD	Т9
NC	T2	PB8	C1	RESET	T4
NC	T15	PB9	D3	RXD	G2
NMI	P5	PC0	M1	SC00	M1
PB0	F2	PC1	L4	SC01	L4
PB1	F1	PC2	L3	SC02	L3
PB10	D4	PC3	К3	SC10	J4
PB11	C2	PC4	K4	SC11	J1
PB12	С3	PC5	L2	SC12	J2
PB13	C4	PCAP	T5	SCK0	К3
PB14	В3	PD0	J4	SCK1	K2
PB15	А3	PD1	J1	SCLK	H1
PB16	E4	PD2	J2	SRD0	K4
PB17	C5	PD3	K2	SRD1	L1
PB18	В9	PD4	L1	STD0	L2
PB19	C11	PD5	K1	STD1	K1
PB2	E1	PE0	G2	TA	N5
PB20	D8	PE1	J3	TCK	N1
PB21	A7	PE2	H1	TDI	N2
PB22	В7	PINIT	P5	TDO	МЗ
PB23	C7	PVCL	D6	TIO0	НЗ
PB3	F3	RAS0	P3	TIO1	G1
PB4	E2	RAS1	R3	TIO2	G3
PB5	D1	RAS2	R7	TMS	M4



DSP56301 MAP-BGA Signal Identification by Name (Continued) **Table 3-4.** 

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
TRST	P1	V <sub>CC</sub>	F5	V <sub>CC</sub>	M10
TXD	J3	V <sub>CC</sub>	G12	V <sub>CC</sub>	M11
V <sub>CC</sub>	D10	V <sub>CC</sub>	G4	V <sub>CC</sub>	M12
V <sub>CC</sub>	D11	V <sub>CC</sub>	G5	V <sub>CC</sub>	M5
V <sub>CC</sub>	D5	V <sub>CC</sub>	H12	V <sub>CC</sub>	M6
V <sub>CC</sub>	D9	V <sub>CC</sub>	H4	V <sub>CC</sub>	M7
V <sub>CC</sub>	E10	V <sub>CC</sub>	H5	V <sub>CC</sub>	M8
V <sub>CC</sub>	E11	V <sub>CC</sub>	J12	V <sub>CC</sub>	M9
V <sub>CC</sub>	E12	V <sub>CC</sub>	J13	V <sub>CC</sub>	N11
V <sub>CC</sub>	E13	V <sub>CC</sub>	J5	V <sub>CC</sub>	N12
V <sub>CC</sub>	E5	V <sub>CC</sub>	K12	V <sub>CC</sub>	N6
V <sub>CC</sub>	E6	V <sub>CC</sub>	K13	V <sub>CC</sub>	N7
V <sub>CC</sub>	E7	V <sub>CC</sub>	K5	V <sub>CC</sub>	N8
V <sub>CC</sub>	E8	V <sub>CC</sub>	L12	V <sub>CCP</sub>	R5
V <sub>CC</sub>	E9	V <sub>CC</sub>	L13	WR	Т8
V <sub>CC</sub>	F12	V <sub>CC</sub>	L5	XTAL	R8
V <sub>CC</sub>	F4				

Note: NC stands for Not Connected. The following pin groups are shorted to each other:

<sup>-</sup>pins A2, B1, and B2

<sup>-</sup>pins A15, B15, B16, C14, C15, C16, and D14

<sup>—</sup>pins N3, R1, R2, and T2

<sup>—</sup>pins N16, P13, P15, R15, R16, and T15
Do not connect any line, component, trace, or via to these pins.



## 3.4 MAP-BGA Package Mechanical Drawing

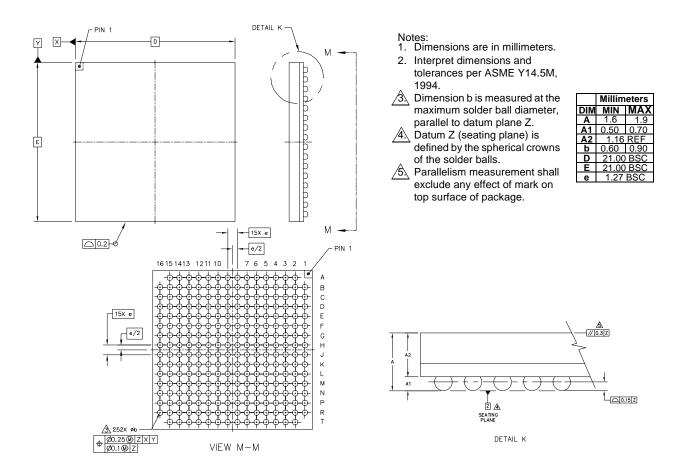


Figure 3-6. DSP56301 Mechanical Information, 252-pin MAP-BGA Package





# **Design Considerations**

# 4

### 4.1 Thermal Design Considerations

An estimate of the chip junction temperature, T<sub>J</sub>, in °C can be obtained from this equation:

Equation 1: 
$$T_I = T_A + (P_D \times R_{\theta IA})$$

Where:

 $T_A$  = ambient temperature  ${}^{\circ}C$ 

 $R_{\theta IA}$  = package junction-to-ambient thermal resistance °C/W

P<sub>D</sub> = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance, as in this equation:

**Equation 2:** 
$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

Where:

 $R_{\theta JA}$  = package junction-to-ambient thermal resistance °C/W  $R_{\theta JC}$  = package junction-to-case thermal resistance °C/W  $R_{\theta CA}$  = package case-to-ambient thermal resistance °C/W

 $R_{\theta JC}$  is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance,  $R_{\theta CA}$ . For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board (PCB) or otherwise change the thermal dissipation capability of the area surrounding the device on a PCB. This model is most useful for ceramic packages with heat sinks; some 90 percent of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system-level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimates obtained from  $R_{\theta JA}$  do not satisfactorily answer whether the thermal performance is adequate, a system-level model may be appropriate.

A complicating factor is the existence of three common ways to determine the junction-to-case thermal resistance in plastic packages.

- To minimize temperature variation across the surface, the thermal resistance is measured from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink.
- To define a value approximately equal to a junction-to-board thermal resistance, the thermal resistance is measured from the junction to the point at which the leads attach to the case.



#### an Considerations

• If the temperature of the package case  $(T_T)$  is determined by a thermocouple, thermal resistance is computed from the value obtained by the equation  $(T_I - T_T)/P_D$ .

As noted earlier, the junction-to-case thermal resistances quoted in this data sheet are determined using the first definition. From a practical standpoint, that value is also suitable to determine the junction temperature from a case thermocouple reading in forced convection environments. In natural convection, the use of the junction-to-case thermal resistance to estimate junction temperature from a thermocouple reading on the case of the package will yield an estimate of a junction temperature slightly higher than actual temperature. Hence, the new thermal metric, thermal characterization parameter or  $\Psi_{JT}$ , has been defined to be  $(T_J - T_T)/P_D$ . This value gives a better estimate of the junction temperature in natural convection when the surface temperature of the package is used. Remember that surface temperature readings of packages are subject to significant errors caused by inadequate attachment of the sensor to the surface and to errors caused by heat loss to the sensor. The recommended technique is to attach a 40-gauge thermocouple wire and bead to the top center of the package with thermally conductive epoxy.

### 4.2 Electrical Design Considerations

#### **CAUTION**

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for example, either GND or V<sub>CC</sub>).

Use the following list of recommendations to ensure correct DSP operation.

- Provide a low-impedance path from the board power supply to each V<sub>CC</sub> pin on the DSP and from the board ground to each GND pin.
- Use at least six 0.01– $0.1~\mu F$  bypass capacitors positioned as close as possible to the four sides of the package to connect the  $V_{CC}$  power source to GND.
- Ensure that capacitor leads and associated printed circuit traces that connect to the chip V<sub>CC</sub> and GND pins are less than 0.5 inch per capacitor lead.
- Use at least a four-layer PCB with two inner layers for V<sub>CC</sub> and GND.
- Because the DSP output signals have fast rise and fall times, PCB trace lengths should be minimal. This recommendation particularly applies to the address and data buses as well as the IRQA, IRQB, IRQC, IRQD, TA, and BG pins. Maximum PCB trace lengths on the order of 6 inches are recommended.
- Consider all device loads as well as parasitic capacitance due to PCB traces when you calculate
  capacitance. This is especially critical in systems with higher capacitive loads that could create higher
  transient currents in the V<sub>CC</sub> and GND circuits.
- All inputs must be terminated (that is, not allowed to float) by CMOS levels except for the three pins with internal pull-up resistors (TRST, TMS, DE).
- Take special care to minimize noise levels on the V<sub>CCP</sub>, GND<sub>P</sub>, and GND<sub>P1</sub> pins.
- The following pins must be asserted after power-up: RESET and TRST.

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- If multiple DSP devices are on the same board, check for cross-talk or excessive spikes on the supplies due to synchronous operation of the devices.
- RESET must be asserted when the chip is powered up. A stable EXTAL signal should be supplied before deassertion of RESET.
- At power-up, ensure that the voltage difference between the 5 V tolerant pins and the chip  $V_{CC}$  never exceeds 3.5 V.

### 4.3 Power Consumption Considerations

Power dissipation is a key issue in portable DSP applications. Some of the factors affecting current consumption are described in this section. Most of the current consumed by CMOS devices is alternating current (ac), which is charging and discharging the capacitances of the pins and internal nodes.

Current consumption is described by this formula:

**Equation 3:** 
$$I = C \times V \times f$$

Where:

C = node/pin capacitance

V = voltage swing

f = frequency of node/pin toggle

**Example 1.** Current Consumption

For a Port A address pin loaded with 50 pF capacitance, operating at 3.3 V, with a 66 MHz clock, toggling at its maximum possible rate (33 MHz), the current consumption is expressed in **Equation 4**.

**Equation 4:** 
$$I = 50 \times 10^{-12} \times 3.3 \times 33 \times 10^6 = 5.48 \text{ mA}$$

The maximum internal current ( $I_{CCI}$ max) value reflects the typical possible switching of the internal buses on best-case operation conditions—not necessarily a real application case. The typical internal current ( $I_{CCItyp}$ ) value reflects the average switching of the internal buses on typical operating conditions. Perform the following steps for applications that require very low current consumption:

- 1. Set the EBD bit when you are not accessing external memory.
- 2. Minimize external memory accesses, and use internal memory accesses.
- **3.** Minimize the number of pins that are switching.
- **4.** Minimize the capacitive load on the pins.
- **5.** Connect the unused inputs to pull-up or pull-down resistors.
- **6.** Disable unused peripherals.
- 7. Disable unused pin activity (for example, CLKOUT, XTAL).

One way to evaluate power consumption is to use a current-per-MIPS measurement methodology to minimize specific board effects (that is, to compensate for measured board current not caused by the DSP). A benchmark power consumption test algorithm is listed in **Appendix A**. Use the test algorithm, specific test current measurements, and the following equation to derive the current-per-MIPS value.



**Equation 5:**  $I/\text{MIPS} = I/\text{MHz} = (I_{\text{typF2}} - I_{\text{typF1}})/(\text{F2} - \text{F1})$ 

Where:

 $I_{typF2}$  = current at F2  $I_{typF1}$  = current at F1

F2 = high frequency (any specified operating frequency)

F1 = low frequency (any specified operating frequency lower than F2)

**Note:** F1 should be significantly less than F2. For example, F2 could be 66 MHz and F1 could be 33 MHz. The degree of difference between F1 and F2 determines the amount of precision with which the current rating can be determined for an application.

### 4.4 PLL Performance Issues

The following explanations should be considered as general observations on expected PLL behavior. There is no test that replicates these exact numbers. These observations were measured on a limited number of parts and were not verified over the entire temperature and voltage ranges.

### 4.4.1 Phase Skew Performance

The phase skew of the PLL is defined as the time difference between the falling edges of EXTAL and CLKOUT for a given capacitive load on CLKOUT, over the entire process, temperature and voltage ranges. As defined in **Figure 2-2**, *External Clock Timing*, on page -5 for input frequencies greater than 15 MHz and the MF  $\leq$  4, this skew is greater than or equal to 0.0 ns and less than 1.8 ns; otherwise, this skew is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this skew is between -1.4 ns and +3.2 ns.

### 4.4.2 Phase Jitter Performance

The phase jitter of the PLL is defined as the variations in the skew between the falling edges of EXTAL and CLKOUT for a given device in specific temperature, voltage, input frequency, MF, and capacitive load on CLKOUT. These variations are a result of the PLL locking mechanism. For input frequencies greater than 15 MHz and MF  $\leq$  4, this jitter is less than  $\pm$ 0.6 ns; otherwise, this jitter is not guaranteed. However, for MF < 10 and input frequencies greater than 10 MHz, this jitter is less than  $\pm$ 2 ns.

### 4.4.3 Frequency Jitter Performance

The frequency jitter of the PLL is defined as the variation of the frequency of CLKOUT. For small MF (MF < 10) this jitter is smaller than 0.5 per cent. For mid-range MF (10 < MF < 500) this jitter is between 0.5 per cent and approximately 2 per cent. For large MF (MF > 500), the frequency jitter is 2–3 per cent.

## 4.5 Input (EXTAL) Jitter Requirements

The allowed jitter on the frequency of EXTAL is 0.5 percent. If the rate of change of the frequency of EXTAL is slow (that is, it does not jump between the minimum and maximum values in one cycle) or the frequency of the jitter is fast (that is, it does not stay at an extreme value for a long time), then the allowed jitter can be 2 percent. The phase and frequency jitter performance results are valid only if the input jitter is less than the prescribed values.



# **Power Consumption Benchmark**



The following benchmark program permits evaluation of DSP power usage in a test situation. It enables the PLL, disables the external clock, and uses repeated multiply-accumulate (MAC) instructions with a set of synthetic DSP application data to emulate intensive sustained DSP operation.

```
;* CHECKS Typical Power Consumption
;*
       page
              200,55,0,0,0
       nolist
I VEC EQU$000000; Interrupt vectors for program debug only
START EQU$8000; MAIN (external) program starting address
INT_PROG EQU$100 ; INTERNAL program memory starting address
INT_XDAT EQU$0 ; INTERNAL X-data memory starting address
INT_YDAT EQU$0 ; INTERNAL Y-data memory starting address
       INCLUDE "ioequ.asm"
       INCLUDE "intequ.asm"
       list
              P:START
       movep #$0123FF,x:M_BCR; BCR: Area 3 : 1 w.s (SRAM)
; Area 2 : 0 w.s (SSRAM)
; Default: 1 w.s (SRAM)
       movep #$0d0000,x:M PCTL; XTAL disable
; PLL enable
; CLKOUT disable
;Load the program
       move
              #INT PROG, r0
       move
              #PROG START, r1
       do
              #(PROG_END-PROG_START),PLOAD_LOOP
              p:(r1)+,x0
       move
       move
              x0,p:(r0)+
       nop
PLOAD LOOP
; Load the X-data
              #INT XDAT, r0
       move
              #XDAT_START, r1
       move
```

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#### er Consumption Benchmark

```
#(XDAT END-XDAT START), XLOAD LOOP
               p:(r1)+,x0
       move
       move
               x0,x:(r0) +
XLOAD LOOP
;Load the Y-data
       move
               #INT YDAT, r0
       move
               #YDAT START, r1
       do
               #(YDAT END-YDAT START),YLOAD LOOP
               p:(r1)+,x0
       move
               x0,y:(r0)+
       move
YLOAD LOOP
               INT PROG
       jmp
PROG_START
               #$0,r0
       move
               #$0,r4
       move
       move
               #$3f,m0
       move
               #$3f,m4
       clr
               а
       clr
               b
       move
               #$0,x0
       move
               #$0,x1
       move
               #$0,y0
       move
               #$0,y1
       bset
               #4,omr
                               ; ebd
               #60, end
sbr
       dor
               x0,y0,ax:(r0)+,x1
       mac
                                      y: (r4) + , y1
       mac
               x1,y1,ax:(r0)+,x0
                                      y: (r4) + , y0
       add
               a,b
               x0,y0,ax:(r0)+,x1
       mac
               x1,y1,a
                                      y: (r4) + , y0
       mac
               b1,x:$ff
       move
_end
       bra
               sbr
       nop
       nop
       nop
       nop
PROG END
       nop
       nop
XDAT START
       org
               x:0
       dс
               $262EB9
       dc
               $86F2FE
       dc
               $E56A5F
       dc
               $616CAC
       dс
               $8FFD75
       dс
               $9210A
       dc
               $A06D7B
       dс
               $CEA798
       dc
               $8DFBF1
       dc
               $A063D6
```

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```
dc
               $6C6657
       dc
               $C2A544
       dc
               $A3662D
       dc
               $A4E762
       dc
               $84F0F3
       dc
               $E6F1B0
       dc
               $B3829
       dc
               $8BF7AE
       dc
               $63A94F
       dc
               $EF78DC
               $242DE5
       dc
       dс
               $A3E0BA
       dc
               $EBAB6B
       dc
               $8726C8
       dc
               $CA361
       dc
               $2F6E86
       dc
               $A57347
               $4BE774
       dс
       dc
               $8F349D
               $A1ED12
       dc
               $4BFCE3
       dc
               $EA26E0
       dc
               $CD7D99
       dс
               $4BA85E
       dc
               $27A43F
       dc
               $A8B10C
       dc
               $D3A55
       dc
               $25EC6A
       dc
               $2A255B
       dс
               $A5F1F8
       dc
               $2426D1
       dc
               $AE6536
       dc
               $CBBC37
       dc
               $6235A4
               $37F0D
       dc
       dс
               $63BEC2
       dc
               $A5E4D3
       dc
               $8CE810
       dc
               $3FF09
       dc
               $60E50E
       dc
               $CFFB2F
               $40753C
       dс
       dc
               $8262C5
               $CA641A
       dc
               $EB3B4B
       dc
               $2DA928
       dc
               $AB6641
       dс
               $28A7E6
       dc
               $4E2127
       dc
               $482FD4
       dc
               $7257D
       dc
               $E53C72
       dc
               $1A8C3
               $E27540
       dс
XDAT END
       org
               y:0
       dс
               $5B6DA
```

YDAT\_START \$C3F70B dc



dc	\$6A39E8
dc	\$81E801
dc	\$C666A6
dc	\$46F8E7
dc	\$AAEC94
dc	\$24233D
dc	\$802732
dc	\$2E3C83
	\$A43E00
dc	
dc	\$C2B639
dc	\$85A47E
dc	\$ABFDDF
dc	\$F3A2C
dc	\$2D7CF5
dc	\$E16A8A
dc	\$ECB8FB
dc	\$4BED18
dc	\$43F371
dc	\$83A556
dc	\$E1E9D7
dc	\$ACA2C4
dc	\$8135AD
dc	\$2CE0E2
dc	\$8F2C73
dc	\$432730
dc	\$A87FA9
dc	\$4A292E
dc	\$A63CCF
dc	\$6BA65C
dc	\$E06D65
dc	\$1AA3A
dc	\$A1B6EB
dc	\$48AC48
dc	\$EF7AE1
dc	\$6E3006
dc	\$62F6C7
dc	\$6064F4
dc	\$87E41D
dc	\$CB2692
dc	\$2C3863
dc	\$C6BC60
dc	\$43A519
dc	\$6139DE
dc	\$ADF7BF
dc	\$4B3E8C
dc	\$6079D5
dc	\$E0F5EA
dc	\$8230DB
dc	\$A3B778
dc	\$2BFE51
dc	\$E0A6B6
dc	\$68FFB7
dc	\$28F324
dc	\$8F2E8D
dc	\$667842
dc	\$83E053
dc	\$A1FD90
dc dc	
	\$6B2689
dc	\$85B68E

dc

\$622EAF

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```
$6162BC
      dc
      dc
            $E4A245
YDAT END
           *******************
      EQUATES for DSP56301 I/O registers and ports
      Reference: DSP56301 Specifications Revision 3.00
;
      Last update:
                 November 15 1993
;
        Changes:
                  GPIO for ports C,D and E,
                  HI32
                  DMA status reg
                      PLL control reg
                  AAR
                  SCI registers address
                  SSI registers addr. + split TSR from SSISR
      December 19 1993 (cosmetic - page and opt directives)
            9 1994 ESSI and SCI control registers bit update
;
     *******************
      page 132,55,0,0,0
      opt
           mex
ioequ
     ident 1,0
      EQUATES for I/O Port Programming
  -----
      Register Addresses
M DATH EQU $FFFFCF; Host port GPIO data Register
M DIRH EQU $FFFFCE; Host port GPIO direction Register
M PCRC EQU $FFFFBF; Port C Control Register
M PRRC EQU $FFFFBE; Port C Direction Register
M PDRC EQU $FFFFBD ; Port C GPIO Data Register
M PCRD EQU $FFFFAF; Port D Control register
M_PRRD EQU $FFFFAE ; Port D Direction Data Register
M PDRD EQU $FFFFAD; Port D GPIO Data Register
M PCRE EQU $FFFF9F; Port E Control register
M PRRE EQU $FFFF9E; Port E Direction Register
M PDRE EQU $FFFF9D; Port E Data Register
M OGDB EQU $FFFFFC; OnCE GDB Register
;-----
    EOUATES for Host Interface
;-----
   Register Addresses
M DTXS EQU $FFFFCD; DSP SLAVE TRANSMIT DATA FIFO (DTXS)
M DTXM EQU $FFFFCC; DSP MASTER TRANSMIT DATA FIFO (DTXM)
M DRXR EQU $FFFFCB; DSP RECEIVE DATA FIFO (DRXR)
M DPSR EQU $FFFFCA; DSP PCI STATUS REGISTER (DPSR)
```



```
M DSR EQU $FFFFC9; DSP STATUS REGISTER (DSR)
M DPAR EQU $FFFFC8; DSP PCI ADDRESS REGISTER (DPAR)
M DPMC EQU $FFFFC7; DSP PCI MASTER CONTROL REGISTER (DPMC)
M DPCR EQU $FFFFC6; DSP PCI CONTROL REGISTER (DPCR)
M DCTR EQU $FFFFC5 ; DSP CONTROL REGISTER (DCTR)
        Host Control Register Bit Flags
M HCIE EOU 0 ; Host Command Interrupt Enable
M STIE EQU 1 ; Slave Transmit Interrupt Enable
M SRIE EQU 2 ; Slave Receive Interrupt Enable
M HF35 EQU $38 ; Host Flags 5-3 Mask
M HF3 EQU 3 ; Host Flag 3
             ; Host Flag 4
M HF4 EQU 4
M_HF5 EQU 5 ; Host Flag 5
M_HINT EQU 6 ; Host Interrupt A
M HDSM EQU 13 ; Host Data Strobe Mode
M HRWP EQU 14 ; Host RD/WR Polarity
M HTAP EQU 15 ; Host Transfer Acknowledge Polarity
M HDRP EQU 16 ; Host Dma Request Polarity
M HRSP EOU 17 ; Host Reset Polarity
M HIRP EQU 18 ; Host Interrupt Request Polarity
M HIRC EQU 19 ; Host Interupt Request Control
M HM0 EQU 20 ; Host Interface Mode
M HM1 EQU 21 ; Host Interface Mode
M HM2 EQU 22 ; Host Interface Mode
M HM EQU $700000 ; Host Interface Mode Mask
        Host PCI Control Register Bit Flags
M PMTIE EQU 1 ; PCI Master Transmit Interrupt Enable
M PMRIE EQU 2 ; PCI Master Receive Interrupt Enable
M PMAIE EQU 4 ; PCI Master Address Interrupt Enable
M PPEIE EQU 5 ; PCI Parity Error Interrupt Enable
M PTAIE EQU 7 ; PCI Transaction Abort Interrupt Enable
M PTTIE EQU 9 ; PCI Transaction Termination Interrupt Enable
M PTCIE EQU 12 ; PCI Transfer Complete Interrupt Enable
M CLRT EQU 14 ; Clear Transmitter
M_MTT EQU 15 ; Master Transfer Terminate
M SERF EQU 16 ; HSERR~ Force
M MACE EQU 18 ; Master Access Counter Enable
M MWSD EQU 19 ; Master Wait States Disable
M RBLE EQU 20 ; Receive Buffer Lock Enable
M IAE EQU 21 ; Insert Address Enable
        Host PCI Master Control Register Bit Flags
M ARH EQU $00ffff; DSP PCI Transaction Address (High)
M BL EQU $3f0000; PCI Data Burst Length
M FC EQU $c00000; Data Transfer Format Control
        Host PCI Address Register Bit Flags
M ARL EQU $00ffff; DSP PCI Transaction Address (Low)
M C EQU $0f0000; PCI Bus Command
M BE EQU $f00000; PCI Byte Enables
        DSP Status Register Bit Flags
M HCP EQU 0
            ; Host Command pending
```

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```
M STRQ EQU 1 ; Slave Transmit Data Request
M SRRQ EQU 2 ; Slave Receive Data Request
M HF02 EOU $38; Host Flag 0-2 Mask
M HF0 EOU 3
            ; Host Flag 0
              ; Host Flag 1
M HF1 EQU 4
            ; Host Flag 2
M HF2 EQU 5
       DSP PCI Status Register Bit Flags
M MWS EQU 0
             ; PCI Master Wait States
M MTRQ EQU 1 ; PCI Master Transmit Data Request
M MRRQ EQU 2
             ; PCI Master Receive Data Request
M MARQ EQU 4 ; PCI Master Address Request
              ; PCI Address Parity Error
M APER EQU 5
                ; PCI Data Parity Error
M DPER EOU 6
M MAB EQU 7
               ; PCI Master Abort
              ; PCI Target Abort
M TAB EQU 8
M_TDIS EQU 9 ; PCI Target Disconnect
M_TRTY EQU 10 ; PCI Target Retry
M TO EQU 11
              ; PCI Time Out Termination
M RDC EQU $3F0000; Remaining Data Count Mask (RDC5-RDC0)
M RDC0 EQU 16
              ; Remaining Data Count 0
               ; Remaining Data Count 1
M RDC1 EQU 17
               ; Remaining Data Count 2
M RDC2 EQU 18
               ; Remaining Data Count 3
M RDC3 EQU 19
               ; Remaining Data Count 4
M RDC4 EQU 20
              ; Remaining Data Count 5
M RDC5 EOU 21
M HACT EQU 23
               ; Hi32 Active
      ______
       EQUATES for Serial Communications Interface (SCI)
;
       Register Addresses
M STXH EQU $FFFF97; SCI Transmit Data Register (high)
M STXM EQU $FFFF96; SCI Transmit Data Register (middle)
M STXL EQU $FFFF95; SCI Transmit Data Register (low)
M SRXH EQU $FFFF9A; SCI Receive Data Register (high)
M SRXM EQU $FFFF99; SCI Receive Data Register (middle)
M SRXL EQU $FFFF98; SCI Receive Data Register (low)
M STXA EQU $FFFF94; SCI Transmit Address Register
M SCR EQU $FFFF9C; SCI Control Register
M SSR EQU $FFFF93; SCI Status Register
M SCCR EQU $FFFF9B; SCI Clock Control Register
       SCI Control Register Bit Flags
               ; Word Select Mask (WDS0-WDS3)
M WDS EQU $7
               ; Word Select 0
M WDS0 EQU 0
M WDS1 EQU 1
                ; Word Select 1
               ; Word Select 2
M WDS2 EQU 2
M SSFTD EQU 3
                 ; SCI Shift Direction
                ; Send Break
M SBK EOU 4
M WAKE EQU 5
                ; Wakeup Mode Select
M RWU EQU 6
               ; Receiver Wakeup Enable
M WOMS EQU 7
                ; Wired-OR Mode Select
```



```
M SCRE EQU 8
                ; SCI Receiver Enable
               ; SCI Transmitter Enable
M SCTE EQU 9
               ; Idle Line Interrupt Enable
M ILIE EOU 10
               ; SCI Receive Interrupt Enable
M SCRIE EOU 11
M SCTIE EQU 12
                ; SCI Transmit Interrupt Enable
M TMIE EQU 13 ; Timer Interrupt Enable
M TIR EQU 14 ; Timer Interrupt Rate
M SCKP EQU 15 ; SCI Clock Polarity
M REIE EQU 16 ; SCI Error Interrupt Enable (REIE)
       SCI Status Register Bit Flags
                ; Transmitter Empty
M TRNE EQU 0
               ; Transmit Data Register Empty
M TDRE EQU 1
               ; Receive Data Register Full
M RDRF EOU 2
               ; Idle Line Flag
M IDLE EQU 3
M OR EQU 4
            ; Overrun Error Flag
M PE EOU 5
             ; Parity Error
M FE EQU 6
             ; Framing Error Flag
M R8 EQU 7
              ; Received Bit 8 (R8) Address
       SCI Clock Control Register
M CD EQU $FFF
              ; Clock Divider Mask (CD0-CD11)
              ; Clock Out Divider
M COD EQU 12
               ; Clock Prescaler
M SCP EQU 13
              ; Receive Clock Mode Source Bit
M RCM EOU 14
              ; Transmit Clock Source Bit
M TCM EQU 15
;-----
      EQUATES for Synchronous Serial Interface (SSI)
;
       Register Addresses Of SSIO
M TX00 EQU $FFFFBC; SSI0 Transmit Data Register 0
M TX01 EQU $FFFFBB; SSIO Transmit Data Register 1
M TX02 EQU $FFFFBA; SSIO Transmit Data Register 2
M TSRO EQU $FFFFB9; SSIO Time Slot Register
M RX0 EQU $FFFFB8; SSI0 Receive Data Register
M SSISRO EQU $FFFFB7; SSIO Status Register
M CRBO EQU $FFFFB6; SSIO Control Register B
M CRAO EQU $FFFFB5; SSIO Control Register A
M TSMAO EQU $FFFFB4; SSIO Transmit Slot Mask Register A
M TSMB0 EQU $FFFFB3; SSI0 Transmit Slot Mask Register B
M RSMAO EQU $FFFFB2; SSIO Receive Slot Mask Register A
M RSMBO EQU $FFFFB1; SSIO Receive Slot Mask Register B
       Register Addresses Of SSI1
M TX10 EQU $FFFFAC; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB; SSI1 Transmit Data Register 1
M TX12 EQU $FFFFAA; SSI1 Transmit Data Register 2
M TSR1 EQU $FFFFA9; SSI1 Time Slot Register
M RX1 EQU $FFFFA8; SSI1 Receive Data Register
M SSISR1 EQU $FFFFA7; SSI1 Status Register
M CRB1 EQU $FFFFA6; SSI1 Control Register B
M CRA1 EQU $FFFFA5; SSI1 Control Register A
M TSMA1 EQU $FFFFA4; SSI1 Transmit Slot Mask Register A
```

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```
M TSMB1 EQU $FFFFA3; SSI1 Transmit Slot Mask Register B
M RSMA1 EQU $FFFFA2; SSI1 Receive Slot Mask Register A
M RSMB1 EQU $FFFFA1; SSI1 Receive Slot Mask Register B
        SSI Control Register A Bit Flags
                ; Prescale Modulus Select Mask (PMO-PM7)
M PM EQU $FF
M PSR EQU 11
                ; Prescaler Range
M DC EQU $1F000 ; Frame Rate Divider Control Mask (DC0-DC7)
M ALC EQU 18
             ; Alignment Control (ALC)
M WL EQU $380000; Word Length Control Mask (WLO-WL7)
M SSC1 EQU 22 ; Select SC1 as TR #0 drive enable (SSC1)
        SSI Control Register B Bit Flags
M OF EQU $3
              ; Serial Output Flag Mask
M OFO EQU 0
             ; Serial Output Flag 0
M OF1 EQU 1
            ; Serial Output Flag 1
M SCD EQU $1C ; Serial Control Direction Mask
M SCD0 EQU 2 ; Serial Control 0 Direction
              ; Serial Control 1 Direction
M SCD1 EOU 3
M SCD2 EQU 4
                ; Serial Control 2 Direction
              ; Clock Source Direction
; Shift Direction
M SCKD EQU 5
M SHFD EQU 6
M FSL EQU $180; Frame Sync Length Mask (FSL0-FSL1)
M FSL0 EQU 7 ; Frame Sync Length 0
M_FSL1 EQU 8 ; Frame Sync Length 1
M_FSR EQU 9 ; Frame Sync Relative Timing
M FSP EQU 10 ; Frame Sync Polarity
M CKP EQU 11 ; Clock Polarity
M_SYN EQU 12 ; Sync/Async Control
M MOD EQU 13 ; SSI Mode Select
M SSTE EOU $1C000; SSI Transmit enable Mask
M SSTE2 EQU 14; SSI Transmit #2 Enable
M SSTE1 EQU 15 ; SSI Transmit #1 Enable
M SSTE0 EQU 16; SSI Transmit #0 Enable
M SSRE EQU 17 ; SSI Receive Enable
M SSTIE EQU 18; SSI Transmit Interrupt Enable
M SSRIE EQU 19; SSI Receive Interrupt Enable
M STLIE EQU 20; SSI Transmit Last Slot Interrupt Enable
M SRLIE EQU 21; SSI Receive Last Slot Interrupt Enable
M STEIE EQU 22; SSI Transmit Error Interrupt Enable
M SREIE EQU 23 ; SSI Receive Error Interrupt Enable
        SSI Status Register Bit Flags
M IF EQU $3
                ; Serial Input Flag Mask
              ; Serial Input Flag 0
M IFO EQU 0
                ; Serial Input Flag 1
M IF1 EQU 1
                ; Transmit Frame Sync Flag
M TFS EOU 2
M RFS EQU 3
                ; Receive Frame Sync Flag
M TUE EQU 4
                ; Transmitter Underrun Error FLag
M ROE EQU 5
                ; Receiver Overrun Error Flag
M TDE EQU 6
                ; Transmit Data Register Empty
M RDF EQU 7
                 ; Receive Data Register Full
        SSI Transmit Slot Mask Register A
M SSTSA EQU $FFFF ; SSI Transmit Slot Bits Mask A (TSO-TS15)
```



```
SSI Transmit Slot Mask Register B
;
M SSTSB EQU $FFFF ; SSI Transmit Slot Bits Mask B (TS16-TS31)
        SSI Receive Slot Mask Register A
M SSRSA EQU $FFFF ; SSI Receive Slot Bits Mask A (RSO-RS15)
        SSI Receive Slot Mask Register B
M SSRSB EQU $FFFF ; SSI Receive Slot Bits Mask B (RS16-RS31)
        EQUATES for Exception Processing
        Register Addresses
M IPRC EQU $FFFFFF; Interrupt Priority Register Core
M IPRP EQU $FFFFFE; Interrupt Priority Register Peripheral
        Interrupt Priority Register Core (IPRC)
M IAL EQU $7
               ; IRQA Mode Mask
                ; IRQA Mode Interrupt Priority Level (low)
M IALO EQU 0
                ; IRQA Mode Interrupt Priority Level (high)
M IAL1 EQU 1
M IAL2 EOU 2
                ; IRQA Mode Trigger Mode
M IBL EQU $38 ; IRQB Mode Mask
                ; IRQB Mode Interrupt Priority Level (low)
M IBLO EQU 3
                ; IRQB Mode Interrupt Priority Level (high)
M IBL1 EQU 4
                ; IRQB Mode Trigger Mode
M IBL2 EQU 5
M_ICL EQU $1C0 ; IRQC Mode Mask
               ; IRQC Mode Interrupt Priority Level (low)
M ICLO EOU 6
                ; IRQC Mode Interrupt Priority Level (high)
M ICL1 EQU 7
M ICL2 EQU 8
                ; IRQC Mode Trigger Mode
M IDL EQU $E00 ; IRQD Mode Mask
               ; IRQD Mode Interrupt Priority Level (low)
M IDLO EQU 9
M IDL1 EQU 10 ; IRQD Mode Interrupt Priority Level (high)
M IDL2 EQU 11 ; IRQD Mode Trigger Mode
M DOL EQU $3000 ; DMAO Interrupt priority Level Mask
              ; DMAO Interrupt Priority Level (low)
M DOLO EQU 12
M DOL1 EQU 13
                 ; DMA0 Interrupt Priority Level (high)
M D1L EQU $C000 ; DMA1 Interrupt Priority Level Mask
               ; DMA1 Interrupt Priority Level (low)
; DMA1 Interrupt Priority Level (high)
M D1L0 EQU 14
M D1L1 EQU 15
M D2L EQU $30000 ; DMA2 Interrupt priority Level Mask
M_D2L0 EQU 16 ; DMA2 Interrupt Priority Level (low)
M D2L1 EQU 17
                ; DMA2 Interrupt Priority Level (high)
M D3L EQU $C0000; DMA3 Interrupt Priority Level Mask
              ; DMA3 Interrupt Priority Level (low)
M D3L0 EQU 18
                ; DMA3 Interrupt Priority Level (high)
M D3L1 EOU 19
M D4L EQU $300000; DMA4 Interrupt priority Level Mask
M D4L0 EQU 20 ; DMA4 Interrupt Priority Level (low)
M D4L1 EQU 21
                 ; DMA4 Interrupt Priority Level (high)
```

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```
M D5L EQU $C00000; DMA5 Interrupt priority Level Mask
M D5L0 EQU 22 ; DMA5 Interrupt Priority Level (low)
M D5L1 EOU 23
               ; DMA5 Interrupt Priority Level (high)
       Interrupt Priority Register Peripheral (IPRP)
M HPL EQU $3
              ; Host Interrupt Priority Level Mask
               ; Host Interrupt Priority Level (low)
M HPLO EOU 0
M HPL1 EQU 1
               ; Host Interrupt Priority Level (high)
               ; SSIO Interrupt Priority Level Mask
M SOL EQU $C
              ; SSIO Interrupt Priority Level (low)
M SOLO EQU 2
M SOL1 EQU 3
               ; SSIO Interrupt Priority Level (high)
              ; SSI1 Interrupt Priority Level Mask
M S1L EQU $30
             ; SSI1 Interrupt Priority Level (low)
M S1L0 EOU 4
               ; SSI1 Interrupt Priority Level (high)
M S1L1 EQU 5
M SCL EQU $CO ; SCI Interrupt Priority Level Mask
              ; SCI Interrupt Priority Level (low)
; SCI Interrupt Priority Level (high)
M SCLO EQU 6
M SCL1 EQU 7
M TOL EQU $300 ; TIMER Interrupt Priority Level Mask
               ; TIMER Interrupt Priority Level (low)
M TOLO EOU 8
M TOL1 EQU 9
               ; TIMER Interrupt Priority Level (high)
;-----
       EQUATES for TIMER
;-----
       Register Addresses Of TIMERO
M TCSR0 EQU $FFFF8F; TIMER0 Control/Status Register
M TLRO EQU $FFFF8E; TIMERO Load Reg
M_TCPR0 EQU $FFFF8D; TIMER0 Compare Register
M TCRO EQU $FFFF8C; TIMERO Count Register
       Register Addresses Of TIMER1
M TCSR1 EQU $FFFF8B; TIMER1 Control/Status Register
M TLR1 EQU $FFFF8A; TIMER1 Load Reg
M TCPR1 EQU $FFFF89; TIMER1 Compare Register
M TCR1 EQU $FFFF88; TIMER1 Count Register
       Register Addresses Of TIMER2
M TCSR2 EQU $FFFF87; TIMER2 Control/Status Register
M TLR2 EQU $FFFF8; TIMER2 Load Reg
M TCPR2 EQU $FFFF85; TIMER2 Compare Register
M TCR2 EQU $FFFF84 ; TIMER2 Count Register
M TPLR EQU $FFFF83 ; TIMER Prescaler Load Register
M TPCR EQU $FFFF82; TIMER Prescalar Count Register
       Timer Control/Status Register Bit Flags
              ; Timer Enable
M TE EQU 0
              ; Timer Overflow Interrupt Enable
M TOIE EQU 1
                ; Timer Compare Interrupt Enable
M TCIE EQU 2
```

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```
; Timer Control Mask (TC0-TC3)
M TC EQU $F0
; Timer Restart Mode
M_DIR EQU 11 ; Direction Bit
M_DI EQU 12 ; Data Input
M_DO EQU 13 ; Data Output
M PCE EQU 15 ; Prescaled Clock Enable
{\tt M\_TOF} EQU 20 ; Timer Overflow Flag
M TCF EQU 21
               ; Timer Compare Flag
       Timer Prescaler Register Bit Flags
M PS EQU $600000 ; Prescaler Source Mask
M PS0 EQU 21
M PS1 EQU 22
      Timer Control Bits
M_TC0 EQU 4 ; Timer Control 0
M_TC1 EQU 5 ; Timer Control 1
M_TC2 EQU 6 ; Timer Control 2
M_TC3 EQU 7 ; Timer Control 3
;-----
;
       EQUATES for Direct Memory Access (DMA)
       Register Addresses Of DMA
M DSTR EQU $FFFFF4; DMA Status Register
M DORO EQU $FFFFF3; DMA Offset Register 0
M DOR1 EQU $FFFFF2; DMA Offset Register 1
M DOR2 EQU $FFFFF1; DMA Offset Register 2
M DOR3 EQU $FFFFF0; DMA Offset Register 3
       Register Addresses Of DMA0
M DSR0 EQU $FFFFEF; DMA0 Source Address Register
M DDR0 EQU $FFFFEE; DMA0 Destination Address Register
M DCOO EQU $FFFFED; DMAO Counter
M DCR0 EQU $FFFFEC; DMA0 Control Register
       Register Addresses Of DMA1
M DSR1 EQU $FFFFEB; DMA1 Source Address Register
M DDR1 EQU $FFFFEA; DMA1 Destination Address Register
M DCO1 EQU $FFFFE9; DMA1 Counter
M DCR1 EQU $FFFFE8; DMA1 Control Register
       Register Addresses Of DMA2
M DSR2 EQU $FFFFE7; DMA2 Source Address Register
M DDR2 EQU $FFFFE6; DMA2 Destination Address Register
M DCO2 EQU $FFFFE5; DMA2 Counter
M DCR2 EQU $FFFFE4; DMA2 Control Register
       Register Addresses Of DMA4
```

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```
M DSR3 EQU $FFFFE3; DMA3 Source Address Register
M DDR3 EQU $FFFFE2; DMA3 Destination Address Register
M DCO3 EQU $FFFFE1; DMA3 Counter
M DCR3 EQU $FFFFE0; DMA3 Control Register
        Register Addresses Of DMA4
M DSR4 EQU $FFFFDF; DMA4 Source Address Register
M DDR4 EQU $FFFFDE; DMA4 Destination Address Register
M DCO4 EQU $FFFFDD; DMA4 Counter
M DCR4 EQU $FFFFDC; DMA4 Control Register
        Register Addresses Of DMA5
M DSR5 EQU $FFFFDB; DMA5 Source Address Register
M DDR5 EQU $FFFFDA; DMA5 Destination Address Register
M DCO5 EQU $FFFFD9; DMA5 Counter
M DCR5 EQU $FFFFD8; DMA5 Control Register
       DMA Control Register
M DSS EQU $3 ; DMA Source Space Mask (DSS0-Dss1)
M DSS0 EQU 0 ; DMA Source Memory space 0
M DSS1 EQU 1 ; DMA Source Memory space 1
M_DDS EQU $C ; DMA Destination Space Mask (DDS-DDS1)
M_DDS0 EQU 2 ; DMA Destination Memory Space 0 M_DDS1 EQU 3 ; DMA Destination Memory Space 1
M DAM EQU $3F0; DMA Address Mode Mask (DAM5-DAM0)
M_DAMO EQU 4 ; DMA Address Mode 0
M DAM1 EQU 5 ; DMA Address Mode 1
M DAM2 EQU 6 ; DMA Address Mode 2
M DAM3 EOU 7 ; DMA Address Mode 3
M DAM4 EQU 8 ; DMA Address Mode 4
M DAM5 EQU 9 ; DMA Address Mode 5
M D3D EQU 10 ; DMA Three Dimensional Mode
M DRS EQU $F800; DMA Request Source Mask (DRS0-DRS4)
M DCON EQU 16 ; DMA Continuous Mode
M DPR EQU $60000; DMA Channel Priority
M DPR0 EQU 17 ; DMA Channel Priority Level (low)
M DPR1 EQU 18 ; DMA Channel Priority Level (high)
M DTM EQU $380000; DMA Transfer Mode Mask (DTM2-DTM0)
M DTMO EQU 19 ; DMA Transfer Mode 0
M DTM1 EQU 20 ; DMA Transfer Mode 1
M DTM2 EQU 21 ; DMA Transfer Mode 2
M DIE EQU 22 ; DMA Interrupt Enable bit
              ; DMA Channel Enable bit
M DE EQU 23
        DMA Status Register
M_DTD EQU $3F ; Channel Transfer Done Status MASK (DTD0-DTD5)
              ; DMA Channel Transfer Done Status 0
M DTD0 EOU 0
M DTD1 EQU 1
                 ; DMA Channel Transfer Done Status 1
M DTD2 EQU 2
                 ; DMA Channel Transfer Done Status 2
M DTD3 EQU 3
                 ; DMA Channel Transfer Done Status 3
                ; DMA Channel Transfer Done Status 4
M DTD4 EQU 4
                 ; DMA Channel Transfer Done Status 5
M DTD5 EOU 5
M DACT EQU 8 ; DMA Active State
M DCH EQU $E00; DMA Active Channel Mask (DCH0-DCH2)
M DCHO EQU 9 ; DMA Active Channel 0
```



```
M DCH1 EQU 10 ; DMA Active Channel 1
M DCH2 EQU 11 ; DMA Active Channel 2
;-----
      EQUATES for Phase Lock Loop (PLL)
;------
      Register Addresses Of PLL
M PCTL EQU $FFFFFD; PLL Control Register
      PLL Control Register
M MF EQU $FFF ; Multiplication Factor Bits Mask (MF0-MF11)
M_DF EQU $7000 ; Division Factor Bits Mask (DF0-DF2)
M\_XTLR EQU 15 ; XTAL Range select bit
M XTLD EQU 16 ; XTAL Disable Bit
M PSTP EQU 17 ; STOP Processing State Bit
M PEN EQU 18
             ; PLL Enable Bit
M PCOD EQU 19 ; PLL Clock Output Disable Bit
M PD EQU $F00000; PreDivider Factor Bits Mask (PD0-PD3)
:-----
      EQUATES for BIU
;-----
      Register Addresses Of BIU
M BCR EQU $FFFFFB; Bus Control Register
M DCR EQU $FFFFFA; DRAM Control Register
M AARO EQU $FFFFF9; Address Attribute Register 0
M AAR1 EQU $FFFFF8; Address Attribute Register 1
M AAR2 EQU $FFFFF7; Address Attribute Register 2
M AAR3 EQU $FFFFF6; Address Attribute Register 3
M IDR EQU $FFFFF5; ID Register
      Bus Control Register
M BAOW EQU $1F ; Area 0 Wait Control Mask (BAOW0-BAOW4)
M BA1W EQU $3E0 ; Area 1 Wait Control Mask (BA1W0-BA14)
M BA2W EQU $1C00 ; Area 2 Wait Control Mask (BA2W0-BA2W2)
M BA3W EQU $E000 ; Area 3 Wait Control Mask (BA3W0-BA3W3)
M BDFW EQU $1F0000; Default Area Wait Control Mask (BDFW0-BDFW4)
M_BBS EQU 21 ; Bus State
             ; Bus Lock Hold
M BLH EQU 22
M_BRH EQU 23 ; Bus Request Hold
      DRAM Control Register
             ; In Page Wait States Bits Mask (BCW0-BCW1)
M BCW EOU $3
              ; Out Of Page Wait States Bits Mask (BRWO-BRW1)
M BRW EQU $C
M_BPS EQU $300 ; DRAM Page Size Bits Mask (BPS0-BPS1)
M BPLE EQU 11
              ; Page Logic Enable
```

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```
M BME EQU 12
                ; Mastership Enable
                ; Refresh Enable
M BRE EQU 13
                ; Software Triggered Refresh
M BSTR EOU 14
M BRF EQU $7F8000; Refresh Rate Bits Mask (BRF0-BRF7)
                ; Refresh prescaler
M BRP EQU 23
        Address Attribute Registers
M BAT EOU $3
                ; External Access Type and Pin Definition Bits Mask (BATO-BAT1)
M BAAP EOU 2
                ; Address Attribute Pin Polarity
M BPEN EQU 3
                 ; Program Space Enable
M BXEN EQU 4
                 ; X Data Space Enable
                 ; Y Data Space Enable
M BYEN EQU 5
M BAM EQU 6
                ; Address Muxing
M_BPAC EQU 7 ; Packing Enable
M BNC EQU $F00 ; Number of Address Bits to Compare Mask (BNC0-BNC3)
M BAC EQU $FFF000; Address to Compare Bits Mask (BAC0-BAC11)
        control and status bits in SR
M CP EQU $c00000 ; mask for CORE-DMA priority bits in SR
M CA EQU 0
               ; Carry
M V EQU 1
               ; Overflow
M Z EQU 2
               ; Zero
              ; Negative
M N EQU 3
              ; Unnormalized
M U EQU 4
              ; Extension
M E EOU 5
M L EQU 6
              ; Limit
              ; Scaling Bit
M S EQU 7
               ; Interupt Mask Bit 0
M IO EQU 8
               ; Interupt Mask Bit 1
M I1 EQU 9
M SO EQU 10
               ; Scaling Mode Bit 0
               ; Scaling Mode Bit 1
M S1 EOU 11
M SC EQU 13
                ; Sixteen Bit Compatibility
M DM EQU 14
                ; Double Precision Multiply
M LF EQU 15
                ; DO-Loop Flag
                ; DO-Forever Flag
M FV EQU 16
               ; Sixteen-Bit Arithmetic
M SA EQU 17
               ; Instruction Cache Enable
M CE EOU 19
M SM EQU 20
                ; Arithmetic Saturation
M RM EQU 21
                ; Rounding Mode
M CP0 EQU22
                ; bit 0 of priority bits in SR
M CP1 EQU 23
                ; bit 1 of priority bits in SR
        control and status bits in OMR
M CDP EQU$300 ; mask for CORE-DMA priority bits in OMR
M MA EQU 0
                ; Operating Mode A
M MB EQU 1
                ; Operating Mode B
                ; Operating Mode C
M MC EQU 2
                ; Operating Mode D
M MD EQU 3
                ; External Bus Disable bit in OMR
M EBD EOU 4
M SD EQU 6
                ; Stop Delay
M CDP0 EQU 8
                 ; bit 0 of priority bits in OMR
M CDP1 EQU 9
                 ; bit 1 of priority bits in OMR
M BEN EQU 10
                ; Burst Enable
                ; TA Synchronize Select
M TAS EQU 11
M BRT EOU 12
                ; Bus Release Timing
M XYS EQU 16
                ; Stack Extension space select bit in OMR.
M EUN EQU 17
                 ; Extensed stack UNderflow flag in OMR.
M EOV EQU 18
                 ; Extended stack OVerflow flag in OMR.
```



```
M WRP EQU 19
            ; Extended WRaP flag in OMR.
M SEN EOU 20
           ; Stack Extension Enable bit in OMR.
;***********************************
    EQUATES for DSP56301 interrupts
    Reference: DSP56301 Specifications Revision 3.00
    Last update: November 15 1993 (Debug request & HI32 interrupts)
            December 19 1993 (cosmetic - page and opt directives)
          August 16 1994 (change interrupt addresses to be
;
              relative to I VEC)
132,55,0,0,0
     page
     opt
          mex
intequ ident 1,0
     if
        @DEF(I VEC)
     ; leave user definition as is.
I VEC equ
          $0
     endif
; Non-Maskable interrupts
;-----
I RESET EQU I VEC+$00 ; Hardware RESET
I STACK EQU I_VEC+$02 ; Stack Error
I ILL EQU I VEC+$04 ; Illegal Instruction
I DBG EQU I VEC+$06 ; Debug Request
I TRAP EQU I VEC+$08 ; Trap
I NMI EQU I VEC+$0A ; Non Maskable Interrupt
;-----
; Interrupt Request Pins
;------
I_IRQA EQU I_VEC+$10 ; IRQA
I_IRQB EQU I_VEC+$12 ; IRQB
I_IRQC EQU I_VEC+$14 ; IRQC
I IRQD EQU I VEC+$16 ; IRQD
;-----
; DMA Interrupts
;-----
I DMAO EQU I VEC+$18 ; DMA Channel 0
I_DMA1 EQU I_VEC+$1A ; DMA Channel 1
I_DMA2 EQU I_VEC+$1C ; DMA Channel 2
I_DMA3 EQU I_VEC+$1E ; DMA Channel 3
I DMA4
     EQU I_VEC+$20 ; DMA Channel 4
I DMA5
     EQU I VEC+$22 ; DMA Channel 5
;------
; Timer Interrupts
;-----
I TIMOC EQU I VEC+$24 ; TIMER 0 compare
I TIMOOF EQU I VEC+$26 ; TIMER 0 overflow
```

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```
I TIM1C EQU I VEC+$28
                   ; TIMER 1 compare
I_TIM1OF EQU I_VEC+$2A ; TIMER 1 overflow
\label{eq:compare}  \mbox{I\_TIM2C} \ \ \mbox{EQU} \ \ \mbox{I\_VEC+$2C} \ \ ; \ \mbox{TIMER} \ \mbox{2 compare}
                  ; TIMER 2 overflow
I TIM2OF EQU I VEC+$2E
;-----
; ESSI Interrupts
;-----
I SIORD EQU I VEC+$30 ; ESSIO Receive Data
I SIORDE EQU I VEC+$32 ; ESSIO Receive Data With Exception Status
I SIORLS EQU I VEC+$34 ; ESSIO Receive last slot
I SIOTD EQU I VEC+$36 ; ESSIO Transmit data
I_SIOTLS EQU I_VEC+$3A ; ESSIO Transmit last slot
<code>I_SI1RD</code> EQU <code>I_VEC+$40</code> ; ESSI1 Receive Data
I_SI1RDE EQU I_VEC+$42 ; ESSI1 Receive Data With Exception Status
<code>I_SI1RLS EQU I_VEC+$44</code> ; <code>ESSI1 Receive last slot</code>
I_SI1TD EQU I_VEC+$46 ; ESSI1 Transmit data
<code>I_SI1TDE EQU I_VEC+$48</code> ; <code>ESSI1 Transmit Data With Exception Status</code>
I SI1TLS EQU I VEC+$4A ; ESSI1 Transmit last slot
;-----
; SCI Interrupts
;-----
I SCIRD EQU I VEC+$50 ; SCI Receive Data
<code>I_SCIRDE EQU I_VEC+$52</code> ; SCI Receive Data With Exception Status
I_SCITD EQU I_VEC+$54 ; SCI Transmit Data
I_SCIIL EQU I_VEC+$56 ; SCI Idle Line
I SCITM EQU I VEC+$58 ; SCI Timer
;-----
; HOST Interrupts
;-----
I HPTT EQU I VEC+$60 ; Host PCI Transaction Termination
I HPTA EQU I VEC+$62 ; Host PCI Transaction Abort
I HPPE EQU I VEC+$64
                  ; Host PCI Parity Error
I_HPTC EQU I_VEC+$66 ; Host PCI Transfer Complete
I_HPMR EQU I_VEC+$68 ; Host PCI Master Receive
      EQU I_VEC+$6A ; Host Slave Receive
I HSR
I_HPMT EQU I_VEC+$6C ; Host PCI Master Transmit
      EQU I_VEC+$6E ; Host Slave Transmit
I HST
I HPMA EQU I_VEC+$70 ; Host PCI Master Address
I_HCNMI EQU I_VEC+$72 ; Host Command/Host NMI (Default)
;-----
: INTERRUPT ENDING ADDRESS
;-----
```

I INTEND EQU I\_VEC+\$FF  $\,\,$  ; last address of interrupt vector space

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## **Ordering Information**

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Supply Voltage	Package Type	Pin Count	Core Frequency (MHz)	Solder Spheres	Order Number
DSP56301 3.3 V	3.3 V	Thin Quad Flat Pack (TQFP)	208	80	Lead-free	DSP56301AG80
					Lead-bearing	DSP56301PW80
				100	Lead-free	DSP56301AG100
					Lead-bearing	DSP56301PW100
		Molded Array Process-Ball Grid	252	80	Lead-free	DSP56301VL80
	Array (MAP-BGA)			Lead-bearing	DSP56301VF80	
				100	Lead-free	DSP56301VL100
					Lead-bearing	DSP56301VF100

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