컴퓨터구조 Assignment-5

1. (cf) Exercise 5.10

As described in Section 5.4, virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. This exercise shows how this table must be updated as addresses are accessed. The [Table 1] is a stream of virtual addresses as seen on a system. If pages must be brought in from disk when all the page frames are in use, replace the virtual page with the smallest virtual page number. (All addresses are in Hexadecimal, but tags and page numbers are in Decimal. 답의 모든 tag와 page number는 십진수로 표기할 것. TLB(H/M)에서 Miss는 표시하지 말고 Hit일 때만 H로 표시하고, Page fault(Y/N)도 Yes는 표시하지 말고 No일 때만 N으로 표시하라.)

[Table 1] Reference strings

a.	9E30, FA00, 5580, A368, 2220, 5FC0, 73F0
b.	6C00, BBB8, AA00, 4720, D0D0, 3000, 6EB0

1.1 Given the address stream in [Table 1], and the shown initial state of the TLB (Table 2) and page table (Table 3), show the final state of the TLB and page table. Also fill up [Table 4] for each reference. Assume a four-entry fully associative TLB, true LRU replacement for TLB (초기상태에서는 Tag 15가 사용한지 가장 오래된 것, Tag 10이 그 다음 오래된 것), and 4 KB pages. (표 하나당 1점 x 6 = 6점)

[Table 2] TLB

Valid	Tag	Physical Page Number
1	15	2
1	10	7
1	2	6
0		

[Table 3] Page table

	Valid	Physical Page Number
0	1	4
1	0	
2	1	6
3	1	5
4	1	0
5	0	
6	0	
7	0	
8	0	
9	1	1
10	1	7
11	0	
12	0	
13	0	
14	1	3
15	1	2

1.2 Show the final contents of the TLB if it is two-way set-associative with LRU replacement policy. Also show the contents of the TLB if it is direct-mapped. Assume initially empty TLB and 4 KB pages. 2-way에서 한 set의 두 block이 모두 비어 있으면 왼쪽부터 채울 것. (표 하나 당 1점 x 4 = 4점)

1.3 Given the address stream in [Table 1], and the shown initial state of the TLB (Table 5) and page table (Table 6), show the final state of the TLB and page table. Also fill up [Table 7] for each reference. Assume a two-entry fully associative TLB, true LRU replacement for TLB, and 8 KB pages. (표 하나 당 1점 x 6 = 6점)

[Table 5] TLB

Valid	Tag	Physical Page Number
0		
1	2	2

[Table 6] Page table

	Valid	Physical Page Number
0	0	
1	1	1
2	1	2
3	0	
4	1	0
5	1	3
6	0	
7	0	

There are several parameters that impact the overall size of the page table. Listed below are several key page table parameters.

	Virtual address size	Physical address size	Page size	Page table entry size
a.	32 bits	28 bits	8 KB	4 bytes
b.	40 bits	37 bits	8 KB	4 bytes

1.4 Given the parameters in the table above, calculate the total page table size for a system running 16 applications. (1점 x 2 = 2점)

컴퓨터구조 Assignment-5

수강반 ( ), 학번 ( ), 이름 ( )

(이것을 인쇄한 후 답을 여기에 쓰고, 이것만 제출할 것.)

1.1

[Table 4]

(a)

Address	Virtual page number	TLB (H/M)	Page fault (Y/N)	Physical page number
9E30				
FA00				
5580				
A368				
2220				
5FC0				
73F0				

(b)

Address	Virtual page number	TLB (H/M)	Page fault (Y/N)	Physical page number
6C00				
BBB8				
AA00				
4720				
D0D0				
3000				
6EB0				

Final TLBs

Valid	Tag	Physical Page Number

Valid	Tag	Physical Page Number

Final page tables

	Valid	Physical Page Number	Valid	Physical Page Number
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

1.2

Final TLBs (2-way)

(a) (b)

	V	T	PPN	V	T	PPN	V	T	PPN	V	T	PPN
Set 0												
Set 1												

Final TLBs (Direct)

(a) (b)

	V	T	PPN	V	T	PPN
0						
1						
2						
3						

1.3

[Table 7]

(a)

Address	Virtual page number	TLB (H/M)	Page fault (Y/N)	Physical page number
9E30				
FA00				
5580				
A368				
2220				
5FC0				
73F0				

(b)

Address	Virtual page number	TLB (H/M)	Page fault (Y/N)	Physical page number
6C00				
BBB8				
AA00				
4720				
D0D0				
3000				
6EB0				

Final TLBs

Valid	Tag	Physical Page Number

Valid	Tag	Physical Page Number

Final page tables

	Valid	Physical Page Number
0		
1		
2		
3		
4		
5		
6		
7		

Valid	Physical Page Number

1.4

(a)

(b)