Assignment 1: Lab Report on Self-Learning of the Cadence Virtuoso Design Tool

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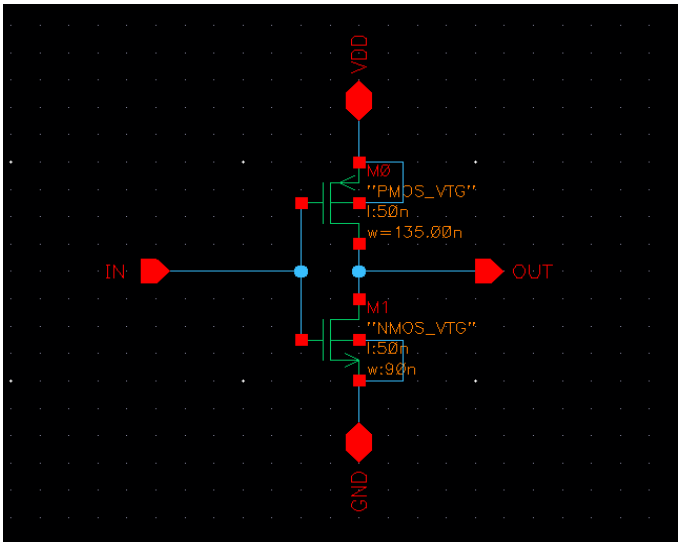
Academic Year 2018-2019

I. Introduction

In this report the procedure of designing and verifying a design for a 1-input 1-output inverter is described. Detailed schematics and layout of the inverter are presented along with the different schematics of experimental setup to test the performance of the schematic and the layout. Procedure of layout, its verification and parasitic extraction are also mentioned. Transient analysis to figure out the the propagation delay, rise and fall time of the signal on various loads are carried out. In the end, some tricks and pitfalls are described so that they can be avoided in the future by a reader of this report. Some conclusions and learnings are described in the end.

II. Lab Procedure

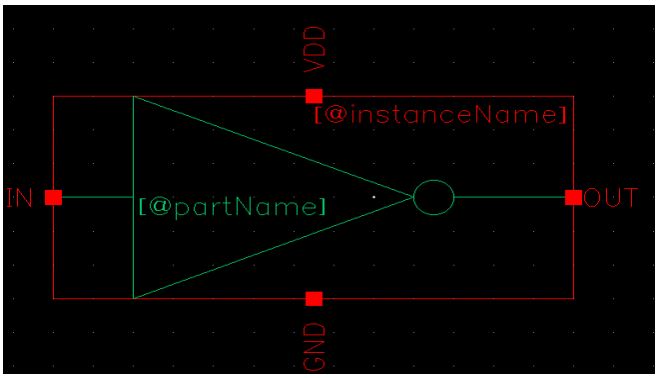
A. Schematic of the Inverter



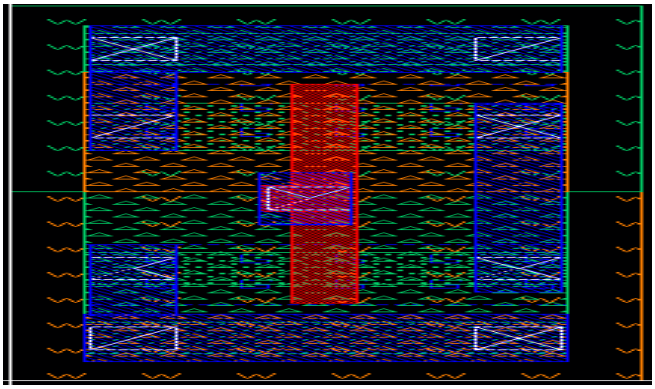
The schematic is designed in the schematic cellview. The schematic described the design the minimum sized Inverter is designed with NMOS of width 90 nanometer and PMOS of width 135 nanometer. Minimum length prescribed for both the transistors is 50 nanometer.

B. Symbol of the Inverter

Symbol for the inverter is defined with pins matching the schematic diagram of the inverter such the IN, OUT, VDD, GND pins.



C. Layout of the Inverter



The layout of thei nverter is designed under the layout cellview of the schematic. The design is done at the nanometer scale keeping in line with the dimensions mentioned in the schematic. The PMOS is 135 nanometer wide and NMOS is 90 nanometer wide. Layers such as Active, Polysilicon, N-Implant, P-Implant, VTG, Metal, Contact, N-Well and P-Well are used to design a real CMOS Inverter.

D. Design Rule Check

nmDRC i.e the Design Rule Check is applied in Calibre to ensure all minimum spacing and width issues recommended by the FreePDK45Guide are followed. The designed layout cleared all the tests.

E. Logic Versus Schematic

The nmLVS-Logic versus Schematic check of Calibre performs the logic comparision of the design mentioned in the schematic and in the layout. All the inputs, outputs, power and ground pins are compared and their logic behavior is evaluated. The designed layout cleared the LVS test.

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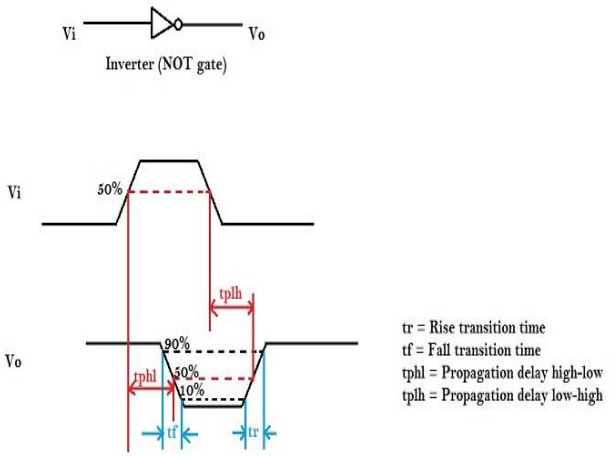
F. Parisitic Extraction

The nmPEX- Parasitic Extraction stage helps in extracting the parasitic capacitances and resistances of the designed layout. These are present because of different conducting, semi-conducting and non-conducting materials present in the layout design. A calibre parasitic resistance and capacitance view is generated at the end of this test as shown below.

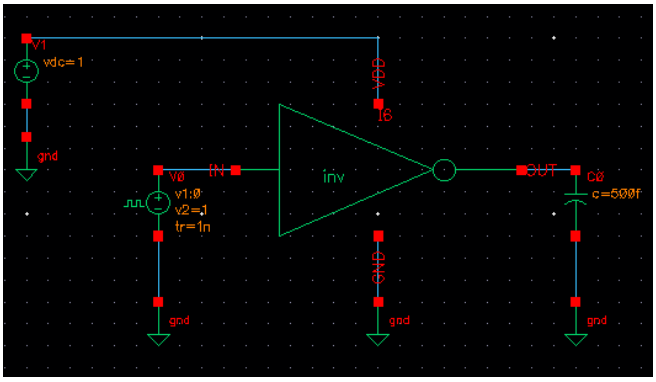
III. TESTING THE INVERTER IN DIFFERENT LOAD CAPACITANCES

The designed inverter is then tested with different load capacitances like 0,50f and 500f Farads. In addition to this the inverter is also tested with one inverter as load capacitance and four inverters in fan out. We would look at the transient analysis of each experiment and their schematics. Testing was done for both schematic and layout.



The inverter and its waveform

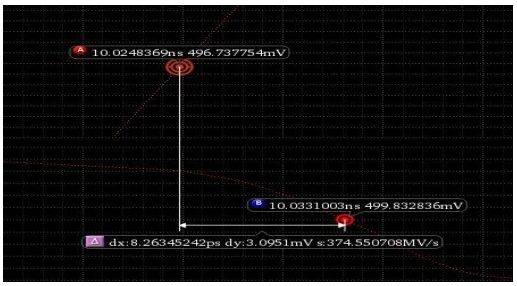
A. Inverter with various load capacitances



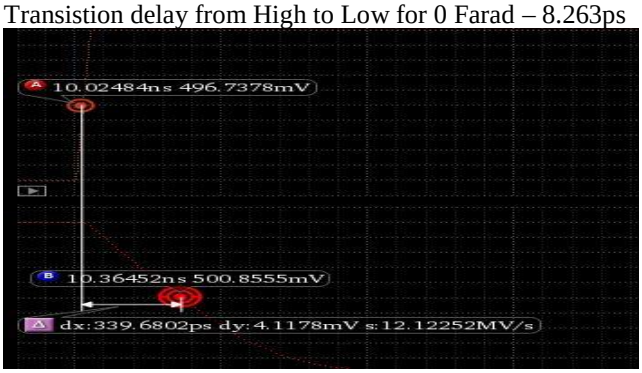
Schematic of 500f Farad load capacitance connected to the inverter design under test. (Similar set up for 0 and 50f Farad was also carried out.)

B. Resulting Wave Forms for schematic testing

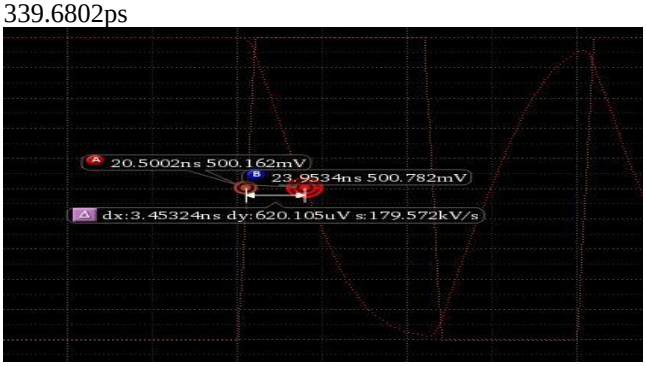
Transition delay is also called propagation delay.



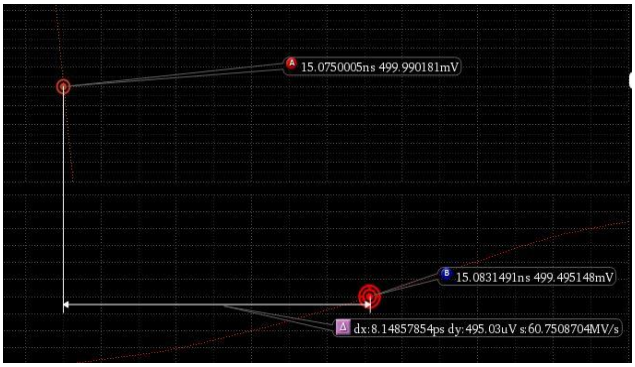
Transistion delay from High to Low for 0 Farad – 8.263ps



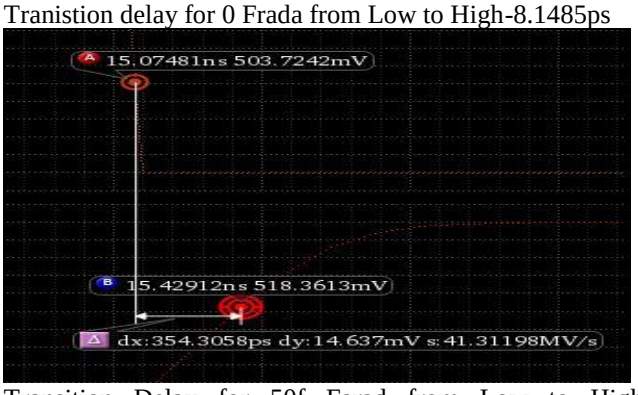
Transition delay from High to Low for 50f Farad-339.6802ps



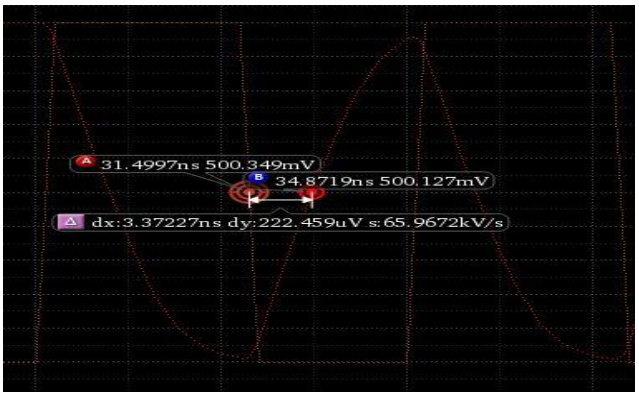
Transition delay from High to Low for 500f Farad – 3.4532ns



Tranistion delay for 0 Frada from Low to High-8.1485ps



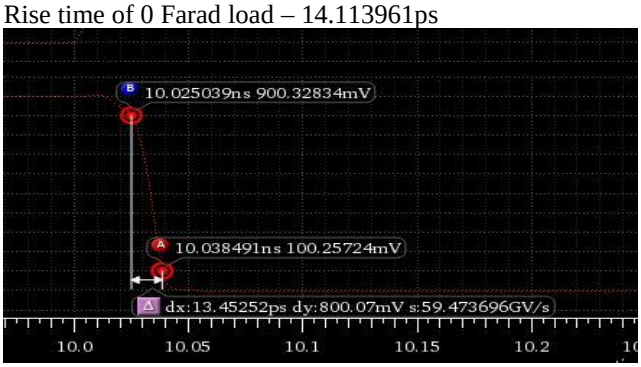
Transition Delay for 50f Farad from Low to High-354.3058ps



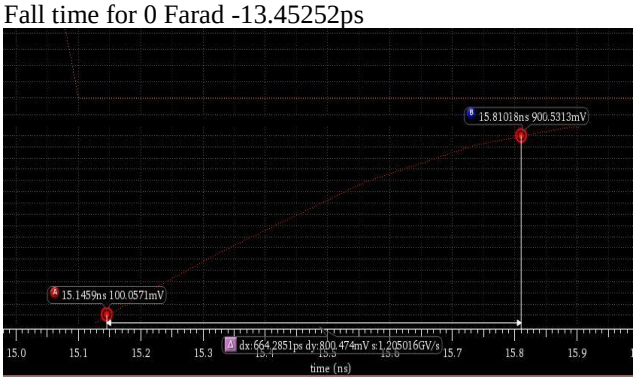
Transition delay for 500f Farad from Low to High- 3.37227ns

It can be noticed from above graphs that the propagation delays from low to high and high to low are almost equivalent for different load capacitances, even as these delays increase for different load capacitances.

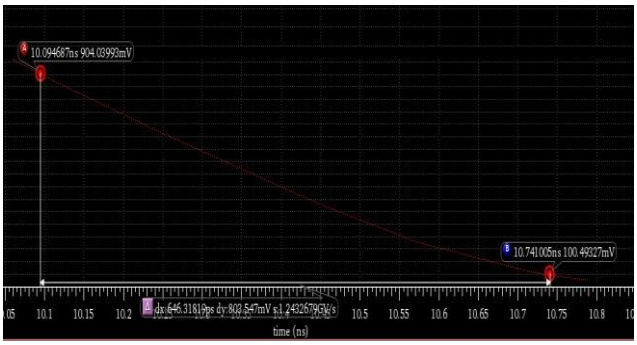
Rise time of 0 Farad load – 14.113961ps



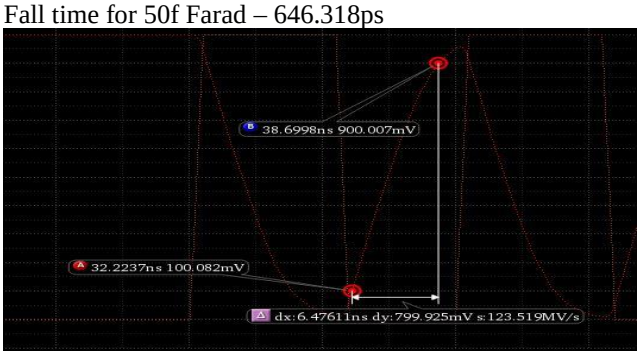
Fall time for 0 Farad -13.45252ps



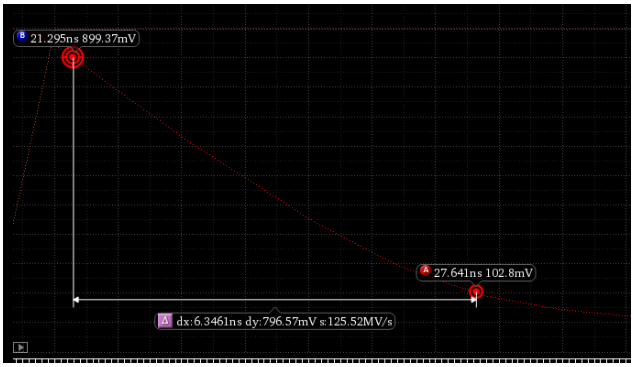
Rise time for 50f Farad- 664.2851ps



Fall time for 50f Farad – 646.318ps



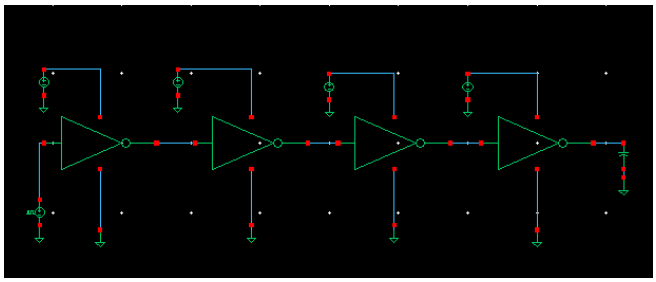
Rise time of 500f Farad Load- 6.47611ns



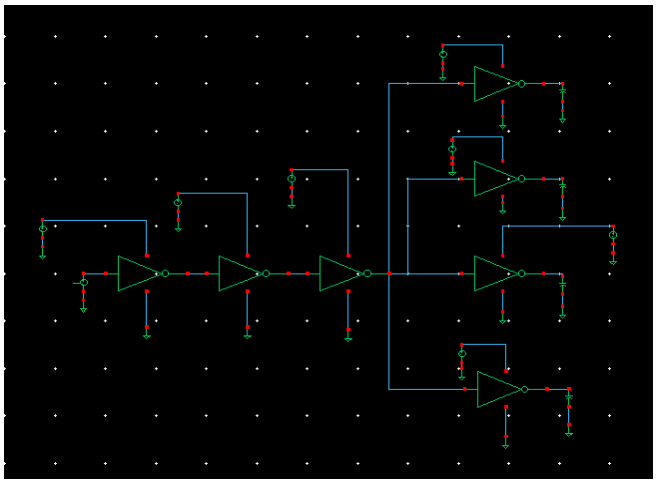
Fall time of 500f Farad – 6.3461ps

It is evident from the above graphs that the rise and fall time of different load capacitances are almost identical even as the rise and fall time values increase with different load capacitances.

C. Inverters as load capacitance



Inverter as load capacitance with 3 driver inverters and 0 Farad load capacitance



4 Fanout inverters as load each with 0 farad load capacitance.

. The Following graph describes the values obtained for schematics transient analysis.

Configuration	Rise Time	Fall Time	Propagation Delay High to Low	Propagation Delay Low to High
0 Farad	14.113ps	13.452	8.148ps	8.263ps
50f Farad	664.285ps	646.318ps	339.682ps	354.305ps
500f Farad	6.476ns	6.382ns	3.4532ns	3.3727ns
Inverter as load	7.6ps	8.466ps	5.779ps	5.8ps
Inverter Fanout 4 As Load	10.756ps	10.186ps	7.217ps	7.143ps

Table of Rise time, fall time and transition values for schematic transient analysis.

It can be noted that the values of rise and fall time are identical in each case as are the values for low to high transition and high to low transition delays.
Each configuration was tested and all graphs are clearly presented in the Appendix. Similar analysis was done for layout and the results were identical

IV. NOISE MARGIN

Noise margin is the difference between threshold input and output voltages which decide whether the input and the output are high or low respectively. Higher noise margin indicates better noise immunity. Lower noise margin means that difference between threshold low and high values is low and the logic circuit is susceptible to errors. The following table enumerates the calculated noise margin values for this inverter.

	Vih mV	Vil mV	Voh mV	Vol mV	Input Noise Margin mV	Output Noise Margin mV
500f Farad	947.48	63.56	953.28	12.653	883.92	940.627
50f Farad	785.86	226	523.84	10.82	559.86	513.02
0 Farad	596	175.57	972.71	46.43	420.43	926.28
Inverter	884.32	496	588.25	80.86	388.32	507.39
Fan out 4	803.23	472.4	597.64	87.89	330.83	509.75

Thus, it can be noticed that the inverter has a good noise margin in each case of its experimental testing. It is also evident from the reliable performance and the transient analysis presented above.

V. PITFALL AND TRICKS

The biggest challenge in the lab is to understand the theory lectures and using that knowledge in the lab effectively. Another thing is to learn the tool properly, by practicing as there are many errors which can occur leading to time wastage.
It should be ensured that the layout and schematic are dimensionally same. It helps to understand the design rules mentioned in the FreePDK45 guide as it will ensure error free designing.
Minimum length and width should be maintained to ensure minimal switching timings. The ratio of PMOS and NMOS should ideally be 2.4 in theory, but in practice it may not work. Different ratio must be tried to ensure proper timing as parasitic capacitances and resistance can affect the timing.
The trick to ensure quicker simulation is to save analysis presets to test configurations quickly. In case of FO4 testing, it helps to take values of only 1 inverter as all other inverters produce equal or equivalent values. Transient Measurement and Noise Analysis tools can be used to generate quicker transient analysis and noise analysis.

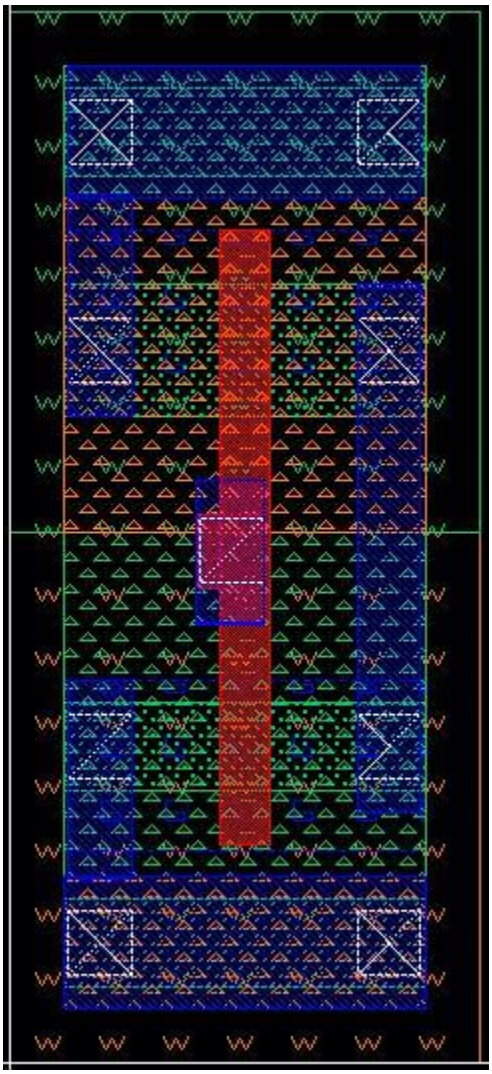
CONCLUSION

In this lab, the designing of an inverter was studied using an industry standard tool. The designing process gave deep insights into the theoretical and practical aspects of IC design and the enormous effort required for designing a simple inverter. Different theoretical and practical constraints were studied in order to arrive at the right design such that the expected transient analysis is observed. The lab helps prepare solid foundation for the next stage of the course i.e designing and fabricating a 16-bit adder.

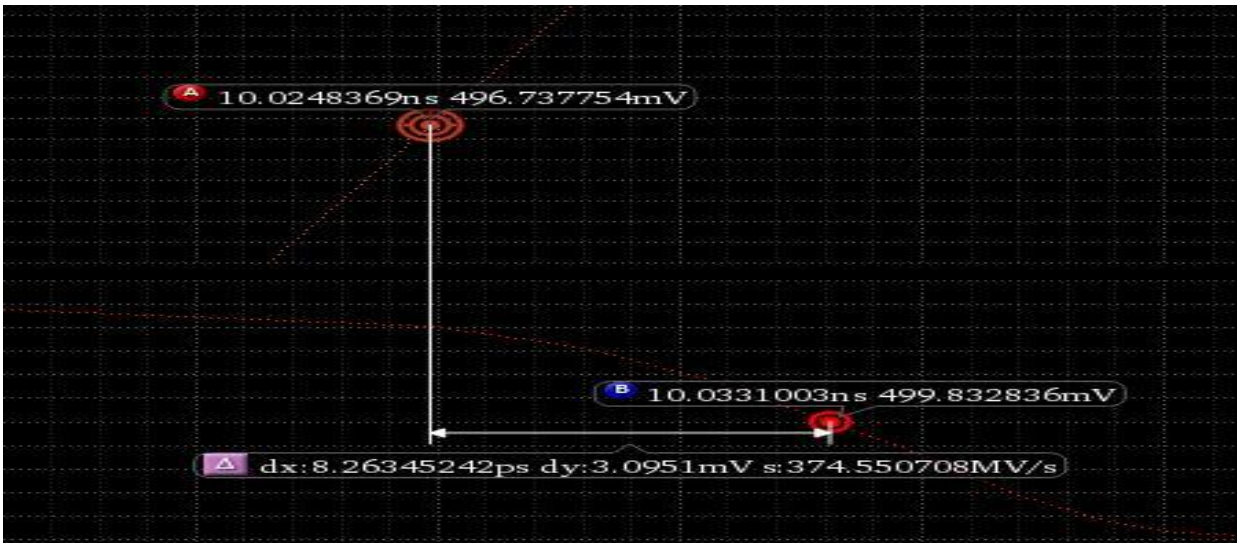
REFERENCES

1. Rabaey, J. M., Chandrakasan, A. P., & Nikolić, B. (2013). Digital integrated circuits: A design perspective. Delhi: PHI Learning Private Limited.

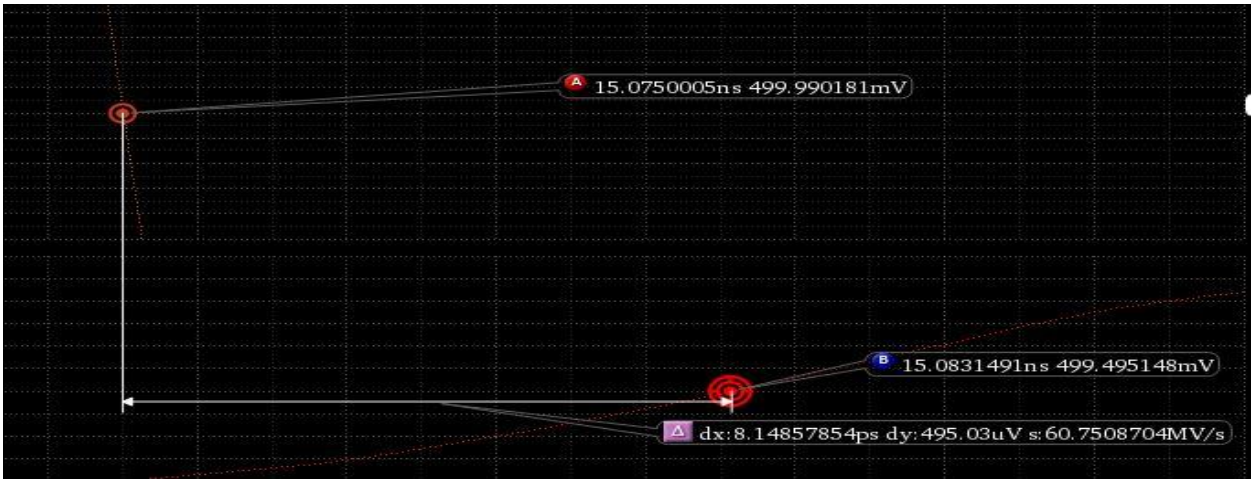
Appendix



Layout

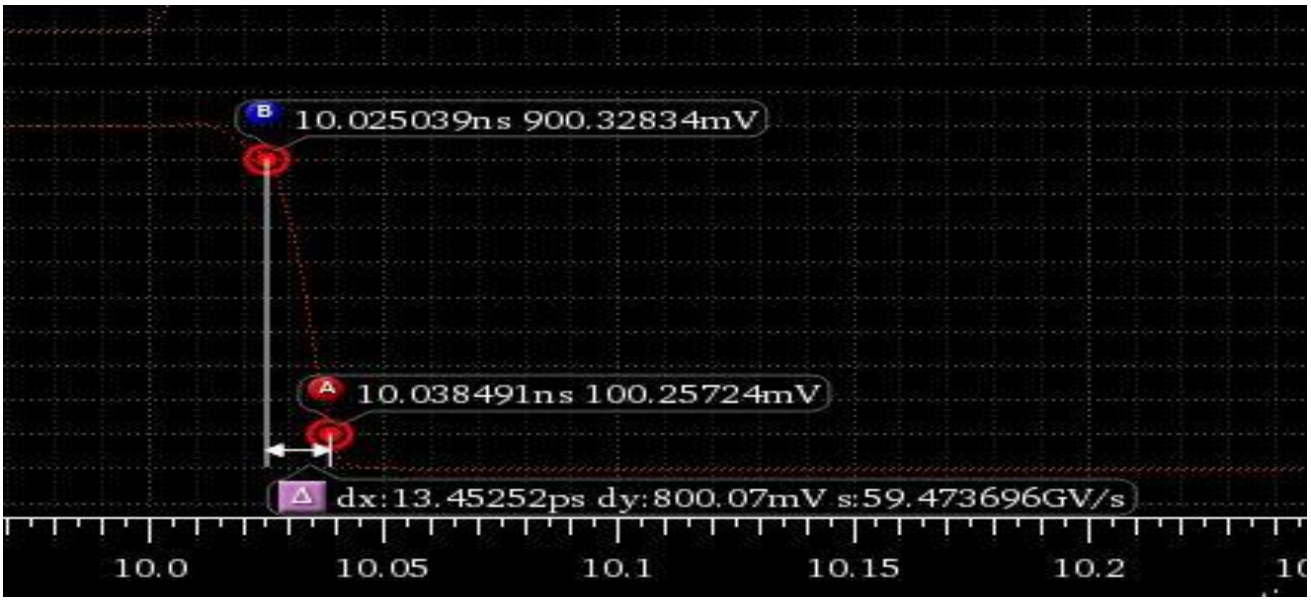


Transition Delay low to high 0 farad



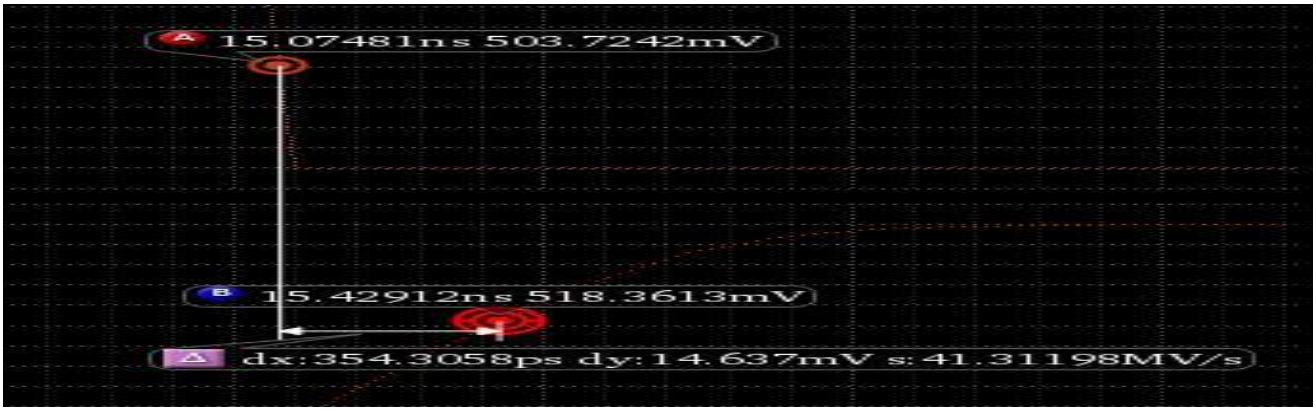
Transition delay high to low 0 farad

Rise time 0 farad

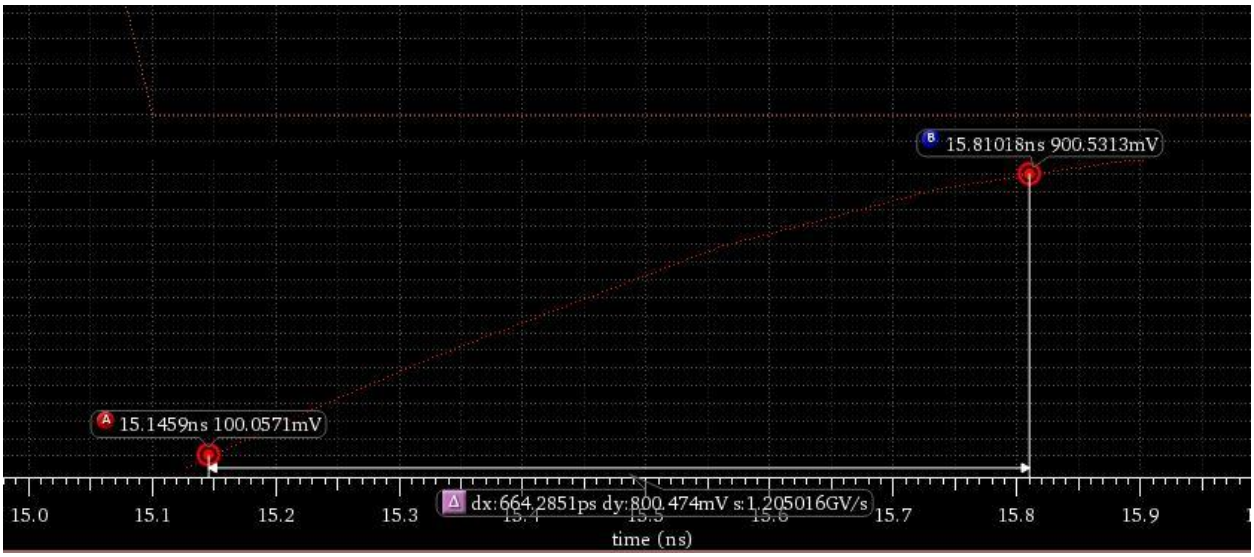


Fall time 0 farad

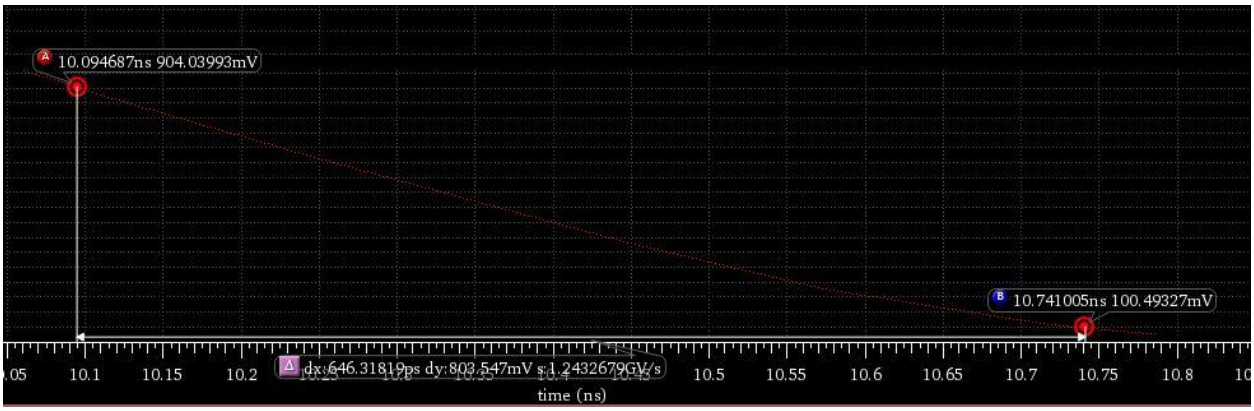
Transition delay high to low 50 femto farad



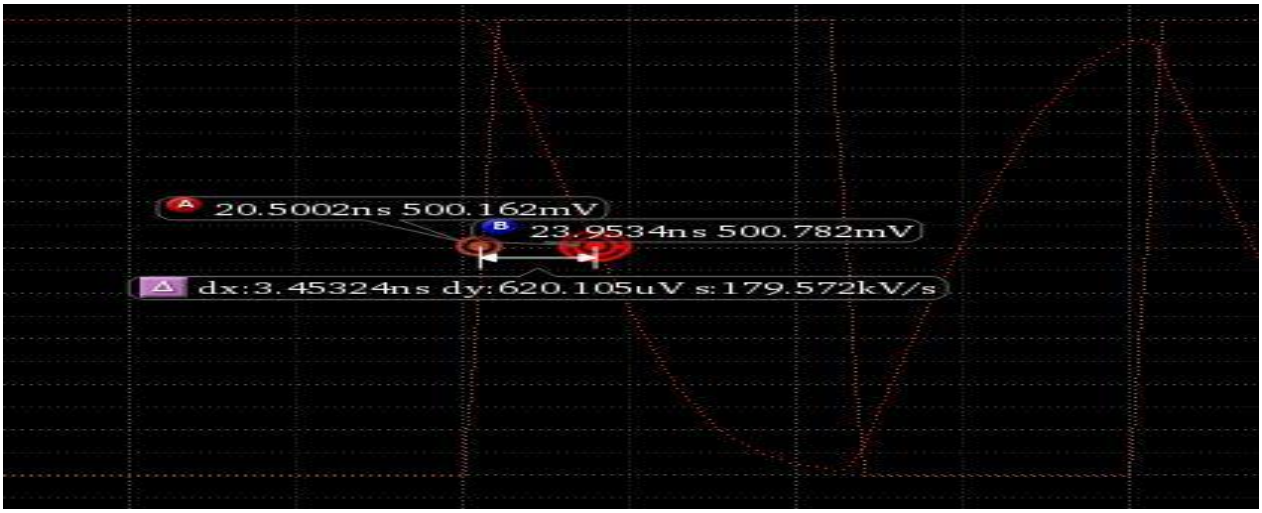
Transition delay low to high 50 femto farad



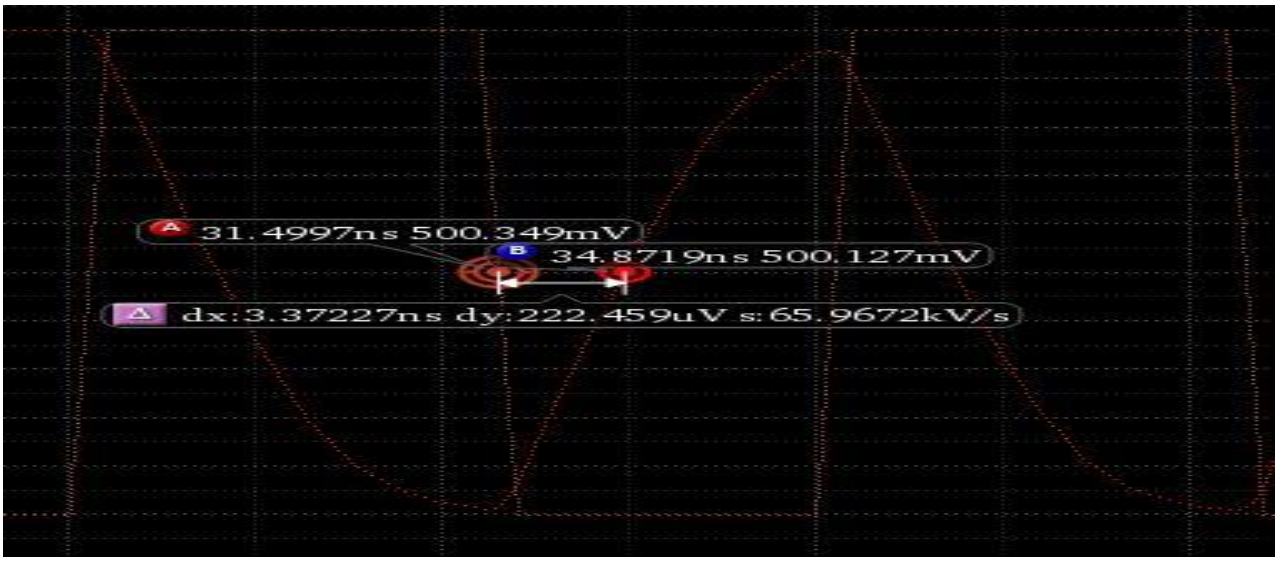
Rise time 50 femto farad



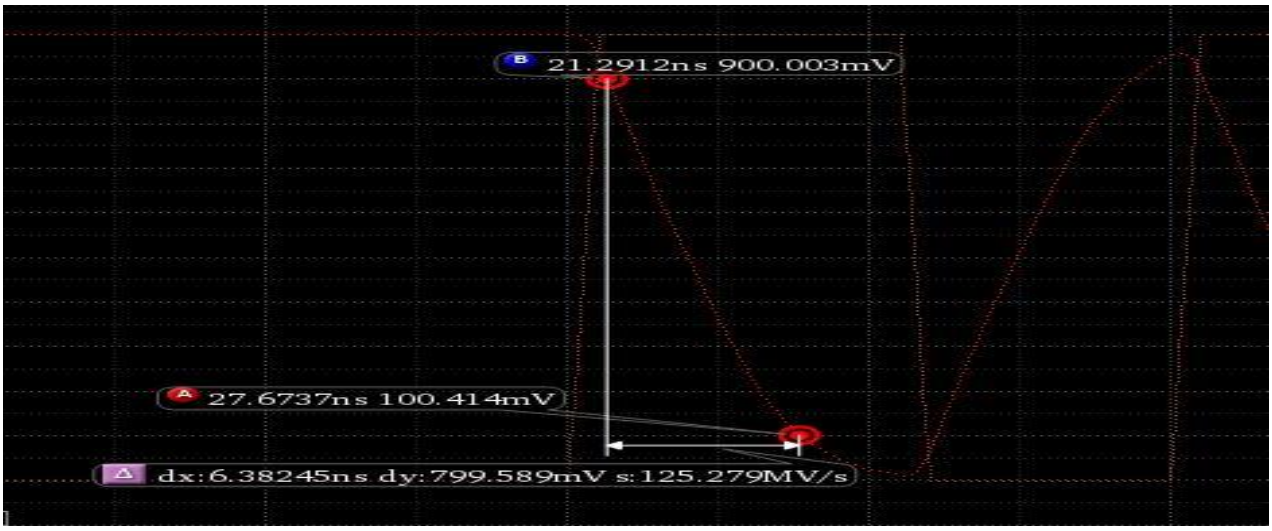
Fall time 50 femto Farad



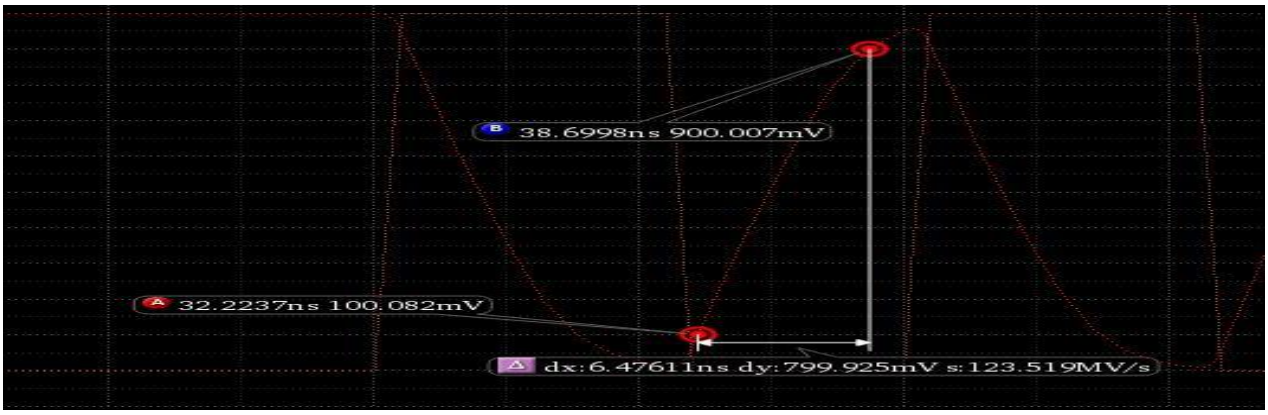
Transition Delay high to low 500femto farad



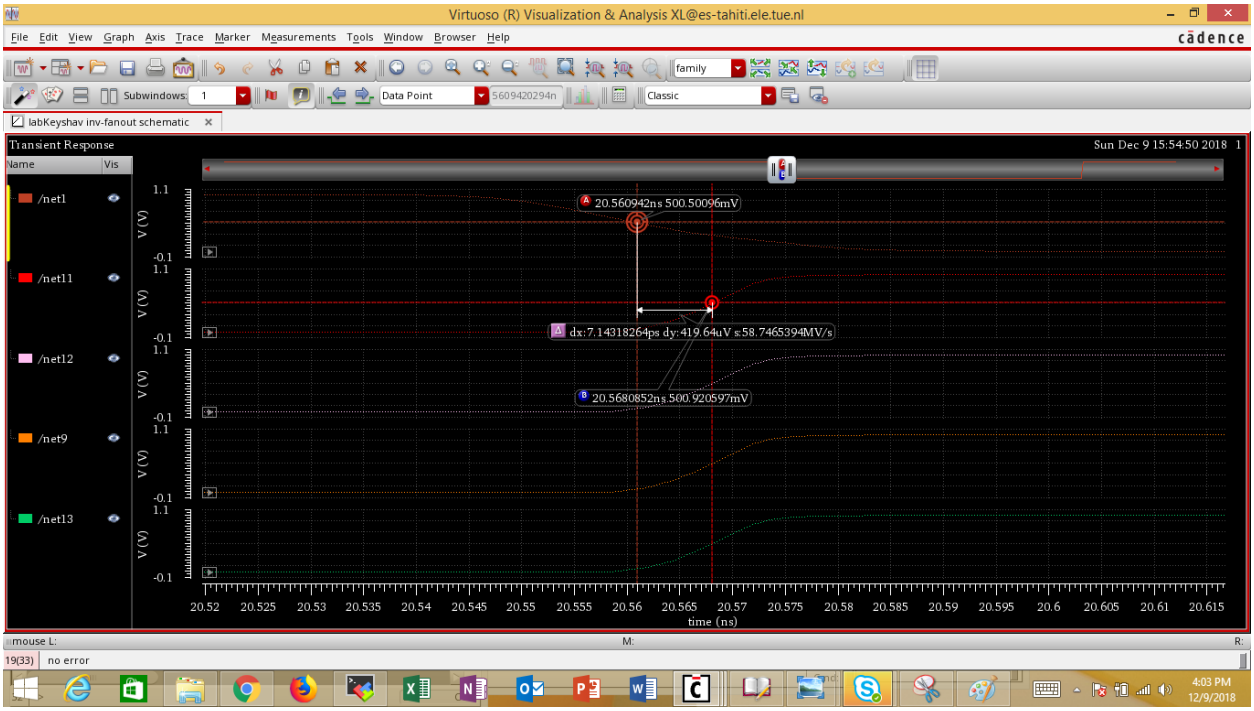
Tranistion delay low to high 500 femto farad



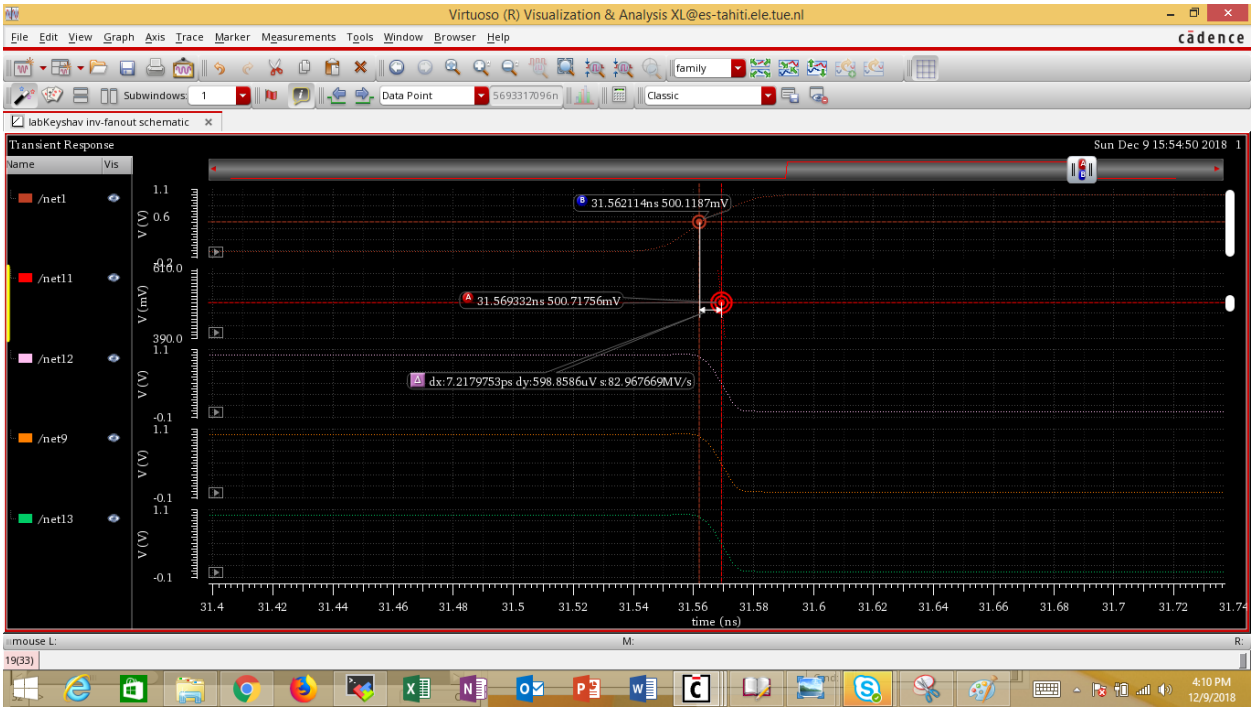
Fall time 500 femto farad



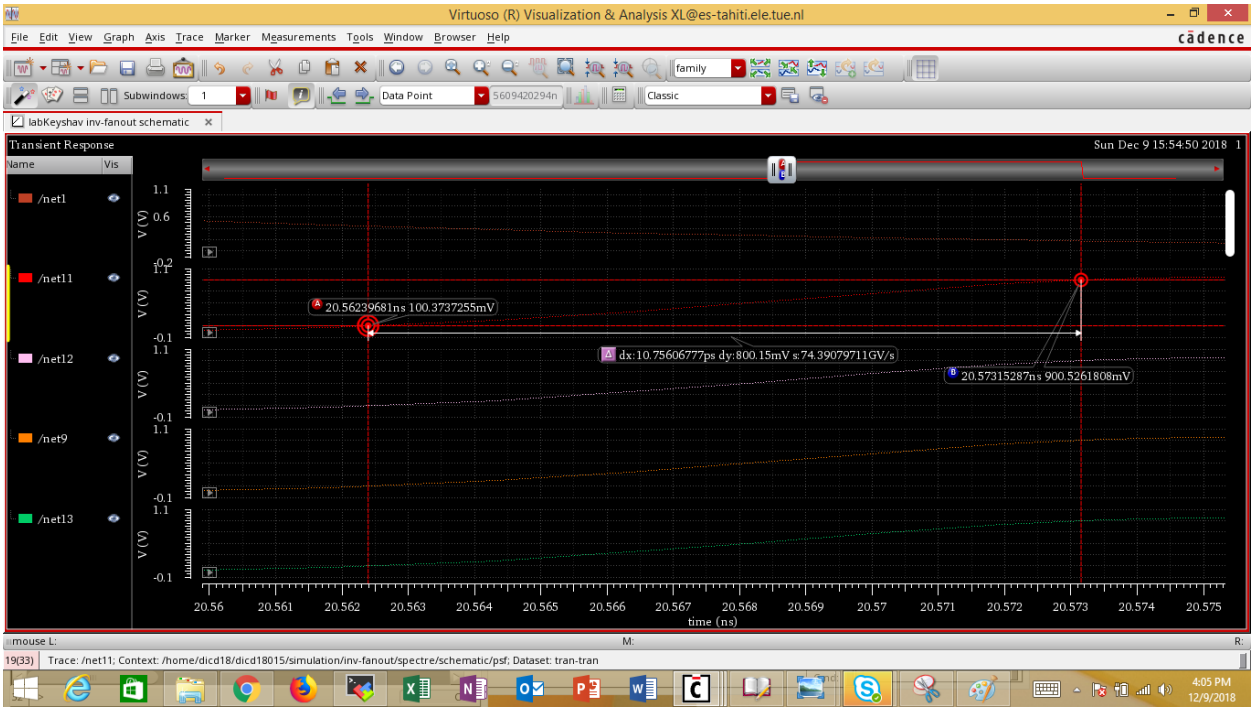
Rise time 500 femto farad



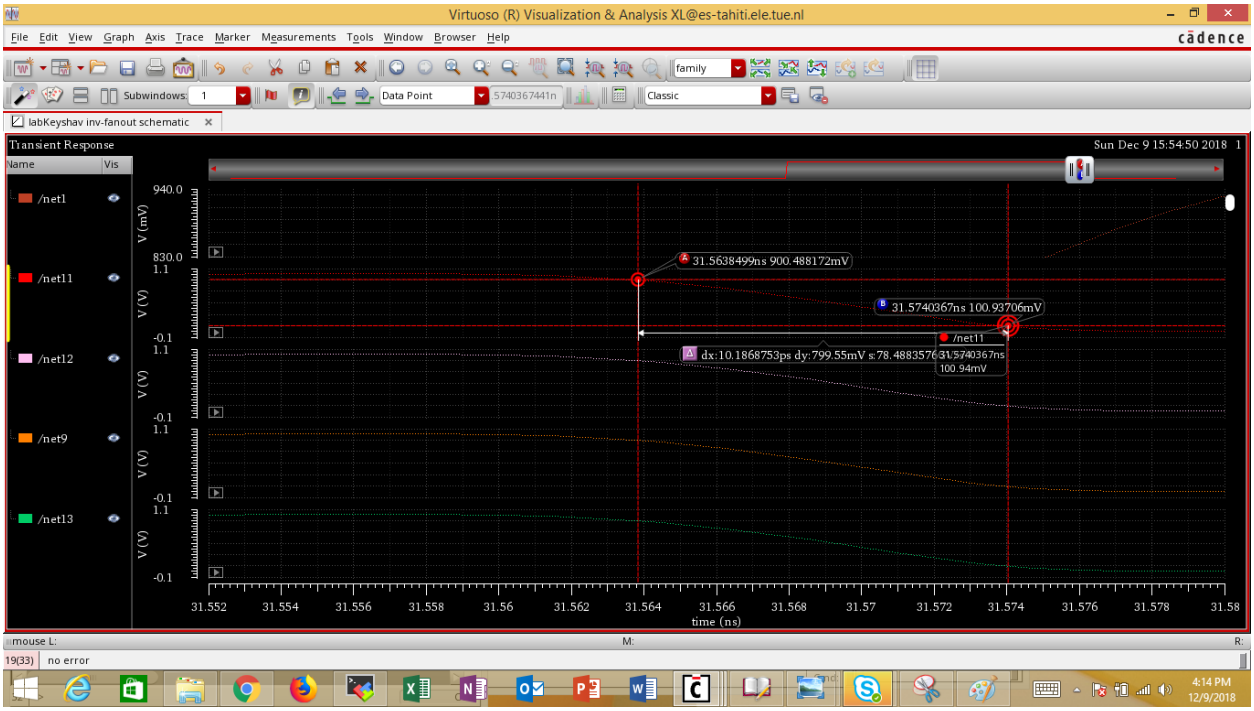
Transition delay low to high FO4



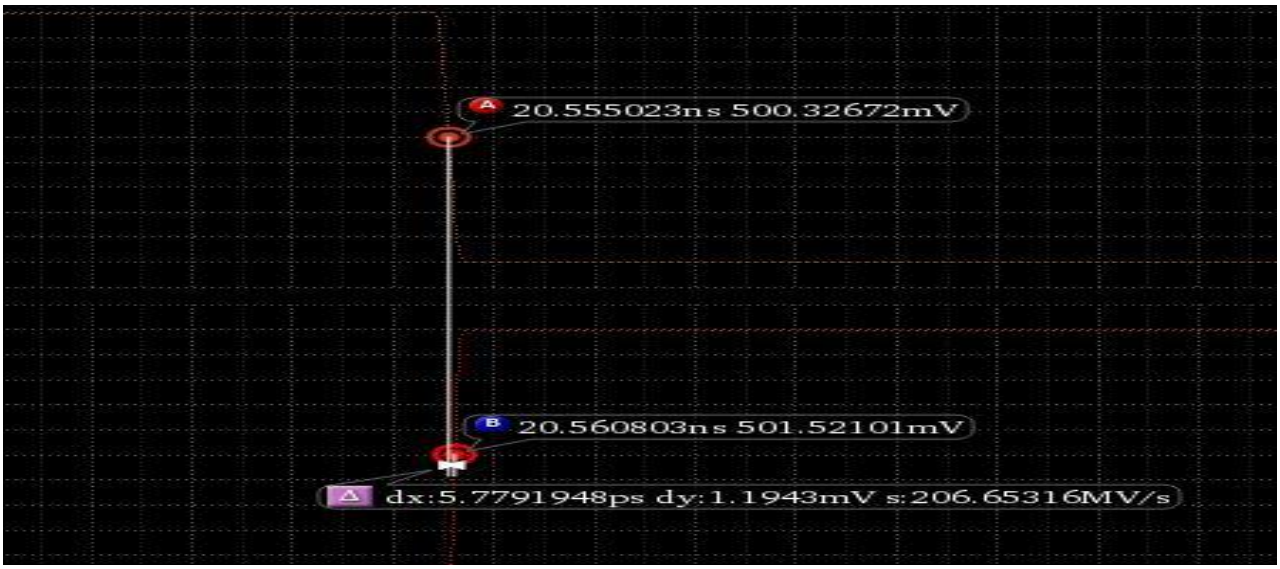
Transition delay high to low F04



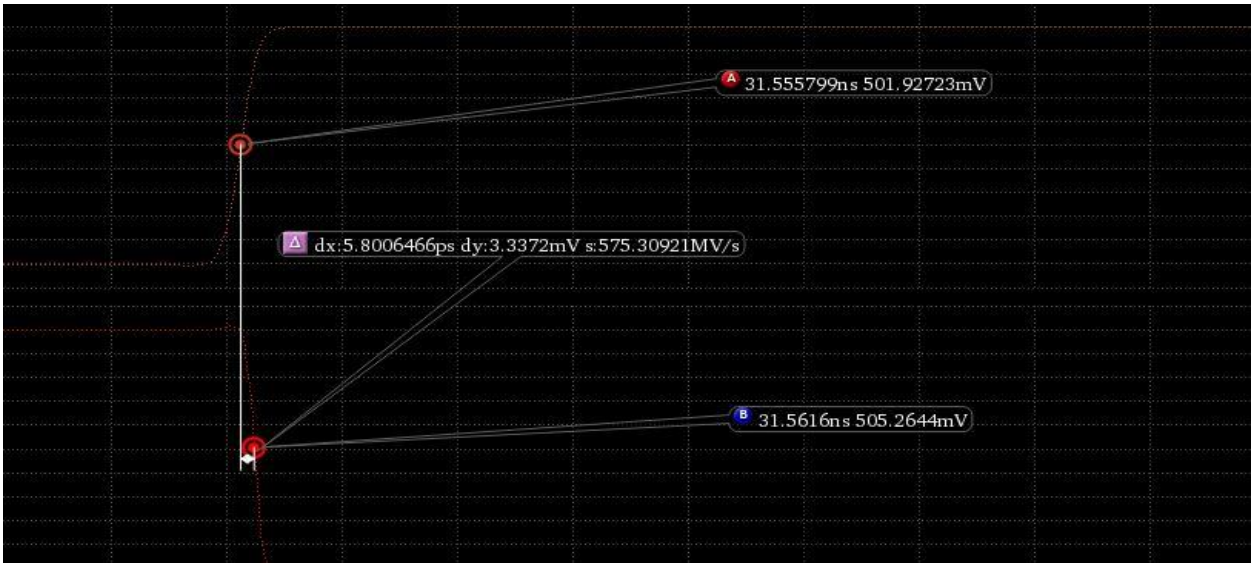
Rise time FO4



Fall time FO4

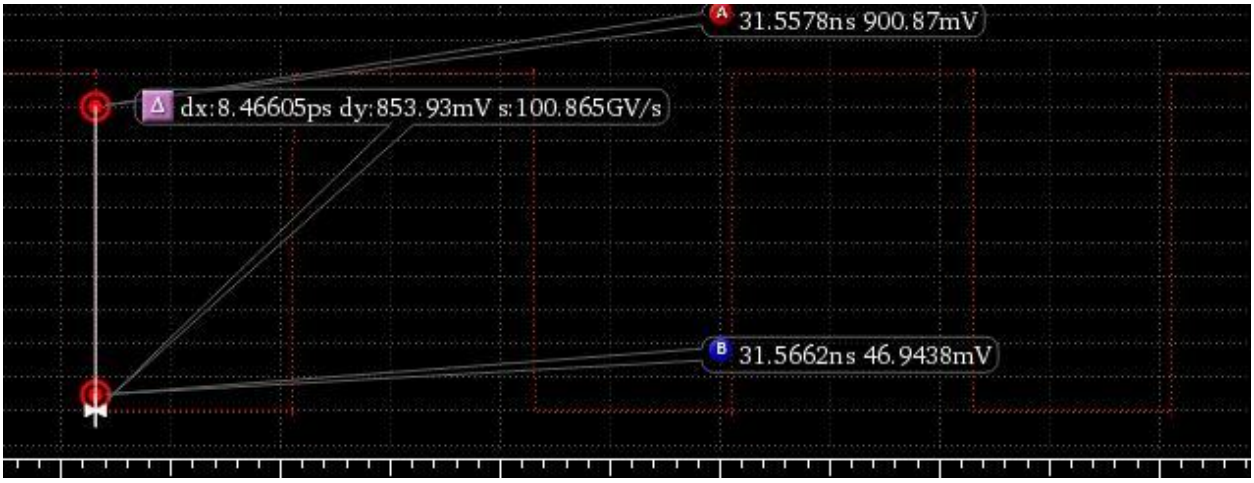


Transition time high to low Inverter as load



Transition time low to high Inverter as load

Rise time Inverter as load



Fall time Inverter as load