Term Project Submission 1 - Student Names

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Progress

- We have created a Multi Cycle MIPS Processor using procedural assigments in a single block.
- As of now, the ISA is just 4 Instructions ADD, SUB, AND and OR.

Specifications

- Five Stage pipelining with **IF, ID, EXE, MEM and WB**
- **32**-bit Program Counter.
- **32** Registers of each **32** bit size.
- **4** Pipeline Registers of IFID-64, IDEX-127, EXMEM-69, MEMWB-37 bits respectively to store the **data between blocks**.
- **3** Pipeline Registers of EX-11, MEM-4 and WB-1 bits respectively to store **control signals**.
- **32 bit** wide instruction and data memory of size 1024.
- Posedge Triggered clock of Time period = **20ns**.
- Main Control which generates control signals is kept in **ID stage** itself.

Problems Faced

- Since we are using procedural assignments there is a problem while implementation.
- We are giving the instructions into the instruction memory by manually converting them into bits and assigning them before the first pipeline block starts.

Future work

- We will try to modify the code so that it can be Implemented.
- Find a dynamic way of storing instructions into memory given the code.
- We will design a ISA with all kinds of instructions.
- To improve the throughput we will deploy **Data Forwarding**, **Branch Target Buffer** etc.
- If time permits, we will also try to design basic compiler that can **Unroll**, **Rename** and try to solve some dependencies in the code given.