Assignment #3

Objectives:

The aim of this laboratory is to introduce to sequential logic design **VERILOG Behavioral modelling** using the Xilinx Vivado 2015.2

Exercises:

1. Design the following using behavioral modelling and test the functionality by writing a test bench.

(a) Gated D Latch
(b) Positive Edge triggered D FF with asynchronous clear and preset.
(c) Negative Edge triggered T FF with synchronous clear and preset.
(d) Positive Edge triggered JK FF with asynchronous clear and preset.

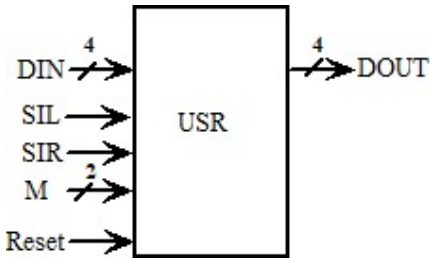
2. Design the following using behavioral modelling and test the functionality by writing a test bench.

(a) Synchronous 4-bit Up-Down counter with mode, preset, clear and load input for loading the count in 'din'.
(b) Asynchronous BCD ripple carry adder using T FF.
(c) 8-bit Johnson counter with reset and initialize input. When the init=1, din is to be loaded and counting starts from this value.

3. Design an 8-bit shift register using D FFs that shifts the dataIn to right.

4. Design a 4-bit Universal shift register using Verilog HDL. USR has two mode bits M[1:0] that selects the operation as given below in table.

Mode	Operation
00	No Change
01	Parallel Load
10	Shift right
11	Shift left



5. Design a frequency divider network to divide ClkIn by 8. (ClkOut=Clk/8).