Assignment # 4

Objectives:

To model Finite State Machines (FSM) using Verilog and test the functioning of the design.

Exercise

1. Design a circuit that glow, the three LEDS R, G, and Y in a cyclic fashion. Model this circuit as Moore machine using Verilog.

2. Design a serial parity detector, that takes input bits on every clock and gives a output '1' for odd number of 1's and output '0' for even number of 1's.

3. Design a circuit using Verilog that produces a '1' o/p iff the current i/p and previous 3 i/ps correspond to either of the sequence 0110 or 1001. The '1' o/p is to occur at the time of the fourth i/p of the recognized sequence. o/ps of '0' are to be produced at all other times. Model it as a Mealy m/c

4. Design a serial bit adder using Verilog.
   (a) Model it as a Mealy machine.
   (b) Model it as Moore machine.

5. Design a sequence detector for the bit pattern "101010"