Assignment #2

Objectives:

The aim of this laboratory is to introduce to **VERILOG Behavioral modelling** using the Xilinx Vivado 2015.2

Exercises:

1 Design a 2 to 4 decoder using
- (a) *case* statements
- (b) *if .. then ... elsif* statements

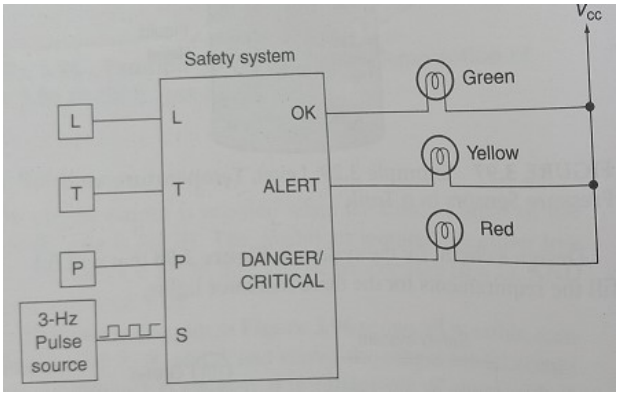
2. Design a 16:4 priority encoder using
- (a) *if .. then ... elsif* statements
- (b) *case* statements

3. Design an 8:1, 4 bit multiplexer using
- (a) *case* statements
- (b) *if .. then ... elsif* statements

4. Design an 4 bit adder/subtractor using behavioral modeling (use for loops).

5. Design a 4x16 decoder using a minimum number of 3:8 decoder and logic gates. Use behavioral modelling for 3:8 decoder.

6. A sealed tank in a chemical factory has mainly three sensors. A level sensor (L), A pressure sensor (P), A temperature sensor (T). Three sensors are to be monitored by a safety system as shown in the figure below:



- All the lamps are **active LOW.**
- **OK** is active when no sensor is active**.**
- **ALERT** is active when one sensor is active
- **DANGER** is active when two sensors are active
- **CRITICAL** is active when all are active.
- Both **DANGER** and **CRITICAL** use same lamp.
- **DANGER** is **steady ON** on the Red lamp, whereas **CRITICAL** is **flashing** at 3Hz.

Design a controller for the same using Verilog.