# **HN62314B Series** HN62334B Series

# 4M (512K x 8-bit) Mask ROM

### DESCRIPTION

The Hitachi HN62314B/HN62334B Series is a 4-Megabit CMOS Mask Programmable Read Only Memory organized as 524,288 x 8-

The low power consumption of this device makes it ideal for battery powered, portable systems. In addition, the high density and high speed provide enough capacity and high performance to be used as a character generator in laser printers.

Hitachi's HN62314B/HN62334B Series are offered with JEDEC-Standard Byte-Wide EPROM pinouts in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. This allows socket replacement with EPROMs and Flash Memory.

#### **■ FEATURES**

· Single Power Supply:  $V_{cc} = 5 V \pm 10\%$ 

· Fast Access Times:

150 ns/170 ns/200 ns (max)

· Low Power Consumption:

100 mW (tvp) Active Current:

Standby Current: 5 µW (typ) · Byte-Wide Data Organization

TTL-Compatible Inputs and Outputs

· Three-State Data Outputs

Pin Arrangement:

JEDEC Standard Byte-Wide EPROM **EPROM** and Flash Memory Compatible

· Packages:

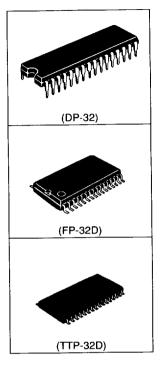
32-pin Plastic DIP

32-lead Plastic SOP

32-lead Plastic TSOP (Type II)

#### ORDERING INFORMATION

Type No.	Access Time	Package
HN62334BP	150 ns	32-pin Plastic DIP
HN62314BP	170 ns/200 ns	(DP-32)
HN62334BF	150 ns	32-lead Plastic SOP
HN62314BF	170 ns/200 ns	(FP-32D)
HN62334BTT	150 ns	32-lead Plastic TSOP
HN62314BTT	170 ns/200 ns	(TTP-32D)



### PIN ARRANGEMENT

HN62314BP/F Series HN62334BP/F Series							
NC A16 A15 A7 A6 A5 A4 A3 A2 A1 A0 D0 D1 D2 Vss		1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16	32-PIN DIP 32-LEAD SOP 32-LEAD TSOP TOP VIEV	25 24		V <sub>CC</sub> A18 A17 A14 A13 A8 A9 A11 OE A10 CE D7 D6 D5 D4 D3	
(PinD32.HN62314B,334B)							

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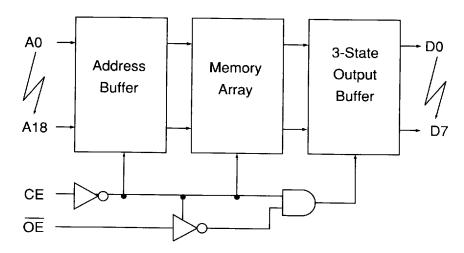
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### ■ PIN DESCRIPTION

Pin Name	Function
A <sub>0</sub> - A <sub>18</sub>	Address
D <sub>0</sub> - D <sub>7</sub>	Output
CE	Chip Enable
ŌĒ	Output Enable
V <sub>cc</sub>	Power Supply
V <sub>ss</sub>	Ground
NC	No Connection

#### **■ BLOCK DIAGRAM**



(BD.HN62314B,334B)

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## HN62314B/HN62334B Series -

### ■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage <sup>1</sup>	V <sub>cc</sub>	-0.3 to +7.0	٧
Terminal Voltage 1	V <sub>T</sub>	-0.3 to V <sub>cc</sub> + 0.3	٧
Operating Temperature Range	T <sub>opB</sub>	0 to +70	° C
Storage Temperature Range	T <sub>stG</sub>	-55 to +125	° C
Temperature Under Bias	T <sub>BIAS</sub>	-20 to +85	° C

Notes: 1. With respect to V<sub>ss</sub>.

### ■ CAPACITANCE

 $(V_{CC} = 5V \pm 10\%, V_{SS} = 0V, T_a = 25^{\circ}C, V_{IN} = 0 V, f = 1MHz)$ 

Item	Symbol	Min.	Max.	Unit
Input Capacitance 1	Cin	-	15	pF
Output Capacitance 1	C <sub>out</sub>	-	15	pF

Notes: 1. This parameter is sampled and not 100% tested.

# ■ DC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

 $(V_{CC} = 5V \pm 10\%, V_{SS} = 0 V, T_a = 0 \text{ to } 70^{\circ}\text{C})$ 

Item	Symbol	Min.	Max.	Unit	Test Condition
Input Leakage Current	I <sub>L1</sub>	-	10	μА	$V_{IN} = 0$ to $V_{CC}$
Output Leakage Current	I <sub>LO</sub>	-	10	μА	$\overline{\text{CE}}$ = 2.2 V, $V_{\text{OUT}}$ = 0 to $V_{\text{CC}}$
Operating V <sub>cc</sub> Current	I <sub>cc</sub>	-	50	mA	$V_{cc} = 5.5 \text{ V}, I_{DOUT} = 0 \text{ mA}, t_{RC} = \text{min}.$
Standby V <sub>cc</sub> Current	I <sub>SB</sub>	-	30	μА	$V_{cc} = 5.5 \text{ V}, \overline{CE} \ge V_{cc} - 0.2 \text{V}$
Input Voltage	V <sub>IH</sub>	2.2	V <sub>cc</sub> +0.3	٧	
	Vil	-0.3	0.8	٧	
Output Voltage	V <sub>OH</sub>	2.4	-	٧	I <sub>OH</sub> = -205 μA
	V <sub>OL</sub>	-	0.4	V	I <sub>OL</sub> = 1.6 mA

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### **AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION**

 $(V_{CC} = 5V \pm 10\%, V_{SS} = 0 \text{ V}, T_a = 0 \text{ to } 70^{\circ}\text{C})$ 

#### **Test Conditions**

· Input pulse levels:

0.8 V / 2.4 V

· Input rise and fall times:

≤10 ns

· Output load:

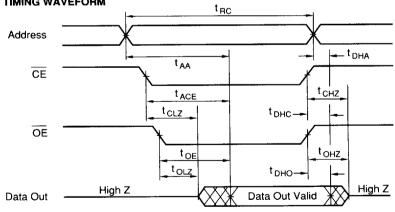
1 TTL Gate + CL = 100 pF (Including jig capacitance)

 Input/Output Timing Reference level: 1.5 V

		HN62334B-15		HN62314B-17		HN62314B-20		
Item	Symbol	Min.	Max.	Min.	Мах.	Min.	Мах.	Unit
Read Cycle Time	t <sub>RC</sub>	150	-	170	-	200	-	ns
Address Access Time	t <sub>AA</sub>	-	150	-	170		200	ns
CE Access Time	t <sub>ACE</sub>	-	150	-	170	-	200	ns
OE Access Time	t <sub>oe</sub>	-	70	-	70	-	100	ns
Output Hold Time from Address Change	t <sub>DHA</sub>	0	-	0	-	0	-	ns
Output Hold Time from CE	t <sub>DHC</sub>	0	-	0	-	0	-	ns
Output Hold Time from OE	t <sub>DHO</sub>	0	-	0	-	0	-	ns
CE to Output in High Z	t <sub>CHZ</sub> 1	-	70	-	70	_	70	ns
OE to Output in High Z	t <sub>OHZ</sub> 1	-	70	-	70	-	70	ns
CE to Output in Low Z	t <sub>cLZ</sub>	10	-	10	-	10	-	ns
OE to Output in Low Z	t <sub>oLZ</sub>	10	-	10	-	10	-	ns

 $t_{\text{CHZ}}$  and  $t_{\text{OHZ}}$  define the time at which the output becomes an open circuit and are not Note: referenced to output voltage levels.

### **READ TIMING WAVEFORM**



(TD.R.HN62314B,334B)

Note:

- $\mathbf{t}_{\mathrm{DHA}},\,\mathbf{t}_{\mathrm{DHC}},\,\mathbf{t}_{\mathrm{DHO}}$  are determined by the faster time.
- $t_{\rm AA}$ ,  $t_{\rm ACE}$ ,  $t_{\rm OE}$  are determined by the slower time.
- $t_{\text{CLZ}}$ ,  $t_{\text{OLZ}}$  are determined by the slower time.

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