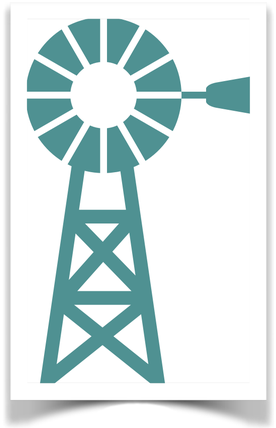
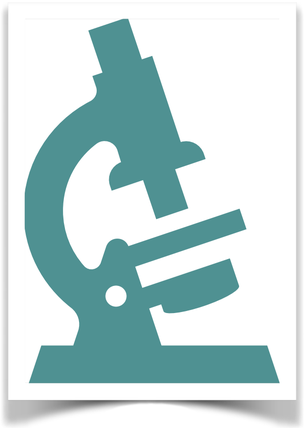
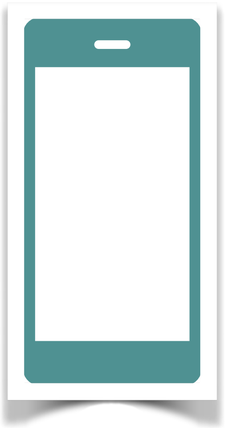
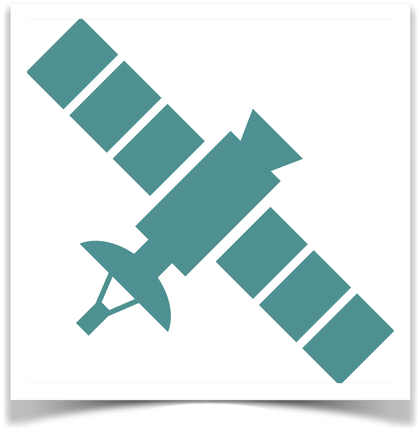
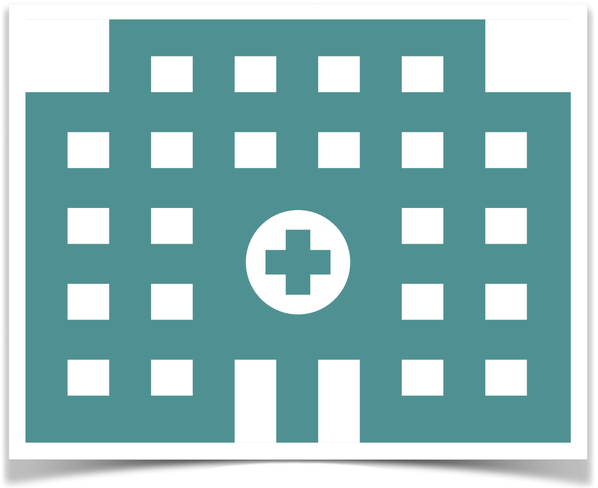
# Simple and Efficient Concurrent Programming via Synchronization Synthesis

Kostas Ferles

UToPiA

The University of Texas at Austin
Computer Science

# Software-Powered Society

# Bugs Everywhere!

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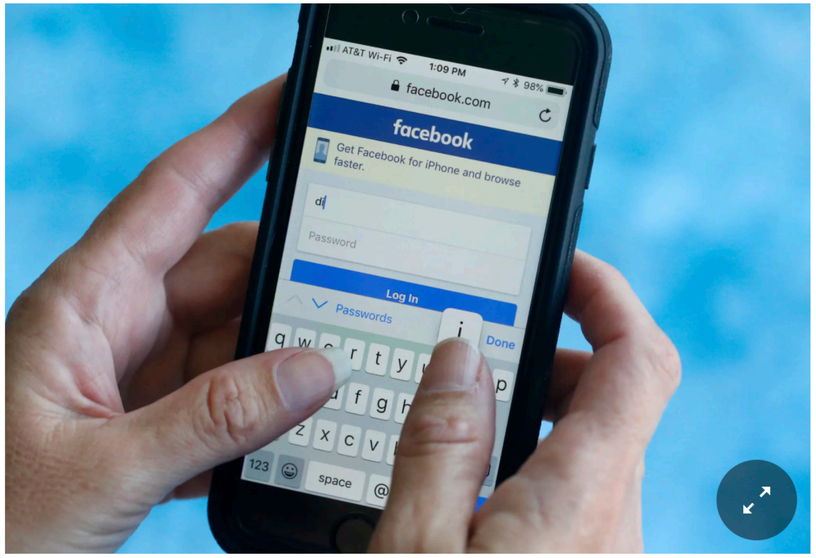
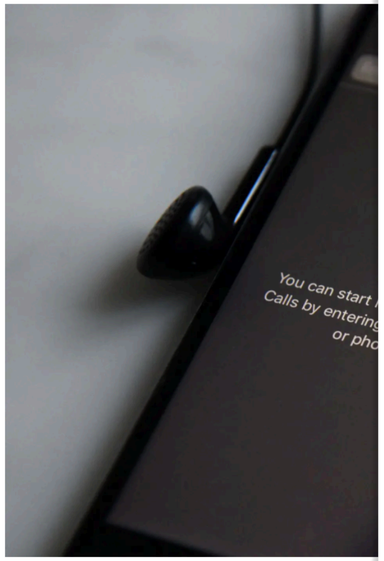



Facebook said Friday that a security breach had affected 30 million users, 20 million fewer than originally thought. Wilfredo Lee/Associated Press

## *In a Stumble for Apple, a FaceTime Bug Lets iPhone Users Eavesdrop*



The FaceTime bug could also give a caller
camera. Roslan Rahman/Agence France-Pres

## *Cisco to Pay $8.6 Million to Settle Government Claims of Flawed Tech*


A vulnerability in Cisco surveillance software was identified in 2008 by a whistle-blower, but the company continued to sell the software until July 2013. Albert Gea/Reuters

# Bugs Everywhere!

## Formal Methods to The Rescue

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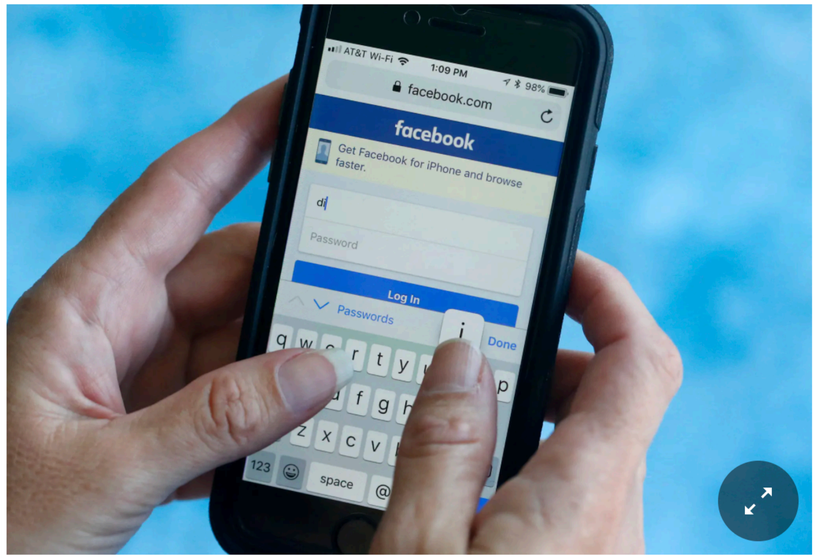


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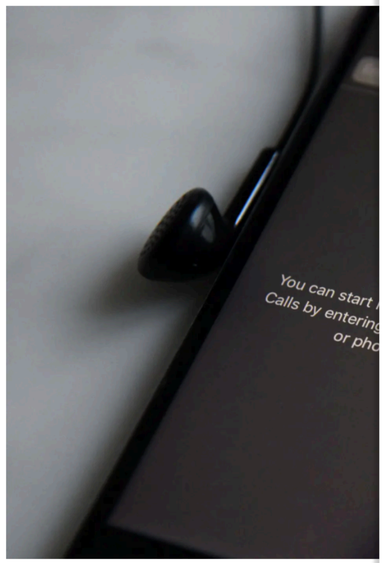


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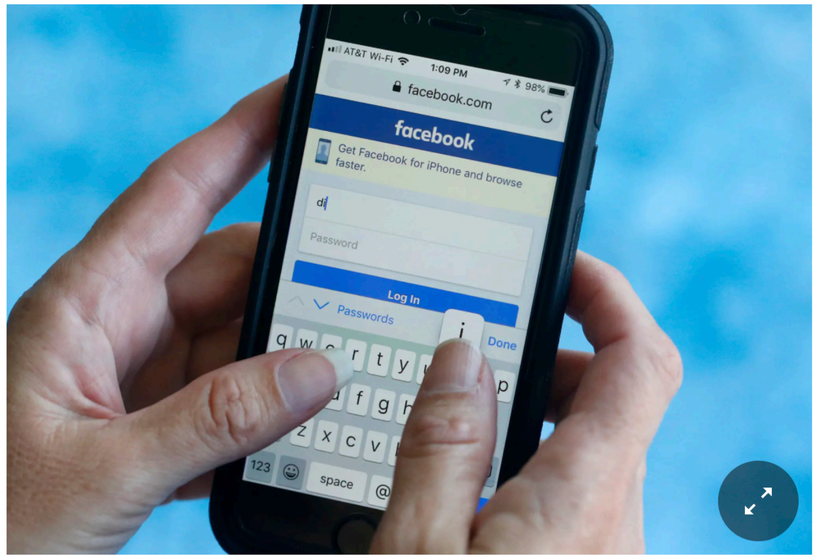


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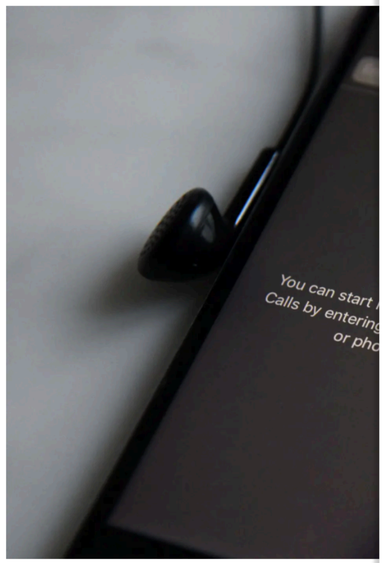

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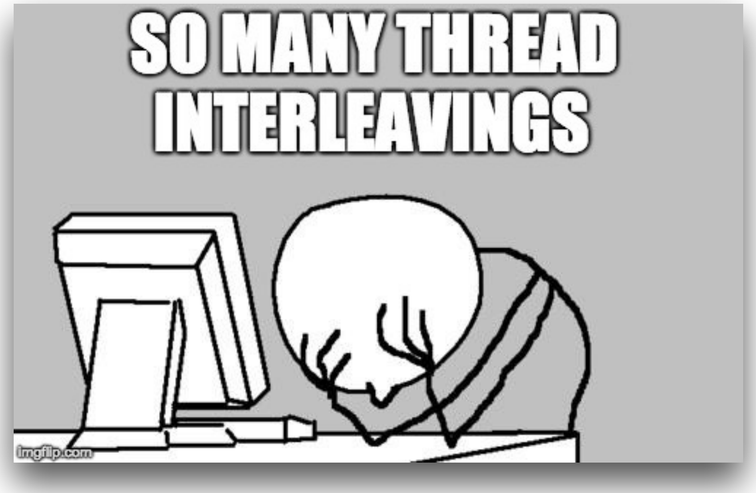
# Motivation

Concurrent programming is hard!



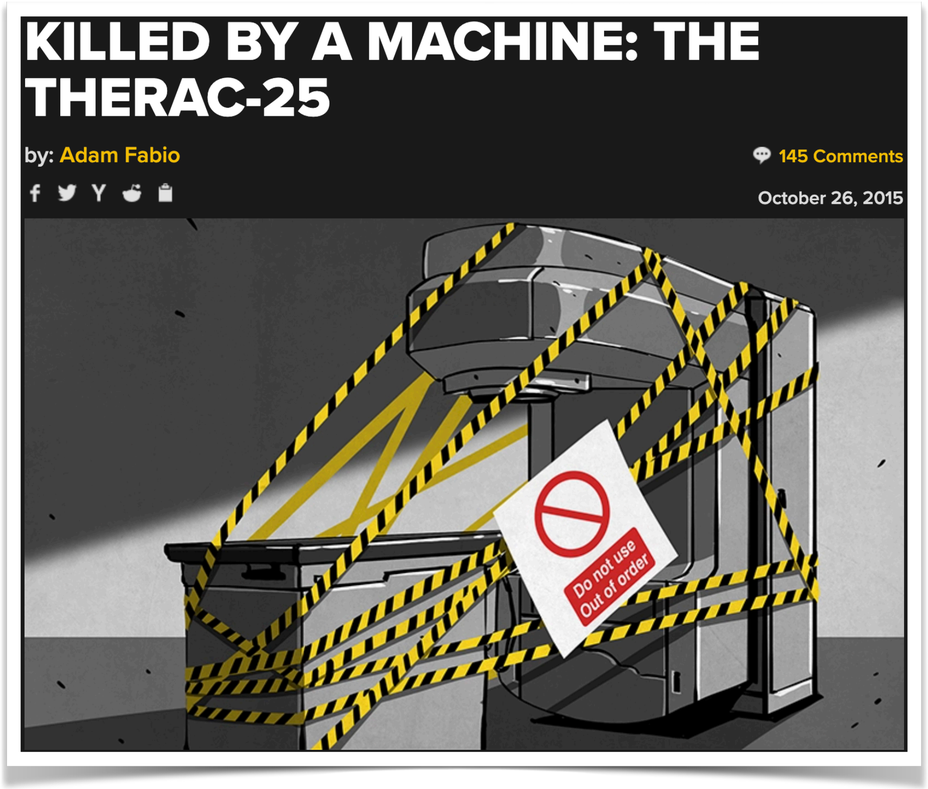

Concurrent code is a perpetual source of painful bugs:

*Deadlocks, atomicity violations, starvation, data races, …*

# Motivation

If buggy concurrent code is deployed, things can go terribly wrong!

## Infamous concurrency bugs

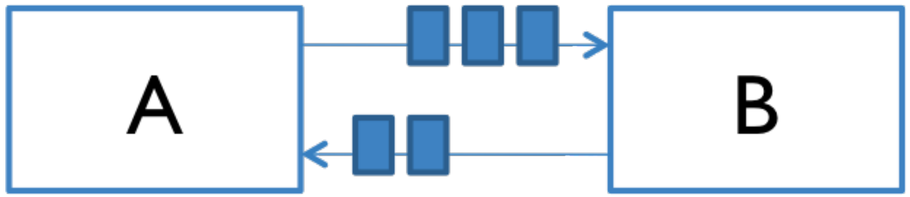


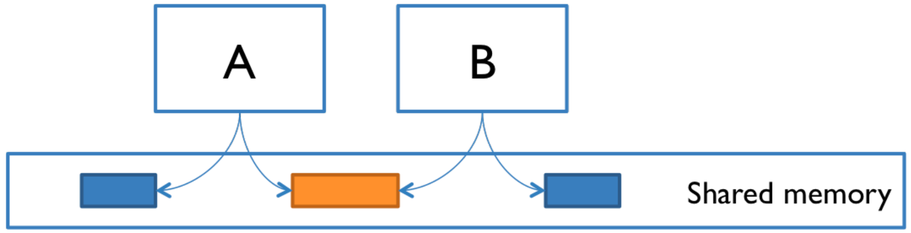

# Research Question

Can we employ formal method techniques to simplify concurrent programming without sacrificing performance?

# Shared Memory vs Message Passing

Two main models of concurrency:
*message-passing* and *shared memory*



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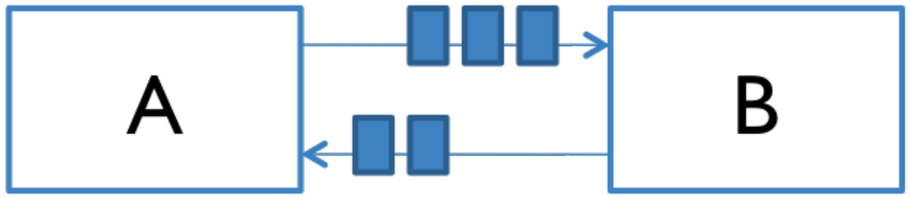


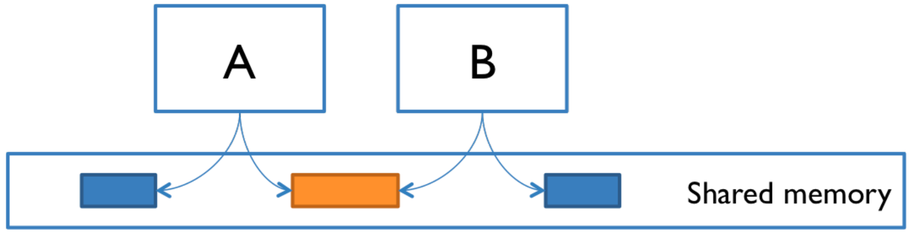


Threads pass messages; no shared state

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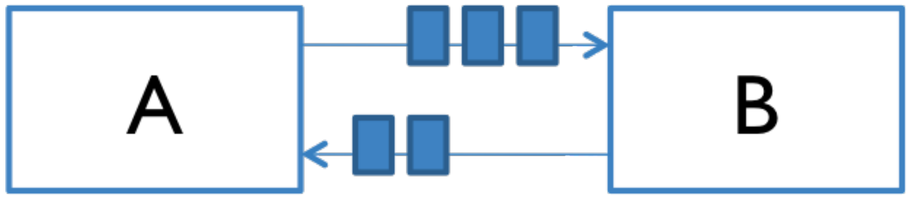


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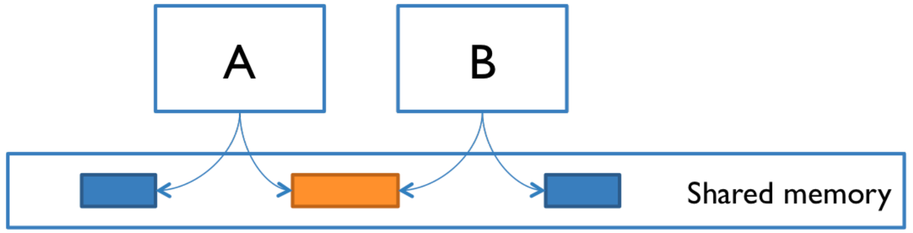


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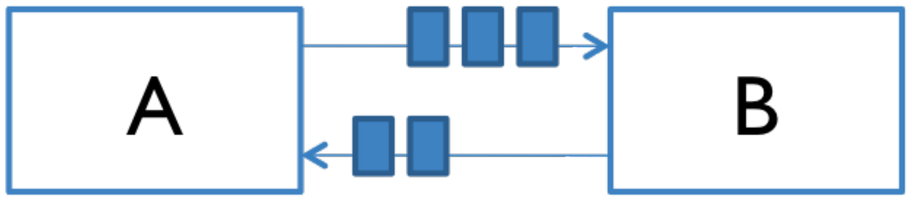


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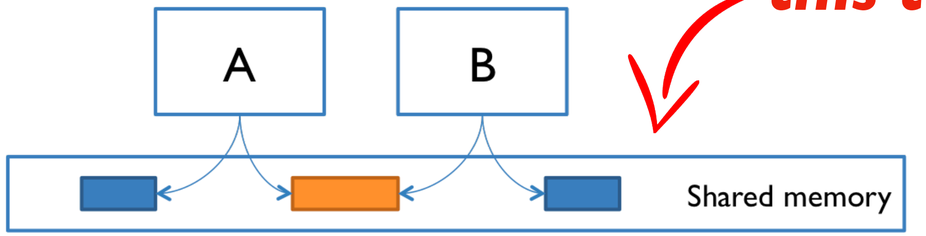


***Focus of this talk***

Threads exchange data through shared memory

# Shared Memory Primitives

Locks

Used to provide mutual exclusion

Condition variables

Signal threads when shared resource becomes available

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Condition variables

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Signal threads when shared resource becomes available

Typically used in conjunction with each other to implement the **monitor** programming abstraction

# The Monitor Abstraction

```
class Mutex {
  private boolean h;

  private Lock l = new ...;
  private Condition heldC
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  public void acq() {
    l.lock();
    while (h)
      heldc.await();

    h = true;
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- Class that mediates access to shared resources
- Threads access shared resources only by calling monitor methods
- Monitor implementation should guarantee **deadlock freedom** and **atomicity**

# Implementing Monitors

```
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- Monitors typically implemented using **locks** and **condition variables**
- But hard to implement both correctly and efficiently
- Improper locking and signaling cause **atomicity violations** or **deadlocks**

# Our Goal

Simplify concurrent programming by making it much easier to implement ***correct and efficient*** monitors

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## Approach:

(1) Use Conditional Critical Regions (CCRs) instead of locks and condition variables

- Provides higher level of abstraction — hence easier

(2) Synthesize efficient & correct low-level code with locks and condition variables

# Conditional Critical Region (CCRs)

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waituntil(P) {S}
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- Blocks when P is false and atomically executes S when P becomes true

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Called *implicit monitor*

**Assumption**: Each monitor method is a sequence of CCRs

# Back to Monitors

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class Mutex {
  private boolean h;

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}
```

***Explicit monitor***

```
class Mutex {
  private boolean h;

  public void atomic acq() {
    waituntil (!h) {
      h = true;
    }
  }

  public void atomic rel() {
    h = false;
  }
}
```

***Implicit monitor***

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***Explicit monitor***

Omit waituntil if predicate is true.

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$Preds(M)$ →

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***Explicit monitor***

Implicit Monitor = Explicit Monitor - Synchronization Code

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***Implicit monitor***

# Explicit vs Implicit Trade-offs

## Explicit

Pro: Efficient

Con: Hard to get right

## Implicit

Pro: Easy to get right

Con: Inefficient

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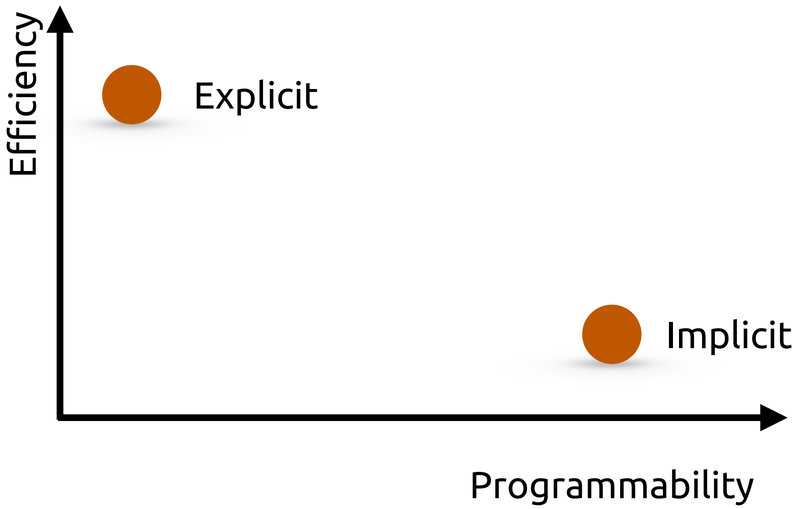
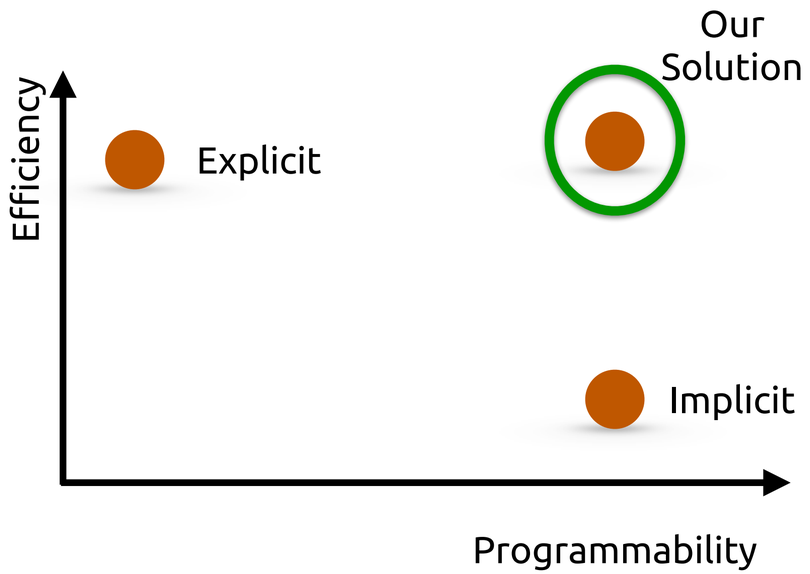
All existing solutions require run-time support

# Synthesis-Based Solution



# Synthesis-Based Solution




Goal: *Synthesize* explicit monitor from implicit

- Correct-by-construction
- As efficient as possible

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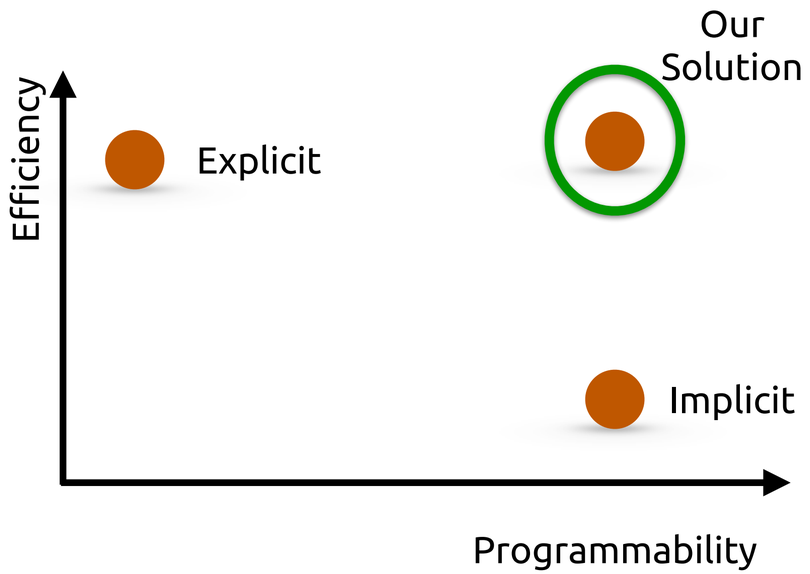


Goal: *Synthesize* explicit monitor from implicit

- Correct-by-construction
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Provides best of both worlds in terms of efficiency & programmability!

# Road Map

**Part I:** How to automatically synthesize necessary signaling code

Symbolic Reasoning for Automatic Signal Placement.
Ferles et al, PLDI'18.

**Part II:** How to automatically synthesize efficient locking

Synthesizing Fine-grained Synchronization Protocols for Implicit Monitors.
Ferles et al, OOPSLA'22.

# Part 1: Synthesizing Signaling Code

**The task:**

Given an implicit monitor:

- instrument code with condition vars
- add all necessary wait/signal operations on these variables

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*Key difficulty:* Where and how to signal so that each thread can make progress and there are no spurious wake-ups?

# Signaling Decisions

For each CCR C and predicate p $\in Preds(M)$, decide *whether* to signal or not, and if so, *how*?

Is any signaling necessary?

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Is any signaling necessary? —No→ Do not emit any signaling

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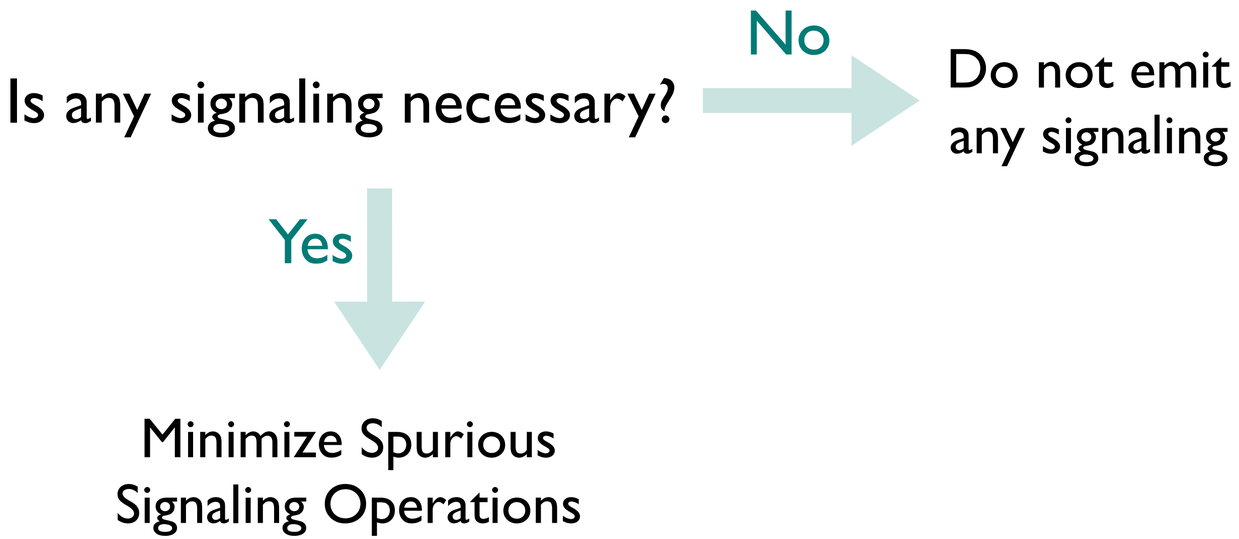

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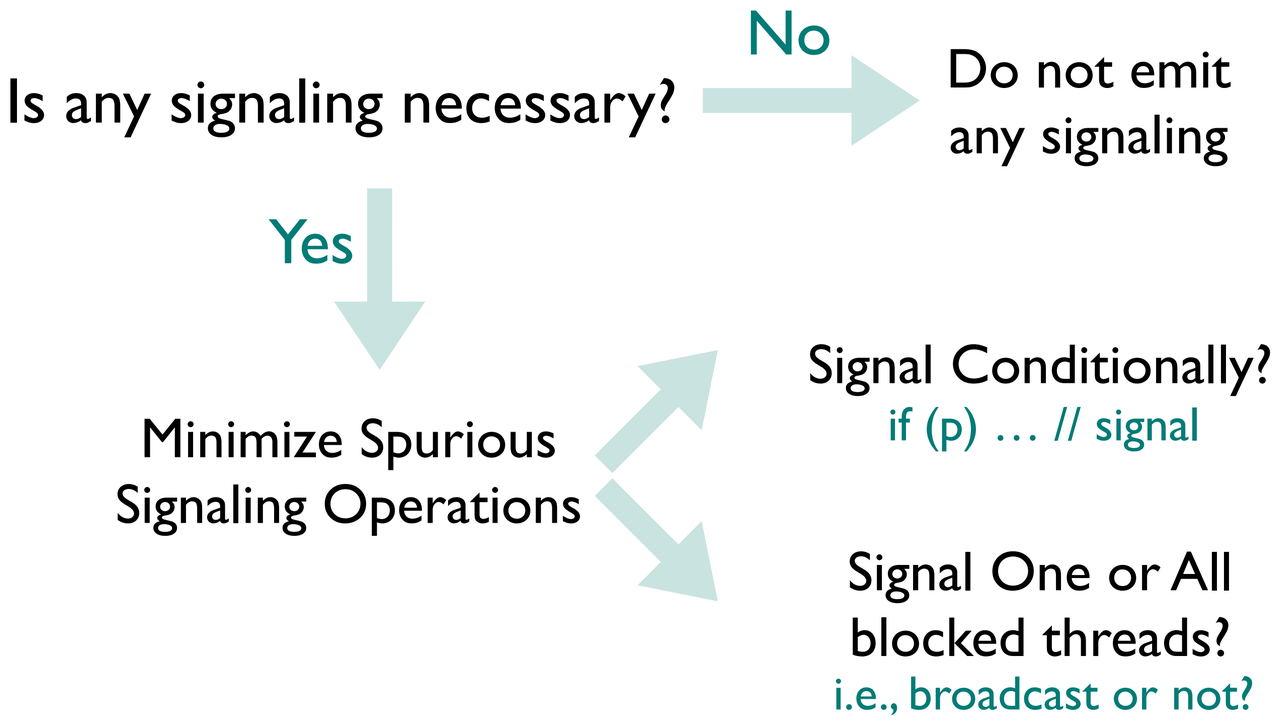

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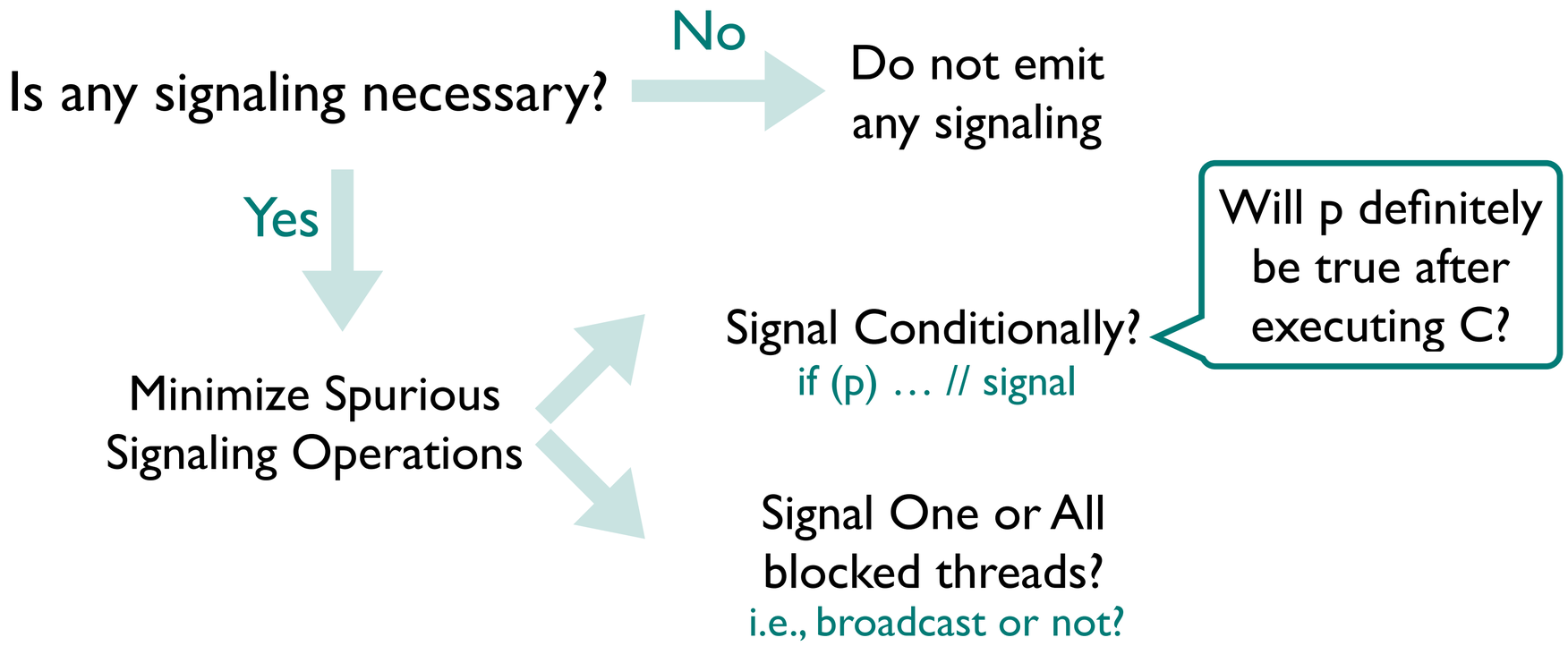
For each CCR C and predicate p $\in Preds(M)$, decide *whether* to signal or not, and if so, *how*?



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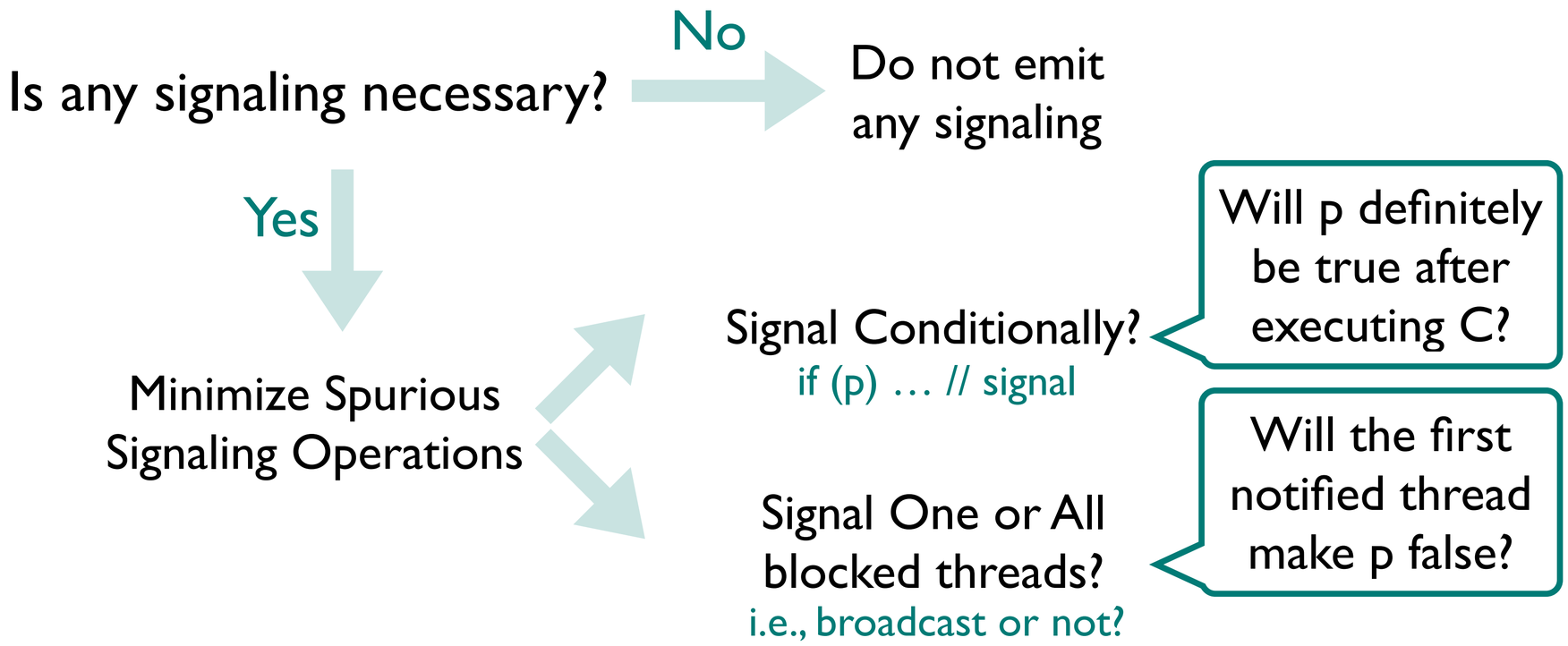

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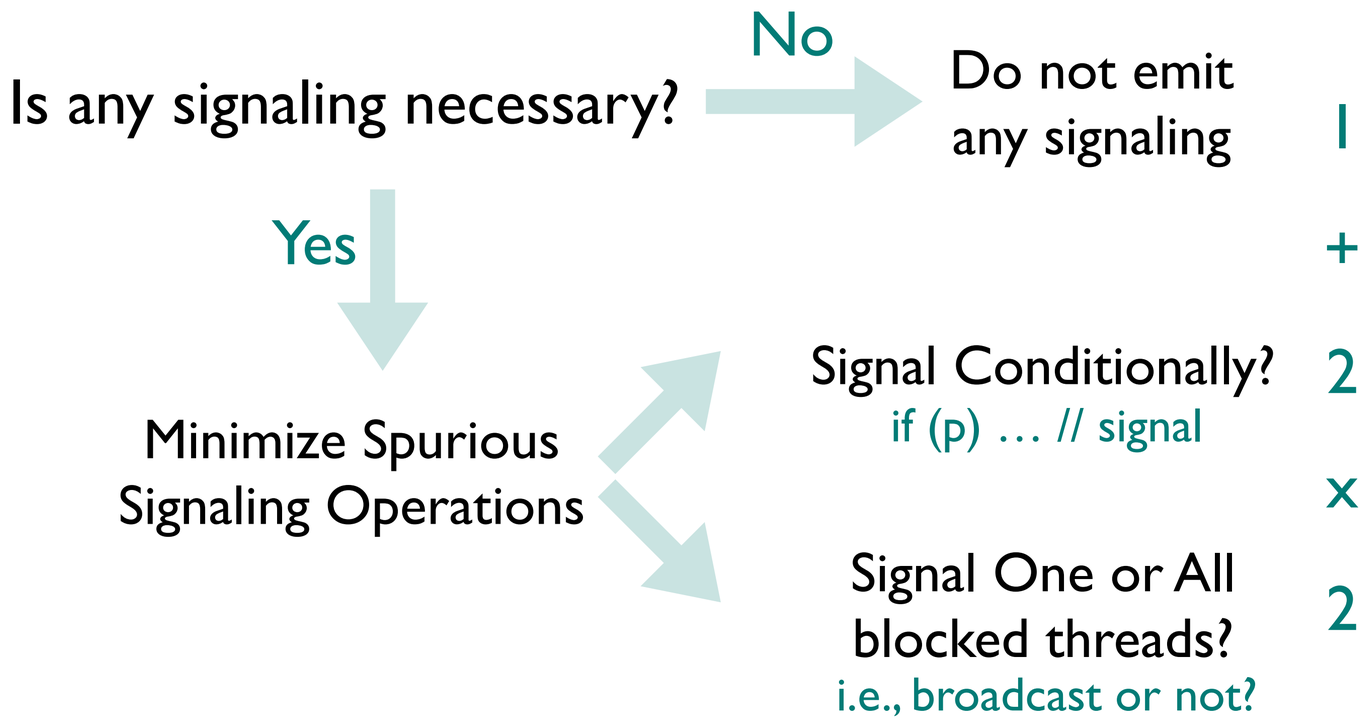


For each CCR and predicate, 5 possible outcomes

# Running Example

```
class RWLock {
  int readers = 0;
  boolean writerIn = false;

  atomic void enterReader() {
    waituntil(!writerIn) {
     readers++; }
  }

  atomic void exitReader() {
    if (readers > 0) readers—;
  }

  atomic void enterWriter() {
    waituntil(readers == 0 && !writerIn)
    { writerIn = true; }
  }

  atomic void exitWriter() {
    writerIn = false;
  }
}
```

# Running Example

```
class RWLock {
  int readers = 0;
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  atomic void enterWriter() {
    waituntil(readers == 0 && !writerIn)
    { writerIn = true; }
  }

  atomic void exitWriter() {
    writerIn = false;
  }
}
```

```
RWLock l = new …();
Readers:
l.enterReader();
… // Access Resource
l.exitReader();

Writers:
l.enterWriter();
… // Access Resource
l.exitWriter();
```

# Lots of Possible Implementations

```
class RWLock {
  int readers = 0;
  boolean writerIn = false;

  atomic void enterReader() {
    waituntil(!writerIn) {
     readers++; }
  }

  atomic void exitReader() {
    if (readers > 0) readers–;
  }

  atomic void enterWriter() {
    waituntil(readers == 0 && !writerIn)
    { writerIn = true; }
  }

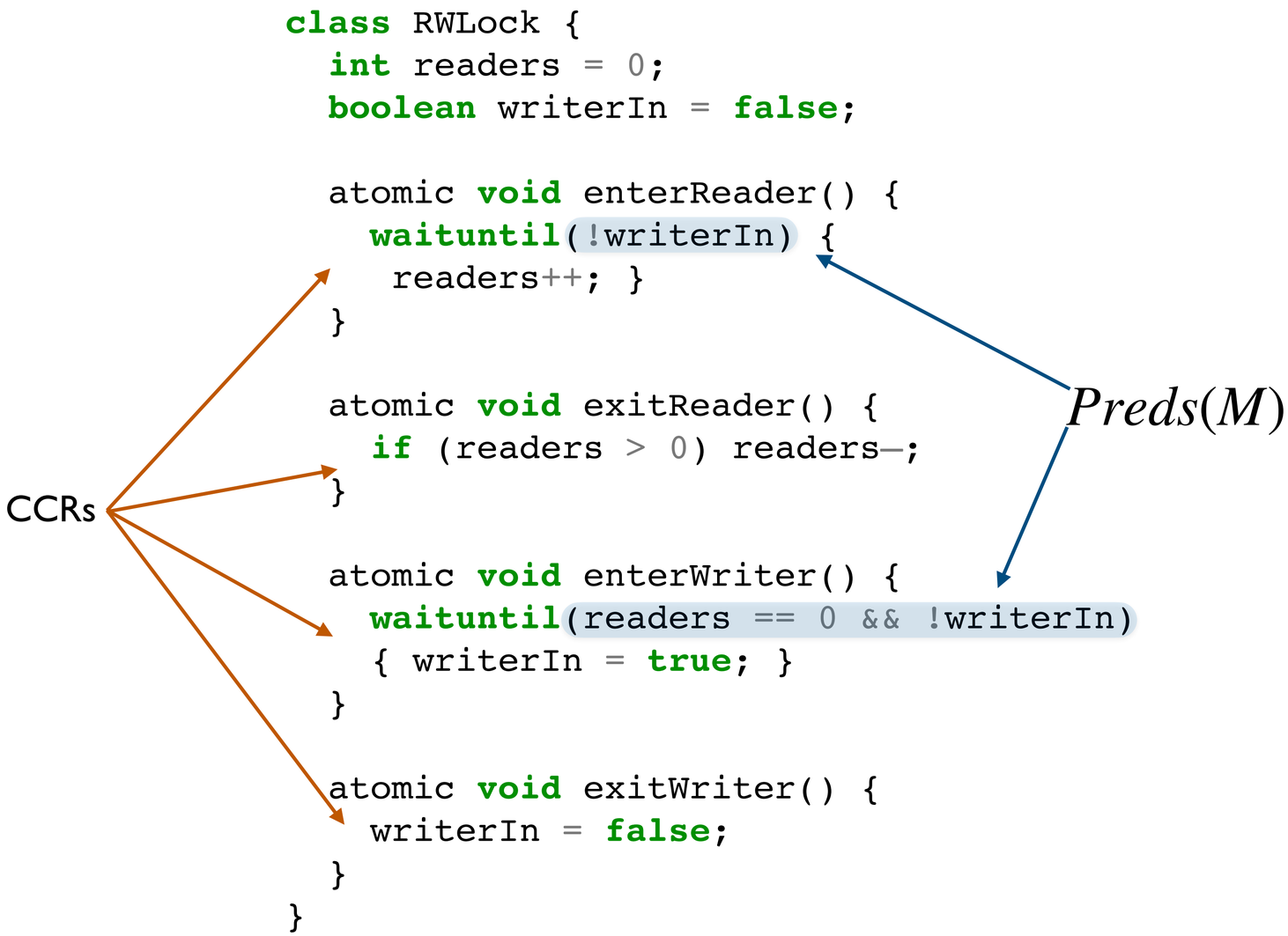
  atomic void exitWriter() {
    writerIn = false;
  }
}
```

CCRs

$Preds(M)$

Need to make signaling decisions for each combination of CCRs and predicates (8 pairs)

# Lots of Possible Implementations




Need to make signaling decisions for each combination of CCRs and predicates (8 pairs)

So $5^8$ different ways to implement explicit monitor! (ignoring locking)

# Optimal Signaling for this Example

```
class RWLock {
  int readers = 0;
  boolean writerIn = false;

  atomic void enterReader() {
    waituntil(!writerIn) {
     readers++; }
  }

  atomic void exitReader() {
    if (readers > 0) readers–;
  }

  atomic void enterWriter() {
    waituntil(readers == 0 && !writerIn)
    { writerIn = true; }
  }

  atomic void exitWriter() {
    writerIn = false;
  }
}
```

← No signaling necessary

# Optimal Signaling for this Example

```
class RWLock {
  int readers = 0;
  boolean writerIn = false;

  atomic void enterReader() {
    waituntil(!writerIn) {
     readers++; }
  }

  atomic void exitReader() {
    if (readers > 0) readers–;
  }

  atomic void enterWriter() {
    waituntil(readers == 0 && !writerIn)
    { writerIn = true; }
  }

  atomic void exitWriter() {
    writerIn = false;
  }
}
```

No signaling necessary

Condition var representing !writerIn

```
readC.signalAll();
```

Unconditional broadcast to readers

# Optimal Signaling for this Example

```
class RWLock {
  int readers = 0;
  boolean writerIn = false;

  atomic void enterReader() {
    waituntil(!writerIn) {
     readers++; }
  }

  atomic void exitReader() {
    if (readers > 0) readers--;
  }

  atomic void enterWriter() {
    waituntil(readers == 0 && !writerIn)
    { writerIn = true; }
  }

  atomic void exitWriter() {
    writerIn = false;
  }
}
```

Conditionally signal a single writer:

```
if(readers == 0) writeC.signal();
```

No signaling necessary

Condition var representing !writerIn

```
readC.signalAll();
```

Unconditional broadcast to readers

# Optimal Explicit Monitor

```
class RWLock {
  int readers = 0;
  boolean writerIn = false;

  Lock l = new ReentrantLock();
  Condition readC = l.newCondition(), writeC = l.newCondition();

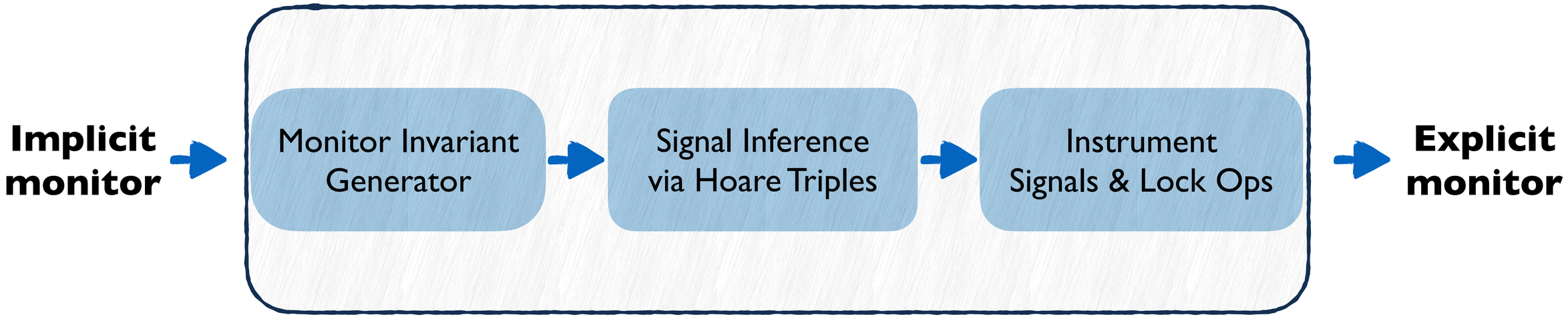
  void enterReader() {
    l.lock();
    while(writerIn) readC.await();
    readers++;
    l.unlock();
  }

  void exitReader() {
    l.lock();
    if (readers > 0) readers--;
    if (readers == 0 && !writerIn) writeC.signal();
    l.unlock();
  }

  void enterWriter() {
    l.lock();
    while(readers != 0 || writerIn) writeC.await();
    writerIn = true;
    l.unlock();
  }

  void exitWriter() {
    l.lock();
    writerIn = false;
    if (readers == 0 && !writerIn) writeC.signal();
    readeC.signalAll();
    l.unlock();
  }}
```

# Synthesis Workflow



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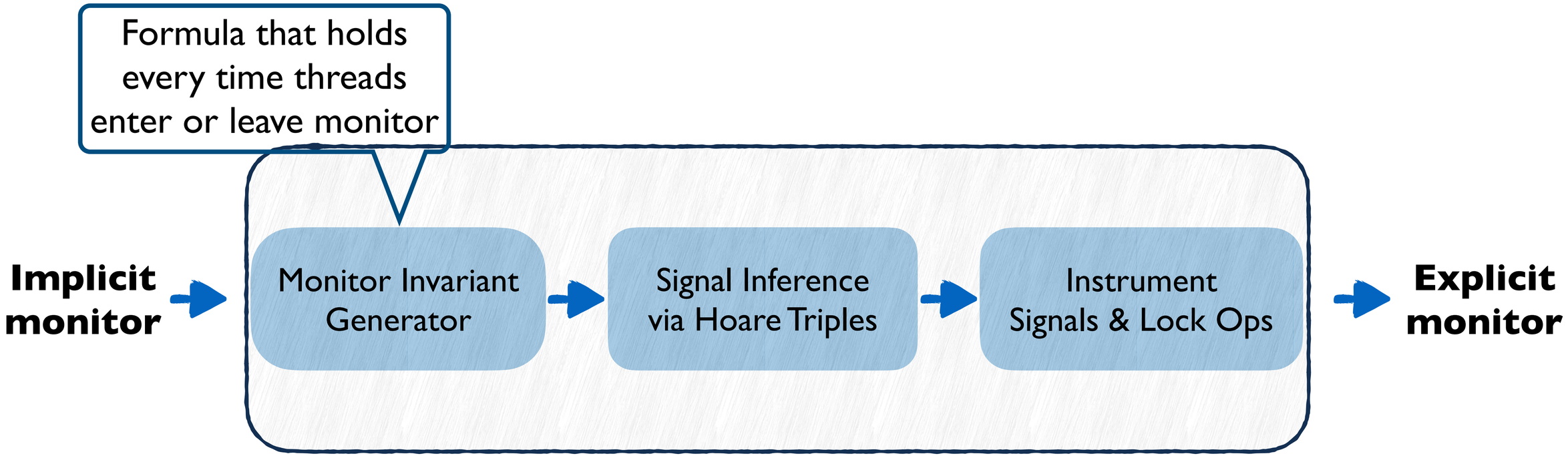

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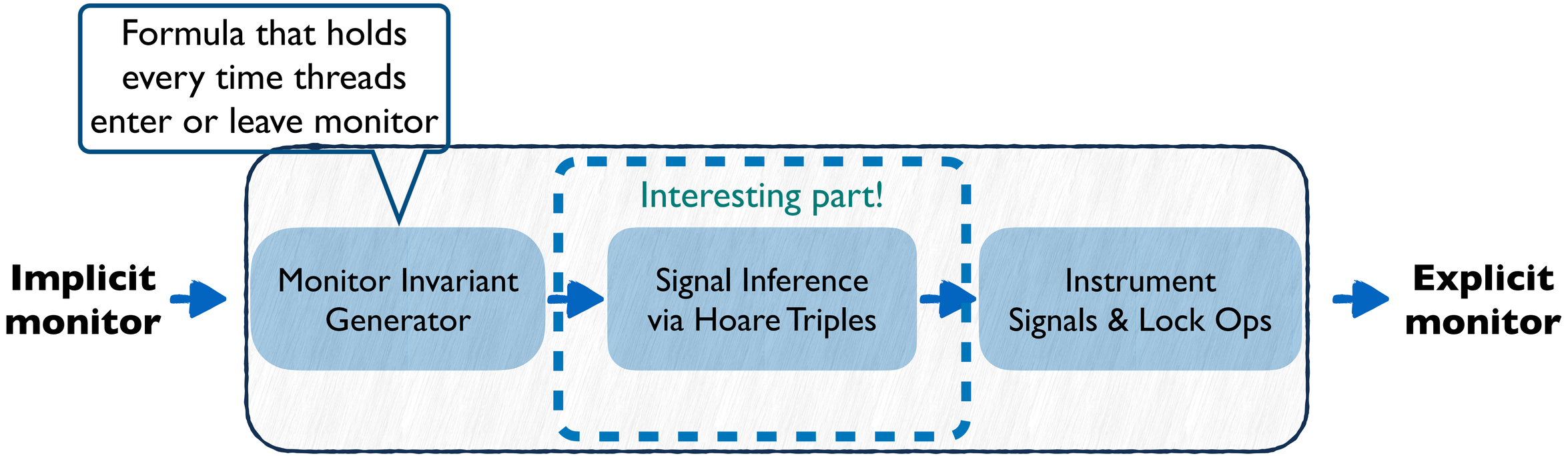

# Primer on Hoare Triples

Hoare Triple: $\{ P \} S \{ Q \}$

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Is Q guaranteed to hold after executing S?

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$$\{ count \geq 0 \}$$

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**Example of valid triple**

$\{ count \geq 0 \}$ `count++;`

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Starting in a state where P holds

Is Q guaranteed to hold after executing S?

Hoare Triple: $\{ P \} S \{ Q \}$

If yes, we call a triple valid

**Example of valid triple**

$\{ count \geq 0 \}$ `count++;` $\{ count \geq 0 \}$

# Signaling Decisions as Hoare Triples


To Signal or Not:
Given CCR $C$, do we need any signaling for threads blocked on predicate $P \in Preds(M)$?

$$\{Inv \wedge \neg P\}\ C\ \{\neg P\}$$

# Signaling Decisions as Hoare Triples


To Signal or Not:
Given CCR $C$, do we need any signaling for threads blocked on predicate $P \in Preds(M)$?

If this triple is valid, **no need** to **signal** threads blocked on P!

$$\{Inv \wedge \neg P\}\ C\ \{\neg P\}$$

# Example: Signal or Not?

**CCR:**

```
atomic void enterReader() {

  waituntil(!writerIn){
    readers++;
  }

}
```

Need to signal writers after enterReader?

# Example: Signal or Not?

**Predicate:** $P_w \equiv readers = 0 \wedge \neg writerIn \quad \neg P_w \equiv readers \neq 0 \vee writerIn$

**CCR:**

```
atomic void enterReader() {

  waituntil(!writerIn){
    readers++;
  }

}
```

Need to signal writers after enterReader?

# Example: Signal or Not?

**Predicate:** $P_w \equiv readers = 0 \wedge \neg writerIn \quad \neg P_w \equiv readers \neq 0 \vee writerIn$ **Invariant:** $readers \geq 0$

**CCR:**

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atomic void enterReader() {

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}
```

Need to signal writers after enterReader?

# Example: Signal or Not?

**Predicate:** $P_w \equiv readers = 0 \wedge \neg writerIn \quad \neg P_w \equiv readers \neq 0 \vee writerIn$ **Invariant:** $readers \geq 0$

**CCR:**

```
atomic void enterReader() {
  {readers ≥ 0 ∧ ¬P_w}
  waituntil(!writerIn){
    readers++;
  }
  {¬P_w}
}
```

Need to signal writers after enterReader?

# Example: Signal or Not?

**Predicate:** $P_w \equiv readers = 0 \wedge \neg writerIn$ $\neg P_w \equiv readers \neq 0 \vee writerIn$ **Invariant:** $readers \geq 0$

**CCR:**

```
atomic void enterReader() {
  {readers ≥ 0 ∧ ¬P_w}
  waituntil(!writerIn){
     readers++;
  }
  { ¬P_w}
}
```

Need to signal writers after enterReader?

Triple is valid, no need to signal writers!

# Summary of Signaling

Key Idea: Reduce signaling decisions to validity of Hoare triples

- Once the signaling decisions are made, straightforward to instrument code with operations on condition vars

- To ensure atomicity and data-race-freedom, use one global lock acquired/released before/after each operation

# Implementation & Evaluation


- Evaluated on several monitors from popular GitHub repos.
  - Real-world applications: *Spring*, *Gradle*, etc.
  - Efficient explicit-signal implementations.
- Converted explicit monitor to implicit and pass it to Expresso

# Evaluation, cont

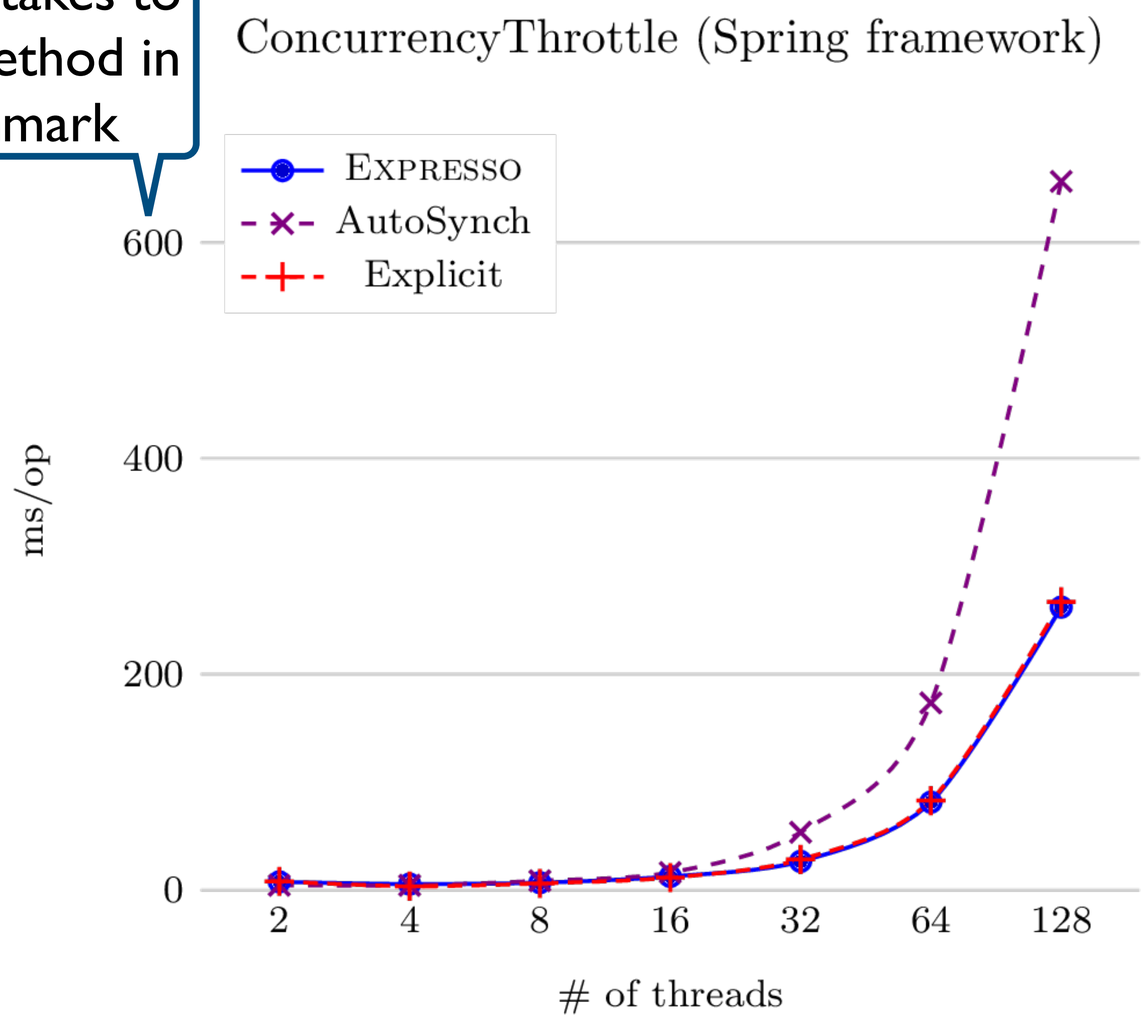
Compared ***EXPRESSO*** against:

- AutoSynch [1]: **state-of-the-art** runtime system for implicit monitors.
- Explicit: original implementation by expert programmer.

[1] Wei-Lun Hung et al. **AutoSynch**: An Automatic signal Monitor Based on Predicate Tagging **PLDI'13**

# Results

How long it takes to execute a method in the benchmark



# Results

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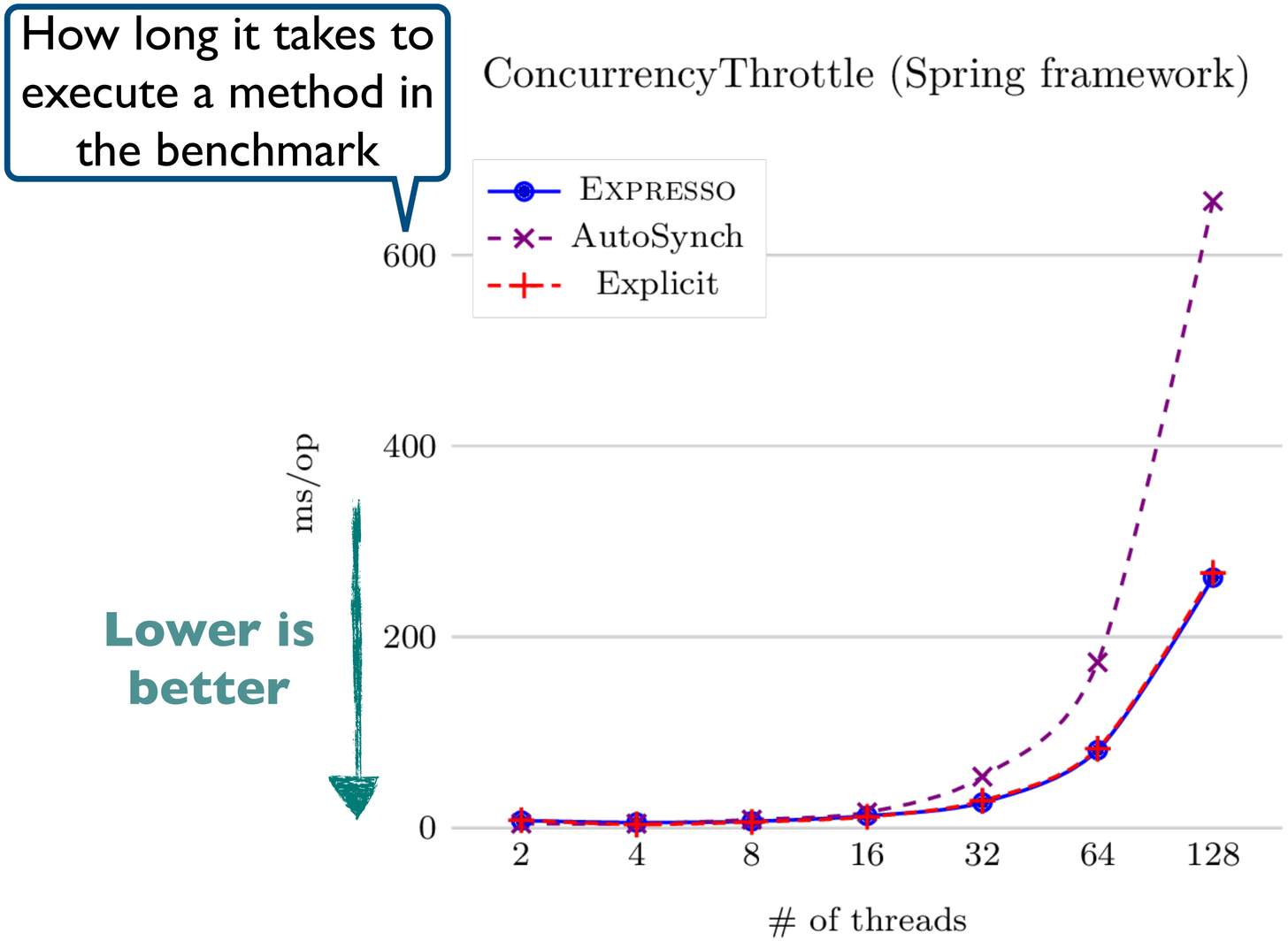
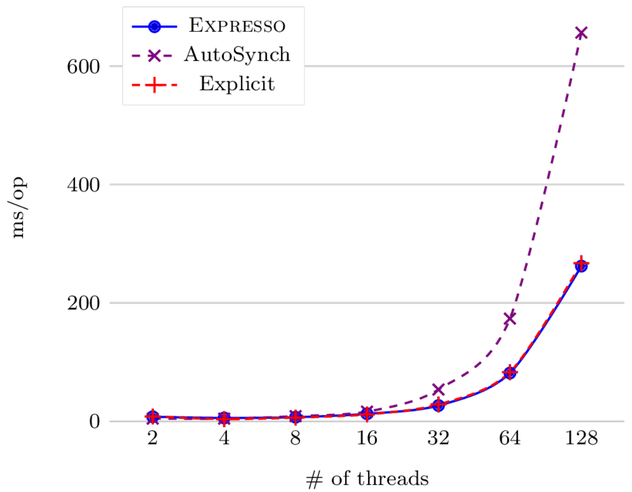


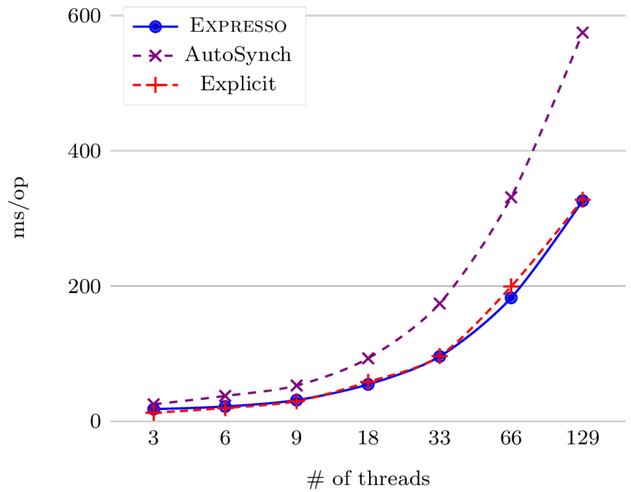

**Lower is better**

# Results, cont

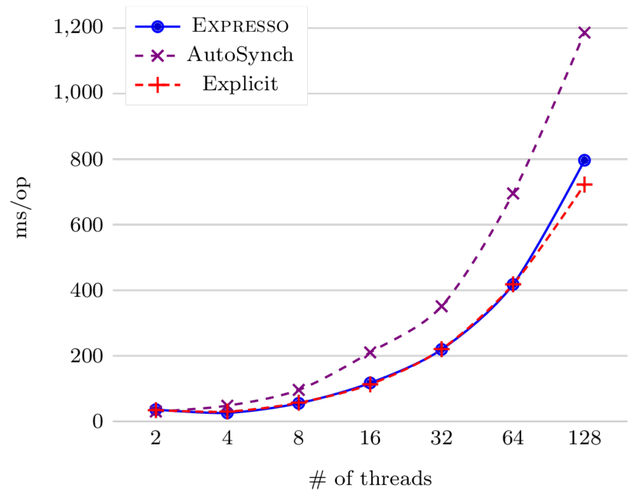
ConcurrencyThrottle (Spring framework)



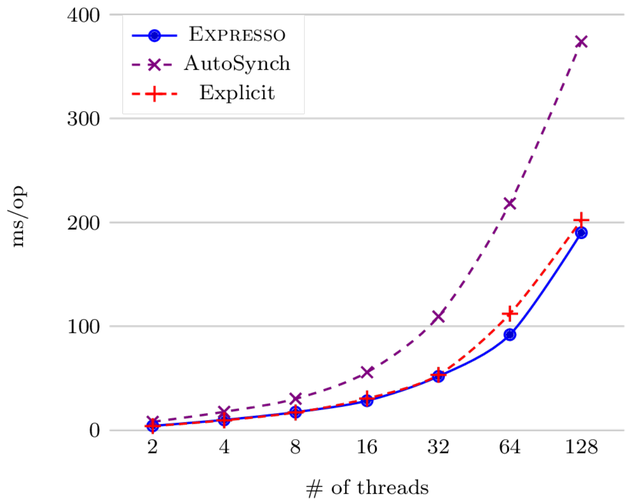

PendingPostQueue (EventBus)



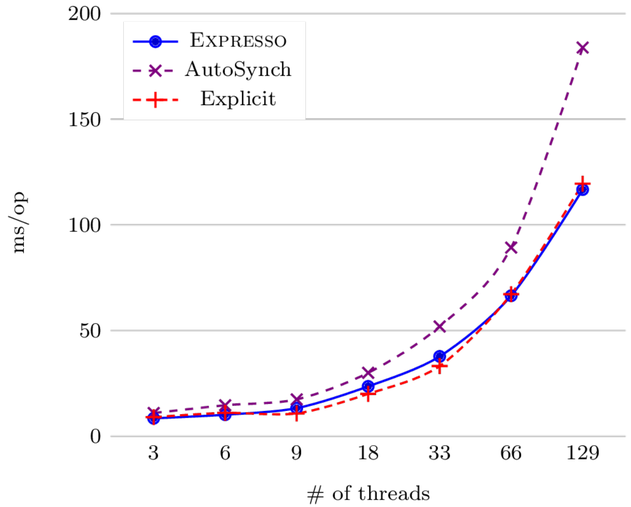

AsyncDispatch (Gradle)



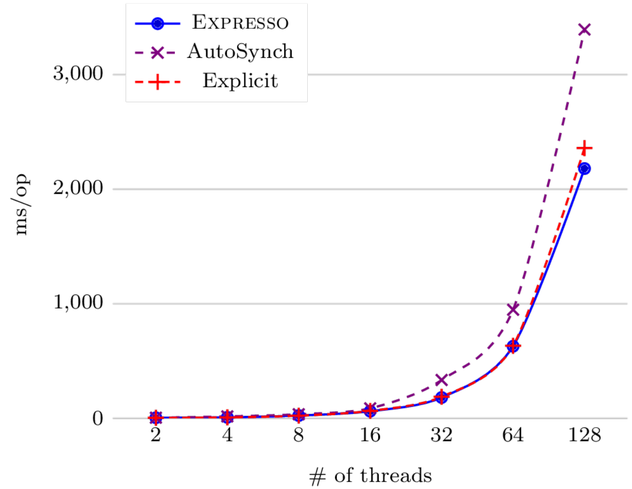

SimpleBlockingDeployment (Gradle)



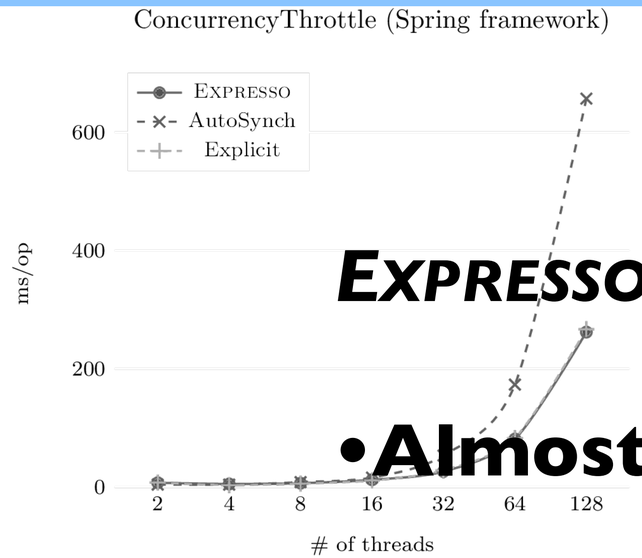

SimpleDecoder (ExoPlayer)

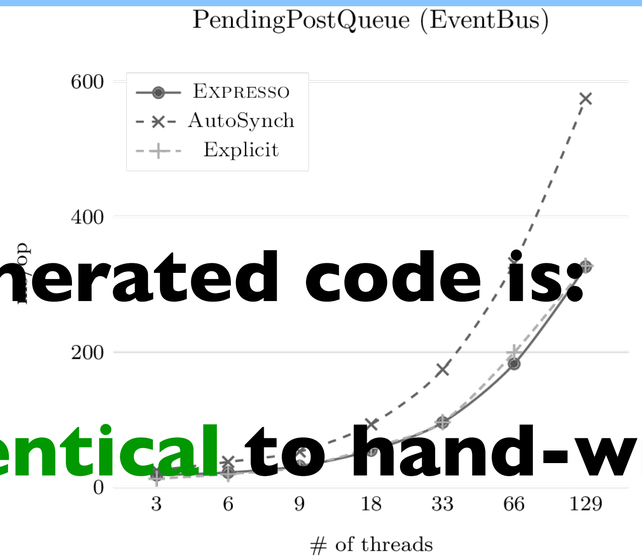


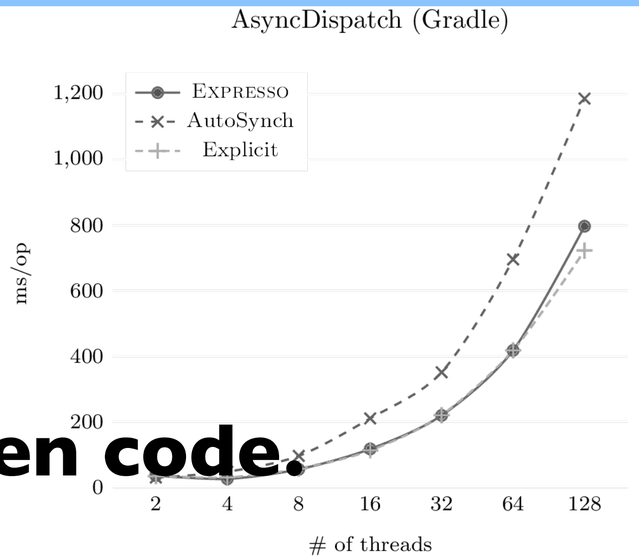

AsyncOperationExecutor (greenDAO)

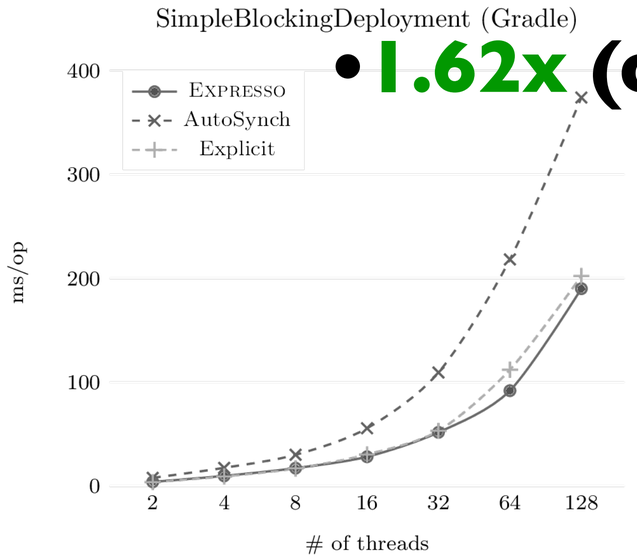


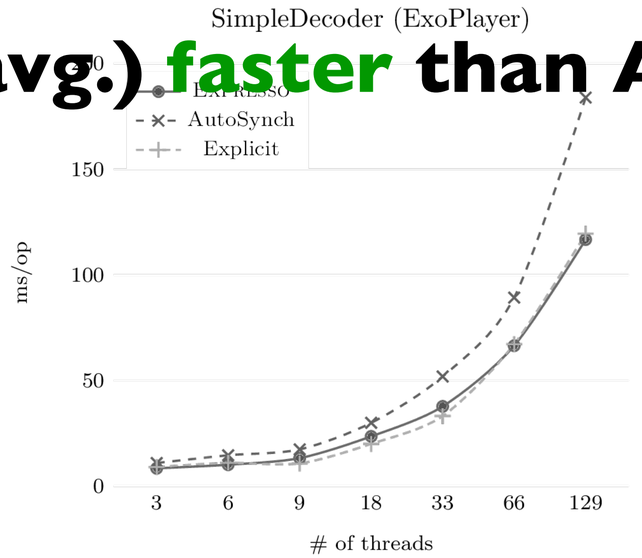
# Results, cont

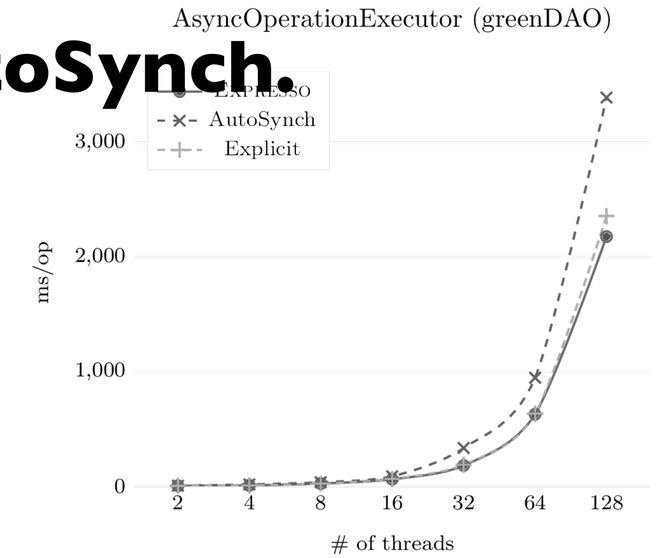



**EXPRESSO generated code is:**

- **Almost identical to hand-written code.**
- **1.62x (on avg.) faster than AutoSynch.**

# Road Map

**Part I:** How to automatically synthesize necessary signaling code

Symbolic Reasoning for Automatic Signal Placement.
Ferles et al, PLDI'18.

**Part II:** How to automatically synthesize efficient locking

Synthesizing Fine-grained Synchronization Protocols for Implicit Monitors.
Ferles et al, OOPSLA'22.

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# Recall

*Implicit monitor* → 

→ *Explicit monitor*

Expresso uses a *single global lock* acquired by all CCRs to ensure atomicity

***This can be suboptimal in many cases!***

# Part II: Synthesizing Fine-Grained Locking

In some cases, multiple threads can run ***concurrently*** in a monitor without violating the object's atomicity

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In some cases, multiple threads can run ***concurrently*** in a monitor without violating the object's atomicity

Each method *appears* to execute atomically even though execution of methods can be interleaved

Idea: Improve performance by synthesizing ***fine-grained locking*** in a way that will provide an *illusion* of atomicity

# Example

```
class ArrayBlockingQueue {
  int first = 0, last = 0, count = 0;
  Object[] queue;

  ArrayBlockingQueue(int capacity) {
    assert capacity < 1;
    this.queue = new Object[capacity];
  }

  atomic void put(Object o) {
    waituntil(count < queue.len){
      queue[last] = o;
      last = (last + 1) % queue.len;
      count++;
    }
  }

  atomic Object take() {
    waituntil(count > 0){
      Object r = queue[first];
      queue[first] = null;
      first = (first + 1) % queue.len;
      count--;
      return r;
    }
  }
}
```

Blocking FIFO Queue:

- put blocks if queue is full
- take blocks if queue is empty

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    }
  }
}
```

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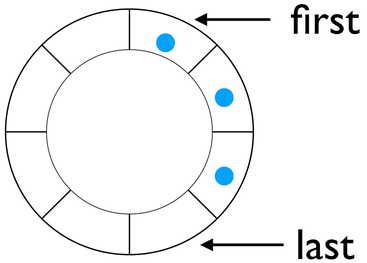
Note: put and take can run *concurrently*



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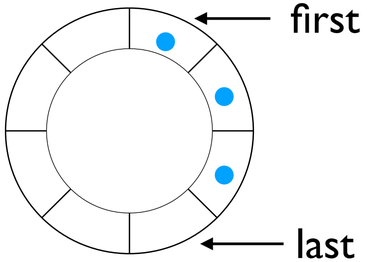


! A global lock would prevent such parallelization opportunities

# Example, cont

```
class ArrayBlockingQueue {
  Lock putLock = new Lock(),
       takeLock = new Lock();
  Condition notFull = putLock.newCondition();
  Condition notEmpty = takeLock.newCondition();

  int first = 0, last = 0; Object[] queue;
  AtomicInteger count = new AtomicInteger(0);

  void put(Object o) {
    putLock.lock();
    while (count.get() == queue.length)
      notFull.await();
    queue[last] = o;
    last = (last + 1) % queue.length;
    count.getAndIncrement();
    putLock.unlock();
    // Signalling code …
  }

  Object take() {
    takeLock.lock();
    while (count.get() == 0)
      notEmpty.await();
    Object r = queue[first];
    queue[first] = null;
    first = (first + 1) % queue.length;
    count.getAndDecrement();
    takeLock.unlock();
    // Signalling code …
    return r;
  }
}
```

**Optimal**:
maximizes parallelism

# Example, cont

```
class ArrayBlockingQueue {
  Lock putLock = new Lock(),
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  void put(Object o) {
    putLock.lock();
    while (count.get() == queue.length)
      notFull.await();
    queue[last] = o;
    last = (last + 1) % queue.length;
    count.getAndIncrement();
    putLock.unlock();
    // Signalling code …
  }

  Object take() {
    takeLock.lock();
    while (count.get() == 0)
      notEmpty.await();
    Object r = queue[first];
    queue[first] = null;
    first = (first + 1) % queue.length;
    count.getAndDecrement();
    takeLock.unlock();
    // Signalling code …
    return r;
  }
}
```

two locks

**Optimal**:
maximizes parallelism

# Example, cont

```
class ArrayBlockingQueue {
  Lock putLock = new Lock(),
       takeLock = new Lock();
  Condition notFull = putLock.newCondition();
  Condition notEmpty = takeLock.newCondition();

  int first = 0, last = 0; Object[] queue;
  AtomicInteger count = new AtomicInteger(0);

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    queue[last] = o;
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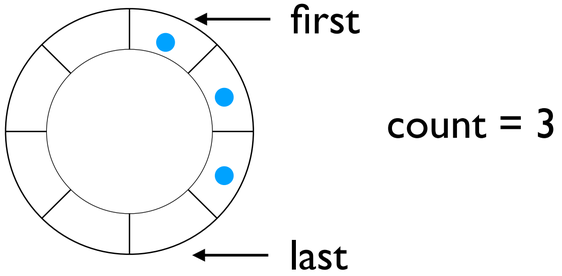
# Why is this correct?

## (1) Does not contain any races

- No race between queue[first] and queue[last]
- Races on count are handled by AtomicInteger



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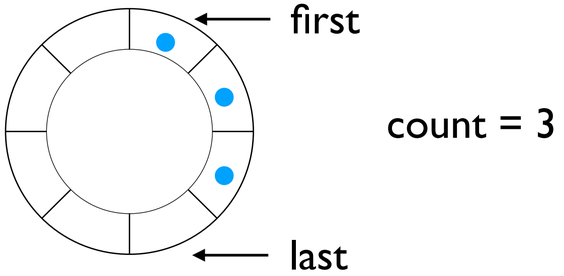
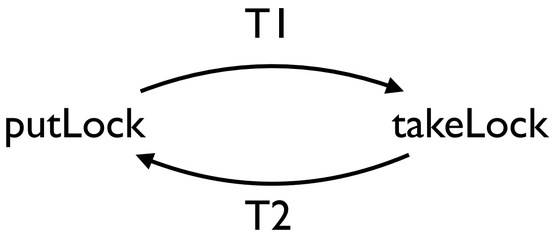



## (2) Monitor is deadlock-free

- No cycles in the lock acquisition order



# Why is this correct? (cont.)

## (3) All operations *appear* to execute as one indivisible unit

- Executions where threads interleave are equivalent to sequential executions.

T1 `wait(count < len)` `queue[last] = o;…` `count++;`

T2 `wait(count > 0)` `r = queue[first];…` `count--;`

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- The locking scheme only allows such *safe interleavings*

Gives an ***illusion*** of atomicity!

# Take-Away from Example

*Goal*: M*aximize* parallelization opportunities & obey correctness requirements:
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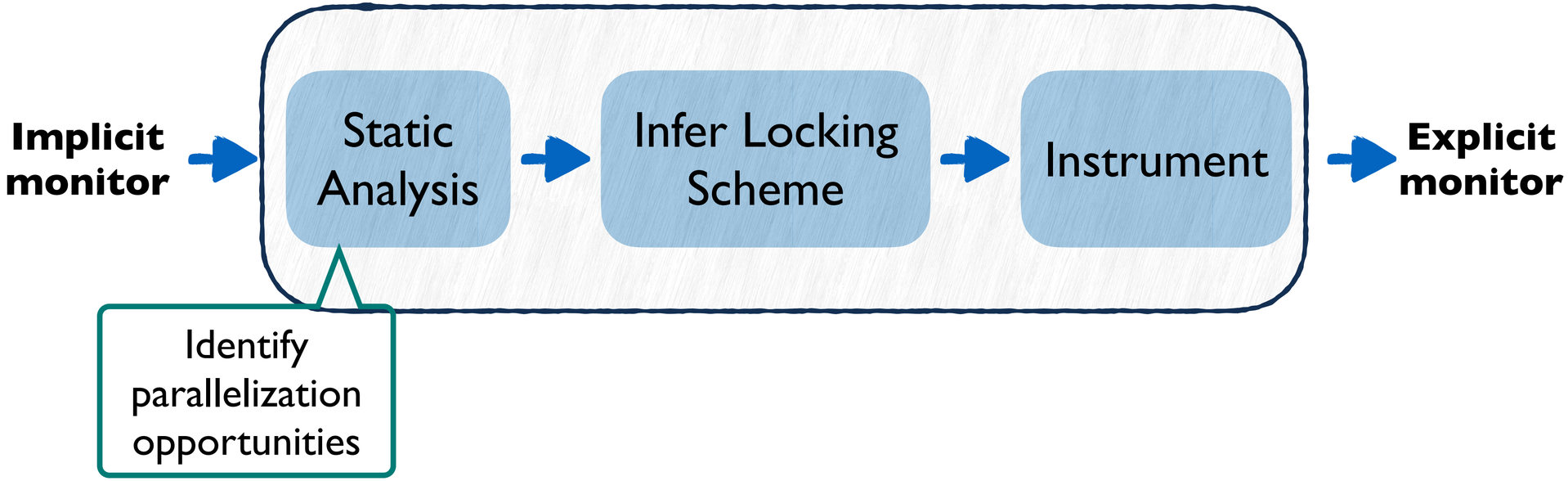

# Static Analysis

**First splits input monitor to disjoint code snippets**

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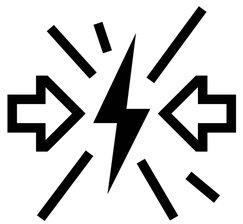

*Data races*

$\{(S, S') \mid \text{Racy}(S, S')\}$

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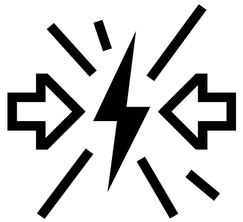

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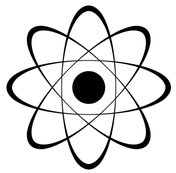

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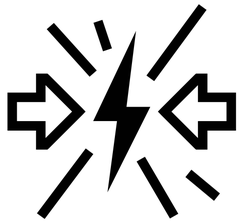

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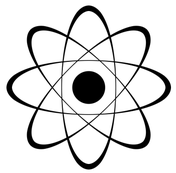

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*Safe interleaving opportunities*

$\{(S, S1, S2) \mid \text{SafeInterleaving}(S, S1, S2)\}$

# Detecting Safe Interleavings

**Theorem:** S can be interleaved in between S1 and S2 if it ***left-commutes*** with every ***predecessor*** of S1 and ***right-commutes*** with every ***successor*** of S2

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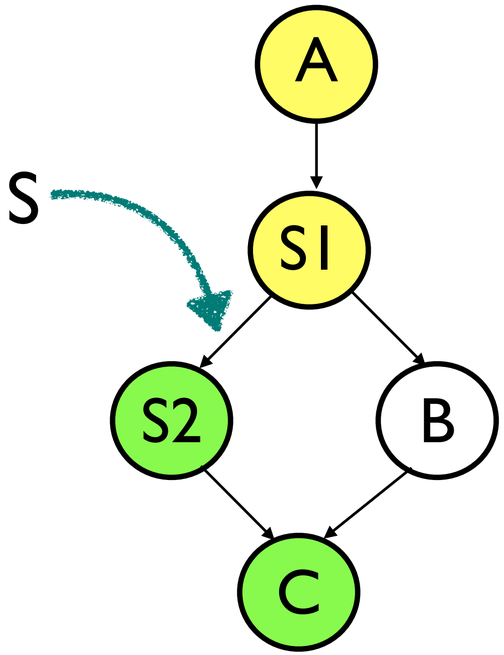


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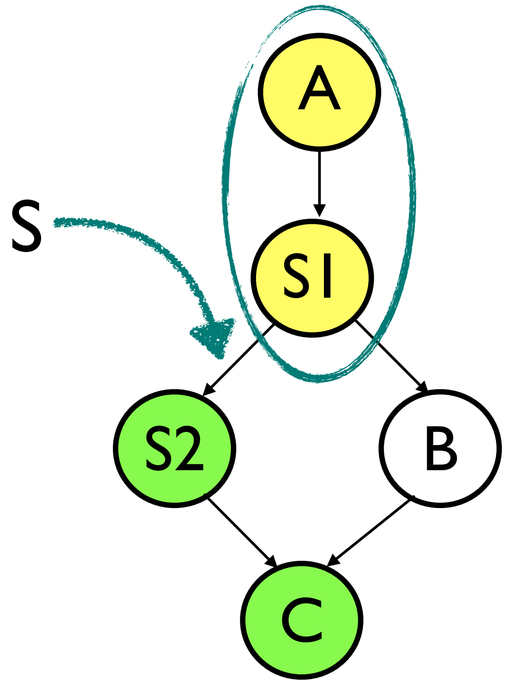


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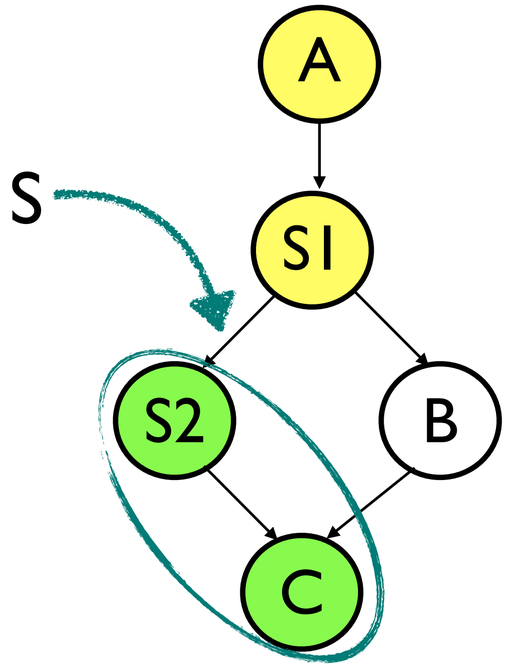


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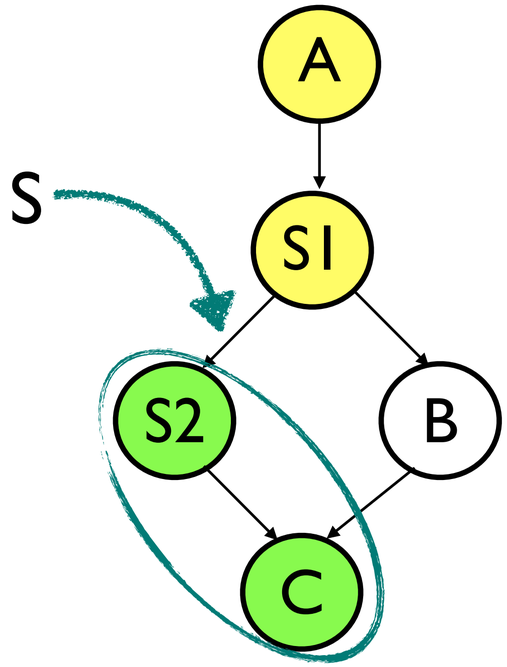


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Program equivalence check

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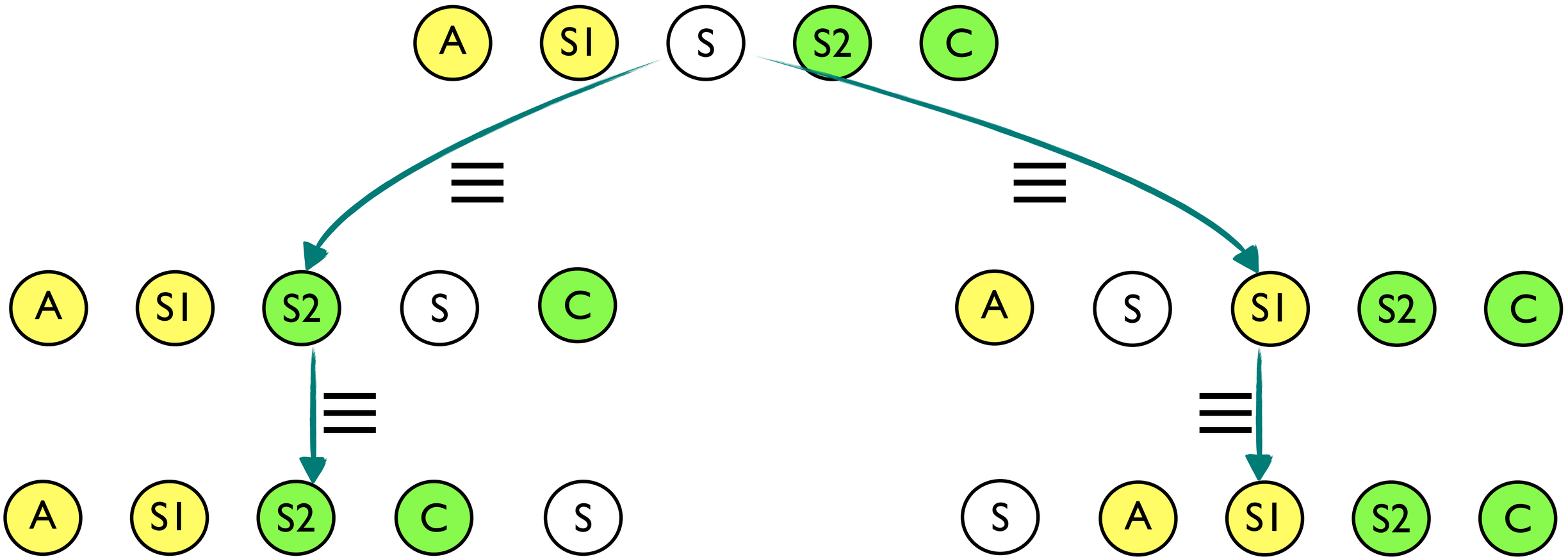
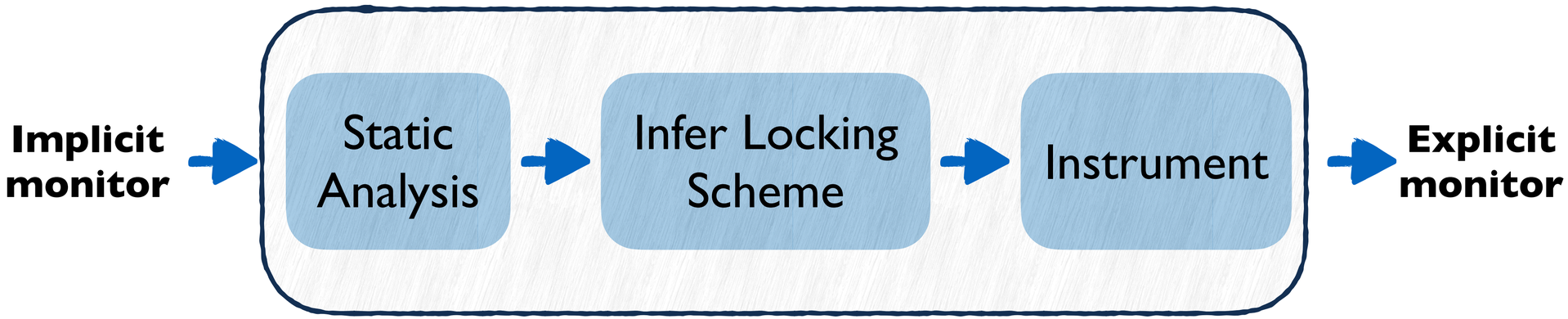


# Synthesis Framework



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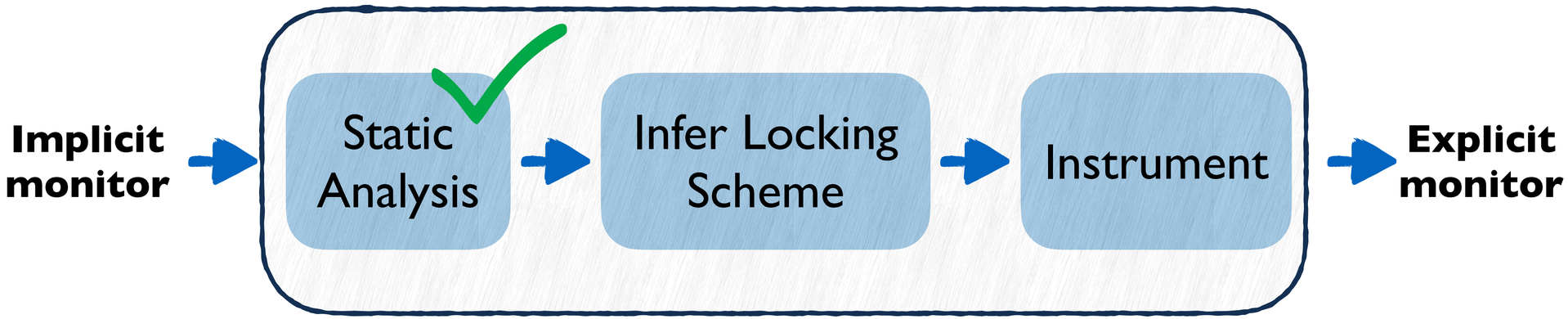

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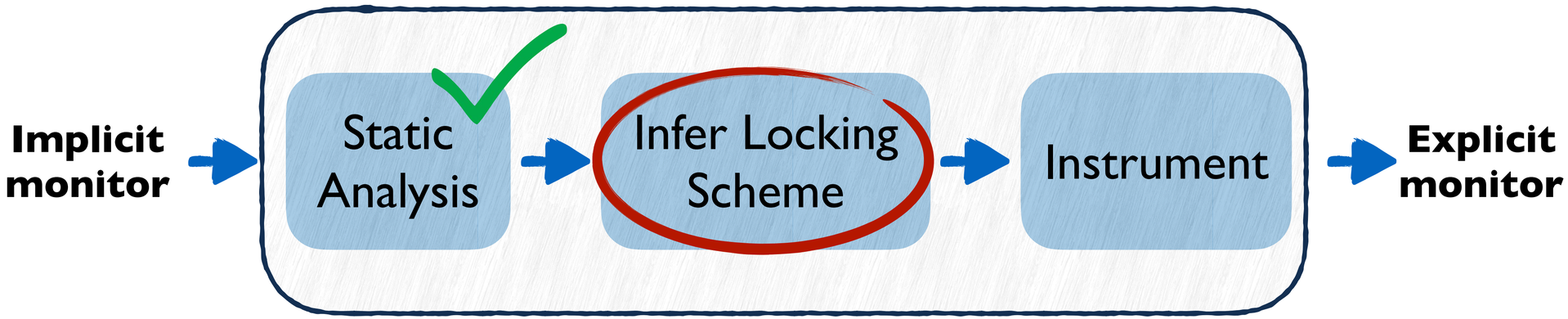

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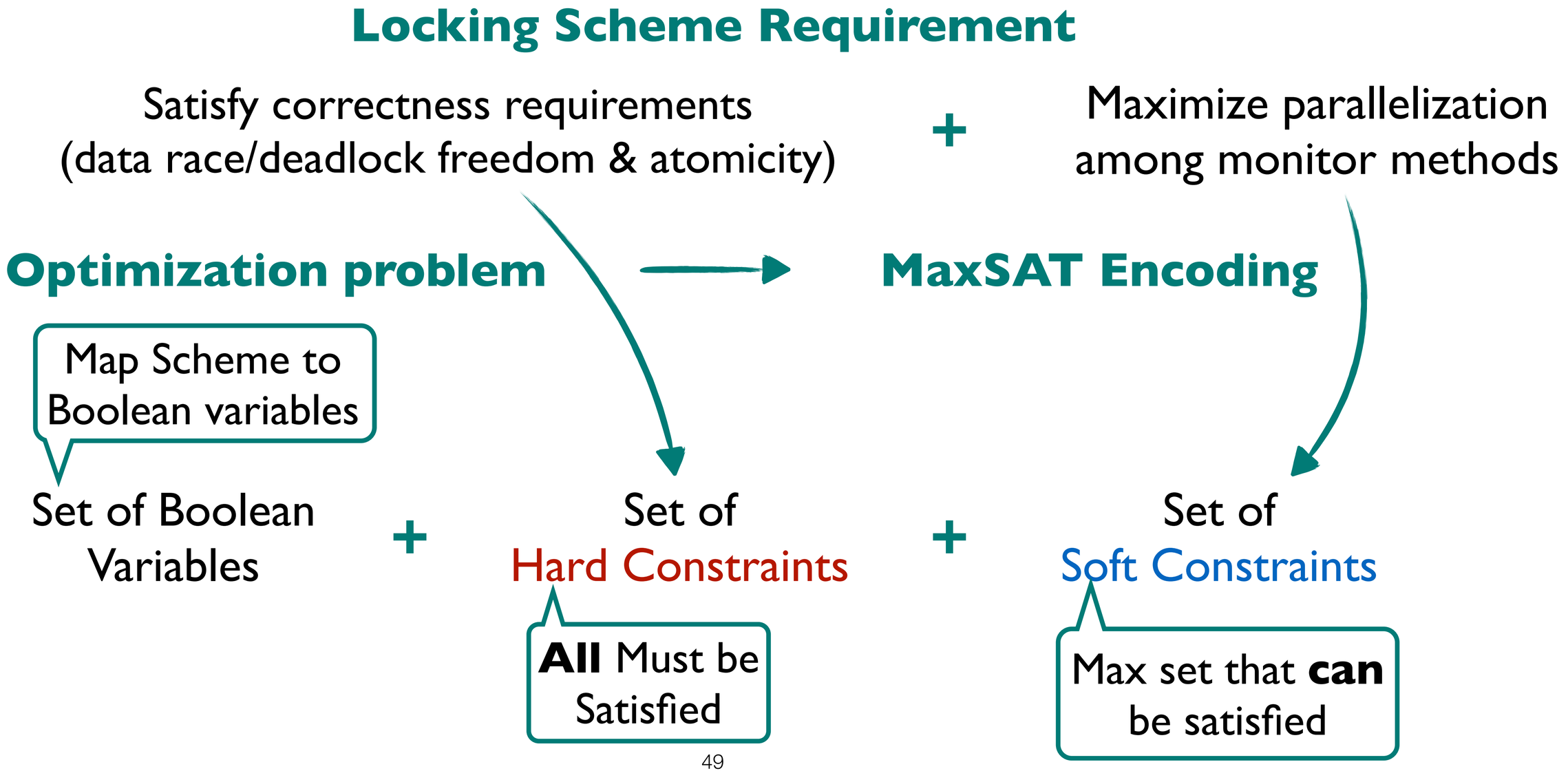

# MaxSAT Encoding Variables

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Lockset for snippet S

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$\alpha_f$ Indicates that field f must be implemented as atomic

$$f \in PossibleAtomicFields(M)$$

# Correctness Requirements
## (Hard constraints)

Data-race freedom

Atomicity

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Resolve data races with locks

If S1 and S2 have a data race, then generate constraint:

$$\mathscr{L}(S1) \cap \mathscr{L}(S2) \neq \emptyset$$

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## Atomicity

Only permit safe interleavings

If (S, S1, S2) is not a safe interleaving, then generate the following constraint

$$\mathscr{L}(S) \cap \mathscr{L}(S_1) \cap \mathscr{L}(S_2) \neq \emptyset$$

# Performance Objectives
## (Soft constraints)

Encode performance objective
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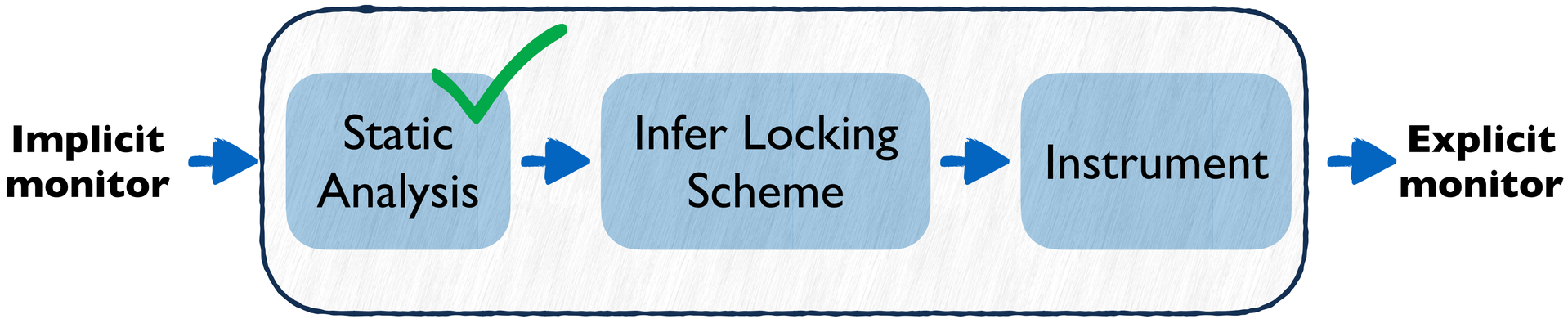
Maximize number of code snippets that can run in parallel

Minimize number of locks and atomic fields

# Synthesis Framework



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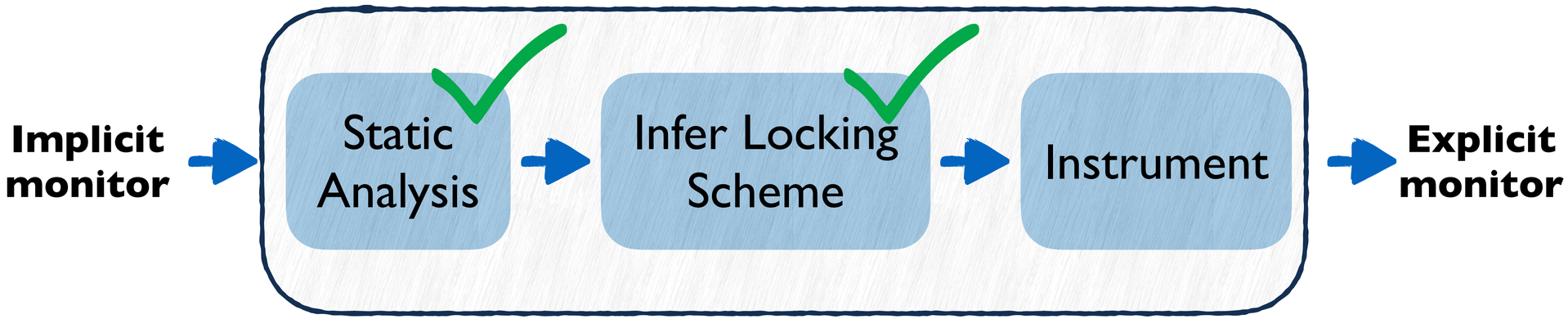
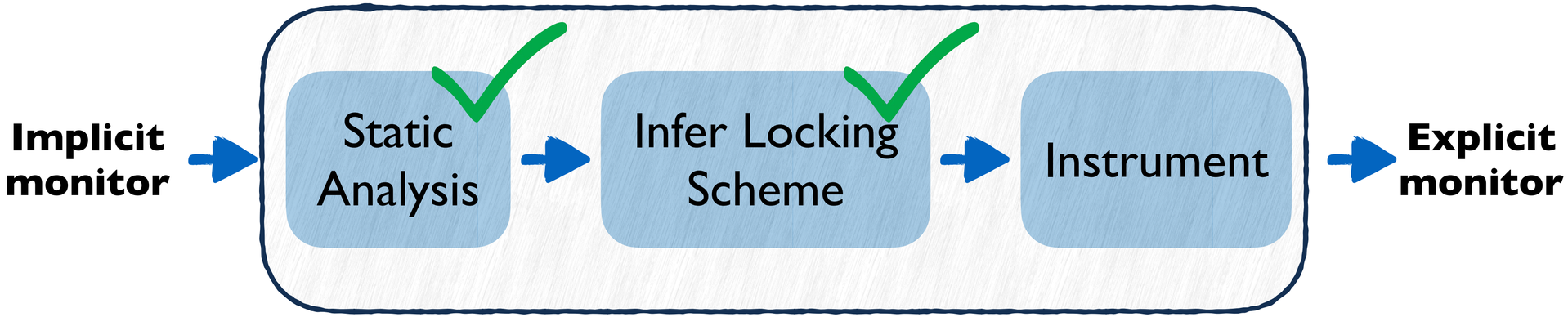
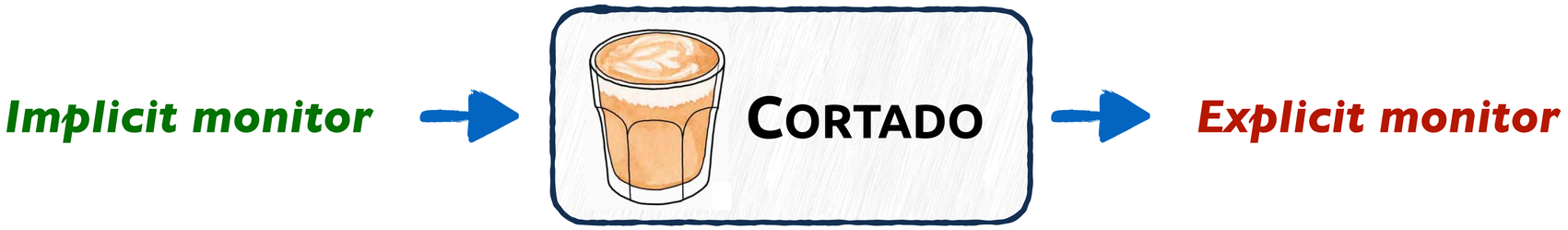


# Synthesis Framework

Key Idea: Statically detect parallelism and reduce locking scheme inference to MaxSAT

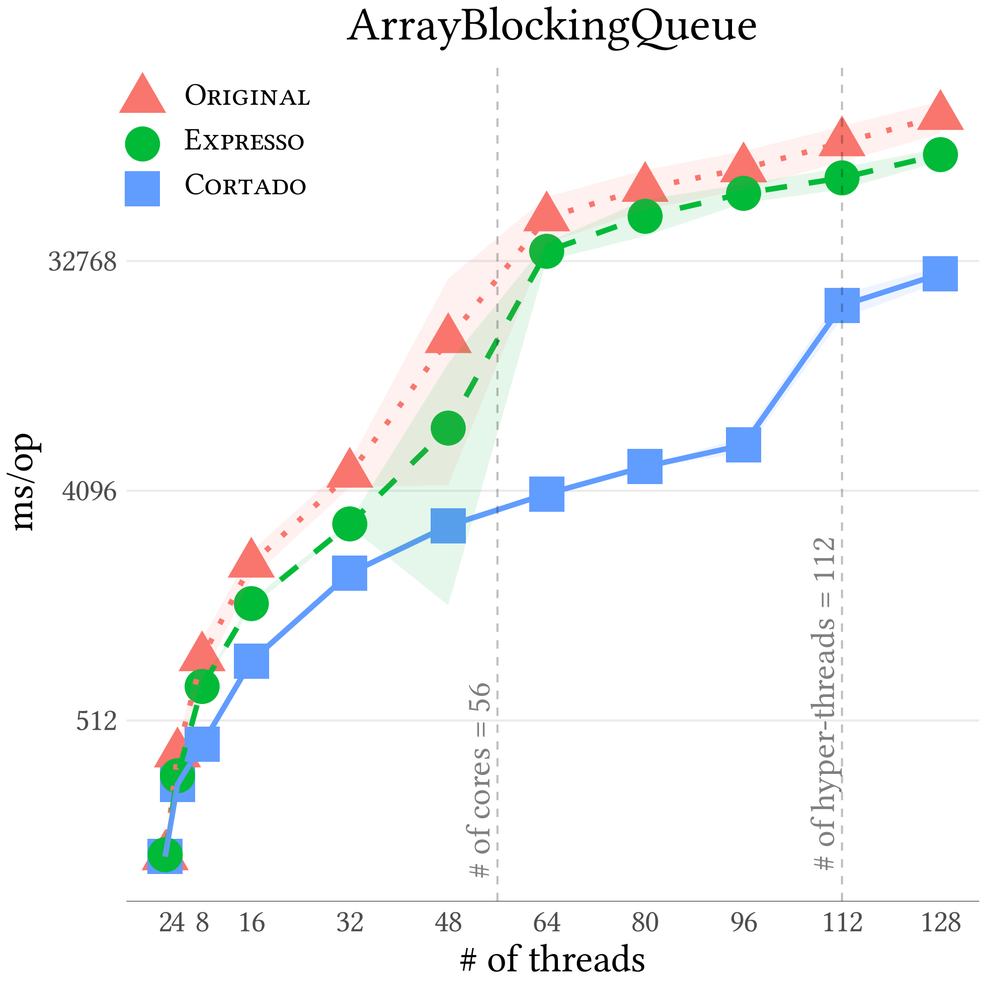


# Implementation & Evaluation



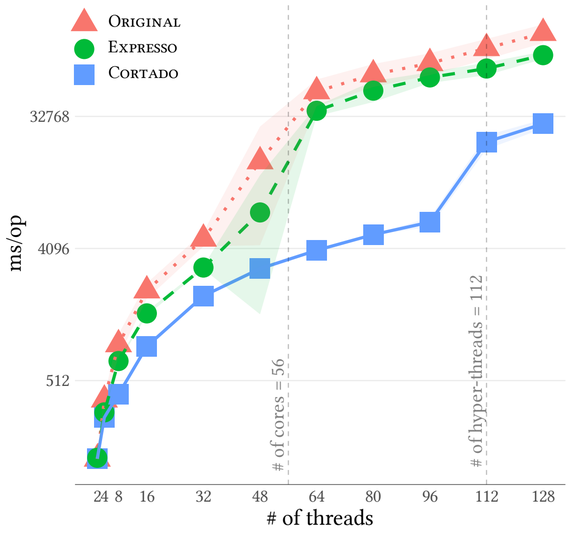

- Evaluated Cortado on monitors with parallelization opportunities
- Manually converted explicit monitor to implicit version
- Compared performance of Cortado-synthesized code against:
  - Manual version as collected from the project
  - The version generated by Expresso (uses a global lock)

# Results

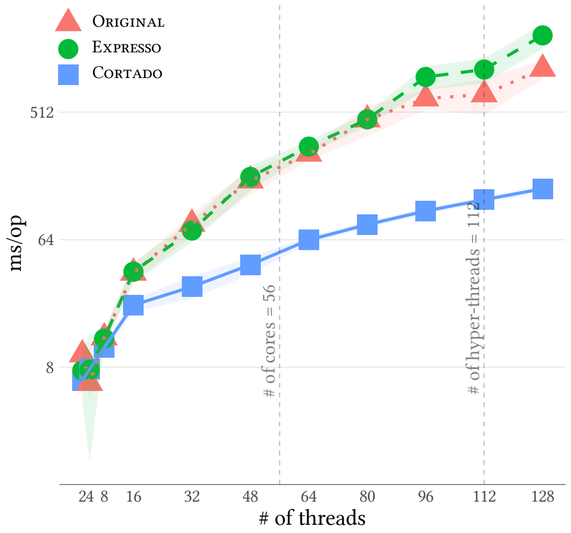

ArrayBlockingQueue
Original
Expresso
Cortado
32768
4096
512
ms/op
# of cores = 56
# of hyper-threads = 112
24 8 16 32 48 64 80 96 112 128
# of threads

# Results

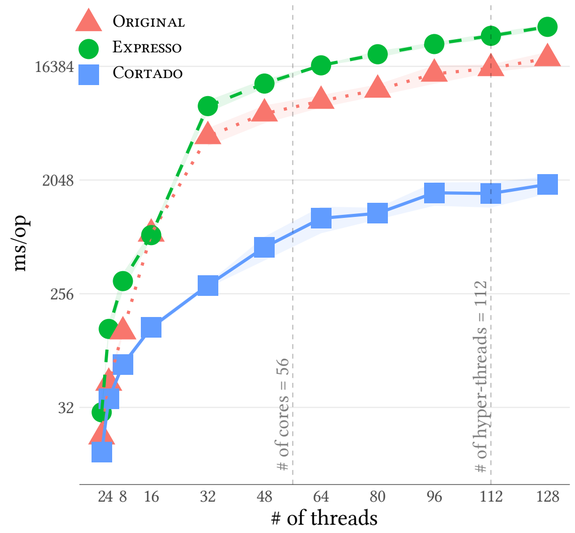
ArrayBlockingQueue



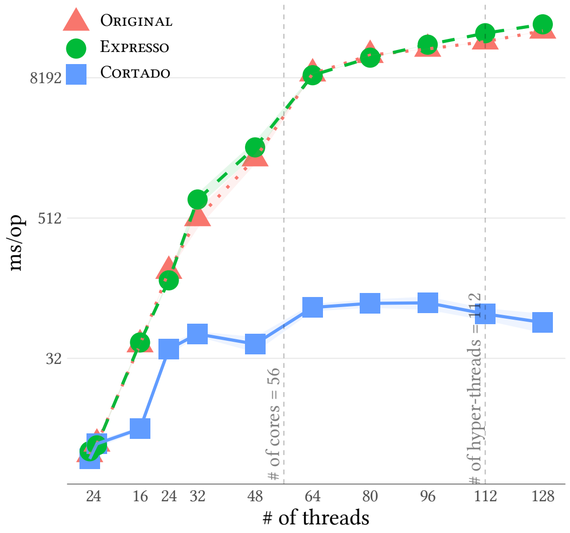

ConcurrencyThrottleSupport



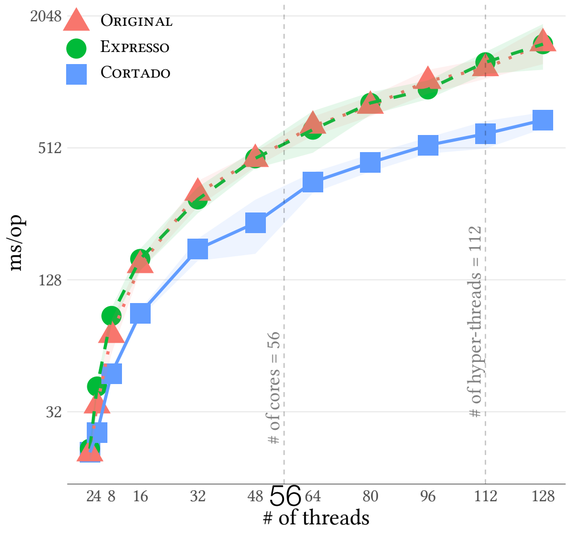

SinkQueue



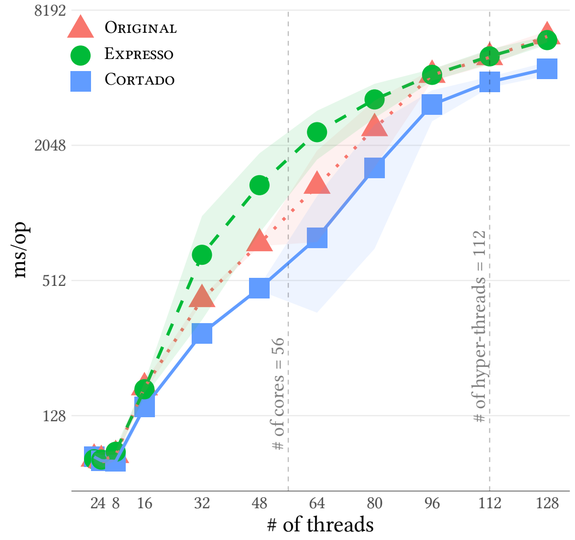

JobWrapper



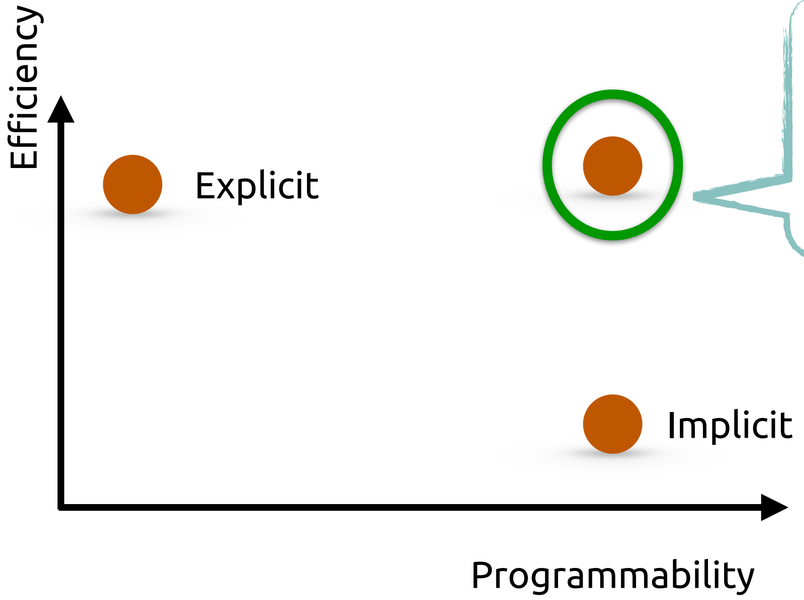

PausableThreadPoolExecutor



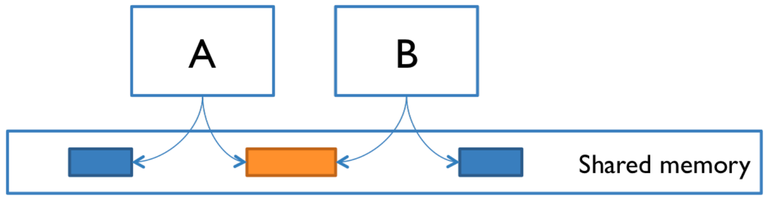

CountableThreadPool



# Summary




Provide best of both worlds wrt correctness & performance




*Implicit monitor* → EXPRESSO → *Explicit monitor*

*Implicit monitor* → CORTADO → *Explicit monitor*

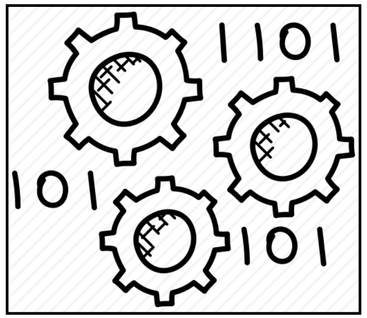
A set of formal methods techniques for simplifying concurrent programming

# Research Highlights

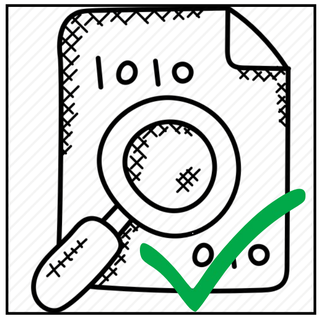
**Research Goal:** ***Formal methods for correct, efficient, and secure code!***

**Simplifying Concurrent Programming**
[PLDI'18,OOPSLA'22]

Synthesis



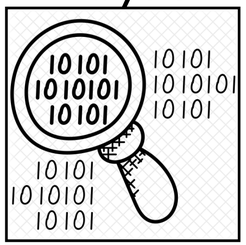

Verification




**Preventing Security Vulnerabilities**
[FSE'18,VSTTE'19,S&P'21]

**Verifying Correct Usage of APIs**
[POPL'21]

Core Program Analysis

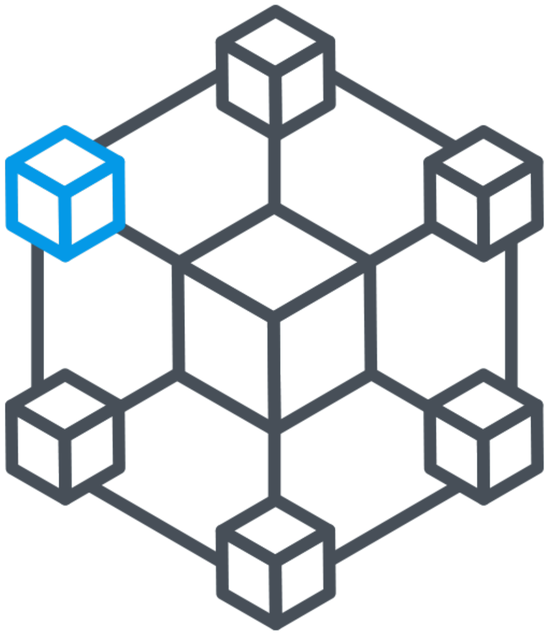



**Improve Scalability & Precision**
[FSE'17,SOAP'17,CC'18]

# Verification Techniques

## Preventing Security Vulnerabilities In Smart Contracts

**Programs running on a decentralized ledger**



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- Vulnerabilities in a contract can severely harm stakeholders

# Verification Techniques

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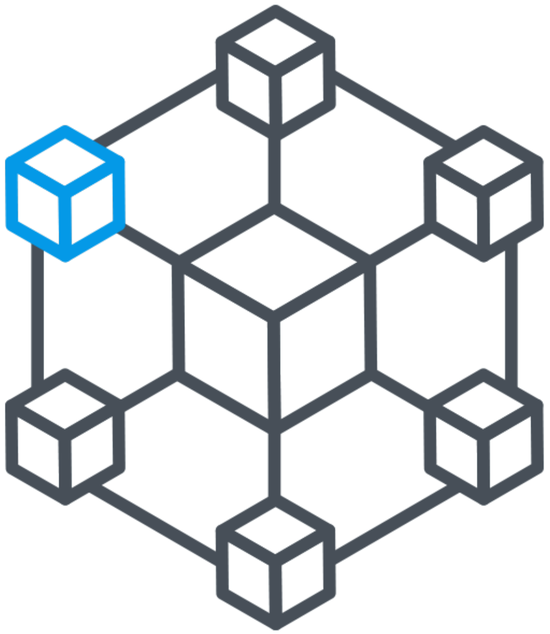


- *Motivation*: They manage a huge mount of user monetary funds
- Vulnerabilities in a contract can severely harm stakeholders
- Verification to the rescue!
  - ***VeriSol[VSTTE'19]***: contract won't reach an undesired state
  - ***SmartPulse[S&P'21]***: contract will reach a desired state

# Verification Techniques

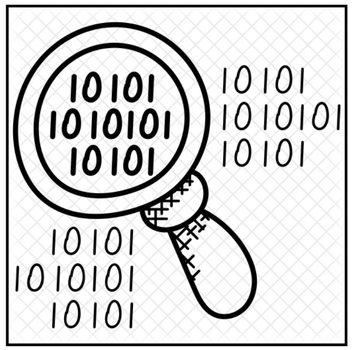
## Verifying Correct API Usage


- *Motivation*: Developers tend to misuse APIs written by others
- Prior work cannot handle important classes of APIs

  Reentrant lock API: $\texttt{l.acquire()}^n\ \texttt{l.release()}^n$

- ***CFPChecker[POPL'21]***: closes the theoretical gap for such APIs

# Core Program Analysis

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- Better program analysis tools imply better verifiers and synthesizers

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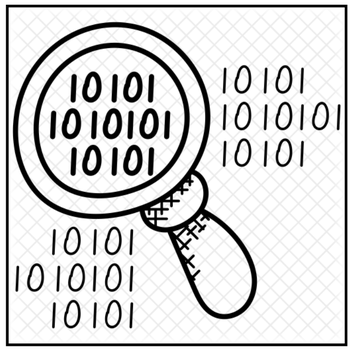


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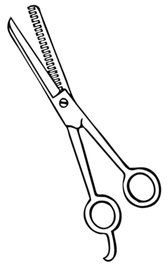

- ***Timmer[FSE'17]***: Program transformation that eliminates safe paths
- Transparently increases precision and scalability of other tools

# Future Directions

Can we push at the boundaries of formal method applications and further boost developers' confidence in their code?

**Direction I**

Verification & Synthesis Techniques in More Contexts

**Direction II**

Make Formal Method Techniques More Accessible

# Simplify More Aspects of Shared Memory Concurrency

**Several Concurrent Programming Setups Based on Guarantees Provided by Underlying Memory System**

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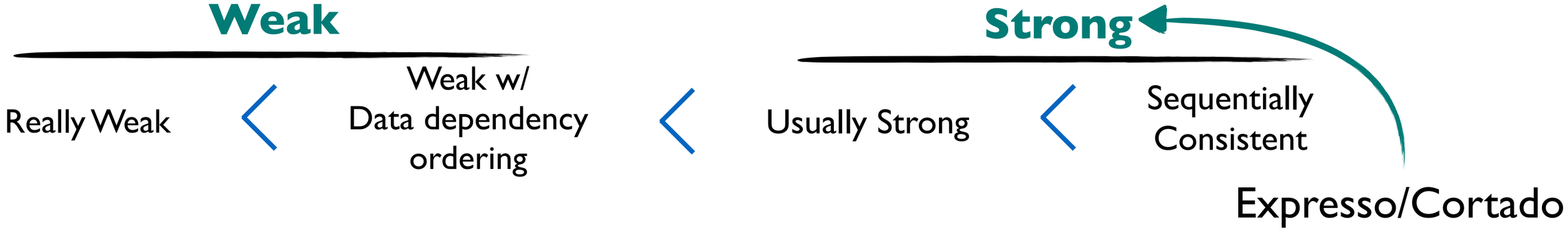

# Simplify More Aspects of Shared Memory Concurrency

**Several Concurrent Programming Setups Based on Guarantees Provided by Underlying Memory System**


Used to write extremely fast specialized programs, e.g., RCU data structures in Linux Kernel

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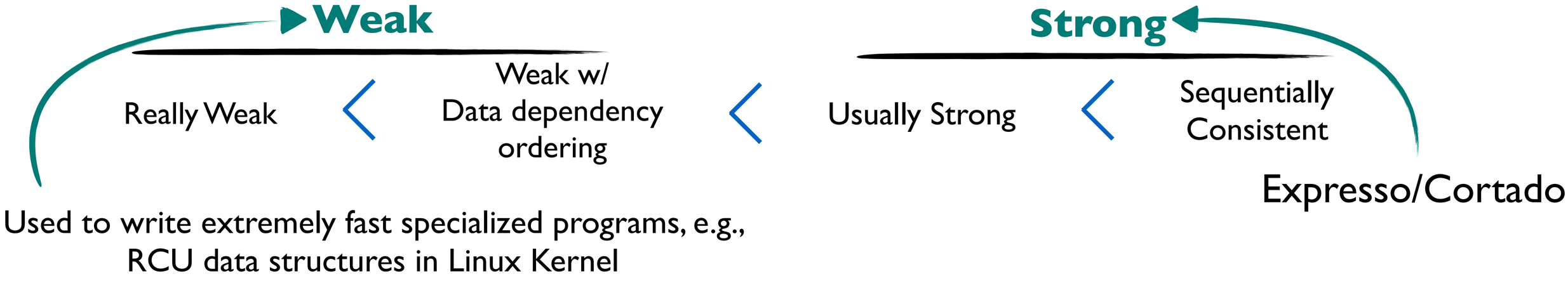
**Several Concurrent Programming Setups Based on Guarantees Provided by Underlying Memory System**

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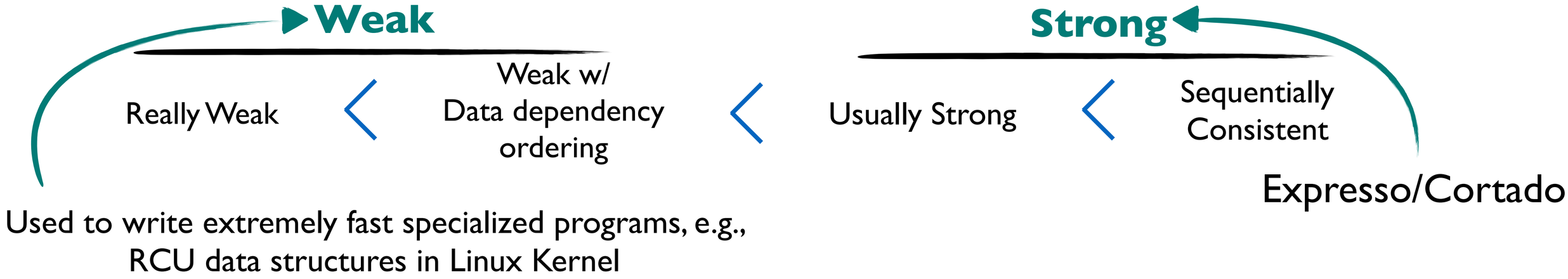
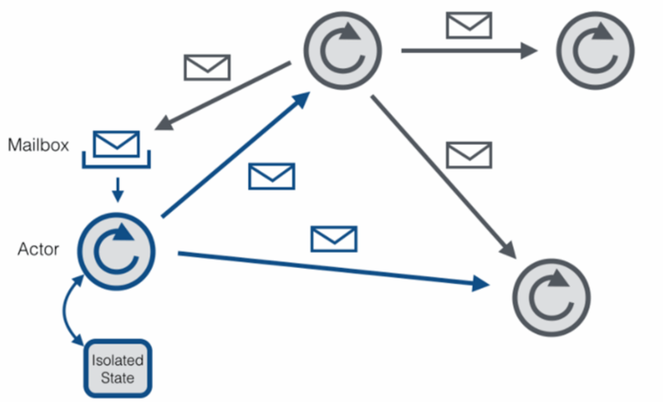



- Challenging to prove correctness of programs written with weak memory primitives
  - Many implementations have manually-written proofs
- ***Solutions:*** 1. More automation in verification
  2. Synthesize concurrent programs w/ weak memory primitives

# Simplify Other Concurrency Models




- Several other concurrency models based on message passing, e.g., MPI, Actor Model, etc.
- Nodes (i.e., threads) must conform to a communication protocol
  - Developers fail to implement the protocol correctly

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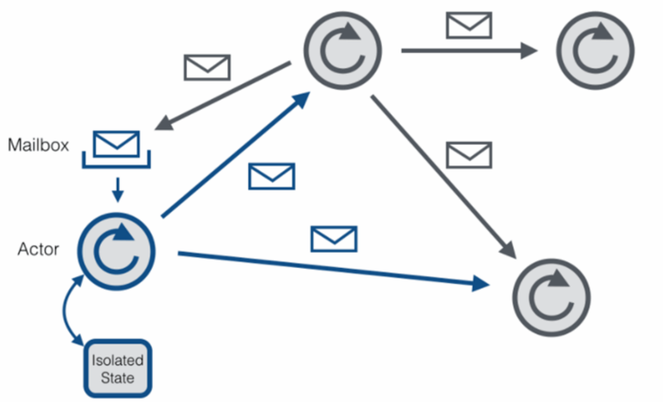


- Several other concurrency models based on message passing, e.g., MPI, Actor Model, etc.
- Nodes (i.e., threads) must conform to a communication protocol
  - Developers fail to implement the protocol correctly

- Automatically verify conformance to protocol given its formal description
- Automatically synthesize message passing programs from their specification

# Make Formal Methods More Accessible


- Users must be familiar with complex concepts and write specifications
- Even experts can write buggy specifications

# Make Formal Methods More Accessible


- Users must be familiar with complex concepts and write specifications
- Even experts can write buggy specifications

- Develop techniques that help developers fix wrong specifications
- Synthesize specifications from codebase artifacts (e.g., test cases)

# Acknowledgements

Isil Dillig

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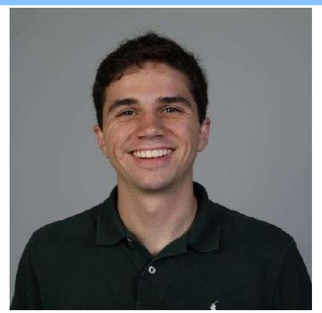
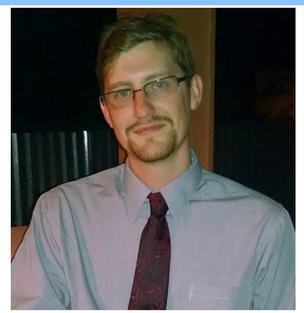


Ben Sepanski



Jon Stephens

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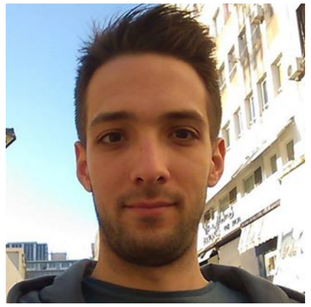
Yu Feng

Jiayi Wei

Ben Mariano

Rahul Krishnan

George Balatshouras



George Kastrinis

Maria Christakis

Valentin Wüstholz

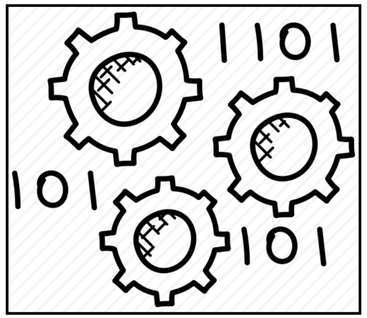
...

# Questions?

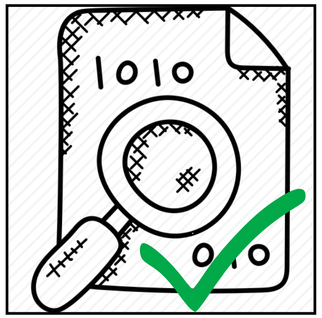
**Research Goal:** ***Formal methods for correct, efficient, and secure code!***

Synthesis

**Simplifying Concurrent Programming**
[PLDI'18,OOPSLA'22]




Verification

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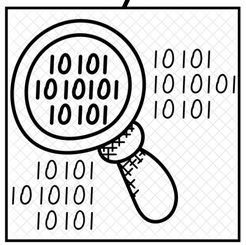
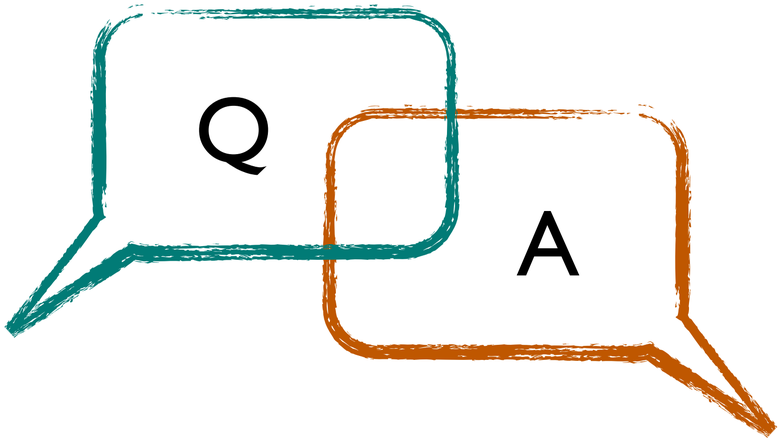
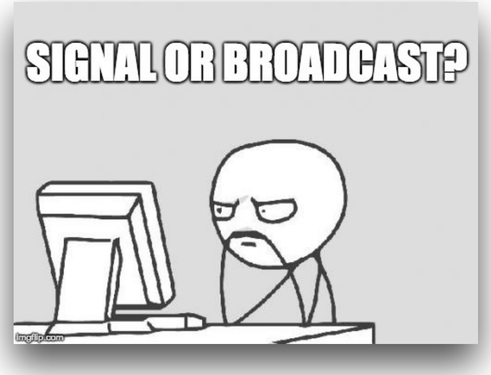



**Improve Scalability & Precision**
[FSE'17,SOAP'17,CC'18]



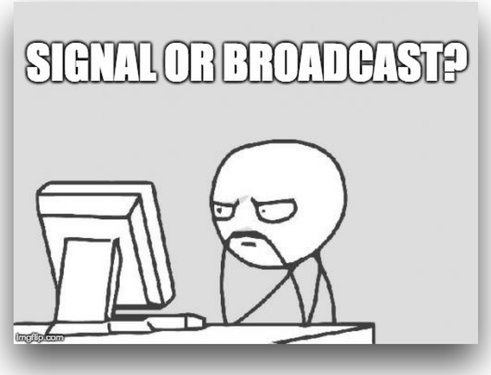
# Back Up Slides

# Signal or broadcast?




Do we need to wake up all threads block on P $\in Preds(M)$?

# Signal or broadcast?

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Simulate what happens when a thread gets woken up

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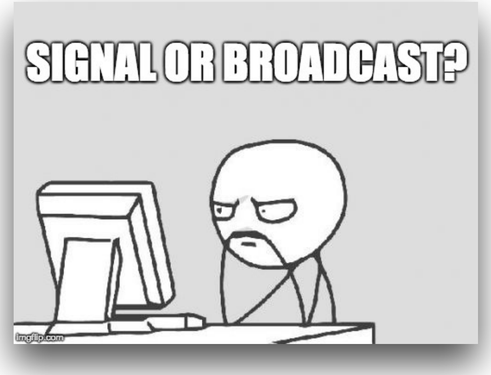


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For each CCR C of the form `waituntil(P) S`, check validity of Hoare triple:

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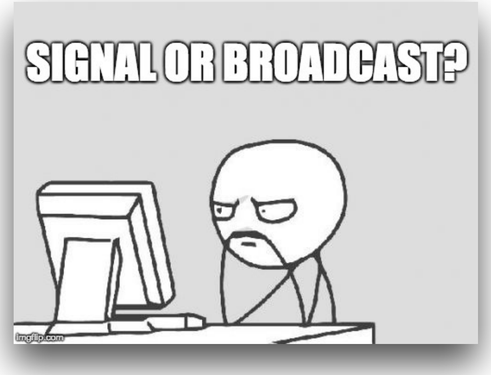


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For each CCR C of the form `waituntil(P) S`, check validity of Hoare triple:

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If ***all*** of them are valid, no need to broadcast!

# Example: Signal or broadcast?

**Predicate:** $P_w \equiv readers = 0 \wedge \neg writerIn \quad \neg P_w \equiv readers \neq 0 \vee writerIn$ **Invariant:** $readers \geq 0$

**CCR:**

```
atomic void enterWriter() {

  waituntil(readers == 0 && !writerIn);
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Triple is valid, safe to notify a single writer!

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Decision 2: Given CCR `waituntil(C) S` and predicate P, do we need to check P before signaling threads blocked on it?

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If this triple is valid, no need to test P at run-time!

# Example: Conditional Signal?

Can we signal readers unconditionally?

**CCR:**

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atomic void exitWriter() {

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Data-race freedom

Atomicity

Deadlock-freedom

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Data-race freedom

Atomicity

Deadlock-freedom

Resolve race through locks or atomic fields

$$\mathsf{Racy}(S1,S2)$$
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$$\vee$$
$$\exists f.\ (\mathit{Races}(S1,S2) = \{f\} \wedge a_f)$$

# Hard constraints

## Data-race freedom

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## Atomicity

Only permit safe interleavings

$$\neg\text{Safe}(S, S1,S2)$$
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## Deadlock-freedom

# Hard constraints

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## Deadlock-freedom

Impose a static lock acquisition order

$$\text{Edge}(S1,S2)$$
$$\Rightarrow$$
$$\left(l_1 \in \mathscr{L}(S1) \cap \mathscr{L}(S2)\right.$$
$$\wedge\, l_2 \in \mathscr{L}(S2) \setminus \mathscr{L}(S1)$$
$$\left.\Rightarrow l_1 \prec l_2\ \right)$$

# Soft constraints

Maximize parallelism

Minimize locks

Minimize atomics

# Soft constraints

Maximize parallelism

Minimize locks

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Prefer: field not converted to atomic

$$\neg a_f$$