An abstract graphic in the bottom-left corner of the slide. It features a network of orange lines of varying thicknesses, some solid and some dotted, connecting numerous small blue circular dots. The dots and lines are scattered across the lower-left quadrant, creating a sense of dynamic movement or a complex system. The lines radiate from a central area towards the corners, with some crossing each other.

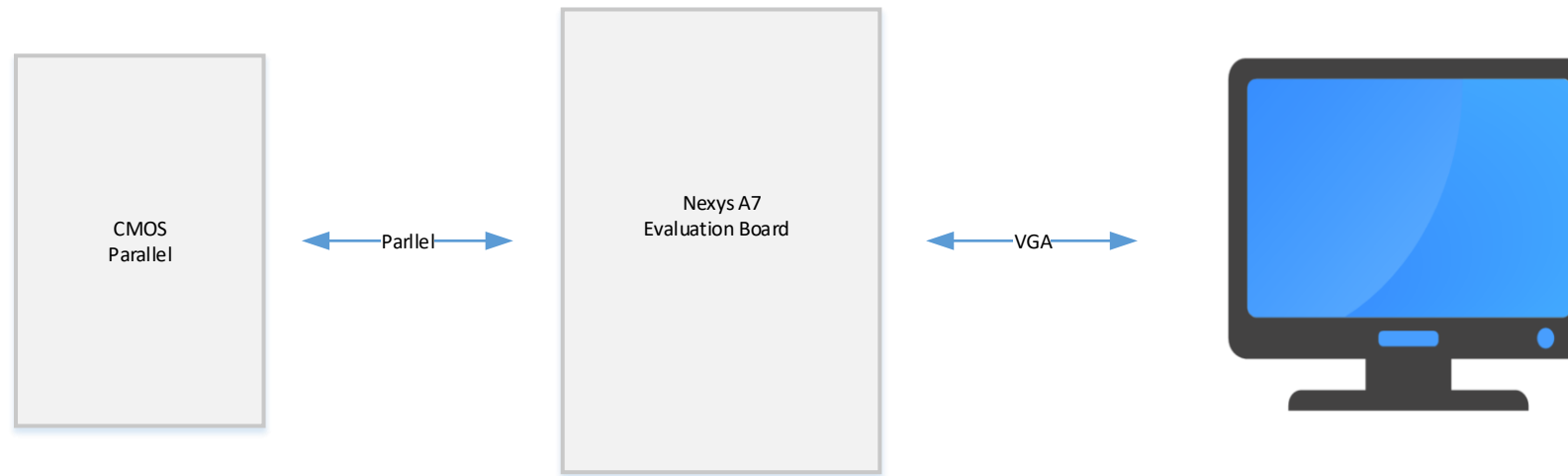
# Camera Module FPGA Artix7

# Agenda

- Camera Module major requirements
- Design Flow
  - Main Block Diagram
  - Major components
  - Design flow

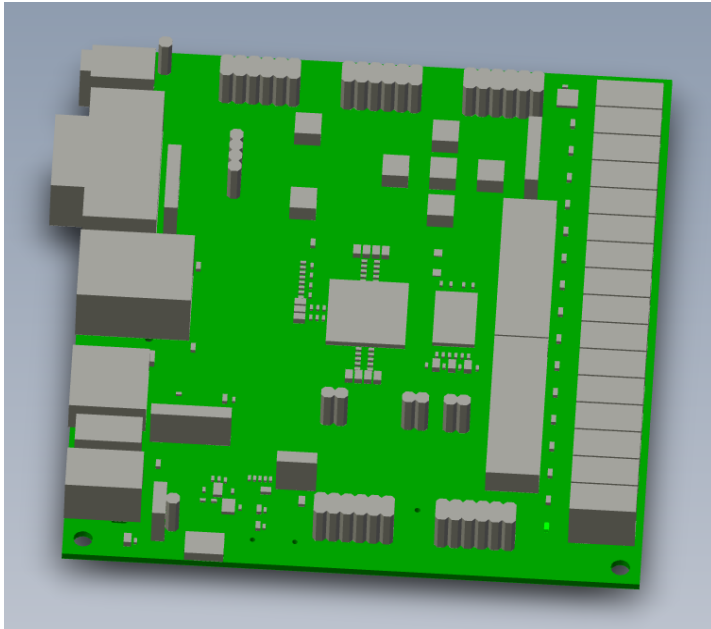
# Camera Module major requirements

- Project main purpose :
  - Live stream video display using FPGA Artix 7

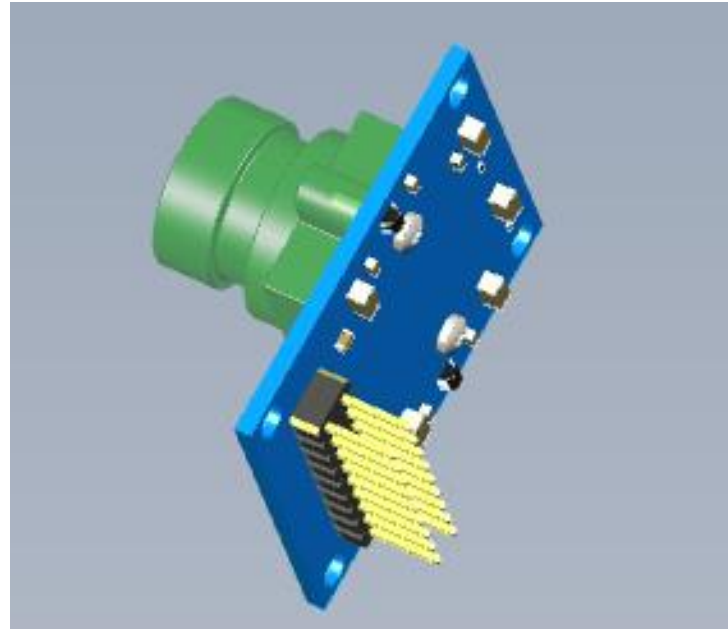


- Project Major components :
  - Nexys A7 FPGA Evaluation Board - Digilent
  - CMOS camera Interface ov7670 - Ominivision

# Design Flow : Major Components

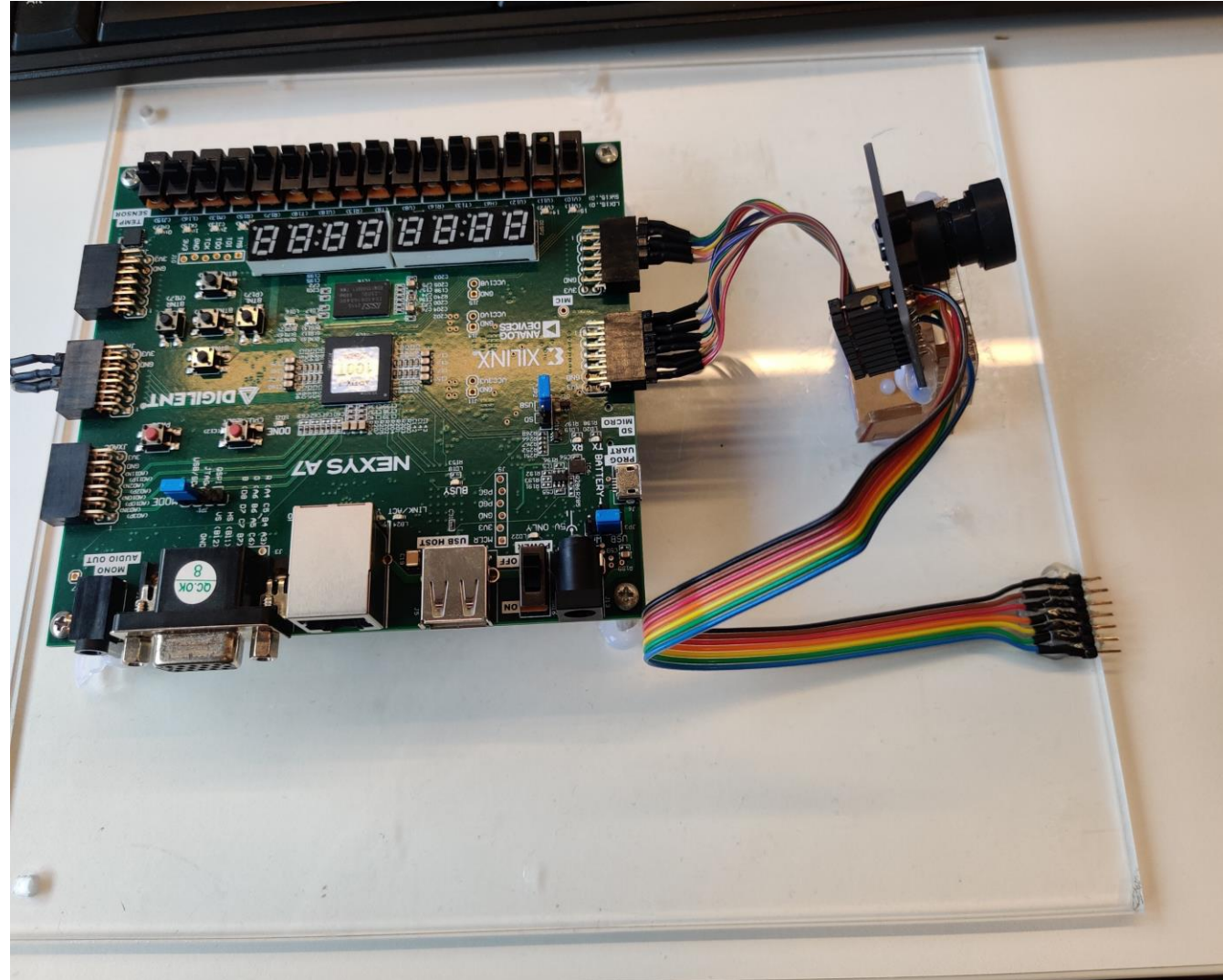


Nexys A7 FPGA Evaluation Board  
Xilinx Artix 7 FPGA-  
"XC7A100T-1CSG324C "



OV7670 Ominivision VGA sensor  
Output format :RGB565  
Operation Voltage :3.3V  
Communication : I2C

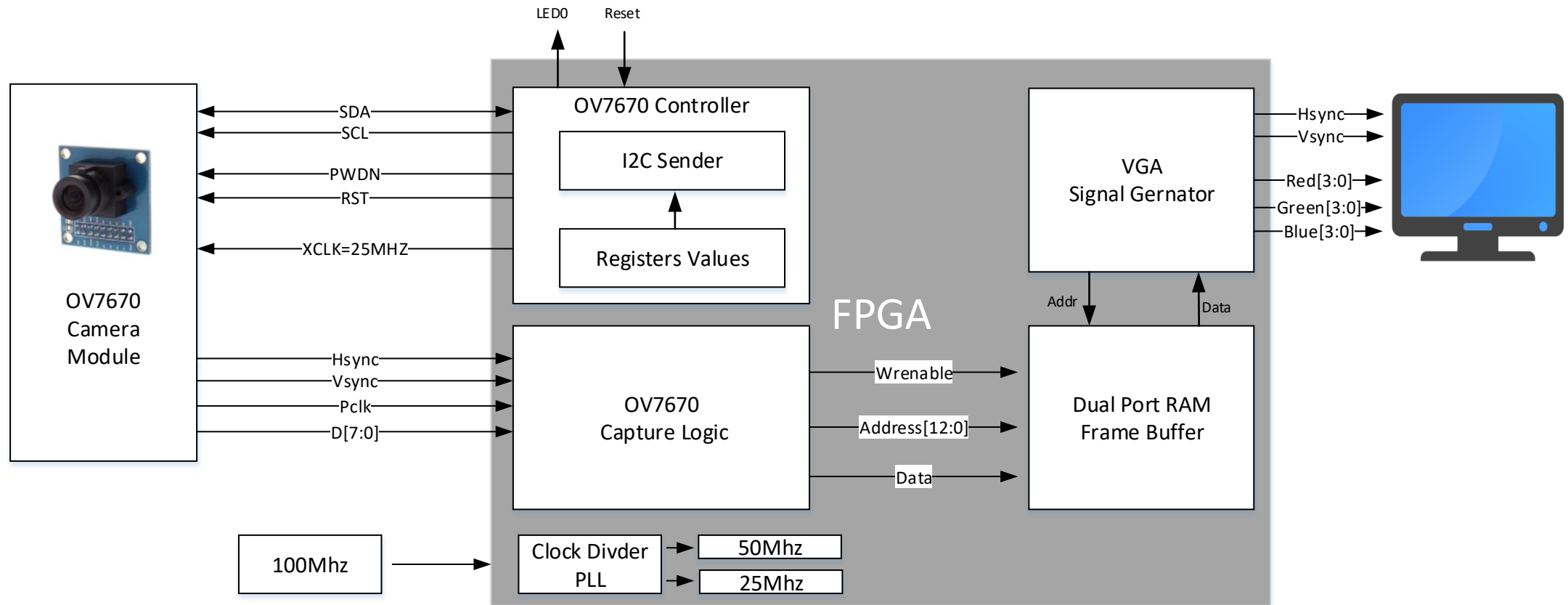
# Design Flow : Major Components



Nexys A7 with Ominivision OV7670

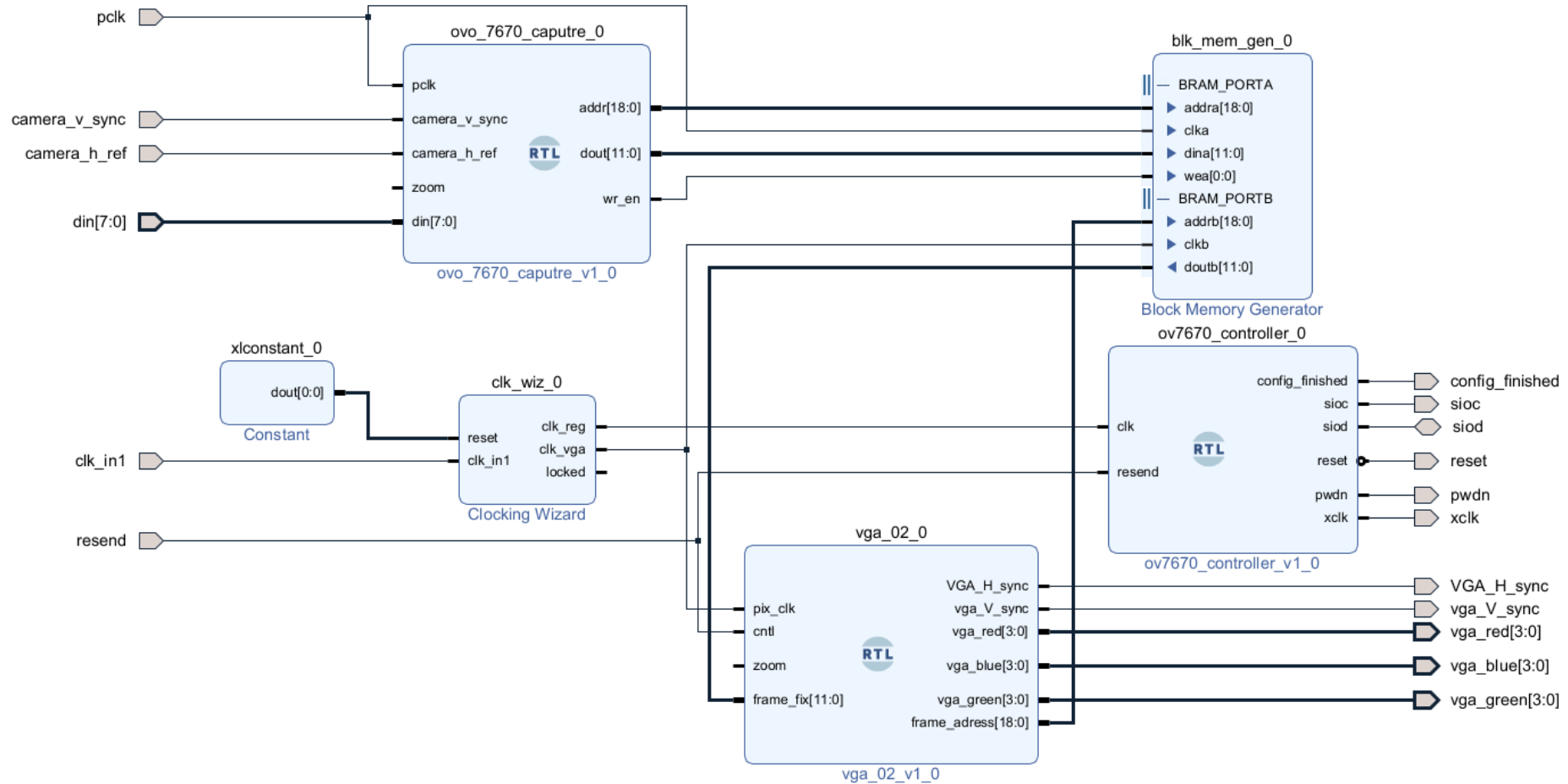
# FPGA Blocks

# Design Flow : Main Block Diagram



Block Diagram concept

# Vivado Block Diagram





# Clock Domains

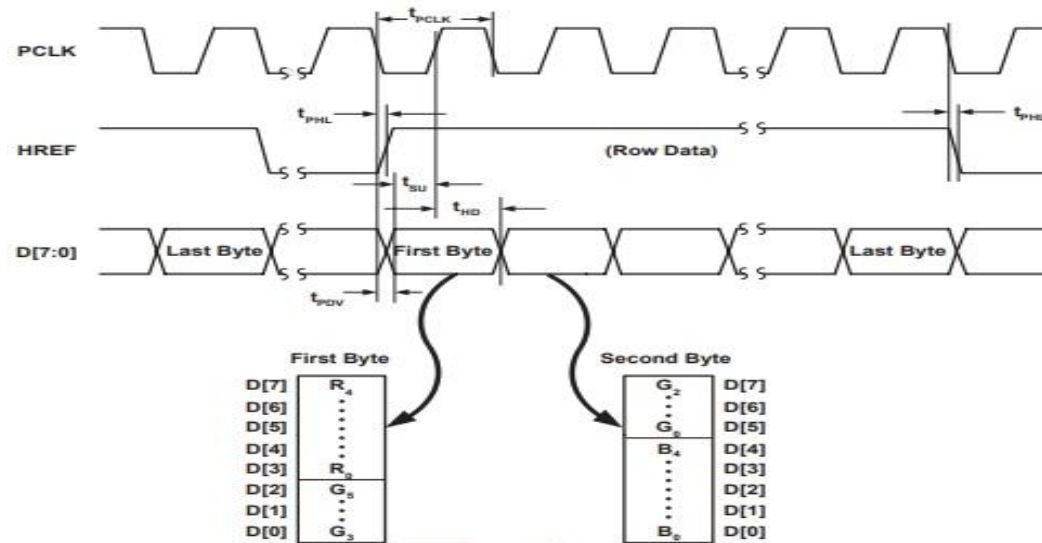
- Input CLK- 100Mhz from Oscillator of the Nexues 7
- Xclk – 25Mhz
- Pxclk – 25Mhz
- clk\_wiz
  - Vga - 50Mhz
  - Reg - 25Mhz

# OV7670 Camera Controller

- To configure the OV7670 camera ,it is required to configure the camera register list via I2c communication protocol
- Camera register list controls all sensor configuration such as output format and timing of output signals etc...
- Camera Controller Block also control :
  - Reset signal for the sensor - active low
  - Power down signal of the sensor - active high
  - Xclk System clock signal

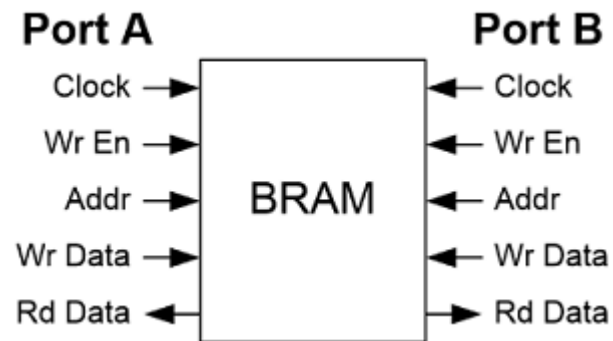
# OV7670 Capture Logic

- Input Data 8 bits
- RGB565 format is 16 bits (Red – 5 bits ,Green- 6 bits ,Blue -5 bits).
- 2 Clock for each pixel.



# Dual Port Ram Frame Buffer

- Allows multiple reads or writes to occur at the same time    format and timing of output signals etc...



# VGA Signal Gubernator

- A VGA signal contains 5 active signals

Two TTL compatible signals for synchronization.

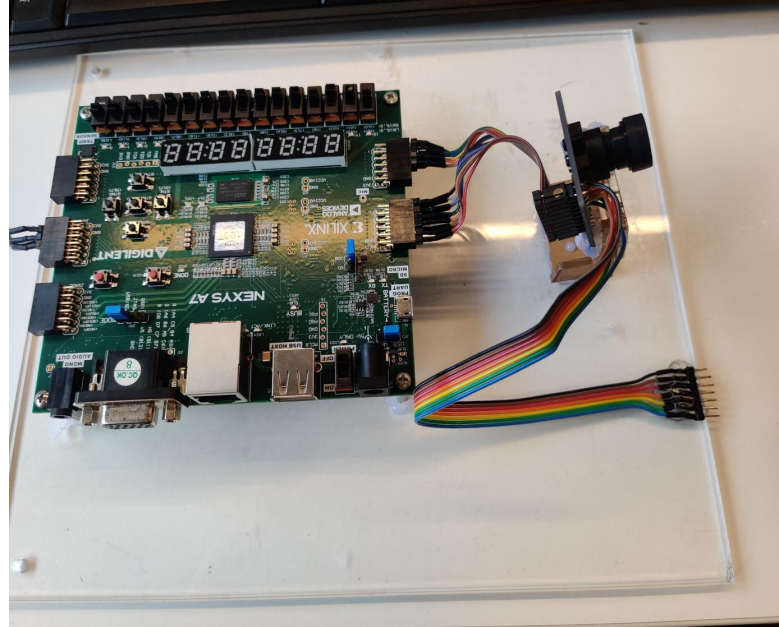
- HSYNC – horizontal synchronization
- VSYNC – vertical synchronization

- Three analog for color control

- Red
- Green
- Blue

- All other color combinations are generated by changing the analog levels of the three RGB signals
- In standard VGA format, the screen contains 640x480 pixels
- The standard refresh rate for a screen is 60 Hz

# Short Video performances



[Link](#)

An abstract geometric pattern in the bottom-left corner of the slide. It consists of numerous small blue dots connected by thin orange lines. Some lines are solid, while others are dotted. The lines and dots are arranged in a way that suggests a network or a series of connected points, possibly representing a mathematical or scientific concept. The pattern is dense and intricate, with many lines intersecting and dots clustered together.

**Thanks**