Introduction to Clock Constraints Demo Script

Introduction

This demonstration script provides high-level instructions on how to constrain the clock and perform basic timing analysis in a design using the Vivado® Design Suite.

Preparation:

- Required files: `$TRAINING_PATH/ClkConstr_Intro/demo/KCU105/verilog`
- Required hardware: None
- Supporting materials: None

Clock Creation

Action with Description	Point of Emphasis and Key Takeaway
• Launch Vivado Design Suite 2021.2.	
• Open the **wave_gen.xpr** design in the `$TRAINING_PATH/ClkConstr_Intro/demo/KCU105/verilog` directory.	
• Open the **wave_gen_timing.xdc** file.	Note that there are no timing constraints entered in the XDC file. You will be entering the clock constraints for the design by using the Constraints Wizard.
• Open the synthesized design.	

Action with Description	Point of Emphasis and Key Takeaway
• Launch the **Constraints Wizard** from **Synthesis** > **Open Synthesized Design** to make the initial clock constraints on the design. • Examine the message in the No Target Constraints File dialog box.	The Constraints Wizard guides you through creating timing constraints. It analyzes the design for missing timing constraints and makes recommendations. From the No Target Constraints File dialog box, it is evident that you need to make the appropriate constraints set and constraint file **active** before making constraints using the Constraints Wizard.
• Open the Constraints Wizard. • Click **Next** in the Welcome page of the Constraints Wizard to identify any missing timing constraints in the design.	The Constraints Wizard is designed to make it as easy as possible to make complete constraints for any design (hence all the questions). In this case, wave_gen does not need any special timing constraints.
• Click **Existing Create Clock Constraints(1)** and see that the clock is already added.	The Primary Clocks dialog box in the Constraints Wizard identifies the missing primary clocks, if any, in the design, and allows you to enter the period/frequency of the primary clock.
• Click **Skip to Finish** after entering the clock constraint. • Select the **View Timing Constraints** option in the Constraints Summary page. • Click **Finish**.	The Summary window will acknowledge the new clock constraint. The utility will then close without opening the Constraints Editor. The Constraints Editor will then open and show the new clock constraint.

Action with Description	Point of Emphasis and Key Takeaway
• Enter **`report_clocks`** in the Tcl Console. Make sure to press the <**Enter**> key.	Describe the contents of this report. From the Clocks report, what is the input clock to the MMCM? How many output clocks are generated from this MMCM?
• Open the **clk_gen.v** file from the Sources window.	Verify that the signals clk_pin_p, clk_out1, and clk_out2 are made from the clk_core (bottom of file). From this you will see that clk_rx and clk_tx are out1 and out2. This matches the output signal names from the top of the file.
• Double-click the **clk_core.xci** file in the Sources window. This will open the Re-customize IP Wizard. • Close the Re-customize IP Wizard without saving any changes.	Review the output frequencies generated by the MMCM. Can you explain how this MMCM was configured to produce clocks of 200 MHz and 193.75 MHz? **Hint:** Go to the Summary tab.
• Click **Report Clock Networks** in the Flow Navigator.	Review how the report generated confirms how the MMCM made the three output clocks.

Basic Static Timing Analysis

Action with Description	Point of Emphasis and Key Takeaway
• Rerun synthesis (two or three minutes) and open the synthesized design.	
• Click **Report Timing Summary** to generate a Timing Summary report from the synthesized design.	Review the following: • Organization of the report in the GUI • Design Timing Summary • Check Timing Report • Intra-Clock paths • Inter-Clock paths • User Ignored Paths • Unconstrained Paths
• Select the longest setup path for clk_out1_clk_core under Intra-Clock Paths.	Review the following: • Path properties • Confirm the slack calculation for hold time (arrival time – required time) • Logic descriptions • Element delay and cumulative delay • Schematic generation and cross probing to source HDL
• Describe the inter-clock paths and the possible need for synchronization circuits. • Select the longest path in the Inter-clock Paths section.	Review the possible need for synchronization circuits. Review the path to show that they have different clocks on the source and destination flip-flops.

Action with Description	Point of Emphasis and Key Takeaway
• Click **Report Clock Interaction** to generate a Clock Interaction report.	Review the following: • Color coding for different type of paths • Source clock/destination clock chart • Right-click options for the paths between each clock domain.
• Facilitate an open-ended discussion on fixing the design.	Review the following: • Synchronization circuitry • Fixing timing problems • Need for path-specific constraints If I do all of these things, will I fix all the timing problems? How accurate are these timing numbers? **Note:** In this demo, all this analysis can be done without having to complete a single implementation (saved huge amount of time).

Summary

This demo illustrated how to create initial clock constraints and verify the clocking structures built into your design using some of the most common reports. It also illustrated the static timing analysis capabilities of the Vivado Design Suite to perform some basic timing verification.

References:

- Supporting materials
  - *Vivado Design Suite User Guide (Using Constraints)* (UG903)
  - *Vivado Design Suite User Guide (Design Analysis and Closure Techniques)* (UG906)