MP-1

Quad UAV Interfacing

# Flight Experience

We are all ace pilots. We earned our wings in WWII fighting in Europe…

Ok, not really. We didn’t get to fly anything.

# Describe PPM

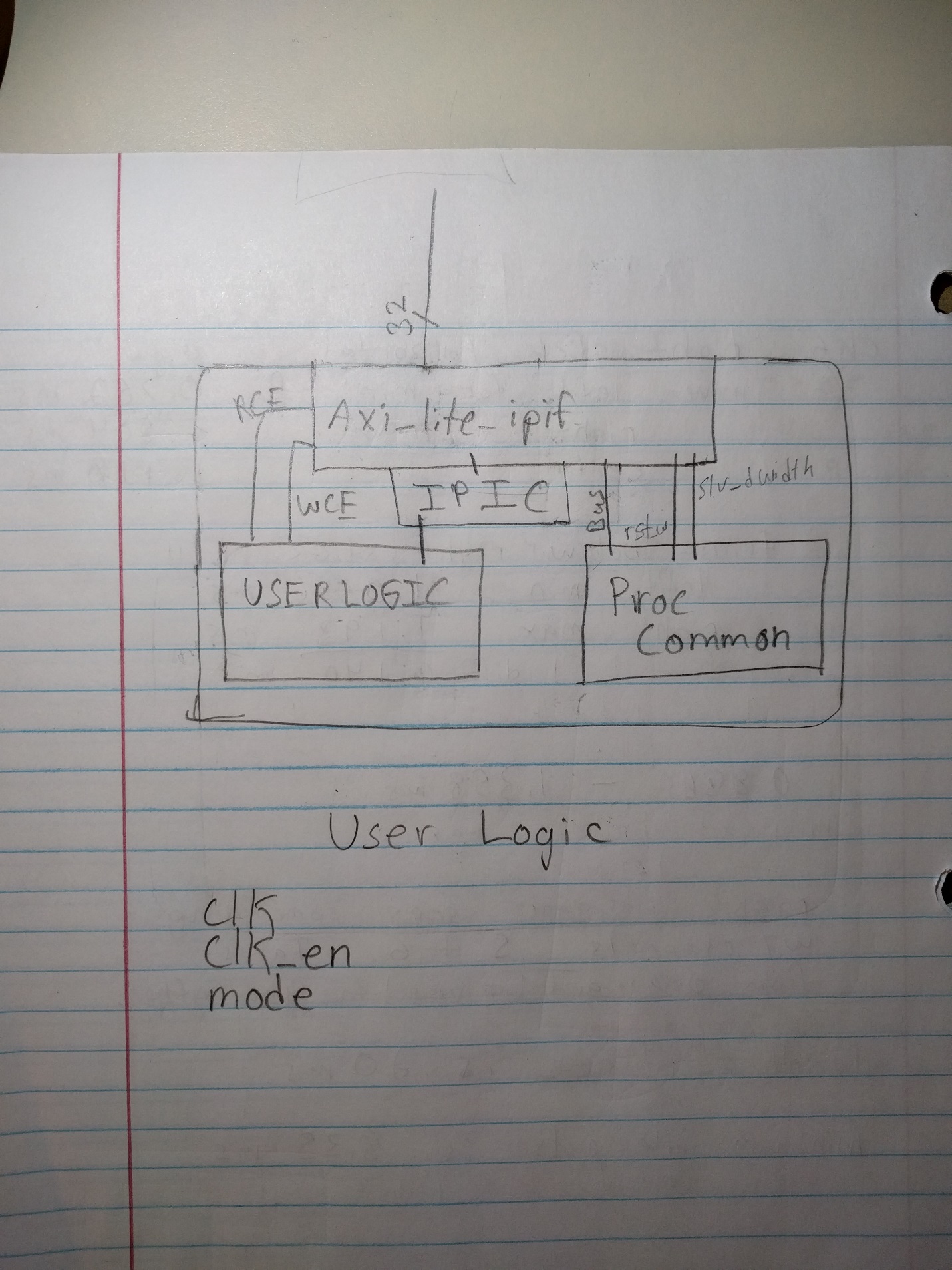
|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Channel # | Min w/o Trim | Max w/o Trim | Min | Max | Description |
| 1 | 0.602 | 1.622 | 0.602 | 1.622 | Left dial |
| 2 | 0.601 | 1.632 | 0.601 | 1.632 | Right dial |
| 3 | 0.935 | 1.332 | 0.9 | 1.375 | Left stick(H) |
| 4 | 0.805 | 1.46 | 0.72 | 1.536 | Left stick(V) |
| 5 | 0.784 | 1.45 | 0.644 | 1.59 | Right stick (V) |
| 6 | 0.752 | 1.504 | 0.896 | 1.358 | Right stick(H) |

The total length of a PPM frame is 20ms. The minimum length of the idle pulse is 20ms – 9.113ms = 10.887ms. In reality, the pulse is expected to be longer than that.

# Concerns About Connecting to ZedBoards

The transmitters use 5 V but the zedboards use 3.3 V. We will have to use a level shifter to convert between the two. The connectors that we have in lab also limit what pins on the pmods that we can use.

# Structural Diagram



The AMBA bus has an array of two Integers called IPIF\_ARD\_NUM\_CE\_ARRAY. This holds two ‘spaces’. The soft reset space and the user logic slave space. The first is set to zero, therefore there are no clock enables in the soft reset space. The second is set to one, therefore there is one clock enable in the user logic slave space. These values get added and placed in to the signals ‘ipif\_Bus2IP\_RdCE’ and ‘ipif\_Bus2IP\_WrCE’. These signals are used directly to indicate the value of ‘user\_Bus2IP\_RdCE’ and ‘user\_Bus2IP\_WrCE’ respectively.

# What Worked, What Didn’t

Everything worked in ModelSim. Hardware passthrough and generate worked when scoped in real life. In the C code the user can enter values to save into the slv\_registers to send to the generate fsm. This produces exactly what the user asks for. The capture fsm on the other hand, does not work in real life. It works in ModelSim, but when it comes to testing real functionality, it leaves much to be desired.

# Participation

Kyle Fischer – 33%

Khoi Cao – 33%

Kris Burney – 33%

WWII experience – 1%

# Conclusion

This lab provides us learning opportunity to review the fundamentals VHDL and finite state machine that we have learned in 381. However, we again encountered some tool chain errors in the lab, which took us a considerable amount of time for debugging and fixing the issue. We will now always check that we our workspace is correct. We learned how to create our own pcore from basically scratch as well as how to direct its input and output to useful nets thereby creating a useful design. Although we didn’t get everything working. We believe we have once again gained a lot of experience with the system and are closer to being able to go a week without major issues.

For the purpose of this lab, we have provided system.mhs, system.ucf, rc\_control.c, and our vhdl files in the submission2.zip file on blackboard.