EXPERIMENT 1 PRELIMINARY WORK

Q1: Read the remainders in the backward direction and add the necessary zeros to the left.

a.

41	
20	1
10	0
5	0
2	1
1	0
0	1

$\Longrightarrow \boxed{(41)_{10} = (00101001)_2}$

b.

79	
39	1
19	1
9	1
4	1
2	0
1	0
0	1

$\Longrightarrow \boxed{(79)_{10} = (01001111)_2}$

c.

108	
54	0
27	0
13	1
6	1
3	0
1	1
0	1

$\Longrightarrow \boxed{(108)_{10} = (01101100)_2}$

d.

127	
63	1
31	1
15	1
7	1
3	1
1	1
0	1

$\Longrightarrow \boxed{(127)_{10} = (01111111)_2}$

e.

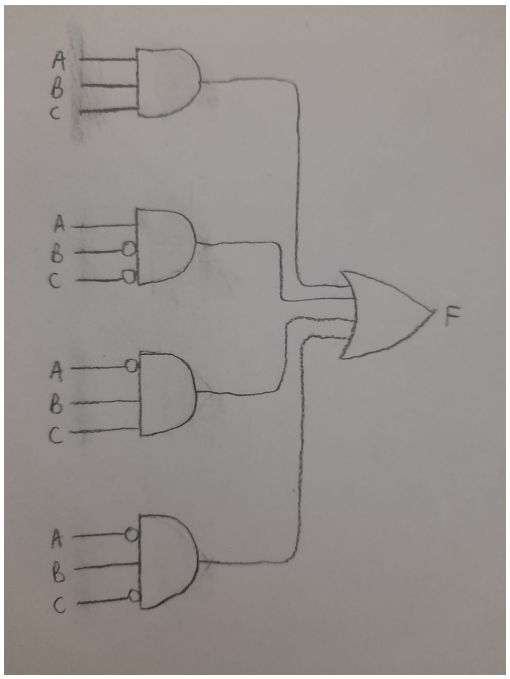
240	
120	0
60	0
30	0
15	0
7	1
3	1
1	1
0	1

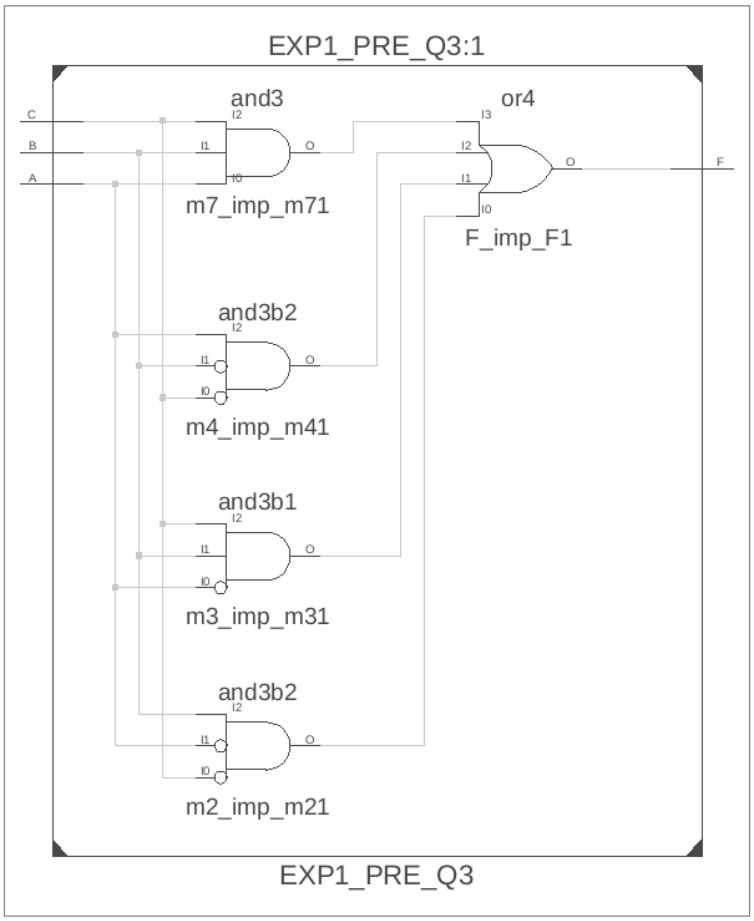
$\Longrightarrow \boxed{(240)_{10} = (11110000)_2}$

Q2:

	Decimal form	Hexadecimal form
a. 01001010	$2^6 + 2^3 + 2^1 = \boxed{74}$	$\underbrace{0100}_{4}\ \underbrace{1010}_{A} = \boxed{4A}$
b. 01110101	$2^6 + 2^5 + 2^4 + 2^2 + 2^0 = \boxed{117}$	$\underbrace{0111}_{7}\ \underbrace{0101}_{5} = \boxed{75}$
c. 11110010	$2^7 + 2^6 + 2^5 + 2^4 + 2^1 = \boxed{242}$	$\underbrace{1111}_{F}\ \underbrace{0010}_{2} = \boxed{F2}$
d. 00101110	$2^5 + 2^3 + 2^2 + 2^1 = \boxed{46}$	$\underbrace{0010}_{2}\ \underbrace{1110}_{E} = \boxed{2E}$
e. 11010000	$2^7 + 2^6 + 2^4 = \boxed{208}$	$\underbrace{1101}_{D}\ \underbrace{0000}_{0} = \boxed{D0}$

Q3: a. *Hand-drawn circuit and RTL schematic*:



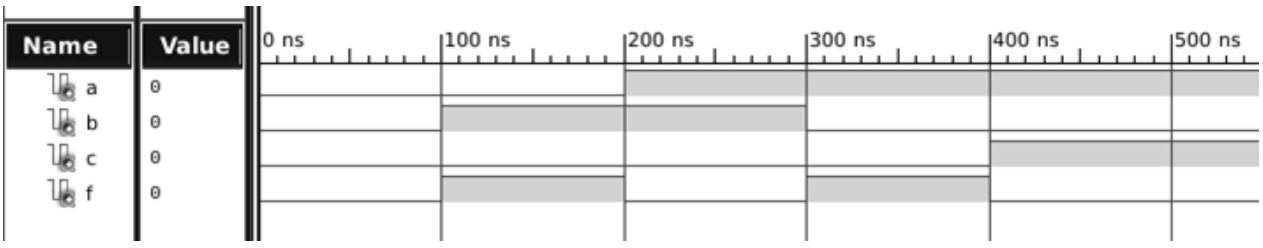


VHDL:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity EXP1_PRE_Q3 is
Port ( A, B, C : in  STD_LOGIC;
       F       : out STD_LOGIC);
end EXP1_PRE_Q3;

architecture Behavioral of EXP1_PRE_Q3 is
    signal m2, m3, m4, m7 : STD_LOGIC;

begin
    m2 <= not A and B and not C;
    m3 <= not A and B and C;
    m4 <= A and not B and not C;
    m7 <= A and B and C;

    F <= m2 or m3 or m4 or m7;
end Behavioral;
```

b. *Test bench*

```
stim_proc: process
begin
    wait for 100 ns;
    A <= '0'; B <= '1'; C <= '0';
    wait for 100 ns;
    A <= '1'; B <= '1'; C <= '0';
    wait for 100 ns;
    A <= '1'; B <= '0'; C <= '0';
    wait for 100 ns;
    A <= '1'; B <= '0'; C <= '1';
    wait;
end process;
```



Q4: a.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

$\implies$ Collect the minterms $\implies$

$$A = x'yz + xy'z + xyz' + xyz$$
$$B = x'y'z + x'yz' + xy'z' + xyz$$
$$C = x'y'z' + x'yz' + xy'z' + xyz'$$

b.

A :

$x \backslash yz$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

,

B :

$x \backslash yz$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

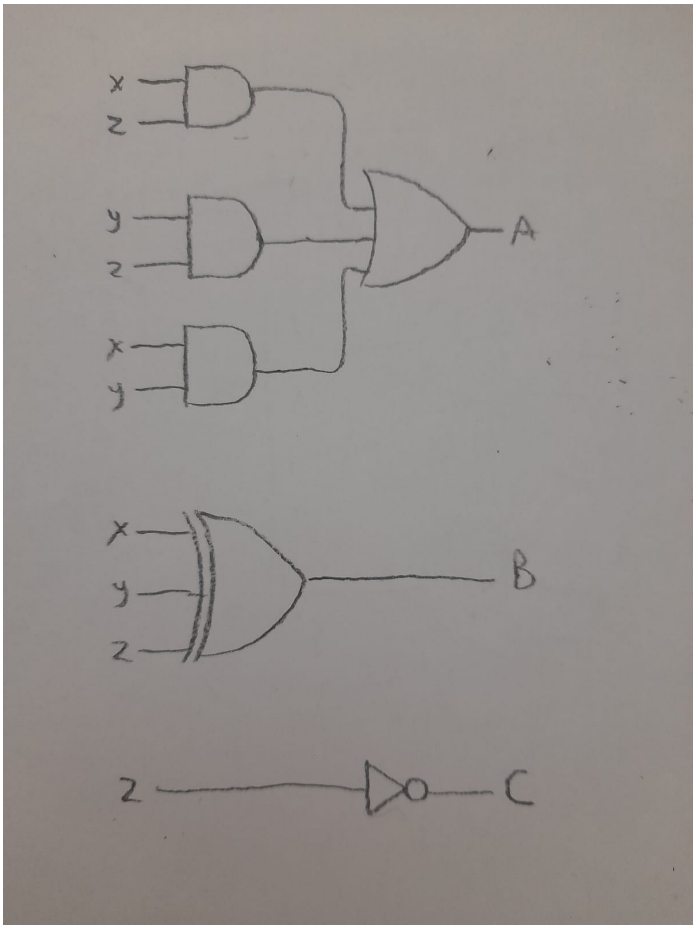
,

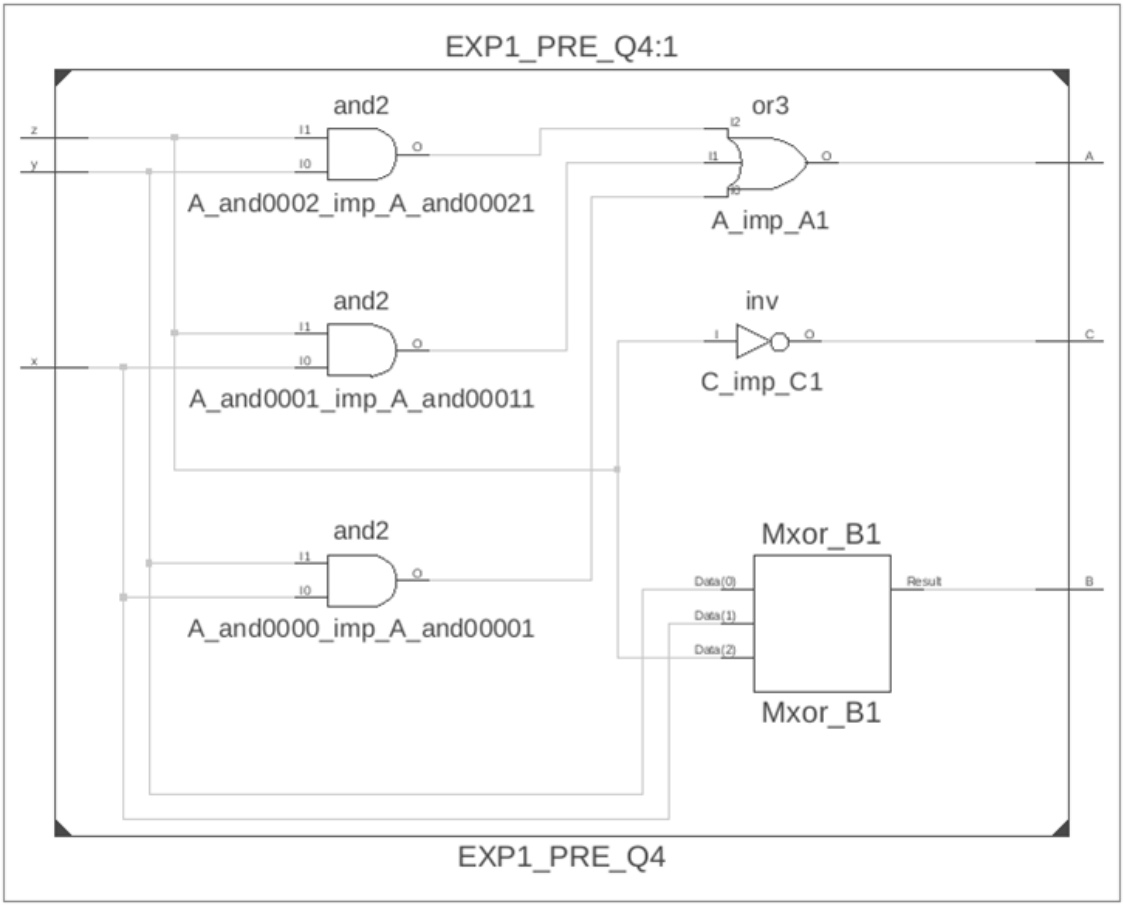
C :

$x \backslash yz$	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$$A = xz + yz + xy, \qquad B = x \oplus y \oplus z, \qquad C = z'$$

c. *Hand-drawn circuit and RTL schematic*:





VHDL:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity EXP1_PRE_Q4 is
    Port ( x, y, z : in  STD_LOGIC;
           A, B, C : out STD_LOGIC);
end EXP1_PRE_Q4;

architecture Behavioral of EXP1_PRE_Q4 is

begin
    A <= (x and y) or (x and z) or (y and z);
    B <= x xor y xor z;
    C <= not z;
end Behavioral;
```

d. *Test bench*

```
stim_proc: process
begin
    wait for 100 ns;
    x <= '0'; y <= '1'; z <= '0';
    wait for 100 ns;
    x <= '1'; y <= '1'; z <= '0';
    wait for 100 ns;
    x <= '1'; y <= '0'; z <= '0';
    wait for 100 ns;
    x <= '1'; y <= '0'; z <= '1';
    wait;
end process;
```