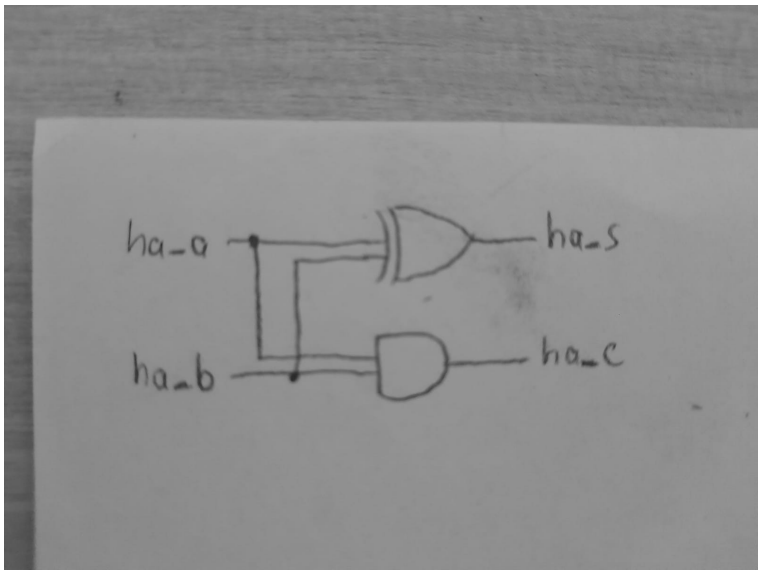
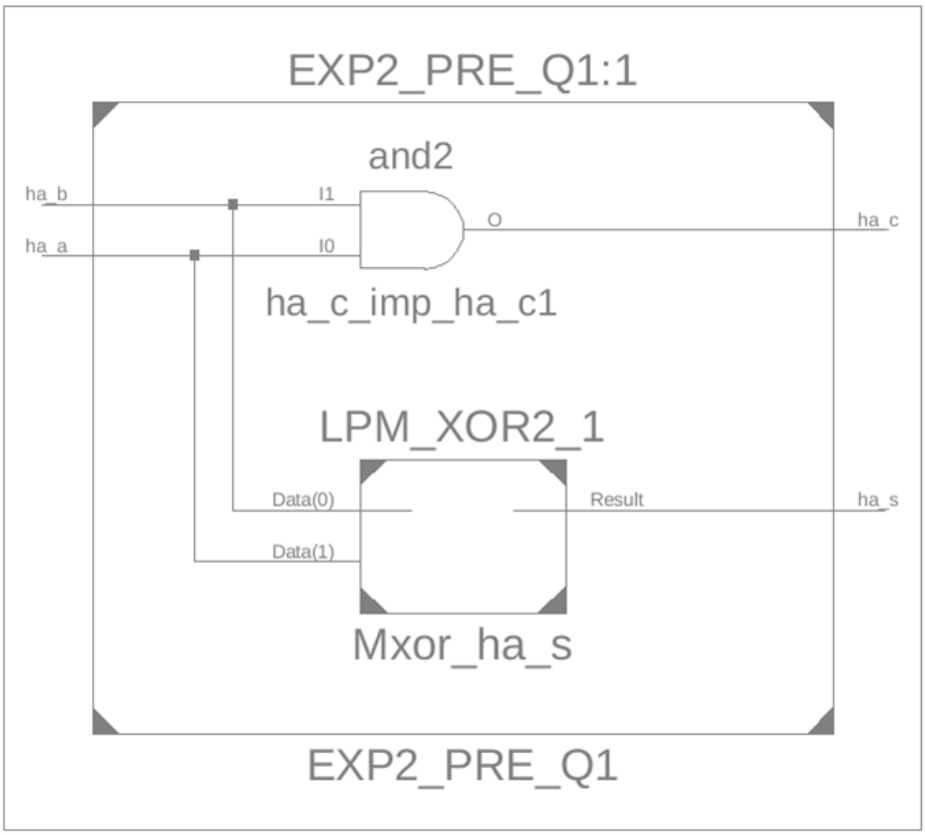
EXPERIMENT 1 PRELIMINARY WORK

Q1: *Hand-drawn circuit and RTL schematic*



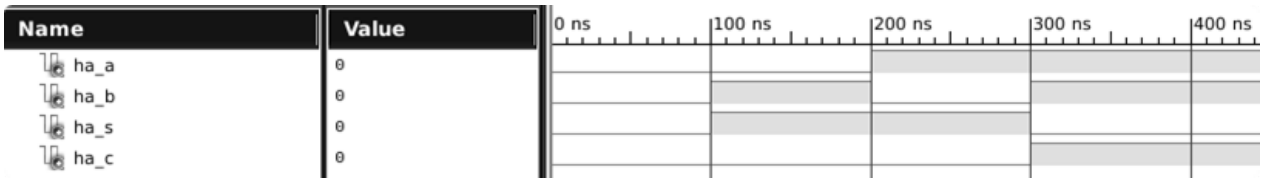


VHDL

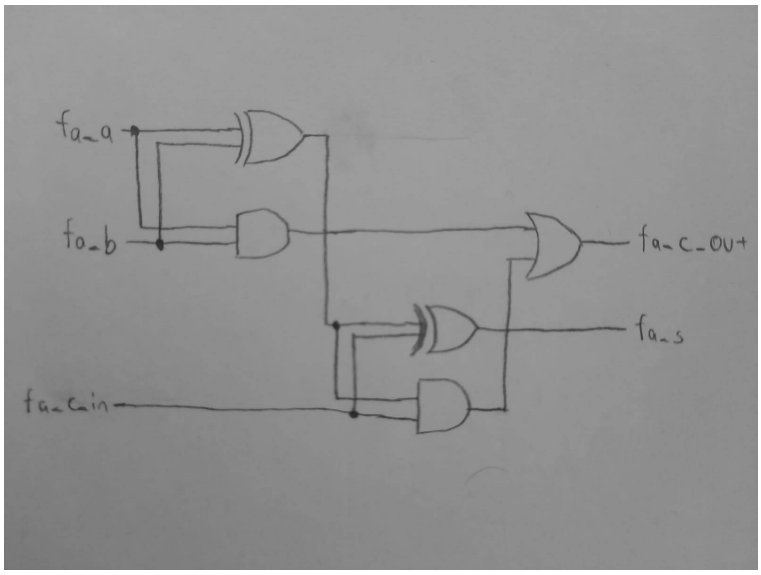
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity EXP2_PRE_Q1 is
    Port (ha_a, ha_b : in  STD_LOGIC;
          ha_s, ha_c : out STD_LOGIC);
end EXP2_PRE_Q1;

architecture Behavioral of EXP2_PRE_Q1 is

begin
    ha_s <= ha_a xor ha_b;
    ha_c <= ha_a and ha_b;
end Behavioral;
```

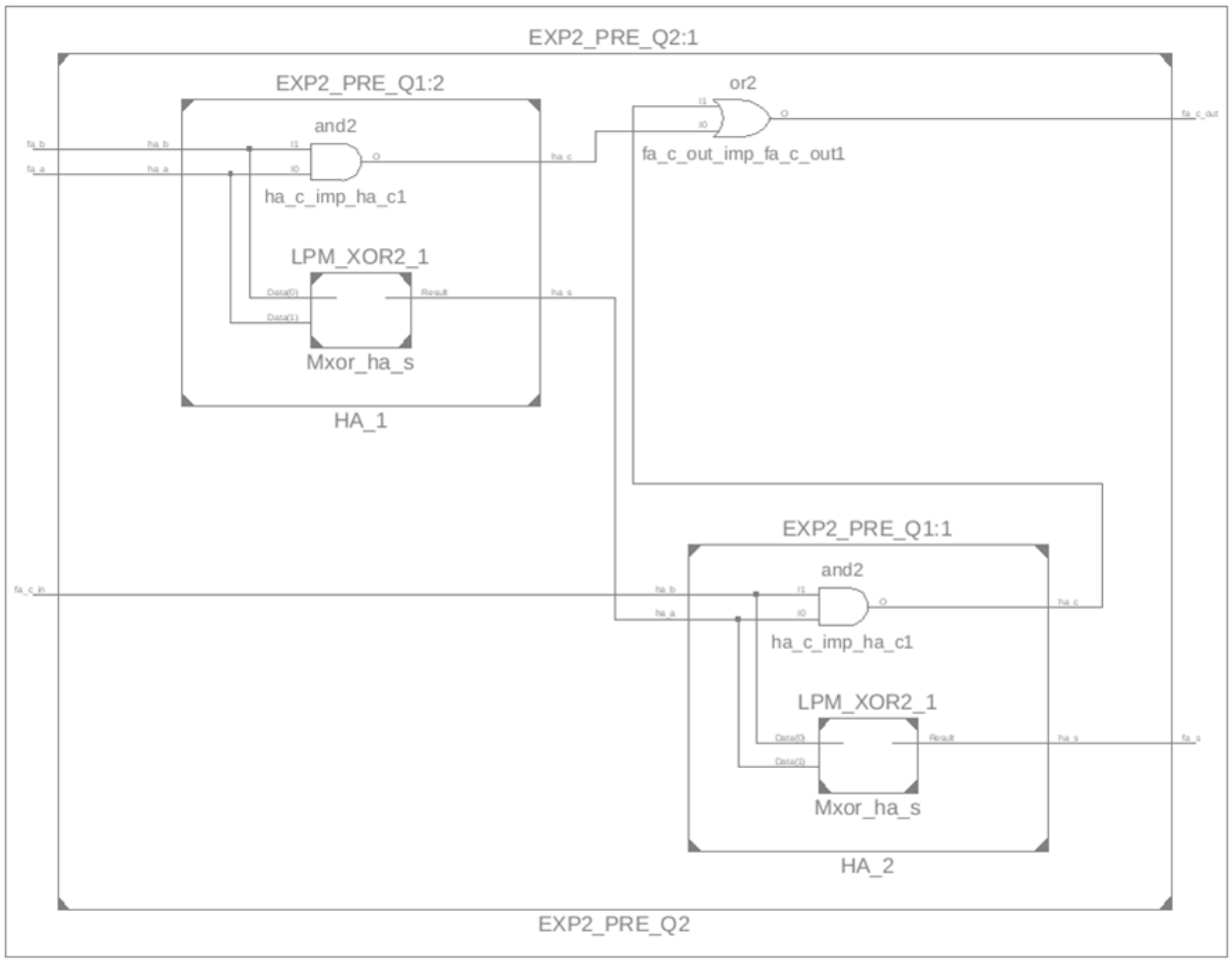
Test bench

```
stim_proc: process
begin
    ha_a <= '0'; ha_b <= '0';
    wait for 100 ns;
    ha_a <= '0'; ha_b <= '1';
    wait for 100 ns;
    ha_a <= '1'; ha_b <= '0';
    wait for 100 ns;
    ha_a <= '1'; ha_b <= '1';
    wait;
end process;
```



Q2: *Hand-drawn circuit and RTL schematic*



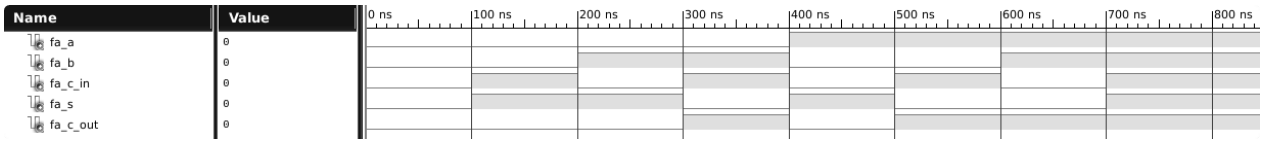


VHDL

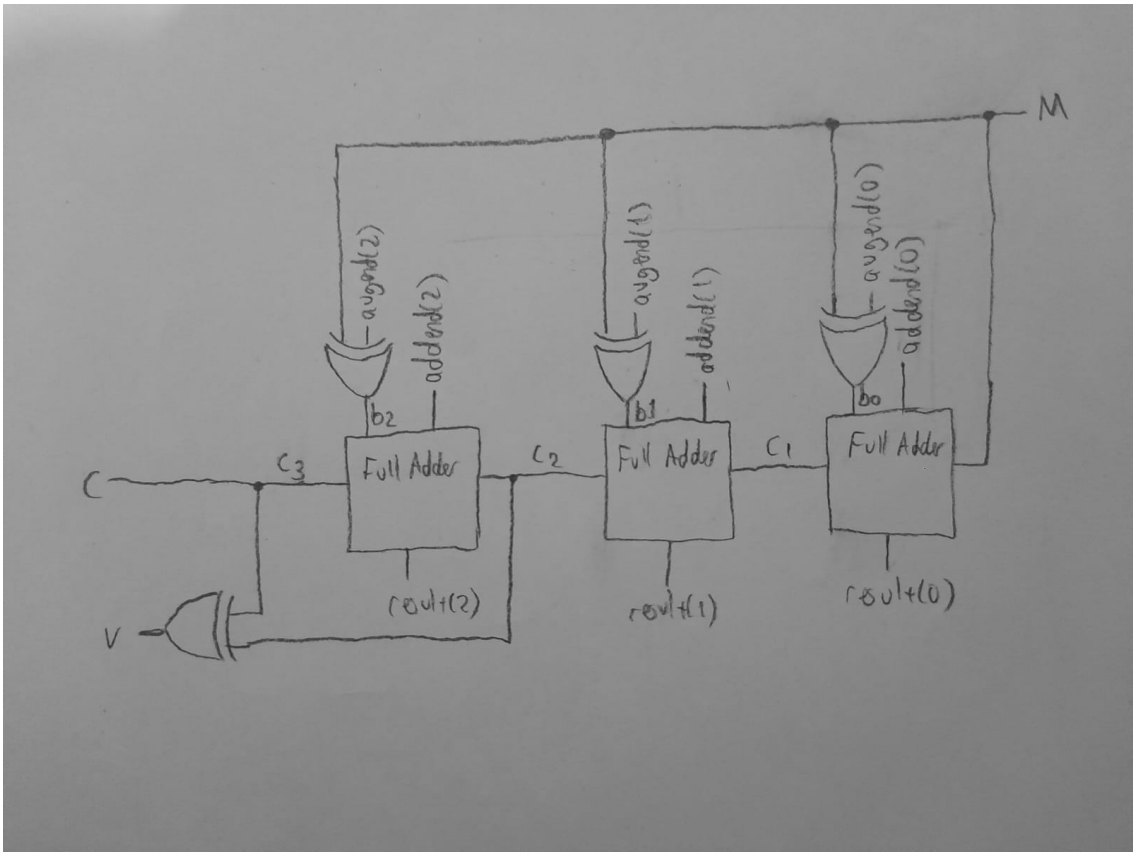
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity EXP2_PRE_Q2 is
    Port (fa_a, fa_b, fa_c_in : in STD_LOGIC;
          fa_s, fa_c_out : out STD_LOGIC);
end EXP2_PRE_Q2;

architecture Behavioral of EXP2_PRE_Q2 is
component EXP2_PRE_Q1
    Port (ha_a, ha_b : in STD_LOGIC;
          ha_s, ha_c : out STD_LOGIC);
end component;
signal s1, c1, c2 : STD_LOGIC;

begin
    HA_1 : EXP2_PRE_Q1
        Port map (fa_a, fa_b, s1, c1);
    HA_2 : EXP2_PRE_Q1
        Port map (s1, fa_c_in, fa_s, c2);
    fa_c_out <= c1 or c2;
end Behavioral;
```

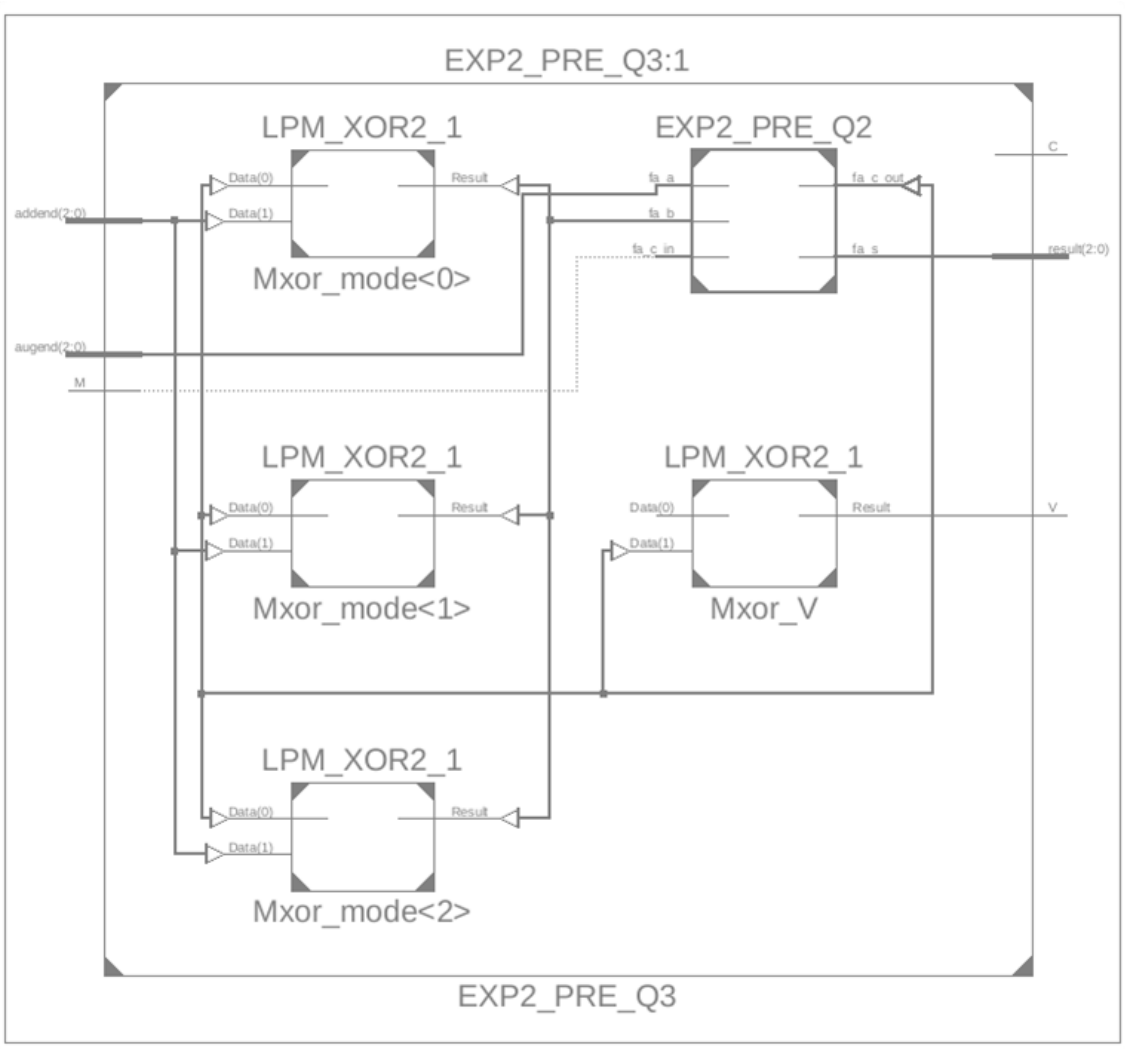
Test bench

```
stim_proc: process
begin
    fa_a <= '0'; fa_b <= '0'; fa_c_in <= '0';
    wait for 100 ns;
    fa_a <= '0'; fa_b <= '0'; fa_c_in <= '1';
    wait for 100 ns;
    fa_a <= '0'; fa_b <= '1'; fa_c_in <= '0';
    wait for 100 ns;
    fa_a <= '0'; fa_b <= '1'; fa_c_in <= '1';
    wait for 100 ns;
    fa_a <= '1'; fa_b <= '0'; fa_c_in <= '0';
    wait for 100 ns;
    fa_a <= '1'; fa_b <= '0'; fa_c_in <= '1';
    wait for 100 ns;
    fa_a <= '1'; fa_b <= '1'; fa_c_in <= '0';
    wait for 100 ns;
    fa_a <= '1'; fa_b <= '1'; fa_c_in <= '1';
    wait;
end process;
```



Q3: *Hand-drawn circuit and RTL schematic*





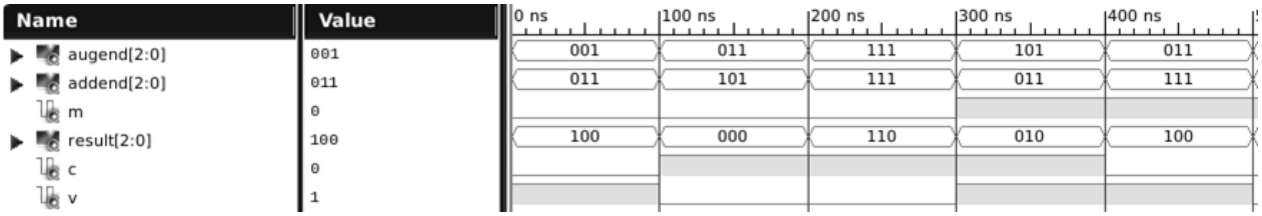
VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity EXP2_PRE_Q3 is
    Port (augend, addend : in  STD_LOGIC_VECTOR (2 downto 0);
                       M : in  STD_LOGIC;
                  result : out STD_LOGIC_VECTOR (2 downto 0);
                    C, V : out STD_LOGIC);
end EXP2_PRE_Q3;

architecture Behavioral of EXP2_PRE_Q3 is
component EXP2_PRE_Q2 is
    Port (fa_a, fa_b, fa_c_in : in  STD_LOGIC;
          fa_s, fa_c_out : out STD_LOGIC);
end component;
```

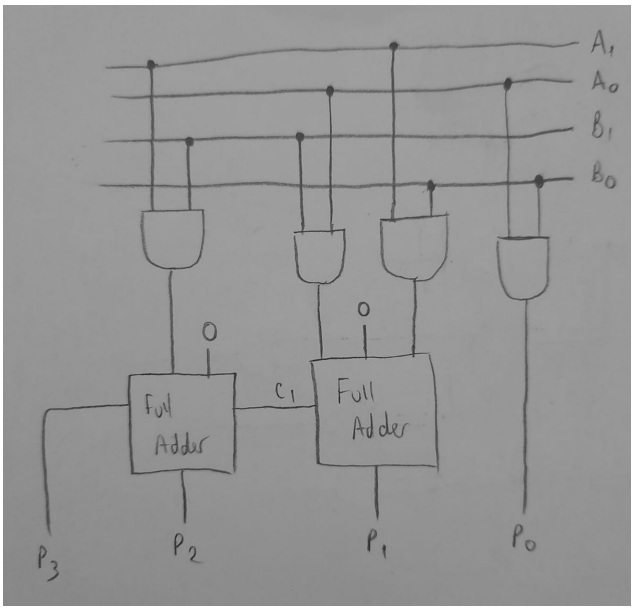
```
signal b, c : STD_LOGIC_VECTOR (2 downto 0);

begin
    b(0) <= addend(0) xor M;
    b(1) <= addend(1) xor M;
    b(2) <= addend(2) xor M;

    FullAdder1 : EXP2_PRE_Q2
        port map (augend(0), b(0), M,  result(0), c(0));
    FullAdder2 : EXP2_PRE_Q2
        port map (augend(1), b(1), c(0), result(1), c(1));
    FullAdder3 : EXP2_PRE_Q2
        port map (augend(2), b(2), c(1), result(2), c(2));
    C <= c(2);
    V <= c(1) xor c(2);
end Behavioral;
```

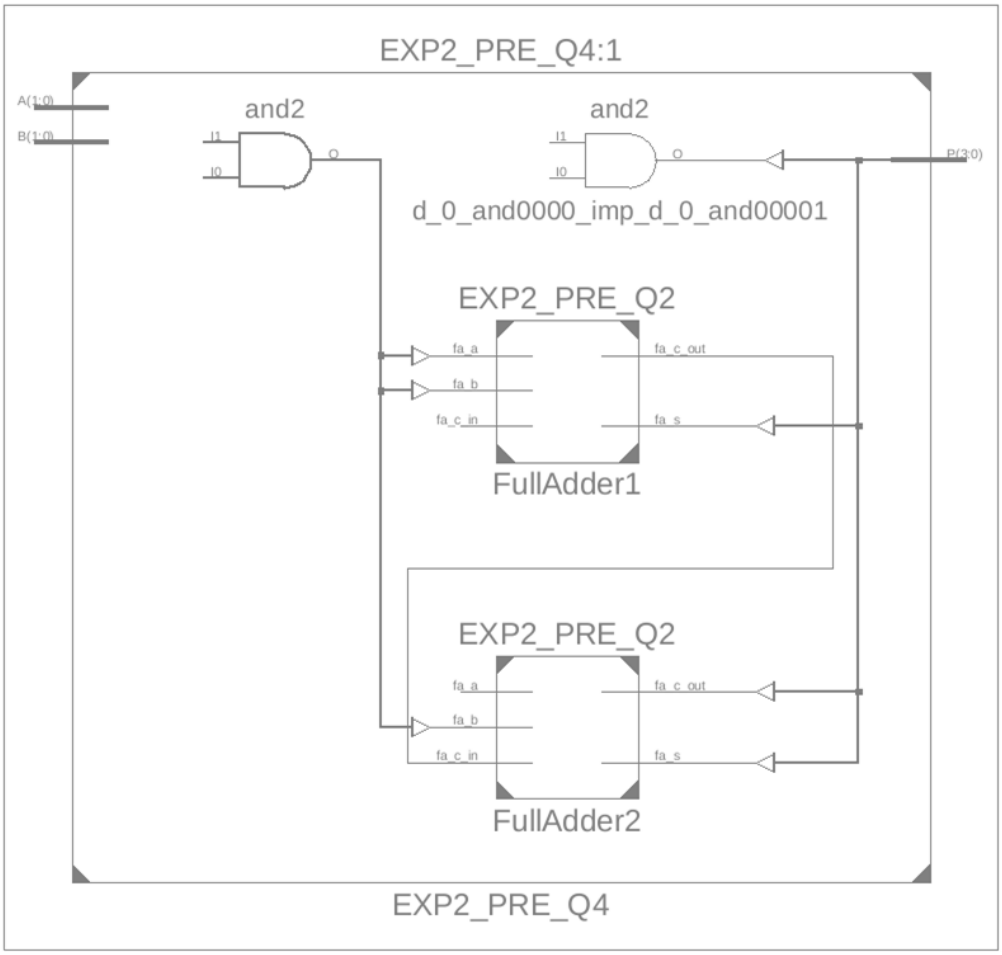
Test bench

```
stim_proc: process
begin
    M <= '0'; augend <= "001"; addend <= "011";
    wait for 100 ns;
    M <= '0'; augend <= "011"; addend <= "101";
    wait for 100 ns;
    M <= '0'; augend <= "111"; addend <= "111";
    wait for 100 ns;
    M <= '1'; augend <= "101"; addend <= "011";
    wait for 100 ns;
    M <= '1'; augend <= "011"; addend <= "111";
    wait;
end process;
```



Q4: *Hand-drawn circuit and RTL schematic*





VHDL

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity EXP2_PRE_Q4 is
    Port ( A, B : in  STD_LOGIC_VECTOR (1 downto 0);
           P : out  STD_LOGIC_VECTOR (3 downto 0));
end EXP2_PRE_Q4;

architecture Behavioral of EXP2_PRE_Q4 is
component EXP2_PRE_Q2 is
    Port (fa_a, fa_b, fa_c_in : in  STD_LOGIC;
          fa_s, fa_c_out : out STD_LOGIC);
end component;
signal d : STD_LOGIC_VECTOR (3 downto 0);
signal c : STD_LOGIC_VECTOR (2 downto 0);

begin
    d(0) <= A(0) and B(0); d(1) <= A(1) and B(0);
    d(2) <= A(0) and B(1); d(3) <= A(1) and B(1);
    P(0) <= d(0);
    FullAdder1 : EXP2_PRE_Q2
        Port map (d(1), d(2), '0', P(1), c(1));
    FullAdder2 : EXP2_PRE_Q2
        Port map ('0', d(3), c(1), P(2), c(2));
    P(3) <= c(2);
end Behavioral;
```

Test bench

```
stim_proc: process
begin
    A <= "00"; B <= "01"; wait for 100 ns;
    A <= "01"; B <= "01"; wait for 100 ns;
    A <= "10"; B <= "10"; wait for 100 ns;
    A <= "10"; B <= "11"; wait for 100 ns;
    A <= "11"; B <= "11"; wait;
end process;
```