

# Chapter 3

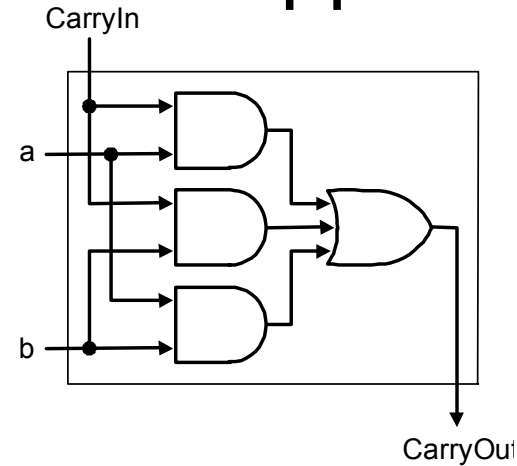
## Arithmetic for Computers



# Can We Make a Faster Adder?

- Worst case delay for N-bit Ripple Carry Adder

- 2N gate delays
- 2 gates per CarryOut
- N CarryOuts

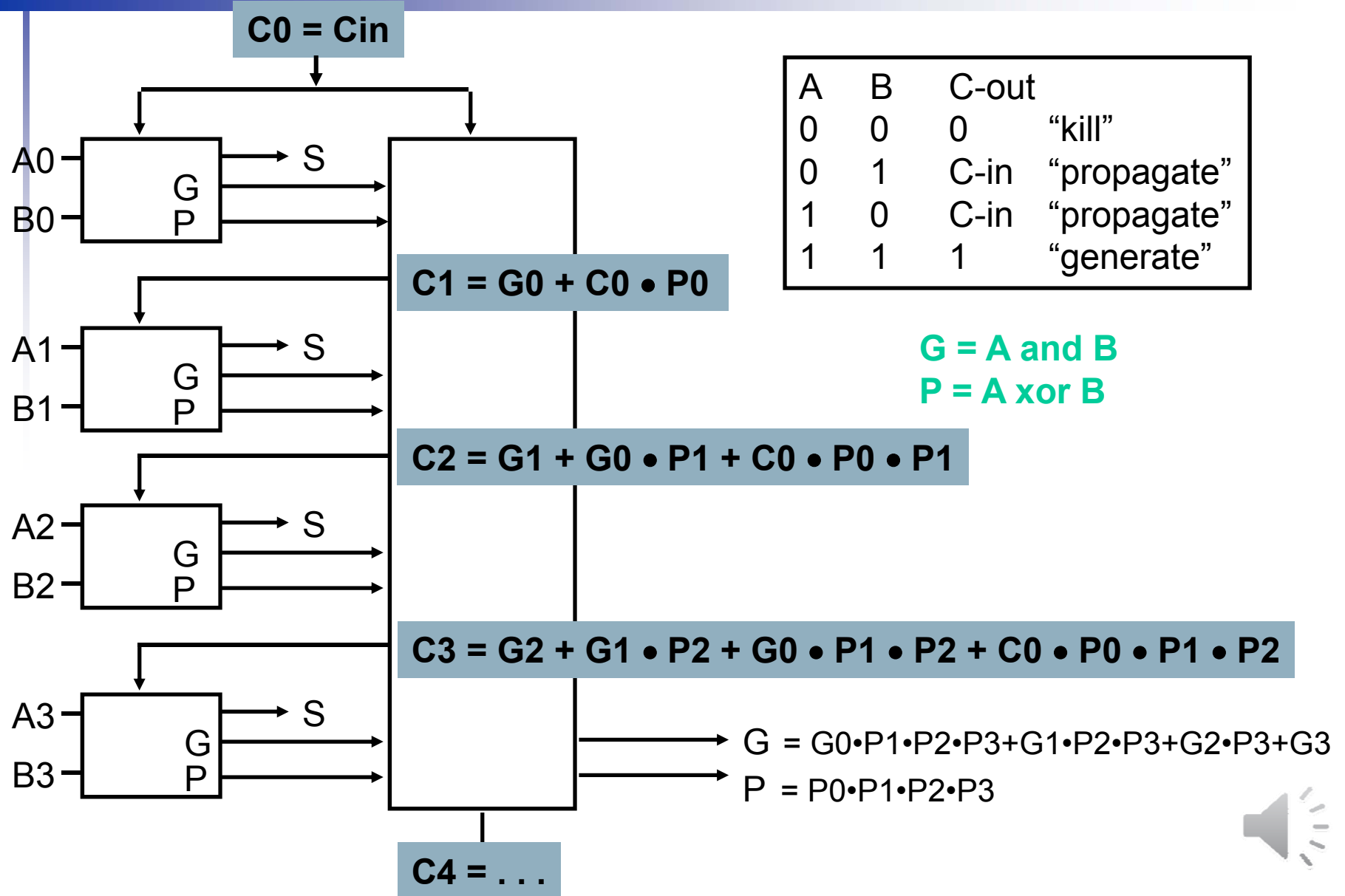


- We will explore the Carry Lookahead Adder

- Generate - Bit i creates new Carry
  - $g_i = A_i \& B_i$

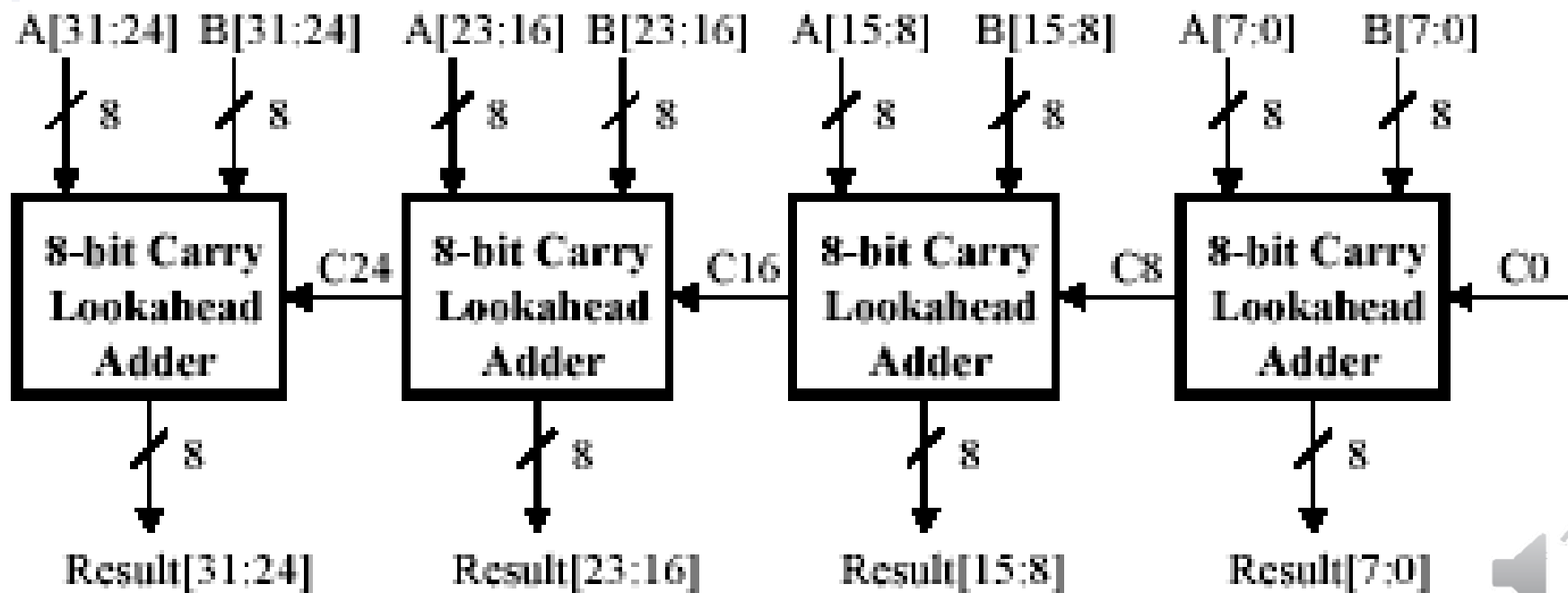


# Carry Look Ahead



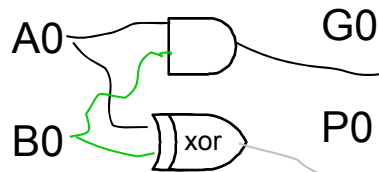
# Partial Carry Lookahead Adder

- Connect several N-bit Lookahead Adders together
- Four 8-bit carry lookahead adders can form a 32-bit partial carry lookahead adder

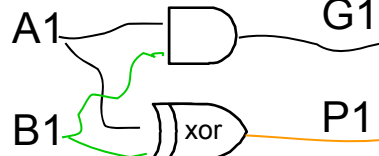


# Generate and Propagate

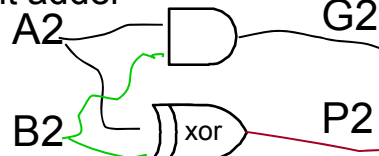
1-bit adder



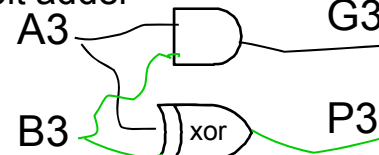
1-bit adder



1-bit adder



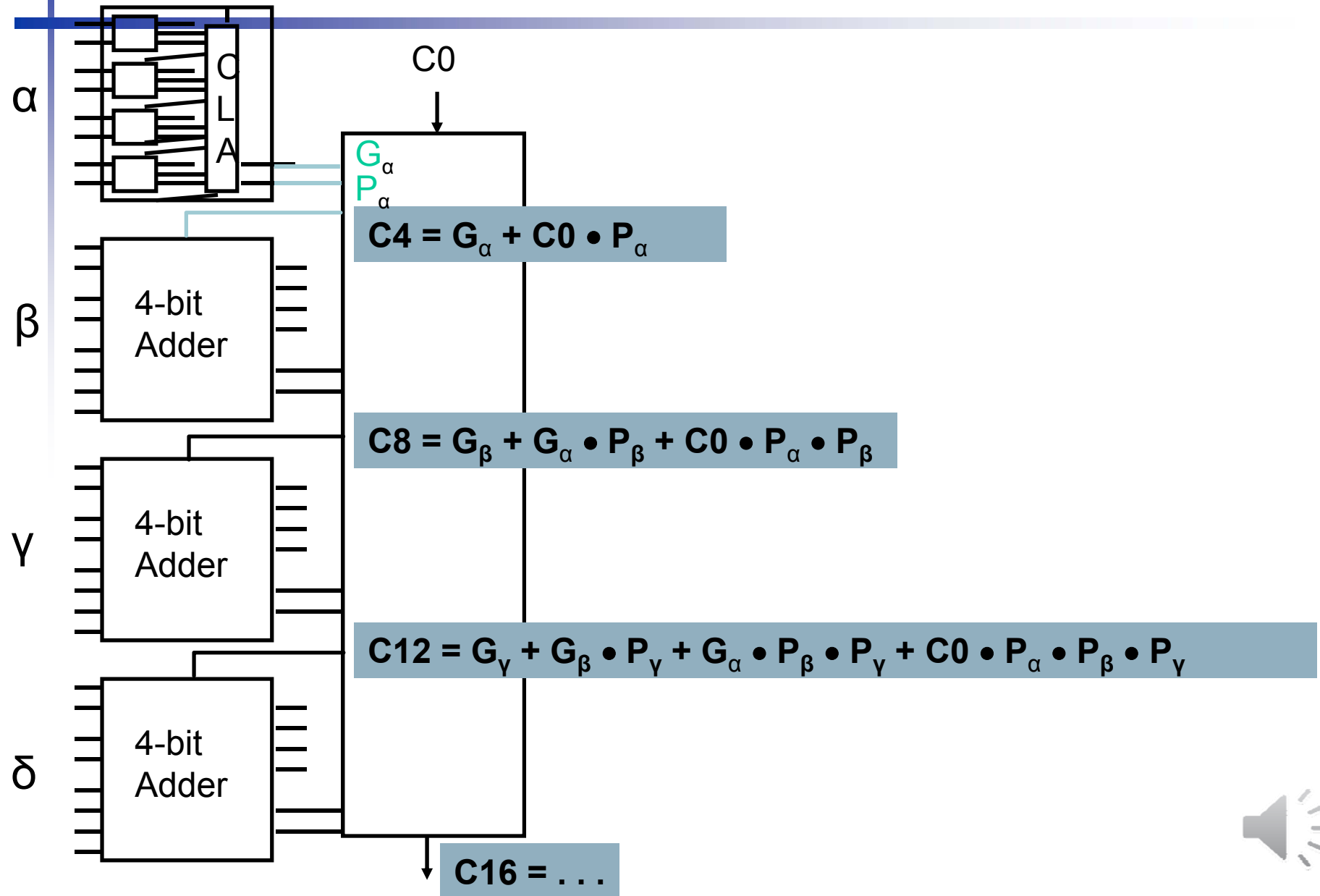
1-bit adder



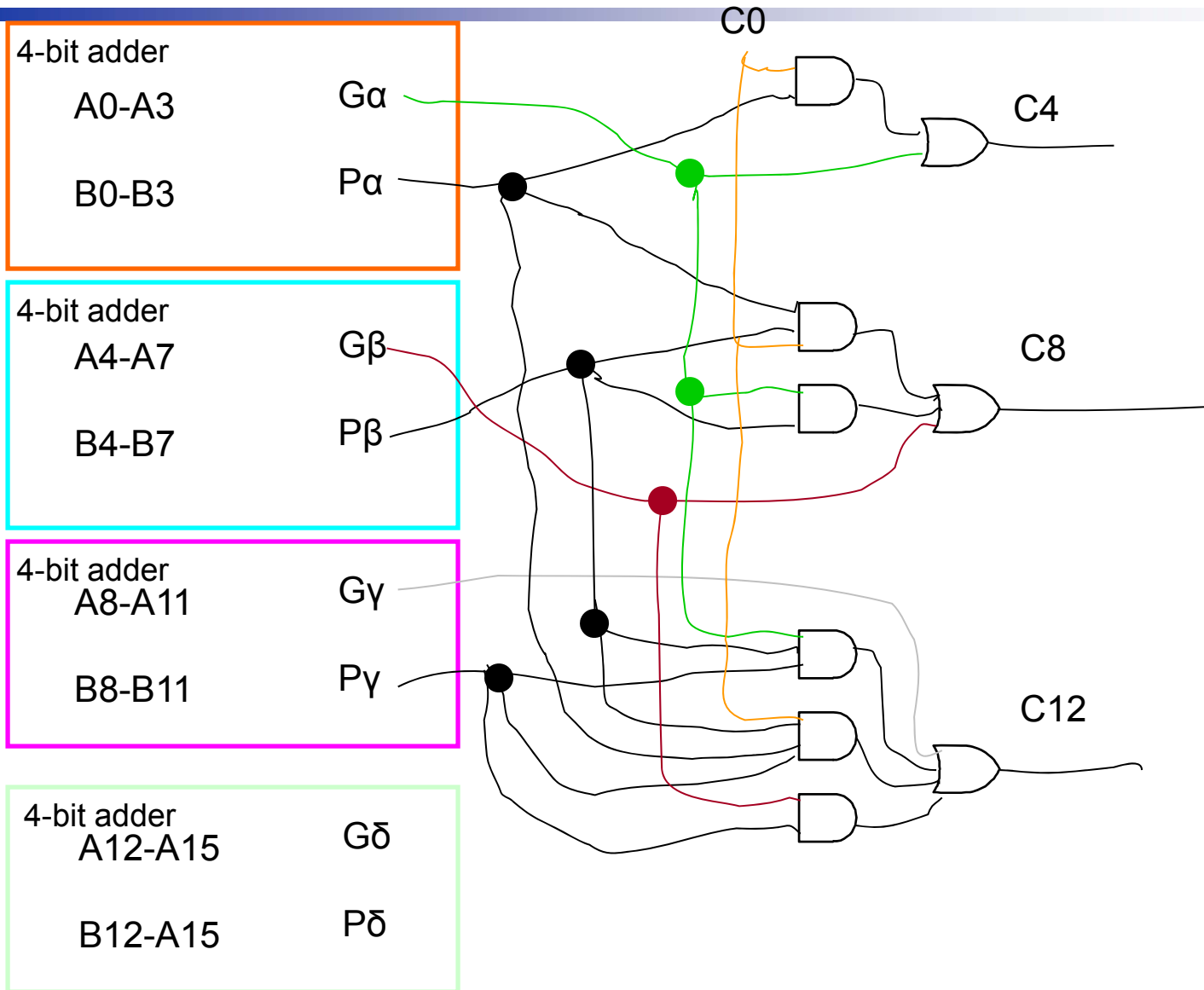
$$G_{\alpha} = G0 \cdot P1 \cdot P2 \cdot P3 + G1 \cdot P2 \cdot P3 + G2 \cdot P3 + G3$$
$$P_{\alpha} = P0 \cdot P1 \cdot P2 \cdot P3$$



# Hierarchical CLA



# Generate and Propagate



# Carry Select Adder

