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Course: CDA 4101

Project#: 4

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I hereby certify that this work is my own and none of

it is the work of any other person.

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The purpose of our assignment is to design all the major components to execute a set of LEGv8 instructions. For that purpose, we have designed a single-cycle processor with necessary combinational logic circuits and sequential logic circuits in Verilog.

The first element we need is a memory unit that stores the instructions of a program and supply instructions given an address. Then we need a program counter(PC) to hold the address of the current location, we use an adder to increment PC to the address of the next instruction. To execute any instruction, we start fetching the instruction from memory , then add 4 bytes to PC to prepare it for the next instruction.

Next, for the R-Format instructions, they will read two registers to perform an ALU operation on the contents of the registers and write the result to a register. All the processors registers are stored in the register file which will have two read ports and one write port. In the case of a load or a store instruction, they will compute a memory address by adding the base address to the 9-bits offset of the instruction. In this case we need a unit to sign-extend the 9-bit offset to a 64-bit signed value, and a data memory unit to read from or write to. For a conditional branch instruction, we have had two operands, a register that is tested for zero and an offset use to compute the branch target address relative to the branch instruction address.

We also build our CPU control unit which is going to get as an input the opcode field from the instruction, the outputs are the signals that go to the multiplexors, the signals that control the reads and writes in the memory register and data memory, a signal that determines if we branch and a 2-bit control signal for the ALU control. The execution of an instruction will take single-cycle implementation.