

Rockchip SLAVE DSMC Developer Guide

ID: RK-KF-YF-C21

Release Version: V1.0.0

Release Date: 2024-09-10

Security Level: ☐Top-Secret ☐Secret ☐Internal ☒Public

DISCLAIMER

THIS DOCUMENT IS PROVIDED "AS IS". ROCKCHIP ELECTRONICS CO., LTD. ("ROCKCHIP") DOES NOT PROVIDE ANY WARRANTY OF ANY KIND, EXPRESSED, IMPLIED OR OTHERWISE, WITH RESPECT TO THE ACCURACY, RELIABILITY, COMPLETENESS, MERCHANTABILITY, FITNESS FOR ANY PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY REPRESENTATION, INFORMATION AND CONTENT IN THIS DOCUMENT. THIS DOCUMENT IS FOR REFERENCE ONLY. THIS DOCUMENT MAY BE UPDATED OR CHANGED WITHOUT ANY NOTICE AT ANY TIME DUE TO THE UPGRADES OF THE PRODUCT OR ANY OTHER REASONS.

Trademark Statement

"Rockchip", "瑞芯微", "瑞芯" shall be Rockchip's registered trademarks and owned by Rockchip. All the other trademarks or registered trademarks mentioned in this document shall be owned by their respective owners.

All rights reserved. ©2024. Rockchip Electronics Co., Ltd.

Beyond the scope of fair use, neither any entity nor individual shall extract, copy, or distribute this document in any form in whole or in part without the written approval of Rockchip.

Rockchip Electronics Co., Ltd.

No.18 Building, A District, No.89, software Boulevard Fuzhou, Fujian, PRC

Website: www.rock-chips.com

Customer service Tel: +86-4007-700-590

Customer service Fax: +86-591-83951833

Customer service e-Mail: fae@rock-chips.com

Preface

Overview

This document provides instructions and usage methods for the kernel development of the ROCKHIP SLAVE_DSMC module.

Product Version

Chipset	Kernel Version
RK3506	kernel 6.1

Intended Audience

This document (this guide) is mainly intended for:

Technical support engineers

Software development engineers

Revision History

Version	Author	Date	Change Description
V1.0.0	Zhihuan He	2024-09-10	Initial version

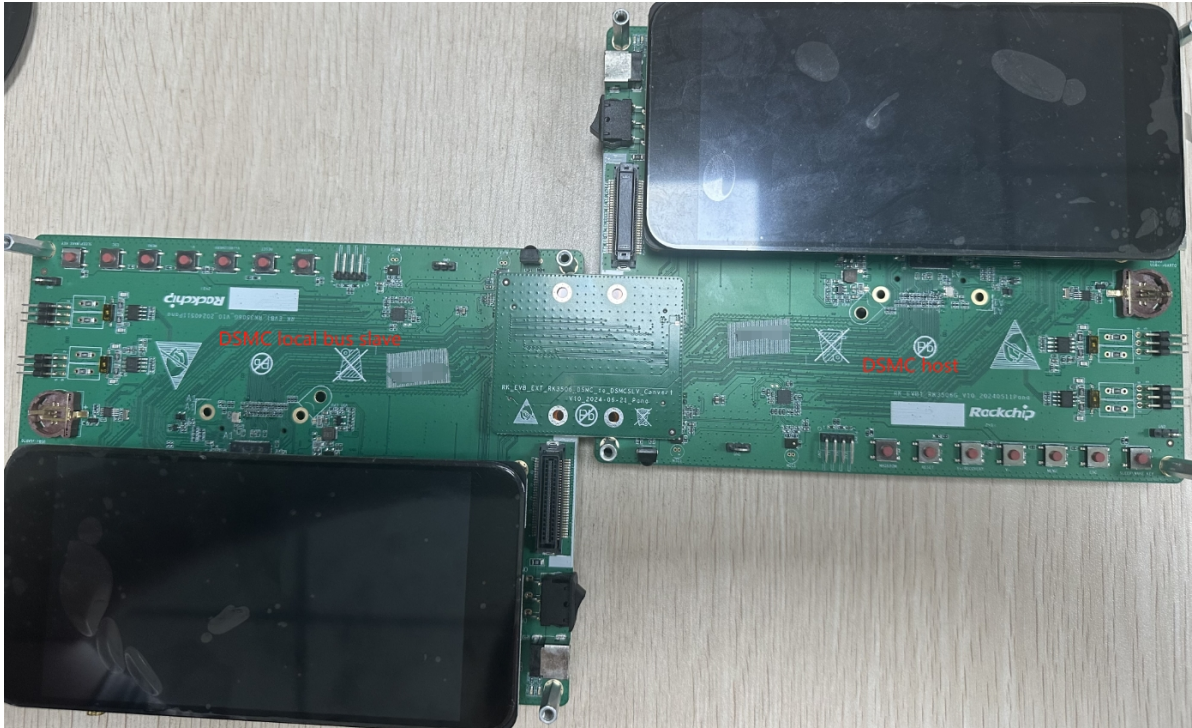
目录

Rockchip SLAVE DSMC Developer Guide

1. Overview
2. SLAVE DSMC Driver
 - 2.1 Driver Files
 - 2.2 DTS Configuration
 - 2.3 Kernel Configuration
3. Interrupts

1. Overview

The Slave Double Data Rate Serial Memory Controller (SLAVE DSMC) acts as a slave to the DSMC, only supporting the Local bus protocol, and needs to be used in conjunction with the RK-developed DSMC host controller or a controller with the same transmission protocol. For example, two RK3506 EVBs can be connected, with one EVB acting as the DSMC host and the other EVB acting as the DSMC local bus slave. The connection method is shown in the following figure:



2. SLAVE DSMC Driver

2.1 Driver Files

The driver files for SLAVE DSMC are located as follows:

```
drivers/memory/rockchip/dsmc-lb-slave.c          /* DSMC local bus slave driver */
```

2.2 DTS Configuration

```
&dsmc_lb_slave {  
    memory-region = <&dsmc_lb_slave_mem>; /* Memory region for dsmc local bus  
slave */  
    status = "okay";    /* Enable dsmc local bus slave */  
};
```

```

&reserved_memory {
    /*
     * Memory region for dsmc local bus slave, generally occupying a continuous
     space in DDR
     */
    dsmc_lb_slave_mem: dsmc-lb-slave-mem@60000000 {
        compatible = "rockchip,dsmc-lb-slave-mem";
        /* Define the start address and size of the memory space for dsmc local
        bus slave */
        reg = <0x60000000 0x20000000>;
    };
};

```

By default, the memory space allocated for the DSMC local bus slave serves as the Merged FIFO space for the DSMC host. Therefore, the memory space range of the DSMC local bus slave needs to be consistent with the rockchip,ranges property configuration on the DSMC host side.

2.3 Kernel Configuration

```

Symbol: ROCKCHIP_DSMC_SLAVE [=y]

|
| Type : tristate
|
| Prompt: Rockchip Double Data Rate Serial Memory Controller(DSMC) slave
driver
|
| Depends on: MEMORY [=y] && ARCH_ROCKCHIP
|
| Location:
|
| -> Device Drivers
|
| -> Memory Controller drivers (MEMORY [=y])
|
| -> Rockchip Double Data Rate Serial Memory Controller(DSMC) slave
driver (ROCKCHIP_DSMC_SLAVE [=y])
|

```

3. Interrupts

The DSMC slave driver registers an interrupt service routine. When the DSMC host writes to the LBC_CONx register of the DSMC slave, it will trigger the SLAVE_DSMC interrupt (host2slave interrupt). After the DSMC slave CPU receives the interrupt, it executes the `rockchip_dsmc_lb_slave_irq` interrupt service routine. If a non-zero value is written to LBC_CON15, it will trigger the slave2host interrupt by writing to APP_CON15.

After the DSMC host receives the interrupt, it will automatically initiate a certain number of DMA hardware requests, triggering DMA transfer.