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Rockchip RK3588

Hardware Design Guide

(Hardware Development Center)

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Preface

Overview

This document presents the key points of hardware design and notices for RK3588 processors, aiming to help customers shorten developing period of product, improving product design stability and reducing fault rate. Please refer to the requirements of this guide for hardware design, and use the relevant core templates released by Rockchip. If you need to modify for special reasons, please strictly follow the design rule of high-speed-digital-circuit and Rockchip Schematic&PCB checklist requirements.

Chipset model

This document is suitable for the following chipset model: **RK3588**

Intended Audience

This document (this guide) is mainly intended for:

- Hardware development engineers
- Layout engineers
- Technical support engineers
- Test engineers

Revision History

This revision history recorded description of each version, and any updates of previous versions are included in the latest one.

Version No.	Author	Revision Date	Revision Description	Remark
V1.0	Hardware Development Center	2022.01.24	Initial release	
V1.1	Hardware Development Center	2022.05.27	<ul style="list-style-type: none">1) 2.3.8.1 "The resistance value of R5008 shall not be modified arbitrarily" is changed to "The resistance value of R5018 shall not be modified arbitrarily";2) 5.4 "The RC circuit between DDR3_CLKP/N, DDR4_CLKP/N, LPDDR3_CLKP/N shall not be deleted, it can improve EMI" delete;3) Correction some mistakes;4) Modify the maximum current parameters and screenshots of each power supply in Section 2.2.2;5) Modify some text description errors in Section 2.3.4;6) Modify section 2.3.7.2;7) Modify section 2.3.8.1;8) Modify some pictures in section 3.2;9) Modify some pictures and descriptions in 3.4;10) Modified the impedance requirements in Chapter 3;11) Change the picture of PORT0/1 of TX RX of MIPI D/C PHY;12) Update the documentation download links.	

Version No.	Author	Revision Date	Revision Description	Remark
V1.2	Hardware Development Center	2022.10.21	<ul style="list-style-type: none"> 1) Added some pictures and tables in chapter 3.4.2. 2) Updated the "8-layer PTH board stackup" diagram and "8-layer PTH board impedance line reference value" table in Section 3.1.3. 3) Change Fig.2-45, Fig.2 120, Fig.2 52, Fig.2-139. 4) Update Table 2-26: The ground resistance update is 590ohm. 5) Update Table 2-6 RK3588 FSPI interface design. 6) Delete the description of the external active crystal and Table 2-1. 7) Update the peak current table in Chapter 2.2.5.3; 8) Update PMU_0V75 peak current and OTP_VDDOTP_0V75 peak current. 9) Added the HDMI2.0 RX use precautions 10) Correction of typos and punctuation. 	
V1.3	Hardware Development Center	2023.02.13	<ul style="list-style-type: none"> 1) Modify the description of CEC pin in chapter 2.3.7.4. 2) Modify the connector way of EMMC_CLK in table 2-5. 3) Delete character “8Mbps” in chapter 2.3.13. 4) Update Figure 1-1 RK3588 Block Diagram. 5) Update Figure 1-2 and Figure 1-136. 	
V1.4	Hardware Development Center	2024.03.01	<ul style="list-style-type: none"> 1) Modify the description about power in chapter 2.2.2 2) Modify the “the center voltage difference must be greater than 123mV” description in SARADC chapter 3) Modify the description about SDA/SDA of I2C in HDMI TX chapter 4) Add the description about router length of PCIE30 5) Add the description of GPIO 6) Modify the description of use 4lane in chapter MIPI D/CPHY RX 	

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1 System Introduction

1.1 Overview

RK3588 is a high-performance, low-power application processor chip. It integrates 4 Cortex-A76, 4 Cortex-A55 and independent NEON coprocessor. Suitable for ARM PC, edge computing, personal mobile Internet devices and other multimedia products.

RK3588 has built-in a variety of powerful embedded hardware engines, providing excellent performance for high-end applications. It supports 8K@60fps H.265 and VP9 decoder, 8k@30fps H.264 decoder and 4K@60fps AV1 decoder; it also supports 8K@30fps H.264 and H.265 encoder, high quality JPEG encoder/decoder, dedicated image pre-processor and post-processor.

RK3588 has a built-in 3D GPU that is fully compatible with OpenGL ES1.1/2.0/3.2, OpenCL 2.2 and Vulkan 1.2. The special 2D hardware engine with MMU will maximize the display performance and provide a smooth operating experience.

RK3588 introduces a new generation of ISP with the largest 48M pixels completely based on hardware. It implements many algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, defogging, fisheye correction, gamma correction, etc.

The NPU embedded in RK3588 supports INT4/INT8/INT16/FP16 mixed operation, and the computing power is up to 6TOP. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3588 has high-performance 4-channel external memory interfaces (LPDDR4/LPDDR4X/LPDDR5), which can support systems with high memory bandwidth requirements, and also provides a complete set of peripheral interfaces to flexibly support various Class application.

1.2 Block Diagram

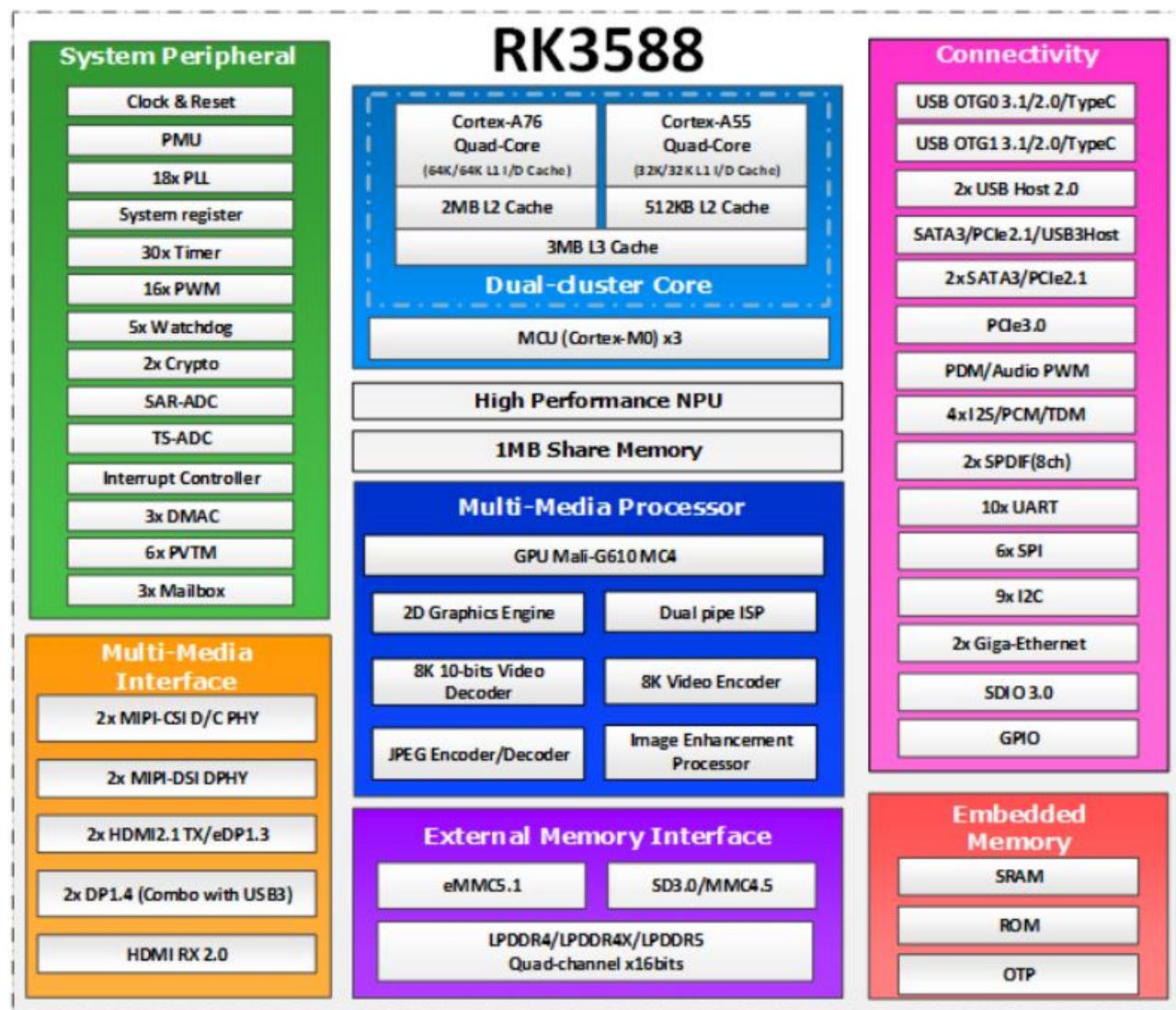


Figure 1-1 RK3588 Block Diagram

1.3 Application Block Diagram

1.3.1 RK3588 EVB Block Diagram

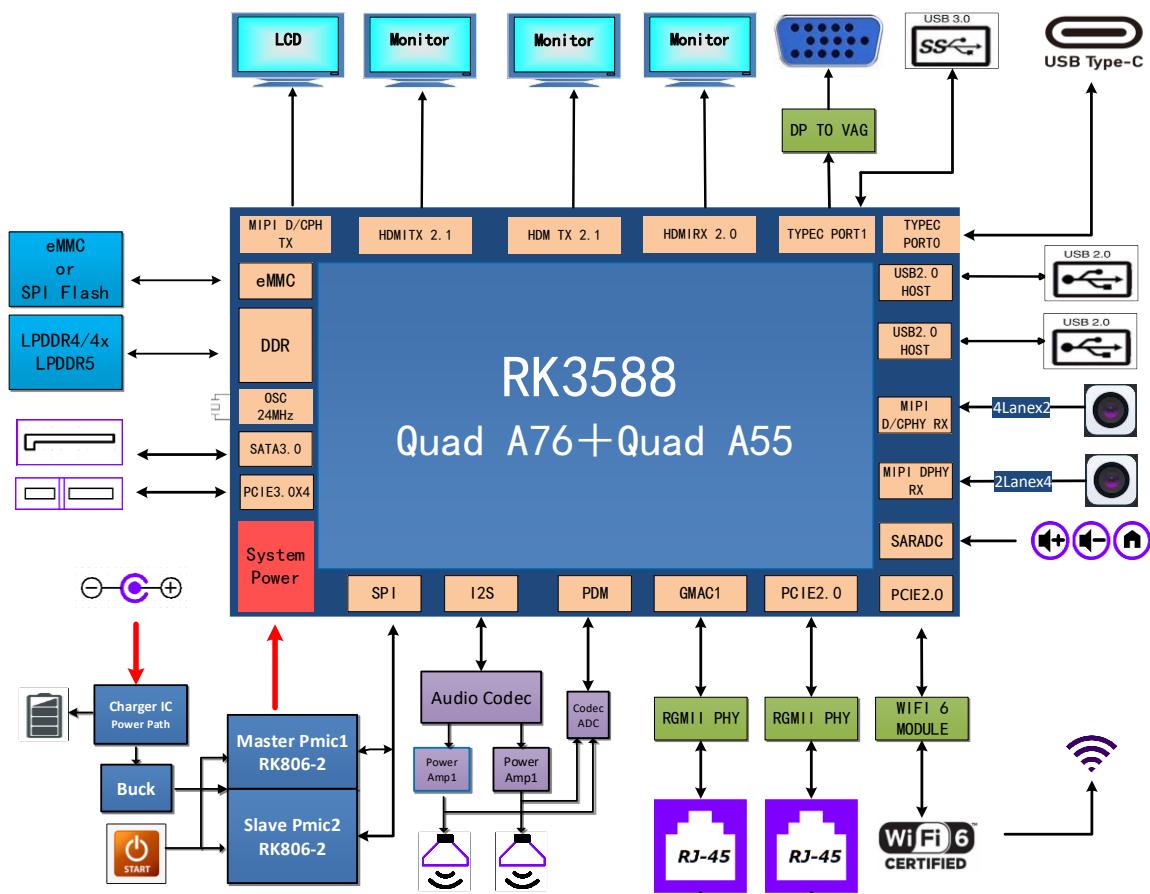


Figure 1-2 RK3588 EVB Block Diagram

1.3.2 RK3588 Smart NVR Block Diagram

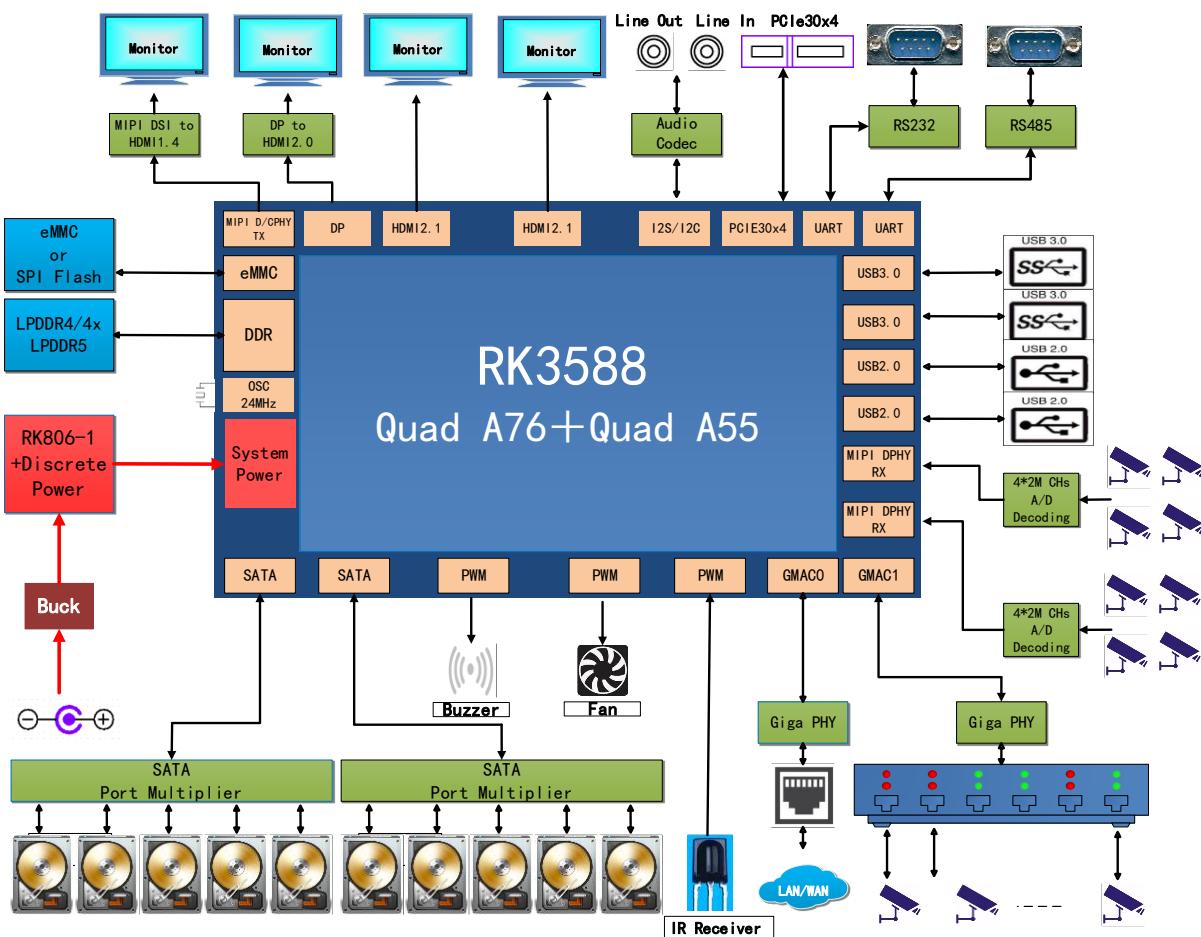


Figure 1-3 RK3588 Smart NVR Block Diagram

The figures above are examples application of RK3588, please refer to the reference design schematic released by RK for more details.

2 Schematic Design Recommendation

2.1 Minimum System Design

2.1.1 Clock Circuit

The oscillator circuit inside RK3588 and the external 24MHz crystal form the system clock, as shown in Figure 2-1. The 22ohm resistor connected to the XOUT24M network in series must be added to limit current and prevent overdrive. The 510Kohm resistor between XOUT24M and XIN24M network cannot be modified at will.

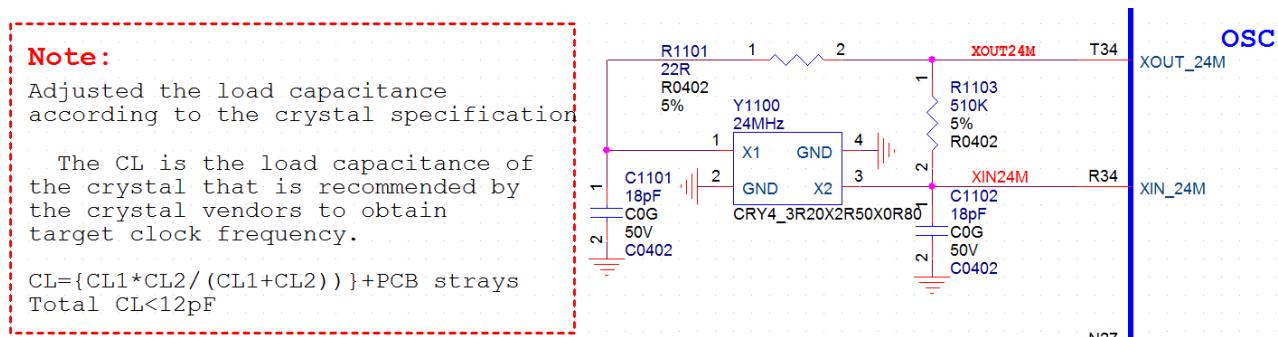


Figure 2-1 RK3588 Crystal Circuit and Components Parameters



NOTE

Note1: The CL value of the selected crystal does not exceed 12pF.

Note2: Please select the crystal load capacitance according to the CL capacitance of the crystal actually used, and control the frequency tolerance at room temperature to be within 20ppm;

18pF is the capacitance corresponding to the crystal selected by RK, not a general value. The load capacitor material is recommended to use COG or NPO;

It is recommended to use a patch 4Pin crystal, in which two GND pins are fully connected to the ground of the PCB board to strengthen the anti-ESD interference ability of the clock.

When the RK3588 is in standby, the working clock source can be switched to the clock provided by the PMU_PVTM module or the 32.768KHz clock input from the outside, and the OSC oscillator circuit is turned off to obtain better standby power consumption of the chip. At this time, only the IO interrupt wake-up in the PMUIO1 and PMUIO2 power domains is supported. If the required wake-up source is related to the 24MHz clock, the 24MHz clock cannot be turned off.

The clock oscillation ring integrated in the Process-Voltage-Temperature Monitor(PVTM) module can generate a clock. The clock frequency is determined by the delay unit of the clock oscillation ring circuit, and the generated clock can be used as the clock source for the chip's standby. When Using the external input 32.768KHz clock as RK3588 chip sleep clock, can get the optimal chip standby power consumption, PVTM module can also

be turned off at this time.

The externally input 32.768KHz clock can be obtained from an external RTC clock source. The RK3588 32.768KHz clock input pin is shown in the figure below:

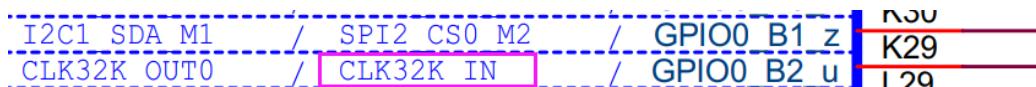


Figure 2-2 RK3588 32.768KHz Clock Input Pin in Standby

The external 32.768kHz RTC clock parameters are shown in Table 2-2 below

Table 2-1 RK3588 32.768KHZ Clock Requirements

Parameters	Spec			Description
	Min.	Max.	Unit	
Frequency	32.768000		kHz	
Frequency tolerance	+/-30		ppm	
Clock amplitude	0.7*VDD	VDD	V	VDD:PMUIO1 voltage
Operating temperature	-20	80	°C	
Duty ratio	45	55	%	



Note

When using this function, the IOMUX pin must be set to CLK32K_IN function, and the input amplitude must meet the power supply requirements of PMUIO1 Domain

RK3588 can provide working clock to peripherals:

- REFCLK_OUT: Reserve the clock output pin, which can be selected according to actual needs;
- CLK32K_OUT0: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock;
- CLK32K_OUT1: 32.768KHz clock output, which can be provided to WIFI, BT, PCIe and other devices as sleep or working clock;
- ETH0_REFCLKO_25M: 25MHz clock output, which can be provided as a working clock for devices such as Ethernet PHY;
- ETH1_REFCLKO_25M: 25MHz clock output, which can be provided as a working clock for devices such as Ethernet PHY;
- MIPI_CAMERA0_CLK-----MIPI_CAMERA4_CLK: The default 24MHz clock output can be provided to Camera and other devices as a working clock; other frequency points can also be obtained according to the PLL frequency division, and each clock supports its own output of different frequencies;
- CIF_CLKOUT: The default clock output frequency is 24Mhz. Other frequency points can be obtained according to the PLL frequency division, which can be provided to Camera and other devices as the working clock.

**Note**

The IO Domain where the above clock is located must match the IO level of the peripheral. If it does not match, a level conversion circuit must be added.

Please evaluate whether it can be met the situation according to the clock requirements of the peripheral device.

2.1.2 Reset/Watchdog/TSADC Circuit

The hardware reset of the RK3588 is input through Pin M31 (NPOR_u), which must be controlled externally and is active at low level. To ensure the stability and normal operation of the chip, the minimum reset time required is 100 24MHz main clock cycles, that is, at least 4us or more.

Pin M31 (NPOR_u) requires a 100nF capacitor to eliminate jitter on the reset signal, enhance anti-interference ability, and prevent abnormal system reset caused by false triggering.

The pull-up power of the RESET_L network must be consistent with the IO power domain (PMUIO1_1V8) where the NPOR pin is located.

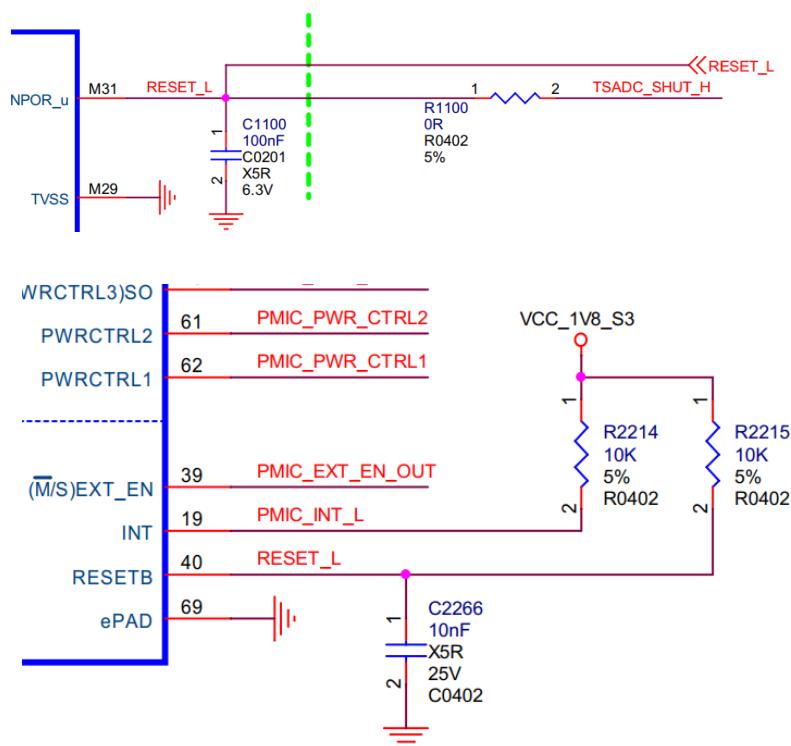


Figure 2-3 RK3588 Reset Input (RK806-1/2 Scheme)

RK3588 integrates Watchdog Timer. When a reset signal is generated, it can output low level through TSADC_SHUT pin to reset RK3588 by hardware.

RK3588 integrates 7 Temperature-Sensor ADC (TSADC) modules. When the internal temperature of the chip exceeds the threshold, the internal TSHUT signal can be sent to the CRU module to reset the RK3588 chip, or it can output low level through the TSADC_SHUT pin to reset RK3588. As shown in Figure 2-3 above, the TSADC_SHUT network is connected to the RESETn network.

RK3588 reset signal path diagram is as follows:

- dual PMIC solution:

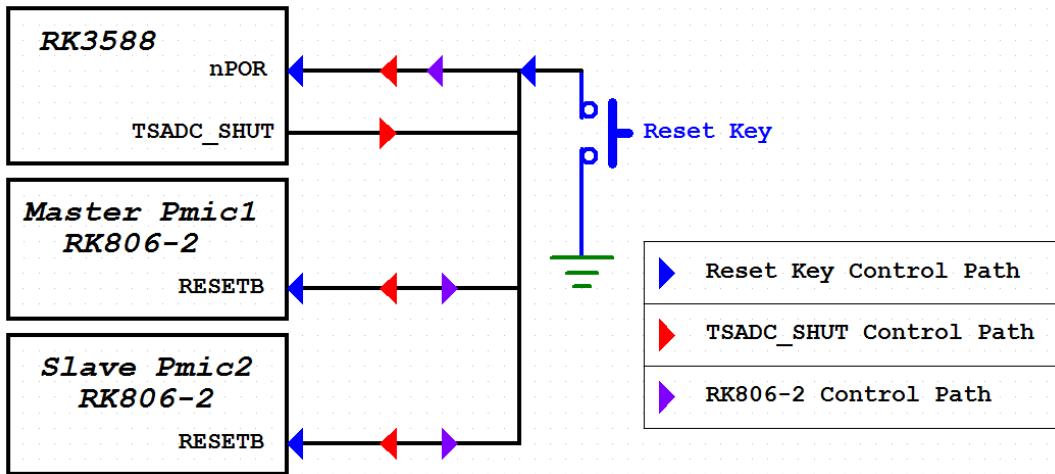


Figure 2-4 RK3588 Reset Signal Path Diagram-Dual PMIC Solution

- single PMIC solution

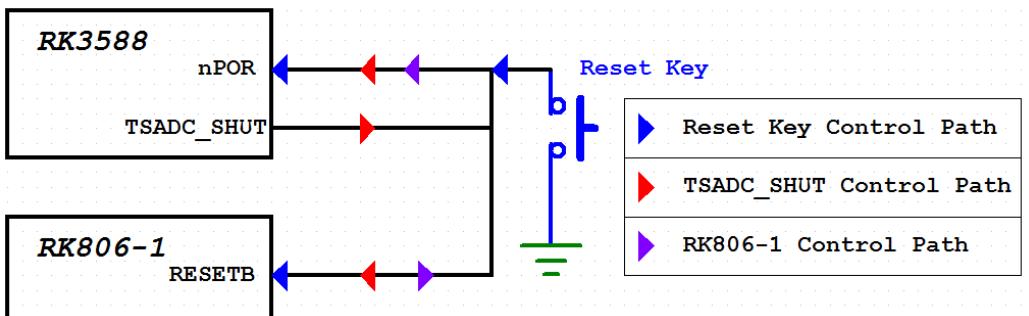


Figure 2-5 RK3588 Reset Signal Path Diagram-Single PMIC Solution

The RESETB pin of RK806-1/2 is powered on for the first time: After each power supply is powered on, RESETB will change from low level to high level (open drain output) after the set time, then completes the power-on reset process. When RK806-1/2 is in work or sleep mode, if the RESETB pin is pulled low, then RK806-1/2 will restart, and the restart power-on sequence is the same as the first power-on.

2.1.3 PMU Circuit

In order to meet the needs of low power consumption, RK3588 has designed two power management units (PMU) to control and manage the internal power supply of the chip.

This module can support chip internal registers or PMUIO power domain IO control peripheral power circuit, realize power supply and power off to other functional modules, and also support IO interrupt wake-up, so as to realize the chip's standby and wake-up functions.

2.1.4 System Boot Sequence

RK3588 supports multiple booting methods. After the chip reset, the boot code integrated in the chip can be booted in the following interface devices. The specific boot sequence can be selected according to actual application

requirements (see "Boot Sequence Selection" description below)

- Serial Flash(FSPI)
- eMMC
- SDMMC Card

If there is no boot code in the above devices, you can download the system code to these devices through the USB2.0 OTG0 interface TYPEC0_USB20_OTG_DP/ TYPEC0_USB20_OTG_DM signal.

Boot sequence selection:

The boot sequence of RK3588 can be set through SARADC_IN0_BOOT Pin (PIN AM16), which can be started from the peripherals corresponding to different interfaces. As shown in the table below, by configuring different pull-up and pull-down resistor values, the peripheral boot sequence of the seven modes of LEVEL1-LEVEL7 can be designed. When in use, it can be configured according to actual application requirements.

BOOT MODE CONFIG

TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	360K	180K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	180K	360K	2730	1.2V	FSPI M1-USB
LEVEL6	20K	100K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB



Figure 2-6 RK3588 Boot Sequence Selection

According to the above LEVEL1 setting, SARADC_IN0_BOOT is short-circuited to ground, which can make the device enter Maskrom state, no need to short-circuit EMMC_CLK/DATA to enter Maskrom. SARADC_IN1 is used to short-circuit ground to enter Recovery state; other SARADC ports can be configured according to application requirements.



NOTE

Note1: SARADC_IN0_BOOT is a dedicated pin for BOOT configuration and cannot be used for other functions

Note2: RK3588 does not support PCIe BOOT. If you need to boot from SSD hard disk with PCIe interface in the application, you need to connect SPI FLASH to FSPI interface. Boot the PCIe driver through the SPI FLASH code at startup, and then load the system in the SSD to complete the startup

2.1.5 System Initialization Configuration Signal

There is an important signal in RK3588 will affect the system boot configuration, which need to be configured and kept stable before power-on:

- SDMMC_DET pin (Pin P31): determine VCCIO2 power domain IO is SDMMC or JTAG function

After the system reset, the chip will configure the default power-on function of the corresponding module according to the input level of this pin.

The ARM JTAG function of RK3588 is multiplexed with the SDMMC function, and the IOMUX function is switched through the SDMMC_DET pin. Therefore, the configuration of this pin also needs to be completed before power-on, otherwise the ARM JTAG function has no output, which will affect the debugging during the boot stage. And no output from SDMMC will affect SDMMC boot function

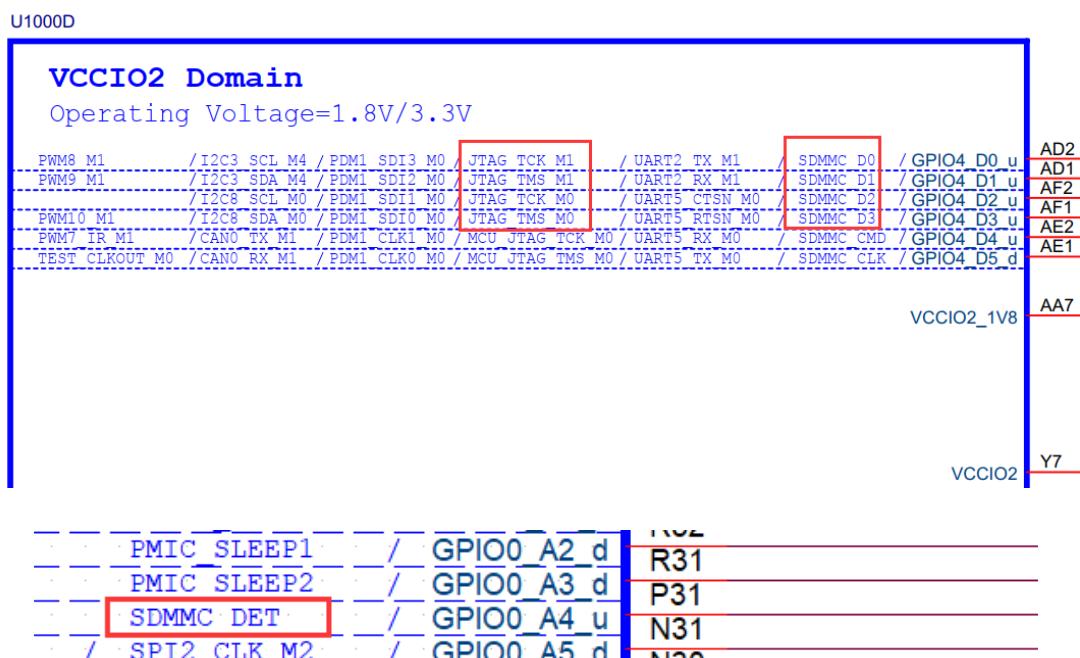


Figure 2-7 RK3588 SDMMC/ARM JTAG Multiplexed Pins and SDMMC DET Pin

- If the pin is high level, the corresponding IO will be switched to the ARM JTAG function;
- When it is low level (most SD card insertion will pull down this pin, if not, special handling is required), the corresponding IO will be switched to SDMMC function;
- After the system is up, it can be switched to register to control IOMUX, then the pin can be released;
- To facilitate the query, the configuration status and function of this pin correspond to the following table:

Table 2-2 RK3588 System Initialization Configuration Signal Description

Signal name	Internal up and down	Description
SDMMC_DET	Pull up	SDMMC/ARM JATG pin multiplexing selection control signal: 0: Recognized as SD card insertion, SDMMC/ARM JATG pins are multiplexed as SDMMC function; 1: Not recognized as SD card insertion, SDMMC/ARM JATG pins are multiplexed as ARM JTAG function (Default)

2.1.6 JTAG and UART Debug Circuit

The ARM JTAG interface of RK3588 conforms to the IEEE1149.1 standard. The PC can be connected to the DSTREAM emulator through SWD mode (two-wire mode) to debug ARM Core inside the chip.

When connecting to emulator during booting, you need to ensure that the SDMMC_DET pin is at a high level, otherwise, it cannot enter the JTAG debugging mode. The management configuration is described in the previous sections.

After the system is up, it will switch to control IOMUX by register. The ARM JTAG interface introduction is shown in the following Table:

Table 2-3 RK3588 JTAG debug interface signal

Signal name	Description
JTAG_TCK_M0/M1	Clock input in SWD mode
JTAG_TMS_M0/M1	Data input and output in SWD mode

The connection method of JTAG and the definition of standard connector pins are shown in the figure below:

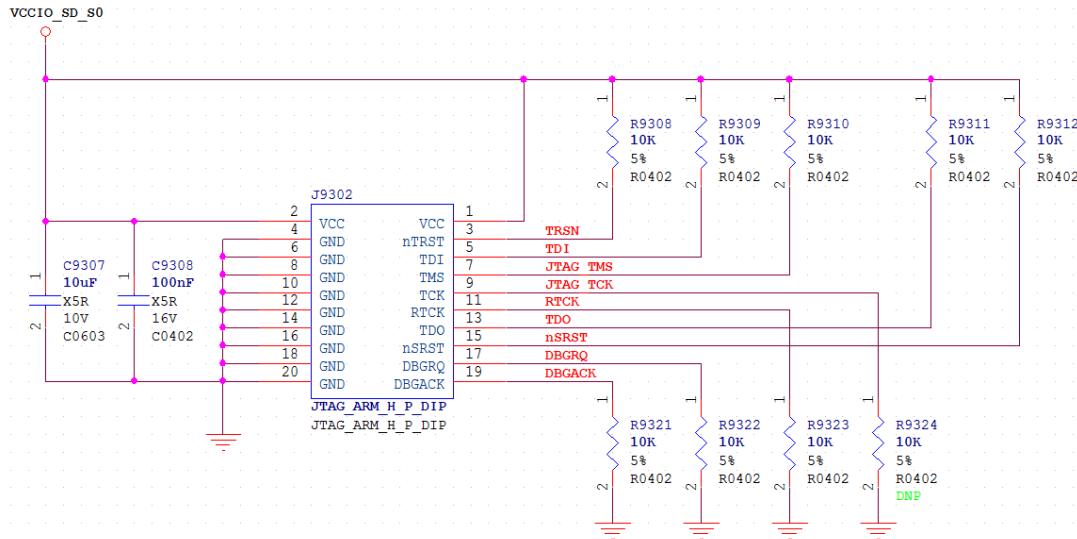


Figure 2-8 RK3588 JTAG Connection Schematic

If there is no SD Card function, it is recommended to reserve the ARM JTAG function to facilitate debugging. The reserved circuit is as shown in the figure below:

- Note that the VCCIO2_1V8 (PIN AA7) power supply must be powered, and the power supply voltage can use VCC_1V8_S3;
- The power supply of VCCIO2 (PIN Y7) must be supplied, and the supply voltage can be VCCIO_SD_S0 or VCC_3V3_S3.

U1000D

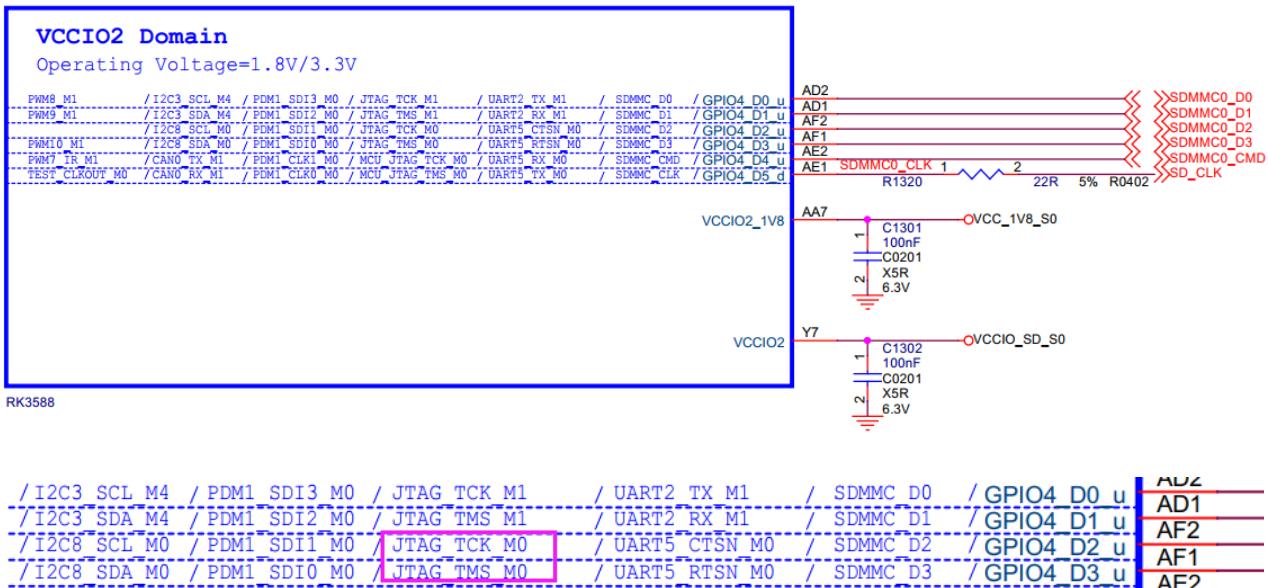


Figure 2-9 RK3588 ARM JTAG Pin

The MCU_JTAG module of RK3588 is temporarily not open to the public, and no special treatment is required. RK3588 UART Debug selects UART2_RX_M0/UART2_TX_M0 by default, and the default baud rate is 1500000bps.



Figure 2-10 RK3588 UART2 M0 Pin

The 100ohm resistor connected in UART2_RX_M0/UART2_TX_M0 should not be deleted, and TVS tube should be added to strengthen the anti-static surge ability to prevent damage to the chip pins during the development process. It is recommended to reserve 2.54 pins as much as possible. If conditions are not allowed, it is recommended to use test points above 0.7mm or larger to facilitate soldering

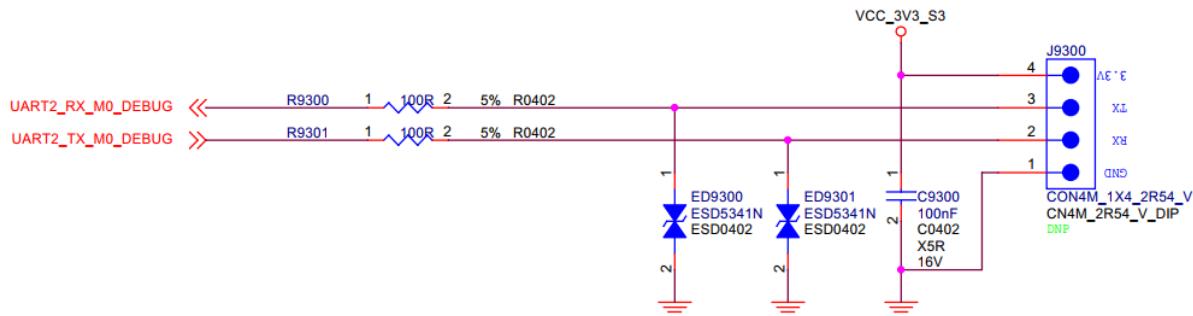


Figure 2-11 RK3588 Debug UART2 Connection Diagram

2.1.7 DDR Circuit

2.1.7.1 DDR Controller Introduction

The RK3588 DDR controller interface supports JEDEC SDRAM standard interface with following features:

- Compatible with LPDDR4/LPDDR4X/LPDDR5 standards;
- Supports 64bits data bus width, composed of 4 16bits DDR channels, each channel has a maximum addressing address of 8GB; 4 channels can support a total capacity of 32GB;
- Two 16bits form a 32bits channel, and the two 32bits channels (that is, CH0 and CH1 channels in the schematic diagram) cannot be configured with different capacities, such as 4GB+2GB;
- Support Power Down, Self Refresh and other modes;
- Programmable output with dynamic PVT compensation and ODT impedance adjustment.

2.1.7.2 Circuit Design Suggestion

The schematic of RK3588 DDR PHY and each DRAM need to be consistent with the reference design diagram, including power supply decoupling capacitors.

RK3588 supports LPDDR4/LPDDR4X, LPDDR5. These DRAM have different I/O signals. Choose the signal according to the DRAM type. The RK3588 DDR PHY I/O Map is as follows:

Table 2-4 RK3588 DDR PHY I/O Map

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH0_DQ0_A	DDR_CH0_DQ0_A	DDR_CH0_DQ0_A
DDR_CH0_DQ1_A	DDR_CH0_DQ1_A	DDR_CH0_DQ1_A
DDR_CH0_DQ2_A	DDR_CH0_DQ2_A	DDR_CH0_DQ2_A
DDR_CH0_DQ3_A	DDR_CH0_DQ3_A	DDR_CH0_DQ3_A
DDR_CH0_DQ4_A	DDR_CH0_DQ4_A	DDR_CH0_DQ4_A
DDR_CH0_DQ5_A	DDR_CH0_DQ5_A	DDR_CH0_DQ5_A
DDR_CH0_DQ6_A	DDR_CH0_DQ6_A	DDR_CH0_DQ6_A
DDR_CH0_DQ7_A	DDR_CH0_DQ7_A	DDR_CH0_DQ7_A
DDR_CH0_DQ8_A	DDR_CH0_DQ8_A	DDR_CH0_DQ8_A
DDR_CH0_DQ9_A	DDR_CH0_DQ9_A	DDR_CH0_DQ9_A
DDR_CH0_DQ10_A	DDR_CH0_DQ10_A	DDR_CH0_DQ10_A
DDR_CH0_DQ11_A	DDR_CH0_DQ11_A	DDR_CH0_DQ11_A
DDR_CH0_DQ12_A	DDR_CH0_DQ12_A	DDR_CH0_DQ12_A
DDR_CH0_DQ13_A	DDR_CH0_DQ13_A	DDR_CH0_DQ13_A
DDR_CH0_DQ14_A	DDR_CH0_DQ14_A	DDR_CH0_DQ14_A
DDR_CH0_DQ15_A	DDR_CH0_DQ15_A	DDR_CH0_DQ15_A
DDR_CH0_WCK0P_A	/	DDR_CH0_WCK0P_A
DDR_CH0_WCK0N_A	/	DDR_CH0_WCK0N_A
DDR_CH0_WCK1P_A	/	DDR_CH0_WCK1P_A
DDR_CH0_WCK1N_A	/	DDR_CH0_WCK1N_A
DDR_CH0_DQS0P_A	DDR_CH0_DQS0P_A	DDR_CH0_DQS0P_A
DDR_CH0_DQS0N_A	DDR_CH0_DQS0N_A	DDR_CH0_DQS0N_A
DDR_CH0_DQS1P_A	DDR_CH0_DQS1P_A	DDR_CH0_DQS1P_A
DDR_CH0_DQS1N_A	DDR_CH0_DQS1N_A	DDR_CH0_DQS1N_A

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH0_DM0_A	DDR_CH0_DM0_A	DDR_CH0_DM0_A
DDR_CH0_DM1_A	DDR_CH0_DM1_A	DDR_CH0_DM1_A
DDR_CH0_A0_A	DDR_CH0_A0_A	DDR_CH0_A0_A
DDR_CH0_A1_A	DDR_CH0_A1_A	DDR_CH0_A1_A
DDR_CH0_A2_A	DDR_CH0_A2_A	DDR_CH0_A2_A
DDR_CH0_A3_A	DDR_CH0_A3_A	DDR_CH0_A3_A
DDR_CH0_A4_A	DDR_CH0_A4_A	DDR_CH0_A4_A
DDR_CH0_A5_A	DDR_CH0_A5_A	DDR_CH0_A5_A
DDR_CH0_A6_A	DDR_CH0_A6_A	DDR_CH0_A6_A
DDR_CH0_CK_A	DDR_CH0_CK_A	DDR_CH0_CK_A
DDR_CH0_CKB_A	DDR_CH0_CKB_A	DDR_CH0_CKB_A
DDR_CH0_LP4/4X_CS0_A	DDR_CH0_LP4/4X_CS0_A	/
DDR_CH0_LP4/4X_CS1_A	DDR_CH0_LP4/4X_CS1_A	/
DDR_CH0_LP4/4X_CKE0/LP5_CS0_A	DDR_CH0_LP4/4X_CKE0_A	DDR_CH0_LP5_CS0_A
DDR_CH0_LP4/4X_CKE1/LP5_CS1_A	DDR_CH0_LP4/4X_CKE1_A	DDR_CH0_LP5_CS1_A
DDR_CH0_ZQ_A	DDR_CH0_ZQ_A	DDR_CH0_ZQ_A
DDR_CH0_RESET_A	DDR_CH0_RESET_A	DDR_CH0_RESET_A
DDR_CH0_DQ0_B	DDR_CH0_DQ0_B	DDR_CH0_DQ0_B
DDR_CH0_DQ1_B	DDR_CH0_DQ1_B	DDR_CH0_DQ1_B
DDR_CH0_DQ2_B	DDR_CH0_DQ2_B	DDR_CH0_DQ2_B
DDR_CH0_DQ3_B	DDR_CH0_DQ3_B	DDR_CH0_DQ3_B
DDR_CH0_DQ4_B	DDR_CH0_DQ4_B	DDR_CH0_DQ4_B
DDR_CH0_DQ5_B	DDR_CH0_DQ5_B	DDR_CH0_DQ5_B
DDR_CH0_DQ6_B	DDR_CH0_DQ6_B	DDR_CH0_DQ6_B
DDR_CH0_DQ7_B	DDR_CH0_DQ7_B	DDR_CH0_DQ7_B
DDR_CH0_DQ8_B	DDR_CH0_DQ8_B	DDR_CH0_DQ8_B
DDR_CH0_DQ9_B	DDR_CH0_DQ9_B	DDR_CH0_DQ9_B
DDR_CH0_DQ10_B	DDR_CH0_DQ10_B	DDR_CH0_DQ10_B
DDR_CH0_DQ11_B	DDR_CH0_DQ11_B	DDR_CH0_DQ11_B
DDR_CH0_DQ12_B	DDR_CH0_DQ12_B	DDR_CH0_DQ12_B
DDR_CH0_DQ13_B	DDR_CH0_DQ13_B	DDR_CH0_DQ13_B
DDR_CH0_DQ14_B	DDR_CH0_DQ14_B	DDR_CH0_DQ14_B
DDR_CH0_DQ15_B	DDR_CH0_DQ15_B	DDR_CH0_DQ15_B
DDR_CH0_WCK0P_B	/	DDR_CH0_WCK0P_B
DDR_CH0_WCK0N_B	/	DDR_CH0_WCK0N_B
DDR_CH0_WCK1P_B	/	DDR_CH0_WCK1P_B
DDR_CH0_WCK1N_B	/	DDR_CH0_WCK1N_B
DDR_CH0_DQS0P_B	DDR_CH0_DQS0P_B	DDR_CH0_DQS0P_B

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH0_DQS0N_B	DDR_CH0_DQS0N_B	DDR_CH0_DQS0N_B
DDR_CH0_DQS1P_B	DDR_CH0_DQS1P_B	DDR_CH0_DQS1P_B
DDR_CH0_DQS1N_B	DDR_CH0_DQS1N_B	DDR_CH0_DQS1N_B
DDR_CH0_DM0_B	DDR_CH0_DM0_B	DDR_CH0_DM0_B
DDR_CH0_DM1_B	DDR_CH0_DM1_B	DDR_CH0_DM1_B
DDR_CH0_A0_B	DDR_CH0_A0_B	DDR_CH0_A0_B
DDR_CH0_A1_B	DDR_CH0_A1_B	DDR_CH0_A1_B
DDR_CH0_A2_B	DDR_CH0_A2_B	DDR_CH0_A2_B
DDR_CH0_A3_B	DDR_CH0_A3_B	DDR_CH0_A3_B
DDR_CH0_A4_B	DDR_CH0_A4_B	DDR_CH0_A4_B
DDR_CH0_A5_B	DDR_CH0_A5_B	DDR_CH0_A5_B
DDR_CH0_A6_B	DDR_CH0_A6_B	DDR_CH0_A6_B
DDR_CH0_CK_B	DDR_CH0_CK_B	DDR_CH0_CK_B
DDR_CH0_CKB_B	DDR_CH0_CKB_B	DDR_CH0_CKB_B
DDR_CH0_LP4/4X_CS0_B	DDR_CH0_LP4/4X_CS0_B	/
DDR_CH0_LP4/4X_CS1_B	DDR_CH0_LP4/4X_CS1_B	/
DDR_CH0_LP4/4X_CKE0/LP5_CS0_B	DDR_CH0_LP4/4X_CKE0_B	DDR_CH0_LP5_CS0_B
DDR_CH0_LP4/4X_CKE1/LP5_CS1_B	DDR_CH0_LP4/4X_CKE1_B	DDR_CH0_LP5_CS1_B
DDR_CH0_ZQ_B	DDR_CH0_ZQ_B	DDR_CH0_ZQ_B
DDR_CH0_RESET_B	DDR_CH0_RESET_B	DDR_CH0_RESET_B
DDR_CH1_DQ0_C	DDR_CH1_DQ0_C	DDR_CH1_DQ0_C
DDR_CH1_DQ1_C	DDR_CH1_DQ1_C	DDR_CH1_DQ1_C
DDR_CH1_DQ2_C	DDR_CH1_DQ2_C	DDR_CH1_DQ2_C
DDR_CH1_DQ3_C	DDR_CH1_DQ3_C	DDR_CH1_DQ3_C
DDR_CH1_DQ4_C	DDR_CH1_DQ4_C	DDR_CH1_DQ4_C
DDR_CH1_DQ5_C	DDR_CH1_DQ5_C	DDR_CH1_DQ5_C
DDR_CH1_DQ6_C	DDR_CH1_DQ6_C	DDR_CH1_DQ6_C
DDR_CH1_DQ7_C	DDR_CH1_DQ7_C	DDR_CH1_DQ7_C
DDR_CH1_DQ8_C	DDR_CH1_DQ8_C	DDR_CH1_DQ8_C
DDR_CH1_DQ9_C	DDR_CH1_DQ9_C	DDR_CH1_DQ9_C
DDR_CH1_DQ10_C	DDR_CH1_DQ10_C	DDR_CH1_DQ10_C
DDR_CH1_DQ11_C	DDR_CH1_DQ11_C	DDR_CH1_DQ11_C
DDR_CH1_DQ12_C	DDR_CH1_DQ12_C	DDR_CH1_DQ12_C
DDR_CH1_DQ13_C	DDR_CH1_DQ13_C	DDR_CH1_DQ13_C
DDR_CH1_DQ14_C	DDR_CH1_DQ14_C	DDR_CH1_DQ14_C
DDR_CH1_DQ15_C	DDR_CH1_DQ15_C	DDR_CH1_DQ15_C
DDR_CH1_WCK0P_C	/	DDR_CH1_WCK0P_C
DDR_CH1_WCK0N_C	/	DDR_CH1_WCK0N_C

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH1_WCK1P_C	/	DDR_CH1_WCK1P_C
DDR_CH1_WCK1N_C	/	DDR_CH1_WCK1N_C
DDR_CH1_DQS0P_C	DDR_CH1_DQS0P_C	DDR_CH1_DQS0P_C
DDR_CH1_DQS0N_C	DDR_CH1_DQS0N_C	DDR_CH1_DQS0N_C
DDR_CH1_DQS1P_C	DDR_CH1_DQS1P_C	DDR_CH1_DQS1P_C
DDR_CH1_DQS1N_C	DDR_CH1_DQS1N_C	DDR_CH1_DQS1N_C
DDR_CH1_DM0_C	DDR_CH1_DM0_C	DDR_CH1_DM0_C
DDR_CH1_DM1_C	DDR_CH1_DM1_C	DDR_CH1_DM1_C
DDR_CH1_A0_C	DDR_CH1_A0_C	DDR_CH1_A0_C
DDR_CH1_A1_C	DDR_CH1_A1_C	DDR_CH1_A1_C
DDR_CH1_A2_C	DDR_CH1_A2_C	DDR_CH1_A2_C
DDR_CH1_A3_C	DDR_CH1_A3_C	DDR_CH1_A3_C
DDR_CH1_A4_C	DDR_CH1_A4_C	DDR_CH1_A4_C
DDR_CH1_A5_C	DDR_CH1_A5_C	DDR_CH1_A5_C
DDR_CH1_A6_C	DDR_CH1_A6_C	DDR_CH1_A6_C
DDR_CH1_CK_C	DDR_CH1_CK_C	DDR_CH1_CK_C
DDR_CH1_CKB_C	DDR_CH1_CKB_C	DDR_CH1_CKB_C
DDR_CH1_LP4/4X_CS0_C	DDR_CH1_LP4/4X_CS0_C	/
DDR_CH1_LP4/4X_CS1_C	DDR_CH1_LP4/4X_CS1_C	/
DDR_CH1_LP4/4X_CKE0/LP5_CS0_C	DDR_CH1_LP4/4X_CKE0_C	DDR_CH1_LP5_CS0_C
DDR_CH1_LP4/4X_CKE1/LP5_CS1_C	DDR_CH1_LP4/4X_CKE1_C	DDR_CH1_LP5_CS1_C
DDR_CH1_ZQ_C	DDR_CH1_ZQ_C	DDR_CH1_ZQ_C
DDR_CH1_RESET_C	DDR_CH1_RESET_C	DDR_CH1_RESET_C
DDR_CH1_DQ0_D	DDR_CH1_DQ0_D	DDR_CH1_DQ0_D
DDR_CH1_DQ1_D	DDR_CH1_DQ1_D	DDR_CH1_DQ1_D
DDR_CH1_DQ2_D	DDR_CH1_DQ2_D	DDR_CH1_DQ2_D
DDR_CH1_DQ3_D	DDR_CH1_DQ3_D	DDR_CH1_DQ3_D
DDR_CH1_DQ4_D	DDR_CH1_DQ4_D	DDR_CH1_DQ4_D
DDR_CH1_DQ5_D	DDR_CH1_DQ5_D	DDR_CH1_DQ5_D
DDR_CH1_DQ6_D	DDR_CH1_DQ6_D	DDR_CH1_DQ6_D
DDR_CH1_DQ7_D	DDR_CH1_DQ7_D	DDR_CH1_DQ7_D
DDR_CH1_DQ8_D	DDR_CH1_DQ8_D	DDR_CH1_DQ8_D
DDR_CH1_DQ9_D	DDR_CH1_DQ9_D	DDR_CH1_DQ9_D
DDR_CH1_DQ10_D	DDR_CH1_DQ10_D	DDR_CH1_DQ10_D
DDR_CH1_DQ11_D	DDR_CH1_DQ11_D	DDR_CH1_DQ11_D
DDR_CH1_DQ12_D	DDR_CH1_DQ12_D	DDR_CH1_DQ12_D
DDR_CH1_DQ13_D	DDR_CH1_DQ13_D	DDR_CH1_DQ13_D
DDR_CH1_DQ14_D	DDR_CH1_DQ14_D	DDR_CH1_DQ14_D

DDR signal	LPDDR4/4x	LPDDR5
DDR_CH1_DQ15_D	DDR_CH1_DQ15_D	DDR_CH1_DQ15_D
DDR_CH1_WCK0P_D	/	DDR_CH1_WCK0P_D
DDR_CH1_WCK0N_D	/	DDR_CH1_WCK0N_D
DDR_CH1_WCK1P_D	/	DDR_CH1_WCK1P_D
DDR_CH1_WCK1N_D	/	DDR_CH1_WCK1N_D
DDR_CH1_DQS0P_D	DDR_CH1_DQS0P_D	DDR_CH1_DQS0P_D
DDR_CH1_DQS0N_D	DDR_CH1_DQS0N_D	DDR_CH1_DQS0N_D
DDR_CH1_DQS1P_D	DDR_CH1_DQS1P_D	DDR_CH1_DQS1P_D
DDR_CH1_DQS1N_D	DDR_CH1_DQS1N_D	DDR_CH1_DQS1N_D
DDR_CH1_DM0_D	DDR_CH1_DM0_D	DDR_CH1_DM0_D
DDR_CH1_DM1_D	DDR_CH1_DM1_D	DDR_CH1_DM1_D
DDR_CH1_A0_D	DDR_CH1_A0_D	DDR_CH1_A0_D
DDR_CH1_A1_D	DDR_CH1_A1_D	DDR_CH1_A1_D
DDR_CH1_A2_D	DDR_CH1_A2_D	DDR_CH1_A2_D
DDR_CH1_A3_D	DDR_CH1_A3_D	DDR_CH1_A3_D
DDR_CH1_A4_D	DDR_CH1_A4_D	DDR_CH1_A4_D
DDR_CH1_A5_D	DDR_CH1_A5_D	DDR_CH1_A5_D
DDR_CH1_A6_D	DDR_CH1_A6_D	DDR_CH1_A6_D
DDR_CH1_CK_D	DDR_CH1_CK_D	DDR_CH1_CK_D
DDR_CH1_CKB_D	DDR_CH1_CKB_D	DDR_CH1_CKB_D
DDR_CH1_LP4/4X_CS0_D	DDR_CH1_LP4/4X_CS0_D	/
DDR_CH1_LP4/4X_CS1_D	DDR_CH1_LP4/4X_CS1_D	/
DDR_CH1_LP4/4X_CKE0/LP5_CS0_D	DDR_CH1_LP4/4X_CKE0_D	DDR_CH1_LP5_CS0_D
DDR_CH1_LP4/4X_CKE1/LP5_CS1_D	DDR_CH1_LP4/4X_CKE1_D	DDR_CH1_LP5_CS1_D
DDR_CH1_ZQ_D	DDR_CH1_ZQ_D	DDR_CH1_ZQ_D
DDR_CH1_RESET_D	DDR_CH1_RESET_D	DDR_CH1_RESET_D

When LPDDR4/LPDDR4x/LPDDR5:

- All DQ and CA sequences cannot be swapped, must be allocated according to the schematic design.
- A 240ohm 1% resistor must be connected between the DDR PHY ZQ and VDDQ_DDR_S0 power supply.

Built-in Retention function, when DDR enters self-refresh, the power supply pin of DDR controller end DDR_CH_VDDQ_CKE needs to keep supplying power, and other power supplies can be turned off;

LPDDR5 introduces the WCK clock; LPDDR5 has two working clocks, one is CK_t and CK_c, which are used to control the operation of commands and addresses; the other is WCK_t and WCK_c, WCK can be 2 times or 4 times the CK frequency to run; when Write , WCK is the clock and Write data strobe; when Read, WCK is the clock of DQ and RDQS, and RDQS is the Read data strobe signal.

RK3588 supports DVFS Mode (when running LPDDR5), DVFS mode supports switching between two voltages VDD2L (0.9V) and VDD2H (1.05V), that is, VDD2H voltage is used for high-frequency operation, and VDD2L voltage is used for low-frequency operation.

2.1.7.3 DDR Peripheral Circuit Design

- ZQ of LPDDR4x/LPDDR5 must be connected to VDDQ_DDR_S0 power supply through 240ohm 1%;
- ZQ of LPDDR4 must be connected to VDD2_DDR_S3 power supply through 240ohm 1%;
- ODT_CA of LPDDR4/4x must be connected to VDD2_DDR_S3 power supply through 10Kohm 5%;

2.1.7.4 DDR Topology and Matching Design

- For LPDDR4/4x 2 32bit, DQ, CA uses point-to-point connection topology.

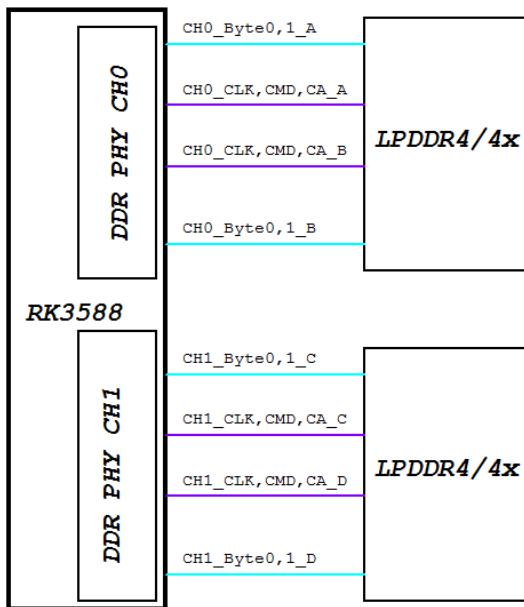


Figure 2-12 LPDDR4 Point-to-Point Topology

Matching method: LPDDR4 particles DQ, CLK, CMD, CA all support ODT, all point-to-point connection is enough.

- For LPDDR5 2 32bit, DQ, CA uses point-to-point connection topology.

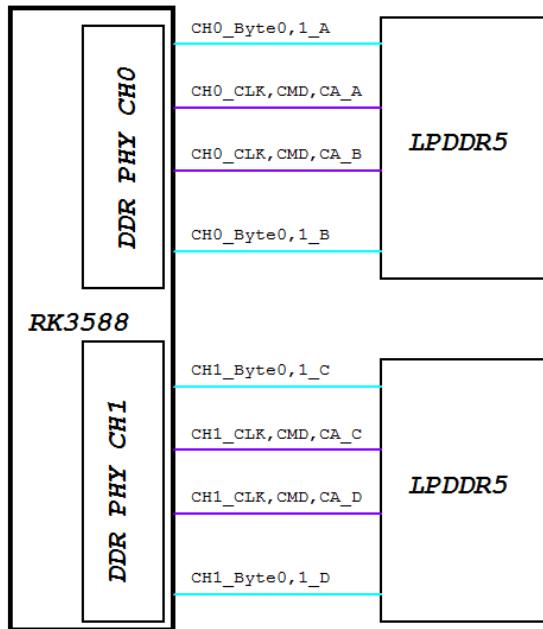


Figure 2-13 LPDDR5 Point-to-Point Topology

Matching method: LPDDR5 particles DQ, CLK, CMD, CA all support ODT, all point-to-point connection is enough.

2.1.7.5 DDR Power Design and Power Up Sequence Requirement

RK3588 DDR PHY power supply is summarized as follows:

DDR PHY Power		LPDDR4/4x	LPDDR5
DDR PLL Power	DDR_CH0/1_PLL_DVDD	0.75v-0.85v	0.75v-0.85v
	DDR_CH0/1_PLL_AVDD1V8	1.8v	1.8v
MEMORY INTERFACE POWER	DDR_CH0/1_VDD_MIF	0.75v-0.85v	0.75v-0.85v
DIGITAL CORE POWER	DDR_CH0/1_VDD	0.75v-0.85v	0.75v-0.85v
DDR IO POWER	DDR_CH0/1_VDDQ	0.6v	0.5v
CK Power	DDR_CH0/1_VDDQ_CK	0.6v	0.5v
LP4/4X_CKE&LP5_CS & Reset Power	DDR_CH0/1_VDDQ_CKE	1.1v	1.05v
Note: The voltage values in the above table are all Typ values			

LPDDR4/4x/LPDDR5 power supply is summarized as follows:

DDR Power		LPDDR4	LPDDR4x	LPDDR5
Core Power1	VDD1	1.8v	1.8v	1.8v
Core Power2&CA Power	VDD2/VDD2H	VDD2=1.1v	VDD2=1.1v	VDD2H=1.05v
	VDD2L	/	/	0.9v
I/O Buffer Power	VDDQ	1.1v	0.6v	0.5v
Note: The voltage values in the above table are all Typ values				

Notes for the power supply circuit when using dual PMIC power supply solutions:

- The PMIC chip type is RK806-2. It is important to note that according to the actual use of DRAM

particles, synchronously modify the PMIC2 RK806-2 FB9 (pin66) voltage divider resistance to make the VDDQ_DDR_S0 output voltage match the particles.

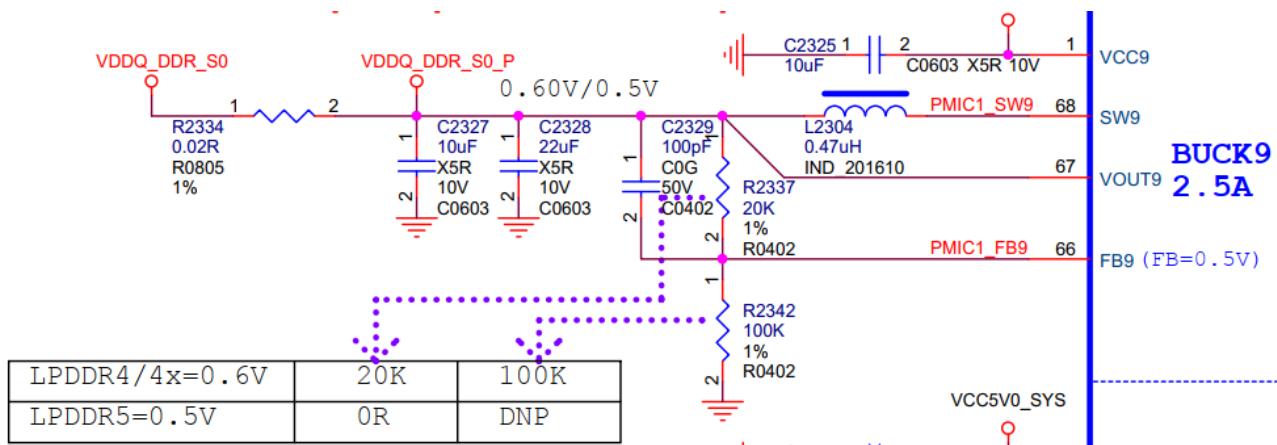


Figure 2-14 RK806-2 BUCK9 FB Parameters Regulation

- The PMIC chip type is RK806-2. It is important to note that according to the actual use of DRAM particles, synchronously modify the PMIC1 RK806-2 FB9 (pin66) voltage divider resistance to make the VDD2_DDR_S3 output voltage match the particles.

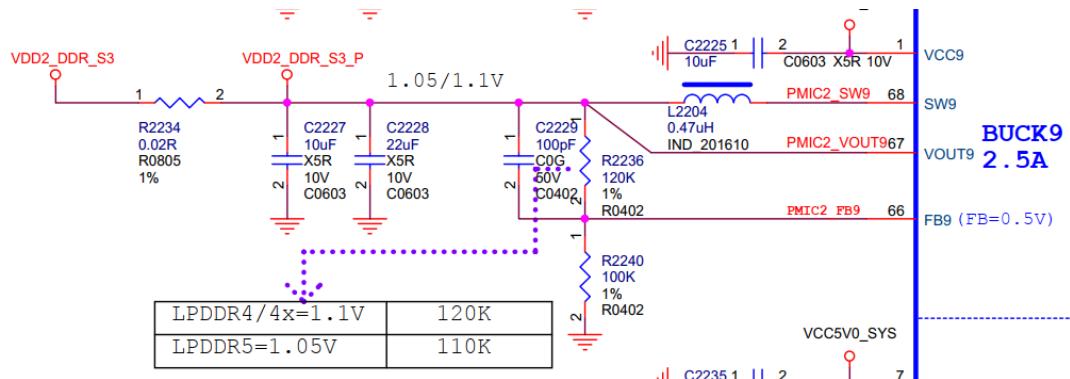


Figure 2-15 RK806-2 BUCK9 FB Parameters Regulation

Notes for the power supply circuit when using single PMIC power supply solutions:

- The PMIC chip type is RK806-1. It is important to note that according to the actual use of DRAM particles, synchronously modify the PMIC RK806-1 FB9 (pin66) voltage divider resistance to make the VDDQ_DDR_S0 output voltage match the particles.

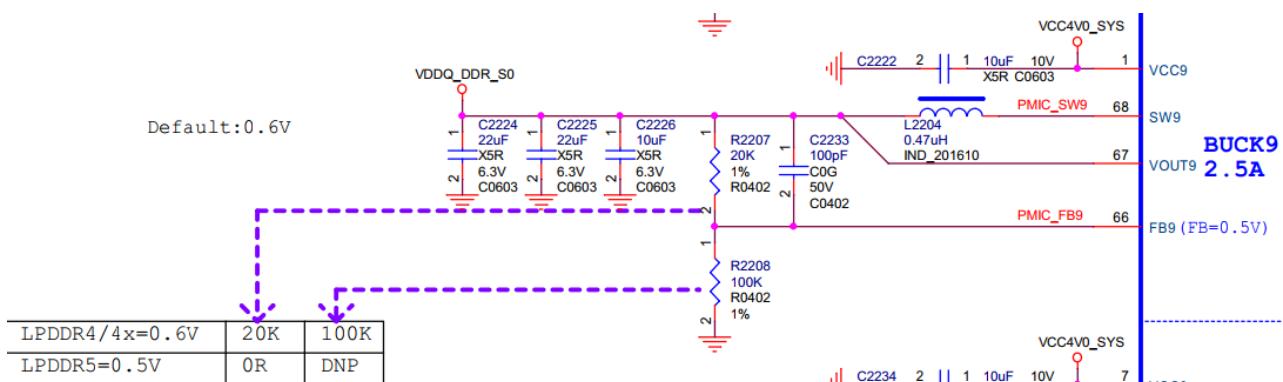


Figure 2-16 RK806-1 BUCK9 FB Parameters Regulation

- The PMIC chip type is RK806-1. It is important to note that according to the actual use of DRAM particles, synchronously modify the PMIC RK806-1 FB6 (pin31) voltage divider resistance to make the VDD2_DDR_S3 output voltage match the particles.

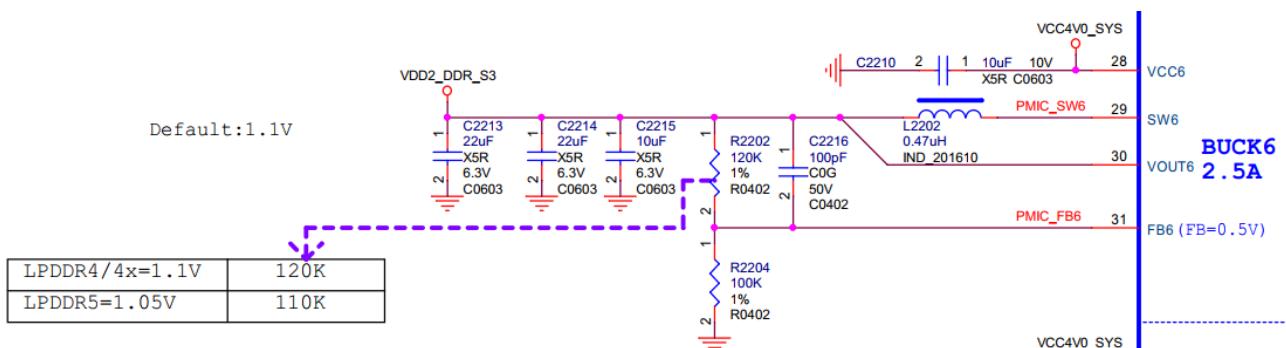


Figure 2-17 RK806-1 BUCK6 FB Parameters Regulation

RK3588 reference template provides LPDDR4 and LPDDR4x compatible design "RK3588_Template_LP4XD200P232SD10H1_4266MHz". It should be noted that the corresponding circuit must be selected according to the actual material.

- When using LPDDR4 particles, you only need to paste the R3811 resistor as shown in the figure below, and R3808 does not paste;
- When using LPDDR4x particles, you only need to paste the R3808 resistor in the figure below, and R3811 does not paste it.

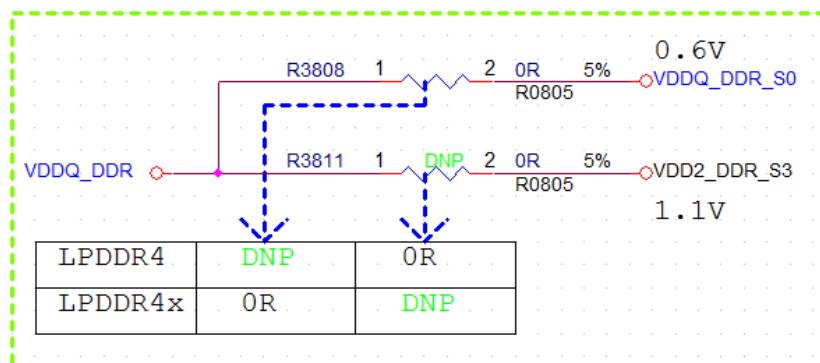


Figure 2-18 LPDDR4/LPDDR4x Compatible Design Power Selection

Please refer to the JEDEC standard for the power-on timing requirements of each type of DRAM.

- The power up sequence of LPDDR4/4x SDRAM is shown in the figure below:

1. While applying power (after T_a), RESET_n is recommended to be LOW ($\leq 0.2 \times V_{DD2}$) and all other inputs must be between $V_{IL\min}$ and $V_{IH\max}$. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 5. V_{DD1} must ramp at the same time or earlier than V_{DD2} . V_{DD2} must ramp at the same time or earlier than V_{DDQ} .

Table 5 — Voltage Ramp Conditions

After	Applicable Conditions
T_a is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than $V_{DDQ} - 200 \text{ mV}$

NOTE 1 T_a is the point when any power supply first reaches 300 mV.

NOTE 2 Voltage ramp conditions in Table 5 apply between T_a and power-off (controlled or uncontrolled).

NOTE 3 T_b is the point at which all supply and reference voltages are within their defined ranges.

NOTE 4 Power ramp duration t_{INIT0} (T_b-T_a) must not exceed 20ms.

NOTE 5 The voltage difference between any of V_{SS} and V_{SSQ} pins must not exceed 100 mV.

Figure 2-19 LPDDR4/4x SDRAM Power Up Sequence

- The power up sequence of LPDDR5 SDRAM is shown in the figure below:
- While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times VDD2H$) and all other inputs shall be between VILmin and VIHmax. The SDRAM outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table 17. VDD1 must ramp at the same time or earlier than VDD2H. VDD2H must ramp at the same time or earlier than VDD2L. VDD2L must ramp at the same time or earlier than VDDQ.

Table 17 — Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	VDD1 must be greater than VDD2H
	VDD2H must be equal to or greater than VDD2L
	VDD2L must be greater than VDDQ-200mV

NOTE 1 Ta is the point when any power supply first reaches 300mV.

NOTE 2 Voltage ramp conditions in Table 17 apply between Ta and power-off (controlled or uncontrolled).

NOTE 3 Tb is the point at which all supply voltages are within their defined ranges.

NOTE 4 Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.

Figure 2-20 LPDDR5 SDRAM Power Up Sequence

2.1.7.6 DDR Support List

For the RK3588 DDR support list, please refer to the document "Rockchip_Support_List_DDR", which can be downloaded from Rockchip redmine platform:

<https://redmine.rock-chips.com/projects/fae/documents>

2.1.8 eMMC Circuit

2.1.8.1 eMMC Controller Introduction

The features of RK3588 eMMC controller are as follows:

- Compatible with 5.1, 5.0, 4.51, 4.41 specifications;
- Support three data bus widths of 1-bit, 4-bit and 8-bit;
- Support HS400 mode, and backward compatible with HS200, DDR50 and other modes;
- Support CMD Queue;

2.1.8.2 eMMC Circuit Design Suggestion

RK3588 eMMC interface is multiplexed with FSPI Flash interface (One multiplex port FSPI_M0), in the design of eMMC interface, please refer to the schematic for the eMMC signal connection method, including the decoupling capacitors of each power supply.

When using eMMC, the boot code is placed in eMMC.

2.1.8.3 eMMC Topology and Matching Method Design

eMMC connection diagram:

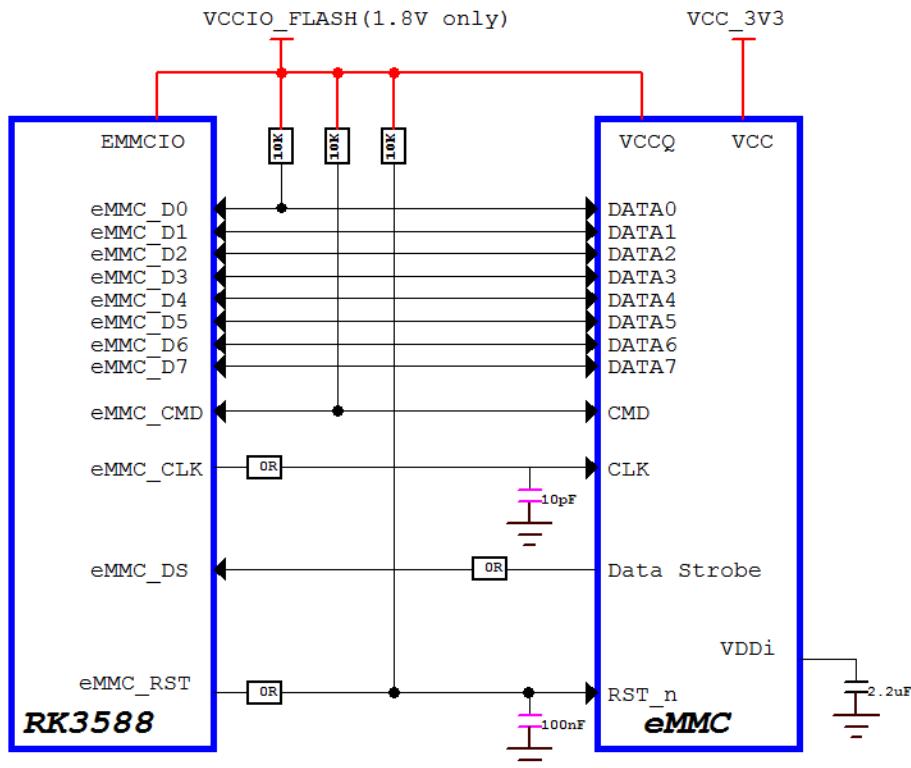


Figure 2-21 eMMC Connection Diagram

The eMMC interface pull-up and pull-down status and matching design recommendations are shown in the following table:

Table 2-5 RK3588 eMMC Interface Design

Signal	Internal pull up/down	Connection mode	Description(chipset))
eMMC_D[7:0]	pull up	Direct connection, D0 external pull-up with a 10K ohm resistor, other data use the pull-up resistor inside the RK3588 chip	eMMC data send/receive
eMMC_CLK	pull down	connect 0ohm resistor in series with RK3588, and pull-down a 10pf capacitor to gnd inside the emmc	eMMC clock send
eMMC_CMD	pull up	Direct connection, external 10K ohm pull-up resistor is required	eMMC command send/receive
eMMC_DATA_Strobe	pull down	connect a 0ohm resistor in series with the eMMC, and reserve a 47K ohm pull-down resistor	eMMC data and command receive refer to Strobe

2.1.8.4 eMMC Power Up Sequence Requirement

The eMMC interface of RK3588 belongs to EMMCIO power domain, only one power supply, so there is no sequence requirements.

The eMMC have two sets of power supplies, refer to JEDEC standard for power-on sequence:

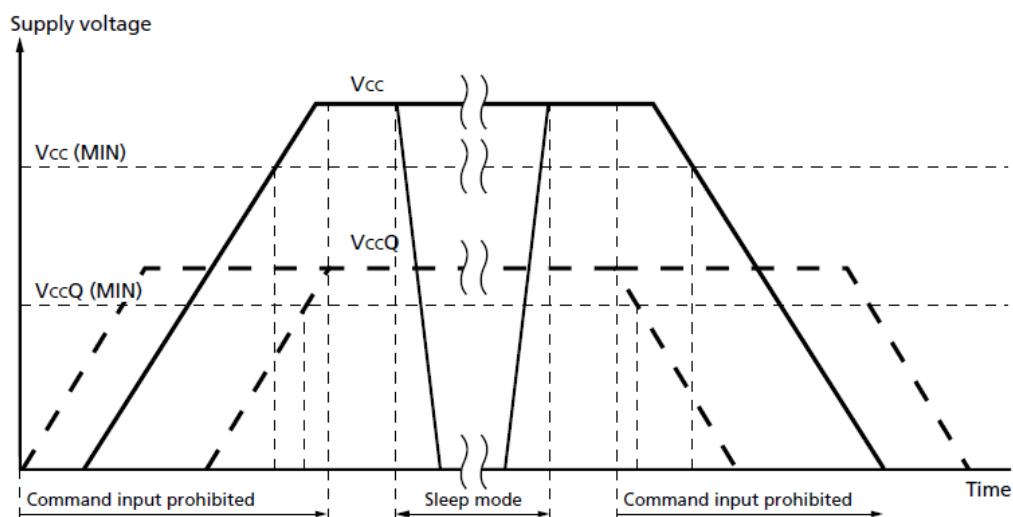


Figure 2-22 eMMC Power Up and Power Down Sequence

2.1.8.5 eMMC Support List

For RK3588 eMMC support list, please refer to the document "RKeMMCSupportList", which can be downloaded from Rockchip redmine platform:

<https://redmine.rock-chips.com/projects/fae/documents>

2.1.9 FSPI Flash Circuit

2.1.9.1 FSPI Flash (Support Boot) Interface Introduction

FSPI is a flexible serial interface controller. There is a FSPI controller in RK3588 chip, which can be used to connect FSPI devices.

The features of RK3588 FSPI controller are as follows:

- Support serial NOR and NAND FLASH;
- Support SDR mode;
- Support single/dual/four-line mode;



NOTE!

RK3588 FSPI interface is used to connect to Boot's SPI Flash. It is not recommended to connect to SPI Flash of other functions!

2.1.9.2 FSPI Flash circuit design suggestions

The RK3588 FSPI Flash interface has three multiplexed interfaces (the suffixs are _M0, _M1, _M2, and only one can be used at the same time). The three multiplexed interfaces are distributed in three power domains: EMMCIO (only supports 1.3V), VCCIO3 (only supports 1.8V) and VCCIO5 (supports 1.8V/3.3V).

When designing the FSPI Flash interface, please refer to the schematic diagram for the FSPI Flash signal connection, including decoupling capacitors for each power supply.

When using FSPI Flash, the boot code is placed in FSPI Flash. Be sure to pay attention to whether the IO drive voltage mode configuration of the corresponding power domain of RK3588 matches the actual power supply voltage.

2.1.9.3 FSPI Flash topology and matching design

FSPI Flash connection diagram:

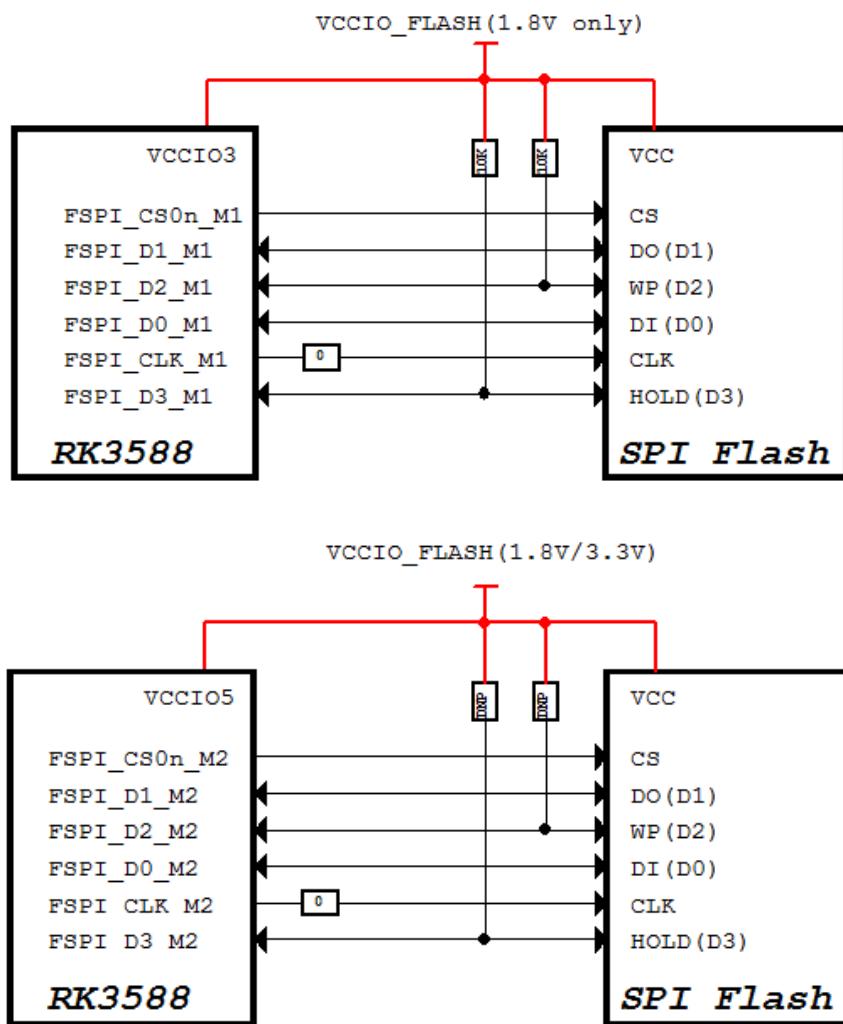


Figure 2-23 FSPI Flash Connection Diagram

The FSPI interface pull-up/down status and matching design recommendations are shown in the table:

Table 2-6 RK3588 FSPI Interface Design

Signal	Internal pull up/down	Connection mode	Description(chipset)
FSPI_D[3:0]	D2 pull up D0/D1/D3 pull up	direct connection. D2, D3 external pull-up with a 10K ohm resistor,	FSPI data send/receive
FSPI_CLK	pull up	connect 0ohm resistor in series with RK3588	FSPI clock send
FSPI_CS0n	pull up	direct connection	FSPI chip select signal

2.1.9.4 FSPI Power Up Sequence Requirment

The FSPI Flash interface of RK3588 chip only has one set of power supply, and there is no timing requirement.

SPI Flash has only one power source, and the power source must be the same as the power domain power source corresponding to the selected FSPI interface.

2.1.9.5 SPI Flash Support List

For RK3588 SPI Flash support list, please refer to the document "RK_SpiNor_and_SLC_Nand_SupportList", which can be downloaded from Rockchip redmine platform:

<https://redmine.rock-chips.com/projects/fae/documents>

2.1.10 GPIO Circuit

2.1.10.1 GPIO Type

The IO of RK3588 has three types, as below:

- 1) 1.8V only type, support max frequency up to 150MHz, It's only need 1.8V (Range:1.65V—1.95V) power rail for work;
- 2) 1.8V\3.3V type, support max frequency up to 150MHz, When configured as 3.3V type io, Need provide two power rails, one is 1.8V (Range:1.65V—1.95V), another is 3.3V (Range:2.7V—3.6V), The power on timing needs to meet the requirements of low voltage first and then high voltage; When configured as 1.8V type io, It's only need 1.8V (Range:1.65V—1.95V) power rail for work.
- 3) eMMC IO type, support max frequency up to 200MHz, It's only need 1.8V (Range:1.65V—1.95V) power rail for work.

The above three types of IO all support Retention IO (Core Power Off and IO Power On), no support fail-Safe(Core Power Off and IO Power off); Please note that Some IO pins need to maintain their pre standby state during standby, The software needs to turn on the retention function, as this time, The LOGIC power of RK3588 can be off, But IO power rail must be powered.

These IO support CMOS input and Schmitt trigger input; The PU(pull-up)\PD(pull-down) and PU/PD Disable can be set through registers, and can be enable or disable according to the application requirements of the product.

These IO support interrupt function.

2.1.10.2 GPIO Pins Description

For example, the GMAC0_RXD2, SDIO_D0_M0, FSPI_D0_M1 and UART6_RX_M0 are multiplexed on GPIO2_A6 as shown in the figure below, and only one of them can be selected for use when assigning.



- Except for boot related GPIO, the rest of IOs are reset to input by defaults;
- GPIOx_xx_u where _u indicates that the default state of this IO reset is internal pull-up;
- GPIOx_xx_d where _d indicates that the default state of this IO reset is internal pull-down;
- GPIOx_xx_z where _z indicates that the default state of this IO reset is high impedance;

- The name suffix of each function with _M0 or M1 or _M2 indicates that the same function is multiplexed on different IO, only one of them can be selected at the same time. For example, when selecting the UART2 function, the UART2_TX_M0 and UART2_RX_M0 combination must be selected. The combination of UART2_TX_M0 and UART2_RX_M1 is not supported. This is the constraint for all functions with different IOMUX.

2.1.10.3 GPIO Drive Capability

In RK3588, GPIO provides multiple levels of adjustable driving strength. Most are Level 0-5 and some GPIO can achieve Level 0-3 adjustment levels. For details, please refer to the "RK3588_PinOut". In addition, depending on the type of GPIO, the initial default driving strength is different. Please refer to the chip TRM for configuration modification, or refer to "SupportDriveStrength" and "DefaultIO DriveStrength" columns in the "RK3588_PinOut".

The driving levels of GPIO are shown in the table below:

Table 2-7 RK3588 GPIO Output Driver Strength

	DS0	DS1	DS2	Output Driver Strength	IOH/IOL
eMMC IO	0	0	0	X0.5(3mA,100ohm)	3mA,4.5mA,6mA,7.2mA,9mA,12mA
	0	0	1	X0.75(4.5mA,66ohm)	
	0	1	0	X1(6mA,50ohm)	
	0	1	1	X1.2(7.2mA,40ohm)	
	1	0	0	X1.5(9mA,30ohm)	
	1	0	1	X2(12mA,25ohm)	
1.8V/3.3V	0	0	0	X1(3mA,100ohm)	3mA,4.5mA,6mA,7.5mA,9mA,12mA
	0	0	1	X2(4.5mA,66ohm)	
	0	1	0	X3(6mA,50ohm)	
	0	1	1	X4(7.5mA,40ohm)	
	1	0	0	X5(9mA,30ohm)	
	1	0	1	X6(12mA,25ohm)	
1.8V only	0	0		X1(2.5mA,100ohm)	2.5mA,5mA,7.5mA,10mA
	0	1		X2(5mA,50ohm)	
	1	0		X3(7.5mA,33ohm)	
	1	1		X4(10mA,25ohm)	

2.1.10.4 GPIO Power

The power pins of the GPIO power domain are described as follows:

Table 2-8 RK3588 GPIO Power Pins Description

Power domain	GPIO Type	Pin name	Description
PMUIO1	1.8V	PMUIO1	1.8V Only IO supply for this GPIO domain (group).
PMUIO2	1.8V/3.3V	PMUIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
EMMCIO	1.8V	EMMCIO	1.8V Only IO supply for this GPIO domain (group).

Power domain	GPIO Type	Pin name	Description
VCCIO1	1.8V	VCCIO1	1.8V Only IO supply for this GPIO domain (group).
VCCIO2	1.8V/3.3V	VCCIO2	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO3	1.8V	VCCIO3	1.8V Only IO supply for this GPIO domain (group).
VCCIO4	1.8V/3.3V	VCCIO4	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO5	1.8V/3.3V	VCCIO5	1.8V or 3.3V IO supply for this GPIO domain (group).
VCCIO6	1.8V/3.3V	VCCIO6	1.8V or 3.3V IO supply for this GPIO domain (group).

PMUIO1, EMMCIO, VCCIO1, VCCIO3 are fixed-level power domains which cannot be configured;

PMUIO2, VCCIO2, VCCIO[4:6] power domains: RK3588 chip can automatically identify the voltage of the hardware configuration, without the need for software to configure according to the hardware supply voltage.

For example: PMUIO2 is configured as 1.8V, PMUIO2_1V8=1.8V, PMUIO2=1.8V; if it is configured as 3.3V, PMUIO2_1V8=1.8V, PMUIO2=3.3V (VCCIO2, VCCIO[4:6] connection is the same as PMUIO2). In addition, it should be noted that these two power pins must be the power supply of S0 or S3 at the same time, and one cannot be S0 and the other is S3 (S0: turn off during standby; S3 needs to be turned on during standby).

Precautions:

- Also, note that the IO level of the power domain should be consistent with the IO level of the peripheral chip/device.
- At least one 100nF decoupling capacitor must be placed nearby the power supply pins of each power domain. See the reference schematic for the detailed design and they cannot be deleted at will.
- If all IOs in a power domain are not used, then the power supply of this power domain does not need to supply power, and the pin leave floating (except TYPEC0).

2.2 Power Supply Design

2.2.1 RK3588 Power Supply Introduction

2.2.1.1 RK3588 Power Supply Requirements

Table 2-9 RK3588 Power Supply Requirements

Module	Power Pin	Description
PLL	PLL_DVDD0V75, PLL_AVDD1V8	System PLL power
DDR PLL	DDR_CH0_PLL_DVDD, DDR_CH0_PLL_AVDD1V8 DDR_CH1_PLL_DVDD, DDR_CH1_PLL_AVDD1V8	DDR PLL power
DDR MIF	DDR_CH0_VDD_MIF, DDR_CH1_VDD_MIF	DDR memory controller power
DDR_VDD	DDR_CH0_VDD, DDR_CH1_VDD	DDR digital CORE power
DDR_VDDQ_CK	DDR_CH0_VDDQ_CK, DDR_CH1_VDDQ_CK	LPDDR4/4X, LPDDR5 CK power
DDR_VDDQ_CKE	DDR_CH0_VDDQ_CKE, DDR_CH1_VDDQ_CKE	LPDDR4/4X_CKE,LPDDR5_CS &RESET power
DDR_VDDQ	DDR_CH0_VDDQ, DDR_CH1_VDDQ	DDR IO power (except ck\cke\reset)
CPU_BIG0	VDD_CPU_BIG0	A76_0,A76_1 power
CPU_BIG0_MEM	VDD_CPU_BIG0_MEM	CPU_BIG0 Memory power
CPU_BIG1	VDD_CPU_BIG1	A76_2,A76_3 power
CPU_BIG1_MEM	VDD_CPU_BIG1_MEM	CPU_BIG1 Memory power
DSU\LIT_CPU	VDD_CPU_LIT	DSU, CPU_LIT(A55), L3 cache power
CPU_LIT_MEM	VDD_CPU_LIT_MEM	DSU, CPU_LIT(A55), L3 cache Memmory power
GPU	VDD_GPU	GPU power
CPU_GPU_MEM	VDD_GPU_MEM	VDD_GPU Memory power
NPU	VDD_NPU	NPU power
CPU_NPU_MEM	VDD_NPU_MEM	VDD_NPU Memory power
LOGIC	VDD_LOG	Logic power
VDENC	VDD_VDENC	DECODE/ENCODE power
VDENC_MEM	VDD_VDENC_MEM	DECODE/ENCODE Memory power
PMU_0V75	PMU_0V75	PMU logic power
OSC	OSC_1V8	Crystal oscillator circuit power
IO	PMUIO1_1V8, PMUIO2_1V8\PMUIO2 , EMMCIO_1V8, VCCIO2_1V8\VCCIO2, VCCIO1_1V8, VCCIO3_1V8, VCCIO4_1V8\VCCIO4, VCCIO5_1V8\VCCIO5,	GPIO power

Module	Power Pin	Description
	VCCIO6_1V8\VCCIO6	
SARADC	SARADC_AVDD_1V8	SAR ADC, TSADC power
OTP	OTP_VDDOTP_0V75	OTP power
USB2.0 PHY	USB20_DVDD_0V75, USB20_AVDD_1V8, USB20_AVDD_3V3	USB2.0 HOST, OTG PHY power
USB3.0 PHY	TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85, TYPEC0_DP0_VDDH_1V8 TYPEC1_DP1_VDD_0V85, TYPEC1_DP1_VDDA_0V85, TYPEC1_DP1_VDDH_1V8	USB3.0 OTG power
PCIe3.0 PHY	PCIE30_PORT0_AVDD0V75, PCIE30_PORT0_AVDD1V8, PCIE30_PORT1_AVDD0V75, PCIE30_PORT1_AVDD1V8	PCIe3.0 PHY power
PCIe2.0 PHY	PCIE20_SATA30_0_AVDD_0V85, PCIE20_SATA30_0_AVDD_1V8, PCIE20_SATA30_1_AVDD_0V85, PCIE20_SATA30_1_AVDD_1V8, PCIE20_SATA30_USB30_2_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_1V8,	PCIE20/SATA30/USB30 COMBO PHY related power
MIPI D/C Combo PHY	MIPI_D/C_PHY0_VDD, MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY0_VDD_1V8, MIPI_D/C_PHY1_VDD, MIPI_D/C_PHY1_VDD_1V2, MIPI_D/C_PHY1_VDD_1V8	MIPI D/C Combo PHY related power
MIPI CSI PHY	MIPI_CSI0_AVDD0V75, MIPI_CSI0_AVCC1V8, MIPI_CSI1_AVDD0V75, MIPI_CSI1_AVCC1V8	MIPI DPHY CSI power
HDMI/eDP TX PHY	HDMI/EDP_TX0_VDD_0V75, HDMI/EDP_TX0_AVDD_0V75, HDMI/EDP_TX0_VDD_IO_1V8, HDMI/EDP_TX0_VDD_CMN_1V8, HDMI/EDP_TX1_VDD_0V75HDMI/EDP_TX1_AVDD_0V75, HDMI/EDP_TX1_VDD_IO_1V8, HDMI/EDP_TX1_VDD_CMN_1V8	HDMI2.1/eDP1.3 Combo phy power
HDMI RX PHY	HDMI_RX_AVDD0V75, HDMI_RX_VPH3V3, HDMI_RX_DVDD3V3	HDMI2.0 RX PHY power

2.2.1.2 RK3588 Power Up Sequence Requirements

Theoretically, it follows the low-voltage first and high-voltage power-on of the same module; the principle of power-on of the same module with the same voltage at the same time, and there is no sequence requirement between different modules. Other peripheral reset, also need to meet the peripheral requirements, the general practice is to release within 5ms-200ms).

The typical power-up sequence recommended with reference to the diagram is as follows:

- Digital power:

PMU_0V75/PLL_DVDD_0V75 → VDD_LOGIC →
VDD_BIG0/1/VDD_GPU/VDD_NPU/VDD_VDENC →
VDD_BIG0/1_MEM/VDD_GPU_MEM/VDD_NPU_MEM/VDD_VDENC_MEM

- SARADC:

VDD_LOGIC → SARADC_AVDD_1V8

- OTP:

VDD_LOGIC → OTP_VDDOTP_0V75

- USB PHY:

USB20_DVDD_0V75 → USB20_AVDD_1V8 → USB20_AVDD_3V3

TYPEC_DP_VDD_0V85 /TYPEC_DP_VDDA_0V85 → TYPEC_DP_VDDH_1V8

- MIPI D/C_PHY:

MIPI_D/C_PHY_VDD → MIPI_D/C_PHY_VDD_1V8 → MIPI_D/C_PHY_VDD_1V2

- MIPI CSI PHY:

MIPI_CSI_AVDD0V75 → MIPI_CSI_AVCC1V8

- HDMI RX PHY:

HDMI_RX_AVDD0V75 → HDMI_RX_VPH3V3 / HDMI_RX_DVDD3V3

- HDMI/eDP TX Combo PHY:

HDMI/EDP_TX_VDD_0V75 / HDMI/EDP_TX_AVDD_0V75 → HDMI/EDP_TX_VDD_IO_1V8 /

HDMI/EDP_TX_VDD_CMN_1V8

- PCIE20/SATA30 Combo PHY:

PCIE20_SATA30_AVDD_0V85 → PCIE20_SATA30_AVDD_1V8

PCIE20/SATA30/USB30 Combo PHY

PCIE20_SATA30_USB30_AVDD_0V85 → PCIE20_SATA30_USB30_AVDD_1V8

- DDR PHY:

● DDR_CH_VDD/DDR_VDD_MIF → DDR_CH_VDDQ_CKE → DDR_VDDQ

According to the power network name assigned by the reference schematic, the overall recommended power-on sequence is as follows:

VDD_0V75_S3, AVDD_0V75_S0, VDD_0V75_PLL_S0, VDD_0V75_HDMI_EDP_S0, VDD_0V85_S0,
AVDD_V085_S0, VDD_DDR_S0, VDD_DDR_PLL_S0, VDD_LOGIC → VCC_1V8_S0, AVDD_1V8_S0,
VCC_1V8_S3, VDD1_1V8_DDR_S3, VDD_1V8_PLL_S0, AVDD1V8_DDR_PLL_S0 → VDD2_DDR_S3,
AVDD_1V2_S0 → VDD2L_0V9_DDR_S3 → VCC_3V3_S0, VCC_3V3_S3, VDDQ_DDR_S0 → VCCIO_SD_S0,
VCC_3V3_SD_S0 → VDD_CPU_LIT_S0, VDD_CPU_LITMEM, VDD_CPU_BIG0_S0,
VDD_CPU_BIG0_MEM_S0, VDD_CPU_BIG1_S0, VDD_CPU_BIG1_MEM_S0 → RESETn

2.2.1.3 RK3588 Power Down Sequence Requirements

During the power-off, RESETn must be pulled down first, and then each power supply will be powered off.

2.2.2 Power Supply Design Suggestion

2.2.2.1 Power Up and Standby Circuit Scheme

The power supply status of each module of RK3588 at the first power-on is as follows:

Table 2-10 RK3588 Power Supply Requirement Table for Each Module at the First Power-On

Module	Power Pin	Power requirements
DDR PLL	DDR_CH0/1_PLL_DVDD, DDR_CH0/1_PLL_AVDD1V8	must be powered
SYSPLL	PLL_DVDD0V75, PLL_AVDD1V8	must be powered
CPU	VDD_CPU_BIG0, VDD_CPU_BIG1, VDD_CPU_BIG0_MEM, VDD_CPU_BIG1_MEM	must be powered
GPU	VDD_GPU, VDD_GPU_MEM	must be powered
NPU	VDD_NPU, VDD_NPU_MEM	must be powered
VDENC	VDD_VDENC, VDD_VDENC_MEM	must be powered
LIT	VDD_CPU_LIT, VDD_CPU_LIT_MEM	must be powered
Logic	VDD_LOGIC	must be powered
PMU Logic	PMU_0V75	must be powered
DDR	DDR_CH0/1_VDD, DDR_CH0/1_VDD_MIF, DDR_CH0/1_VDDQ, DDR_CH0/1_VDDQ_CK, DDR_CH0/1_VDDQ_CKE	must be powered
GPIO	PMUIO1, PMUIO2	must be powered
GPIO	EMMCIO_1V8	must be powered
GPIO	VCCIO2	must be powered
GPIO	VCCIO1, VCCIO3, VCCIO4, VCCIO5, VCCIO6	can be unpowered
SARADC	SARADC_AVDD_1V8	must be powered
OTP	OTP_VDDOTP_0V75	must be powered
USB3.0 PHY	TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85, TYPEC0_DP0_VDDH_1V8	must be powered
	TYPEC1_DP1_VDD_0V85, TYPEC1_DP1_VDDA_0V85, TYPEC1_DP1_VDDH_1V8	can be unpowered
USB2.0 PHY	USB20_DVDD_0V75, USB20_AVDD_1V8, USB20_AVDD_3V3	must be powered
PCIe2.0/SATA3.0 Combo PHY	PCIE20_SATA30_0/1_AVDD_0V85, PCIE20_SATA30_0/1_AVDD_1V8	can be unpowered
PCIe2.0/SATA3.0/USB3.0 Combo PHY	PCIE20_SATA30_USB30_2_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_1V8	can be unpowered

Module	Power Pin	Power requirements
PCIe3.0 PHY	PCIE30_PORT0_AVDD0V75, PCIE30_PORT0_AVDD1V8	can be unpowered
MIPI CSI RX PHY	MIPI_CSI0_AVDD0V75, MIPI_CSI0_AVCC1V8	can be unpowered
MIPI D/C Combo PHY	MIPI_D/C_PHY0/1_VDD, MIPI_D/C_PHY0/1_VDD_1V2, MIPI_D/C_PHY0/1_VDD_1V8	can be unpowered
HDMI/EDP Combo PHY	HDMI/EDP_TX0/1_VDD_0V75, HDMI/EDP_TX0/1_AVDD_0V75, HDMI/EDP_TX0/1_VDD_IO_1V8, HDMI/EDP_TX0/1_VDD_CMN_1V8	can be unpowered
HDMI2.0 RX PHY	HDMI_RX_AVDD_0V75, HDMI_RX_VPH3V3 HDMI_RX_DVDD_3V3	can be unpowered

RK3588 can support a low-power standby solution. When entering the standby mode, the power supply and power-off conditions are as follows:

Table 2-11 RK3588 Standby Power Supply Requirements

Module	Power Pin	Standby power requirements
DDR PLL	DDR_CH0/1_PLL_DVDD,DDR_CH0/1_PLL_AVDD1V8	can be unpowered
SYSPLL	PLL_DVDD0V75,PLL_AVDD1V8	can be unpowered
CPU	VDD_CPU_BIG0,VDD_CPU_BIG1	can be unpowered
GPU	VDD_GPU	can be unpowered
NPU	VDD_NPU	can be unpowered
VDENC	VDD_VDENC	can be unpowered
Logic	VDD_LOGIC	can be unpowered
PMU Logic	PMU_0V75	Must be powered
DDR	DDR_CH0/1_VDDQ_CKE	Must be powered
GPIO	PMUIO1, PMUIO2	Must be powered
GPIO	EMMCIO_1V8	can be unpowered
GPIO	VCCIO2	can be unpowered
GPIO	VCCIO1, VCCIO3, VCCIO4, VCCIO5, VCCIO6	can be unpowered
SARADC	SARADC_AVDD_1V8	can be unpowered
OTP	OTP_VDDOTP_0V75	can be unpowered
USB3.0 PHY	TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85, TYPEC0_DP0_VDDH_1V8	can be unpowered
	TYPEC1_DP1_VDD_0V85, TYPEC1_DP1_VDDA_0V85, TYPEC1_DP1_VDDH_1V8	can be unpowered
USB2.0 PHY	USB20_DVDD_0V75, USB20_AVDD_1V8, USB20_AVDD_3V3	can be unpowered

Module	Power Pin	Standby power requirements
PCIe2.0/SATA3.0 Combo PHY	PCIE20_SATA30_0/1_AVDD_0V85, PCIE20_SATA30_0/1_AVDD_1V8	can be unpowered
PCIe2.0/SATA3.0/USB3.0 Combo PHY	PCIE20_SATA30_USB30_2_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_1V8	can be unpowered
PCIe3.0 PHY	PCIE30_PORT0_AVDD0V75, PCIE30_PORT0_AVDD1V8,	can be unpowered
MIPI CSI RX PHY	MIPI_CSI0_AVDD0V75, MIPI_CSI0_AVCC1V8	can be unpowered
MIPI D/C Combo PHY	MIPI_D/C_PHY0/1_VDD, MIPI_D/C_PHY0/1_VDD_1V2, MIPI_D/C_PHY0/1_VDD_1V8	can be unpowered
HDMI/EDP Combo PHY	HDMI/EDP_TX0/1_VDD_0V75 HDMI/EDP_TX0/1_AVDD_0V75, HDMI/EDP_TX0/1_VDD_IO_1V8, HDMI/EDP_TX0/1_VDD_CMN_1V8	can be unpowered
HDMI2.0 RX PHY	HDMI_RX_AVDD_0V75, HDMI_RX_VPH3V3 HDMI_RX_DVDD_3V3	can be unpowered

In this standby state, it can only support IO interrupt wake-up of PMUIO1 and PMUIO2.

In the standby state, at least the following groups of power supplies should be kept (the following are the power supply pin names):

- DDR_CH0/1_VDDQ_CKE: Provide power for DDR self-refresh;
- PMU_0V75: Provide power for the logic of PMUIO1 & PMUIO2 power domain;
- PMUIO1_1V8: Provide power for PMU1 work; provide IO power for PMUIO1 power domain to maintain output status and interrupt response;
- PMUIO2_1V8: Provide IO power for PMUIO2 power domain to maintain output status and interrupt response.

In standby mode, to support USB HID device wake-up, the USB PHY and VDD_LOG power supply must be reserved; to support VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, EMMCIO_1V8, IO interrupt wake-up, then VCCIO1, VCCIO2, VCCIO3, VCCIO4, VCCIO5, VCCIO6, EMMCIO_1V8 power supply must be reserved.

2.2.2.2 PLL Circuit

The PLL of RK3588 is distributed in two parts as follows:

Table 2-12 RK3588 Internal PLL Introduction

	Power	Standby mode
Inside the PMU unit	PLL_DVDD0V75, PLL_AVDD1V8	Allow turn off the power
DDR PLL	DDR_CH0_PLL_DVDD, DDR_CH0_PLL_AVDD1V8	Allow turn off the power

- PLL_DVDD0V75: Peak current 20mA
- PLL_AVDD1V8: Peak current 40mA

- DDR_CH0_PLL_DVDD: Peak current 20mA
- DDR_CH0_PLL_AVDD1V8: Peak current 30mA

It is recommended to use LDO power supply, and the PSRR@1KHz should be greater than 65dB:

- 0.75V AC requirement: < 20mV;
- 1.8V AC requirement: < 50mV

A stable PLL power supply will improve the stability of the chip. The decoupling capacitors should be placed close to the pins. Refer to the schematic for the detailed number and capacity of the capacitors. Please do not change them at will.

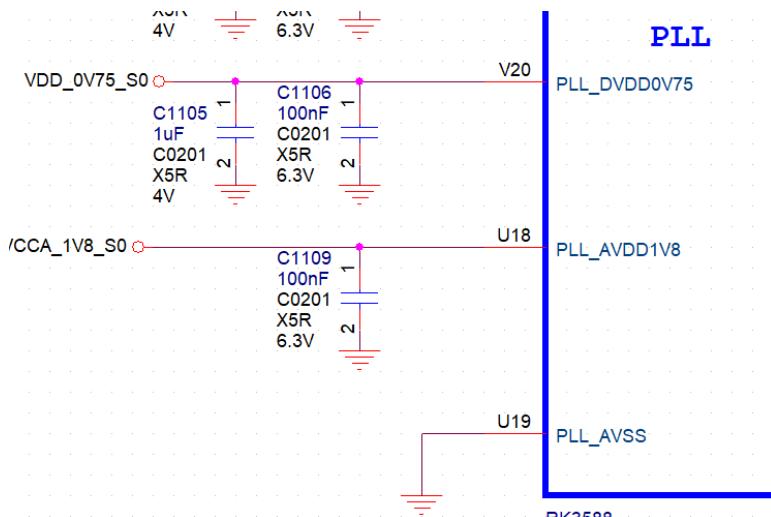


Figure 2-24 RK3588 SYS PLL Power Pin

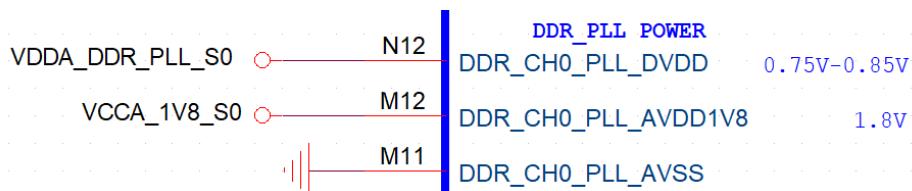


Figure 2-25 RK3588 DDR PLL Power Pin

2.2.2.3 OSC Circuit

The power supply OSC_1V8 of the RK3588 provides power for the crystal oscillator circuit.

- OSC_1V8: peak current<10mA

It is recommended to use LDO power supply:

- 1.8V AC requirement: < 20mV

A stable OSC power supply helps to improve the stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of capacitors. Do not adjust them arbitrarily. Consider using a separate LDO power supply, which can be shared with the PLL power supply considering the cost.

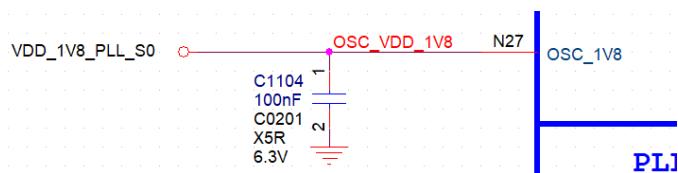


Figure 2-26 Power Pin of RK3588 Crystal Oscillator Circuit

2.2.2.4 PMU LOGIC Power Supply

The PMU_0V75 power supply of RK3588 supplies power to the LOGIC of the internal PMU unit, and the peak current is 30mA. Please do not delete the decoupling capacitor in the RK3588 chip reference design schematic diagram.

Can use DC/DC or LDO power supply.

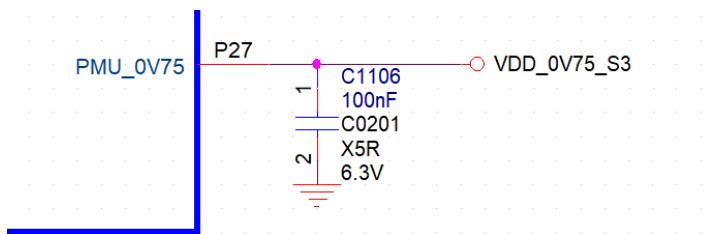


Figure 2-27 PMU_0V75 Power Pin of RK3588

2.2.2.5 VDD_CPU_BIG0 Power Supply

The VDD_CPU_BIG0 power supply of RK3588 is used to supply power to the CORE1 and CORE2 units of A76. It is powered by the BUCK2 or DC/DC power supply of RK806, which can support the function of dynamic frequency regulation and voltage regulation. The default power supply voltage is 0.75V. The peak current can reach more than 3.5A, please do not delete the decoupling capacitor in the RK3588 chip reference design schematic diagram.

The main requirements for DC/DC BUCK are as follows:

- The output current is greater than 3.5A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1A/\mu s$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During Layout, place these capacitors between the green line and the chip on the back of the RK3588 chip. The total capacitance of the VDD_CPU_BIG0 power supply must be greater than 150uF to ensure that the power supply ripple is within $\pm 5\%$ and avoid excessive power supply ripple caused by heavy load.

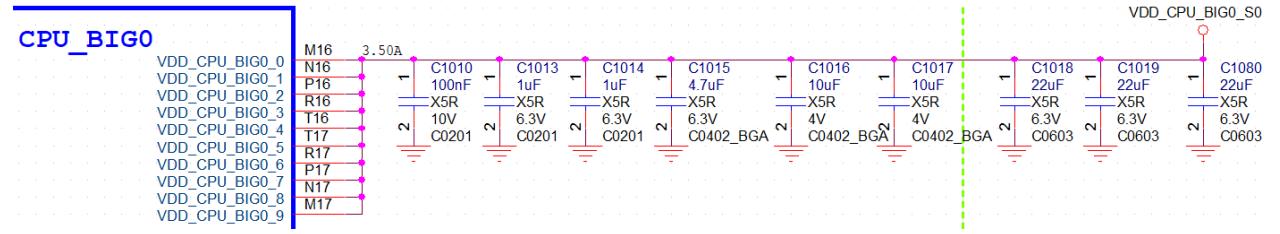


Figure 2-28 VDD_CPU_BIG0 Power Pin of RK3588

The VDD_CPU_BIG0_MEM power supply is the MEMORY power supply of A76 CORE1 and CORE2. The peak current is 100mA. It needs to be regulated and can be powered by BUCK. The following two filter capacitors must be placed under the RK3588 pin.

Note: VDD_CPU_BIG0_MEM can be combined with VDD_CPU_BIG0 to supply power in scenarios with low power consumption requirements.

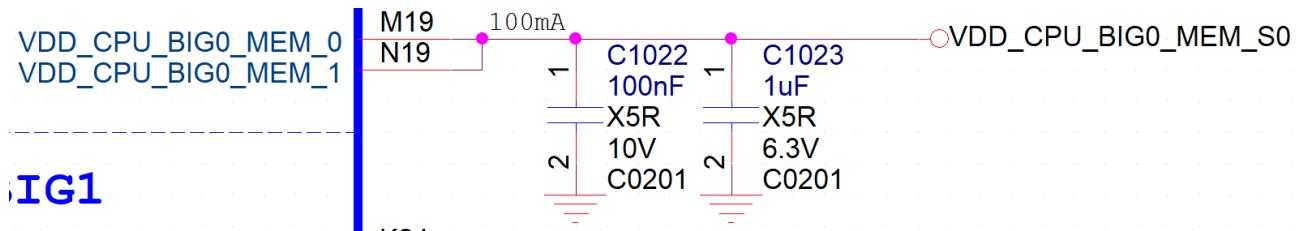


Figure 2-29 RK3588 VDD_CPU_BIG0_MEM Power

2.2.2.6 VDD_CPU_BIG1 Power Supply

The VDD_CPU_BIG1 power supply of RK3588 is to supply power to the CORE3 and CORE4 units of A76. It is powered by the BUCK or DC/DC power supply of RK806, which can support the function of dynamic frequency regulation and voltage regulation. The default power supply voltage is 0.75V. The peak current can reach more than 3.5A, please do not delete the decoupling capacitor in the schematic diagram of the RK3588 chip reference design.

The main requirements for DC/DC BUCK are as follows:

- The output current is greater than 3.5A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1A/\mu s$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During Layout, place these capacitors between the green line and the chip on the back of the RK3588 chip. The total capacitance of the VDD_CPU_BIG1 power supply must be greater than 150uF to ensure that the power supply ripple is within $\pm 5\%$ and avoid excessive power supply ripple caused by heavy load.

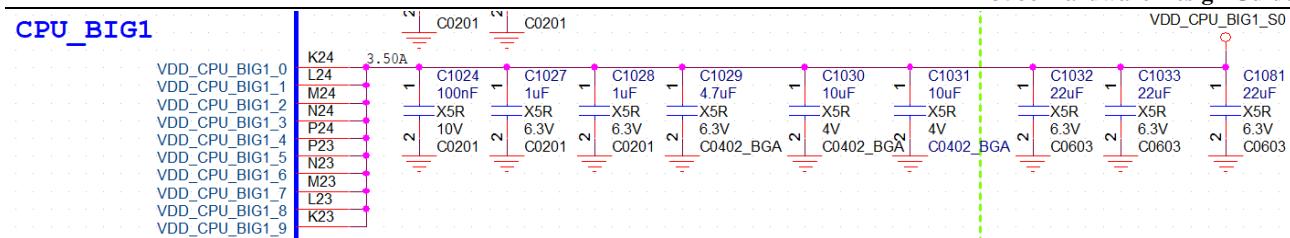


Figure 2-30 RK3588 VDD_CPU_BIG1 Power Pin

The VDD_CPU_BIG1_MEM power supply is the MEMORY power supply of A76 CORE1 and CORE2. The current can reach 100mA, and the voltage needs to be adjusted. BUCK can be used for power supply. The two filter capacitor must be placed under the RK3588 pin as shown in the figure below.

Note: VDD_CPU_BIG1_MEM can be combined with VDD_CPU_BIG1 to supply power in scenarios with low power consumption requirements.

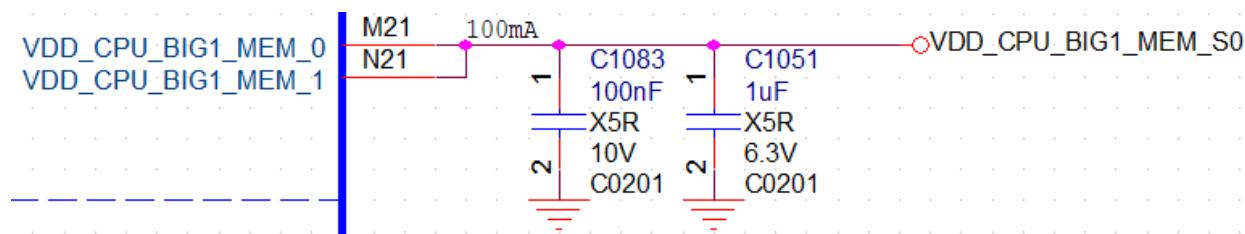


Figure 2-31 RK3588 VDD_CPU_BIG1_MEM Power

2.2.2.7 VDD_CPU_LIT Power Supply

RK3588's VDD_CPU_LIT power supply supplies power to the internal ARM Cortex-A55 core, DSU logic, control, and L3 cache. It uses RK806's BUCK power supply to support dynamic frequency and voltage regulation. The peak current can reach more than 3.0A, please do not delete the decoupling capacitor in the RK3588 chip reference design schematic diagram.

The main requirements for DC/DC BUCK are as follows:

- The output current is greater than or equal to 3.0A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1A/\mu s$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During Layout, place these capacitors from the green line to the chip position below the RK3588 chip. The total capacitance of the VDD_CPU_LIT power supply must be greater than 150uF to ensure power supply traces. The wave is within $\pm 5\%$ to avoid the large power supply ripple caused by the large load.

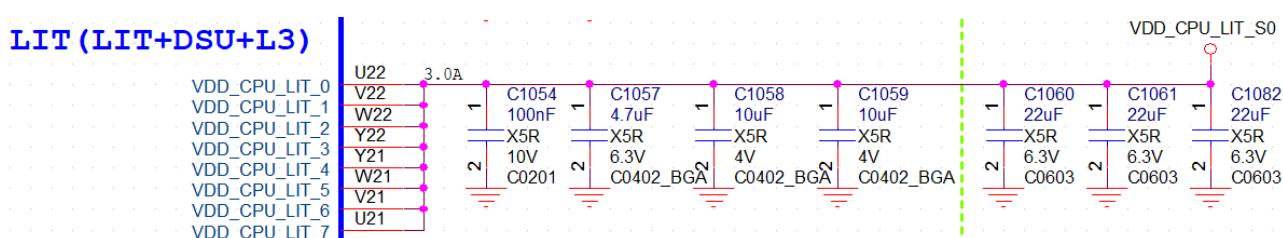


Figure 2-32 VDD_CPU_LIT Power Capacitor

The VDD_CPU_LIT_MEM power supply is the Memory power supply of A55 and DSU. The current can reach 100mA. It needs voltage regulation and can be powered by BUCK. The following two filter capacitors must be placed under the RK3588 pin.

Note: VDD_CPU_LIT_MEM and VDD_CPU_LIT can be combined for power supply in scenarios with low power consumption requirements.

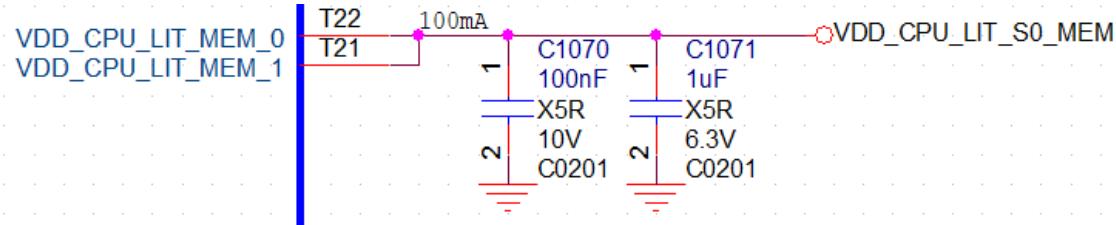


Figure 2-33 RK3588 VDD_CPU_LIT_MEM Power

2.2.2.8 GPU Power Supply

The VDD_GPU power supply of RK3588 supplies power to the internal GPU unit. It uses RK806-2 BUCK1 or DC/DC power supply. It supports dynamic frequency regulation and voltage regulation. The peak current can reach 6.2A. Please do not delete the reference design of the RK3588 chip. Decoupling capacitors.

The main requirements for DC/DC BUCK are as follows:

- The output current is greater than or equal to 6.5A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1A/\mu s$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During layout, place the capacitors from the green line to the chip position on the back of the RK3588 chip. The total capacitance of the VDD_GPU power supply must be greater than 200uF to ensure that the power supply ripple is within $\pm 5\%$ and avoid excessive power supply ripple caused by heavy load.

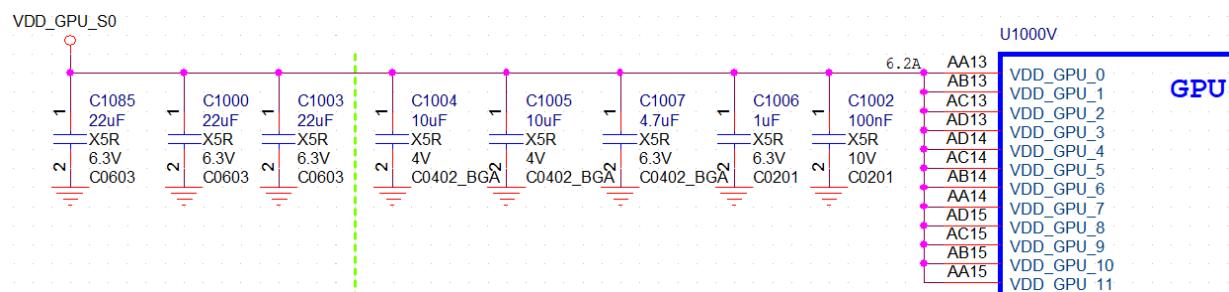


Figure 2-34 RK3588 VDD_GPU Power Poin

The VDD_GPU_MEM power supply is the memory power supply of VDD_GPU_MEM, the current can reach 405mA, and the voltage needs to be adjusted, and it can be powered by BUCK. The following two filter capacitors must be placed under the RK3588 pin.

Note: VDD_GPU_MEM can be combined with VDD_GPU for scenarios with low power consumption requirements.

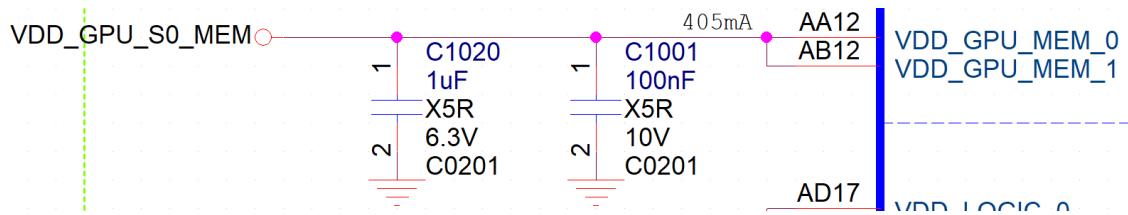


Figure 2-35 RK3588 VDD_GPU_MEM Power Pin

2.2.2.9 NPU Power Supply

The VDD_NPU power supply of RK3588 supplies power to the internal NPU unit. It uses DC/DC power supply. It supports dynamic frequency regulation and voltage regulation. The peak current can reach 4A. Please do not delete the reference design of the RK3588 chip. Decoupling capacitors.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 4.0A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1\text{A}/\mu\text{s}$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During Layout, place these capacitors between the green line and the chip on the back of the RK3588 chip. The total capacitance of the VDD_NPU power supply must be greater than 200uF to ensure that the power supply ripple is within $\pm 5\%$ and avoid excessive power supply ripple caused by heavy load.

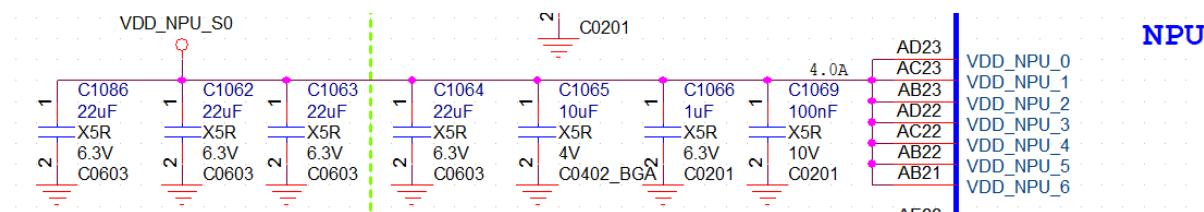


Figure 2-36 RK3588 VDD_NPU Power Pin

The VDD_NPU_MEM power supply is the Memory power supply of VDD_NPU, and the current can reach 405mA. It needs to be adjusted and can be powered by BUCK. The following two filter capacitors should be placed under the RK3588 pin.

Note: VDD_NPU_MEM can be combined with VDD_NPU to supply power in scenarios with low power consumption requirements.

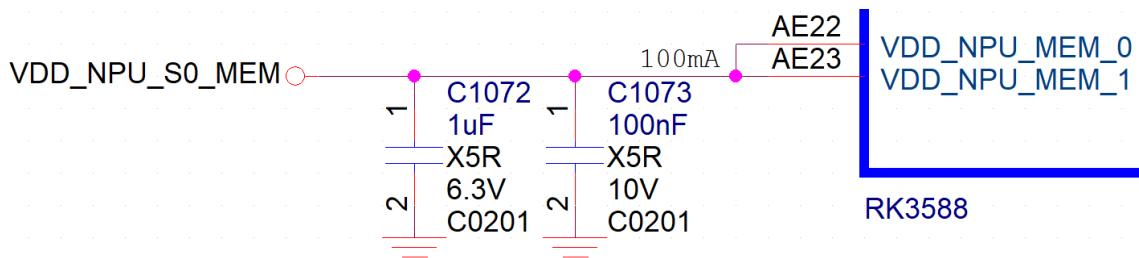


Figure 2-37 RK3588 VDD_NPU_MEM Power Pin

2.2.2.10 Logic Power Supply

The VDD_LOGIC power supply of RK3588 supplies power to the internal logic unit. It adopts DC/DC power supply for independent power supply, and can support dynamic frequency and voltage regulation functions. The default fixed voltage power supply. The peak current can reach more than 2.0A, please do not delete the decoupling capacitor in the schematic diagram of the RK3588 chip reference design.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2.0A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1A/\mu s$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During Layout, place these capacitors between the green line and the chip on the back of the RK3588 chip. The total capacitance of the VDD_LOGIC power supply must be greater than 100uF to ensure that the power supply ripple is within 75mV and avoid large power supply ripple caused by heavy load.

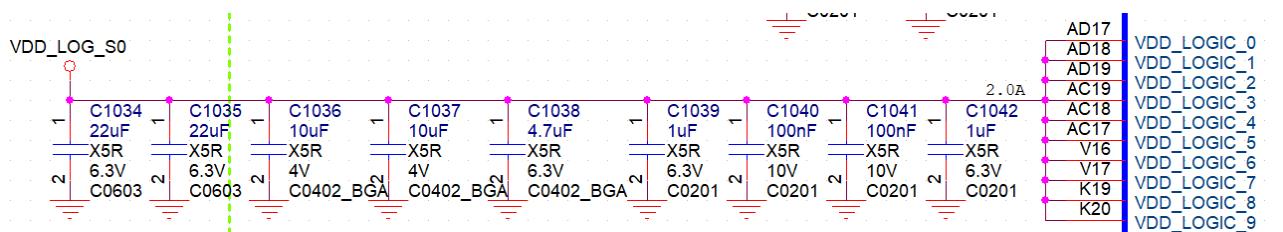


Figure 2-38 RK3588 VDD_LOGIC Power Pin

2.2.2.11 VIDEO Power Supply

The VDD_VDENC power supply of RK3588 supplies power to the internal video codec logic unit. It adopts DC/DC power supply for independent power supply, and can support dynamic frequency modulation and voltage regulation. The default fixed voltage power supply. The peak current can reach more than 2.0A, please do not delete the decoupling capacitor in the schematic diagram of the RK3588 chip reference design.

The main requirements for DC/DC BUCK are as follows:

- Output current is greater than or equal to 2.0A;
- The output voltage accuracy is required at $\pm 1.5\%$;
- BUCK transient response requirements: $I_{load} = \text{BUCK Max current} * 10\% \sim \text{BUCK Max current} * 80\%$ jump, slope $1A/\mu s$, ripple requirement within $\pm 5\%$;
- If it is sensitive to the power consumption of the whole machine, efficiency also needs to be considered.

During layout. Place the capacitors in the figure below on the back of the RK3588 chip. The total capacitance of the VDD_VDENC power supply must be greater than 100uF to ensure that the power supply ripple is within 75mV and avoid excessive power supply ripple caused by heavy load.

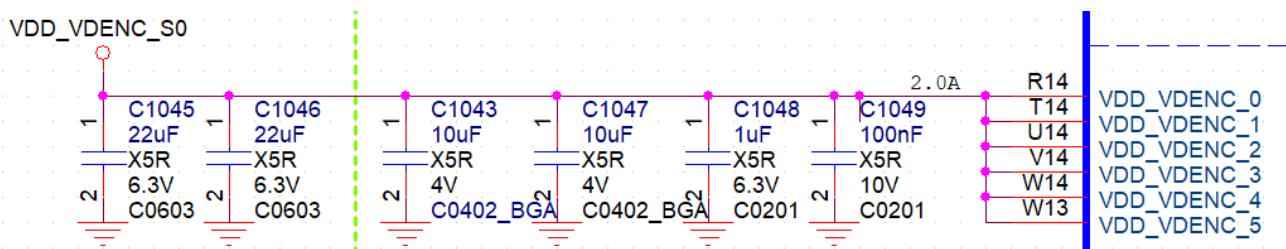


Figure 2-39 RK3588 VDD_VDENC Power Pin

The VDD_VDENC_MEM power supply is the Memory power supply of VDD_VDENC. The current can reach 100mA. It needs to be regulated and can be powered by BUCK. The following two filter capacitors should be placed under the RK3588 pin.

Note: VDD_VDENC_MEM and VDD_VDENC can be combined for power supply in scenarios with low power consumption requirements.

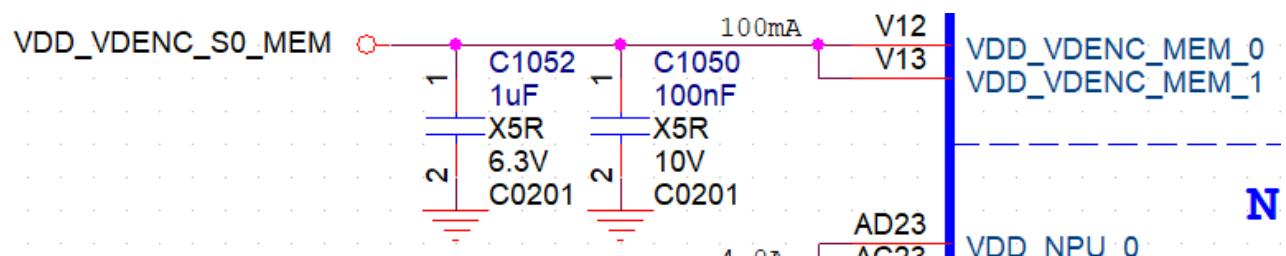


Figure 2-40 RK3588 VDD_VDENC Power Pin

2.2.2.12 DDR Power Supply

The DDR PHY interface of RK3588 supports LPDDR4/LPDDR4x/LPDDR5 standards, a total of two channels, each with 6 power supplies, DDR_CH0/1_PLL_DVDD, DDR_CH0/1_PLL_AVDD1V8, DDR_CH0/1_VDD_MIF, DDR_CH0/1_VDDQ_CKE, DDR_CH0/1_VDDQ_CK, DDR_CH0/1_VDDQ_CK, /1_VDDQ, please refer to **2.1.7.5 DDR power design and power up sequence requirements** for power supply introduction. When designing the product, please confirm that it meets the design requirements according to the usage of the particles.

Similarly, some voltages corresponding to LPDDR4/4X and LP5 particles are different, as shown in the drawing.

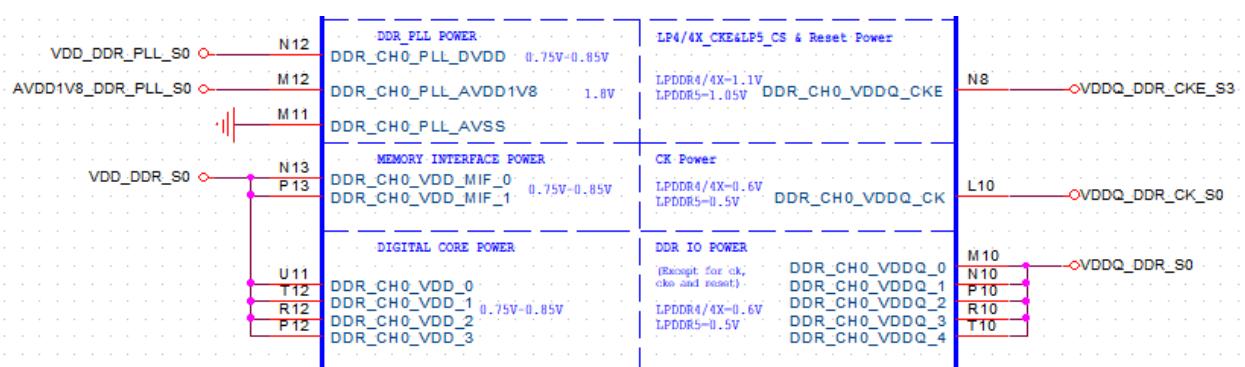


Figure 2-41 RK3588 DDR Power Pin in LPDDR4/4X Mode

During Layout, place the capacitor in the figure below on the back of the RK3588 chip. Ensure that the power

supply ripple is within 80mV and avoid large power supply ripples under heavy load conditions.

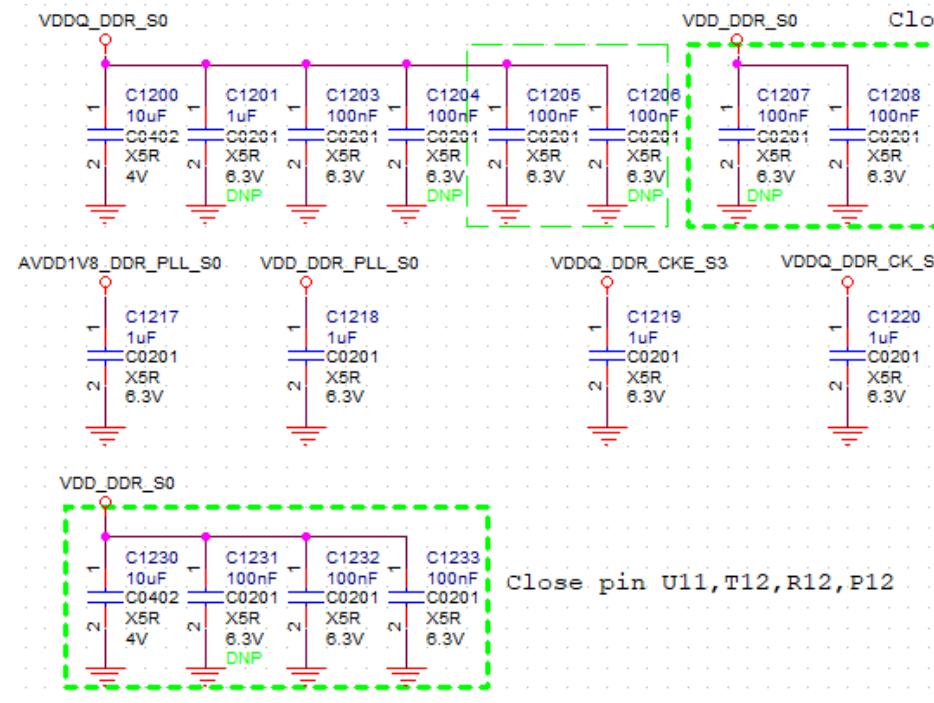


Figure 2-42 RK3588 Power Filter Capacitor in LPDDR4/4x Mode

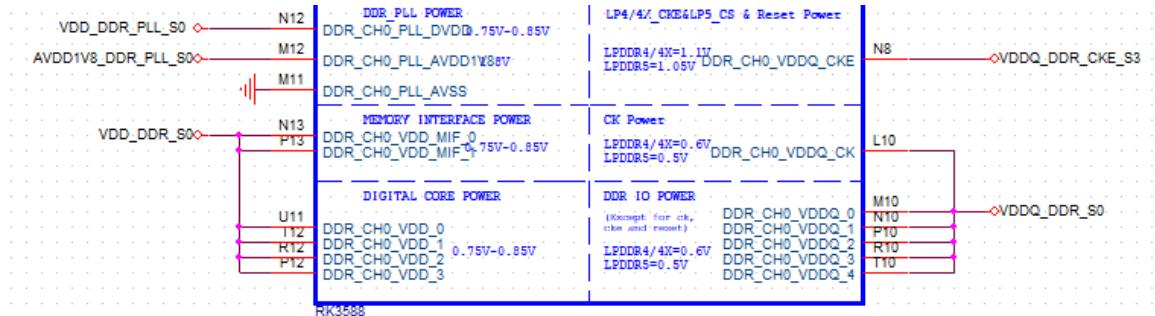


Figure 2-43 RK3588 Power Pin in LPDDR5 Mode

During Layout, place the capacitor in the figure below on the back of the RK3588 chip. Ensure that the power supply ripple is within 80mV and avoid large power supply ripples under heavy load conditions.

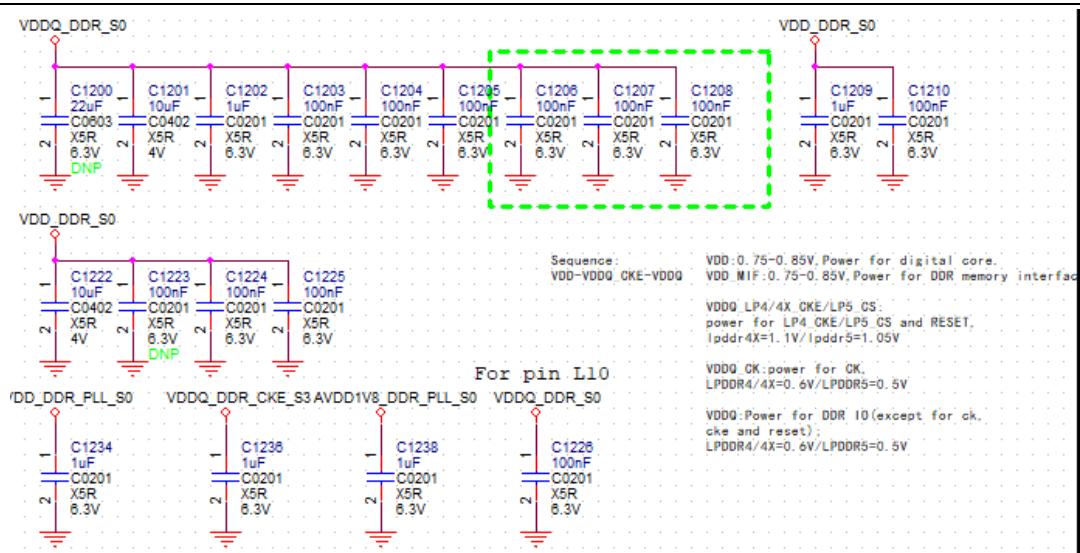


Figure 2-44 RK3588 Power Filter Capacitor in LPDDR5 Mode

2.2.2.13 USB2.0 PHY Power Supply

RK3588 has four USB2.0 interfaces. For details, please refer to **Section 2.3.4 USB2.0/USB3.0 Circuit**.

The `USB20_DVDD_0V75`, `USB20_AVDD_1V8`, and `USB20_AVDD_3V3` power supplies are for `USB2_HOST0/1_DP/M` and `TYPEC0/1_USB20_OTG_DP/M` PHY. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

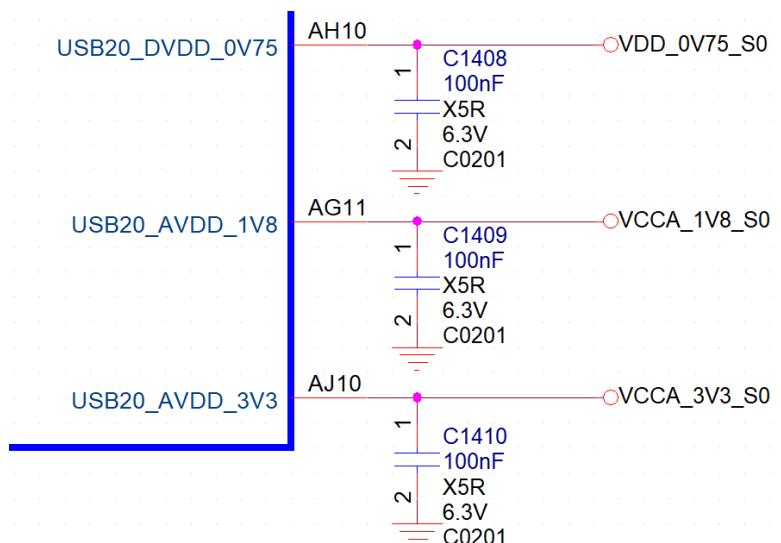


Figure 2-45 RK3588 USB2.0 PHY Power Pin

- `USB20_DVDD_0V75`: peak current 30mA
- `USB20_AVDD_1V8`: peak current 65mA
- `USB20_AVDD_3V3`: peak current 45mA

It is recommended to use LDO for power supply:

- 0.75V AC requirement: < 25mV;
- 1.8V AC requirement: < 50mV;
- 3.3V AC requirement: < 200mV

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

Since the firmware of the RK3588 chip must be downloaded from the TYPEC0_USB20_OTG_DP/M interface, USB20_DVDD_0V75, USB20_AVDD_1V8, USB20_AVDD_3V3 must be powered in the first time power-on.

2.2.2.14 USB3.0/DP1.4 Combo Power Supply

RK3588 has two USB30\DP1.4 Combo PHY interfaces.

The TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85 power supplies are for USB30/DP1.4 Combo0. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

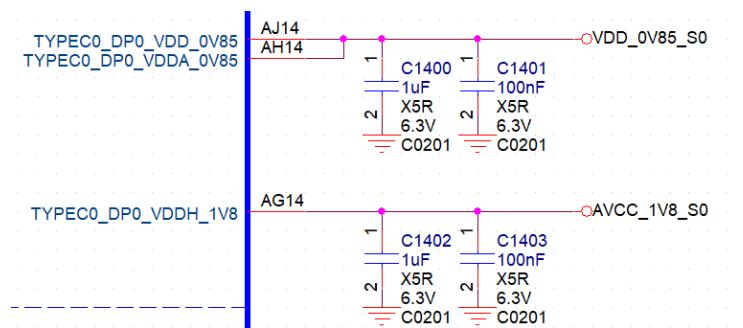


Figure 2-46 RK3588 USB30/DP1.4 Combo0 Power Pin

The TYPEC1_DP1_VDD_0V85, TYPEC1_DP1_VDDH_1V8 power supplies are for USB30/DP1.4 Combo1. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

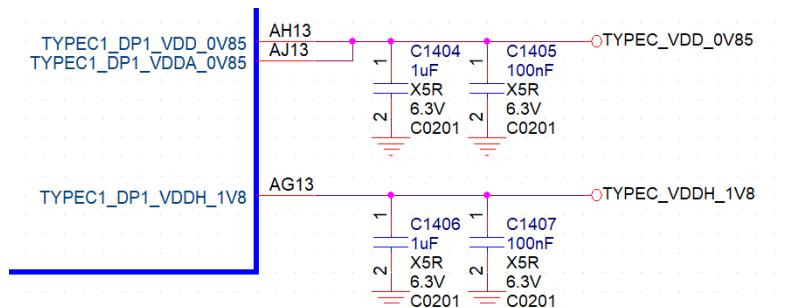


Figure 2-47 RK3588 USB30/DP1.4 Combo1 Power Pin

- TYPEC_VDD_0V85: peak current 40 mA;
- TYPEC_VDDA_0V85: peak current 300 mA;
- TYPEC_VDDH_1V8: peak current 60 mA;

(Note: The above peak current is the combined total current value of the two circuits, the same below.)

It is recommended to use LDO for power supply:

- PSRR@1KHz > 65dB;
- 0.85V AC requirement: <20mV;
- 1.8V AC requirement: <50mV;

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the

capacitors. Please do not adjust it at will.

Because the RK3588 chip firmware must be downloaded from the TYPEC0_USB20_OTG_DP/M interface, and this interface is the same Controller as the PHY0 port of USB30, and there is a logical relationship inside. Therefore, when this function is not in use, the PHY0 port of USB30 must also be powered; if the PHY1 port of USB30 is not used, it is not necessary to supply power.

2.2.2.15 PCIe2.0 PHY Power Supply

RK3588 has two PCIe2.0/SATA30 Combo PHY interfaces, one PCIe2.0/SATA30/USB30 Combo PHY.

There are 6 power supplies for PCIe2.0 Combo PHY: PCIE20_SATA30_0_AVDD_0V85, PCIE20_SATA30_1_AVDD_0V85, PCIE20_SATA30_0_AVDD_1V8, PCIE20_SATA30_1_AVDD_1V8, PCIE20_SATA30_USB30_2_AVDD_0V85, PCIE20_SATA30_USB30_2_AVDD_1V8. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic. As shown in the figure below, the capacitor layout on the left side of the green dotted line needs to be close to the chip pins.

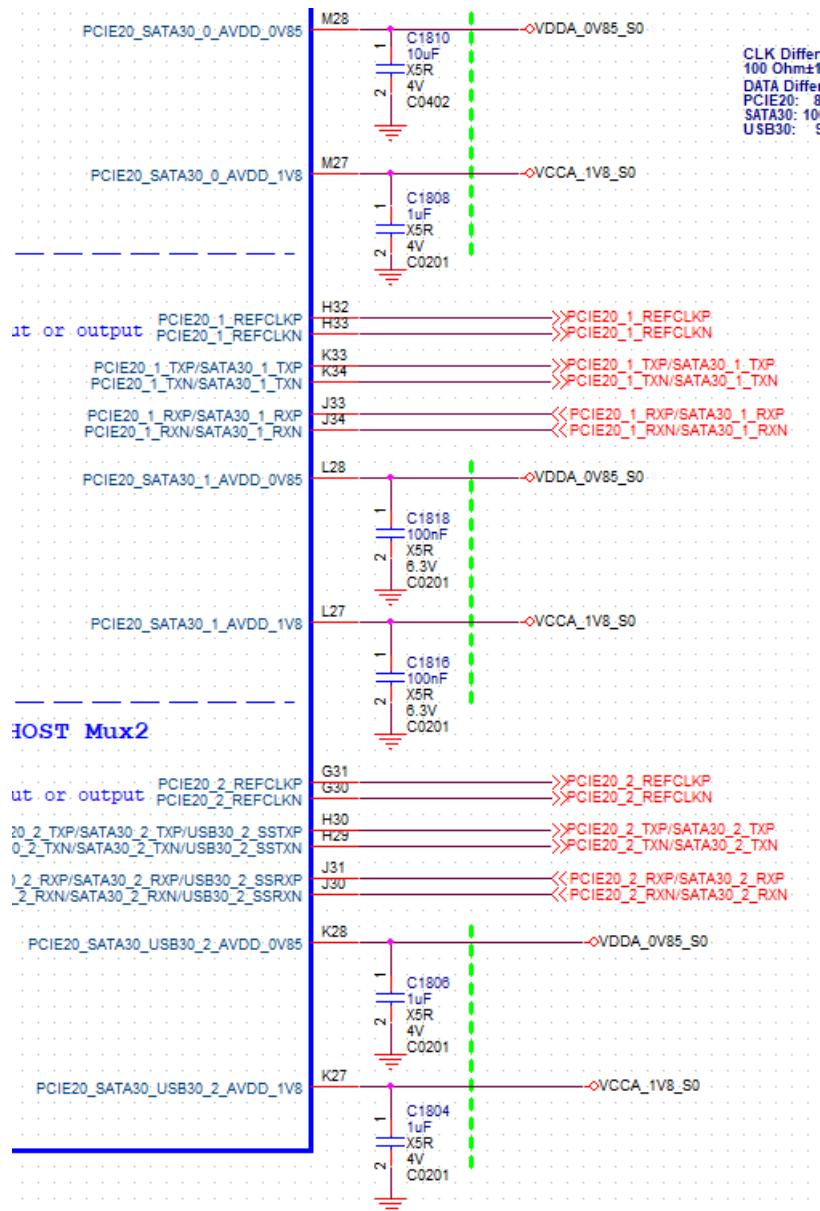


Figure 2-48 RK3588 PCIe2.0 Combo PHY Power Pin

- PCIE20_SATA30_0/1_AVDD_0V85/PCIE20_SATA30_USB30_2_AVDD_0V85: peak current 140mA
- PCIE20_SATA30_0/1_AVDD_1V8/PCIE20_SATA30_USB30_2_AVDD_1V8: peak current 270mA

It is recommended to use LDO for power supply:

- 0.85V AC requirement: <20mV
- 1.8V AC requirement: <50mV

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

The 6-way power supply is independent, and the 2-way power supply (0V85 and 1V8) corresponding to the PHY without the PCIE function and need connected to gnd.

2.2.2.16 PCIe3.0 PHY Power Supply

RK3588 has two PCIe3.0 PHY interfaces. PCIE30_PORT0/ PORT1_AVDD0V75 and PCIE30_PORT0/ PORT1_AVDD1V8 power supplies for PCIe3.0 PHY. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic. As shown in the figure below, the capacitor layout on the left side of the green dotted line needs to be close to the chip pins. (The power of phy1 port is handled the same as phy0 port)

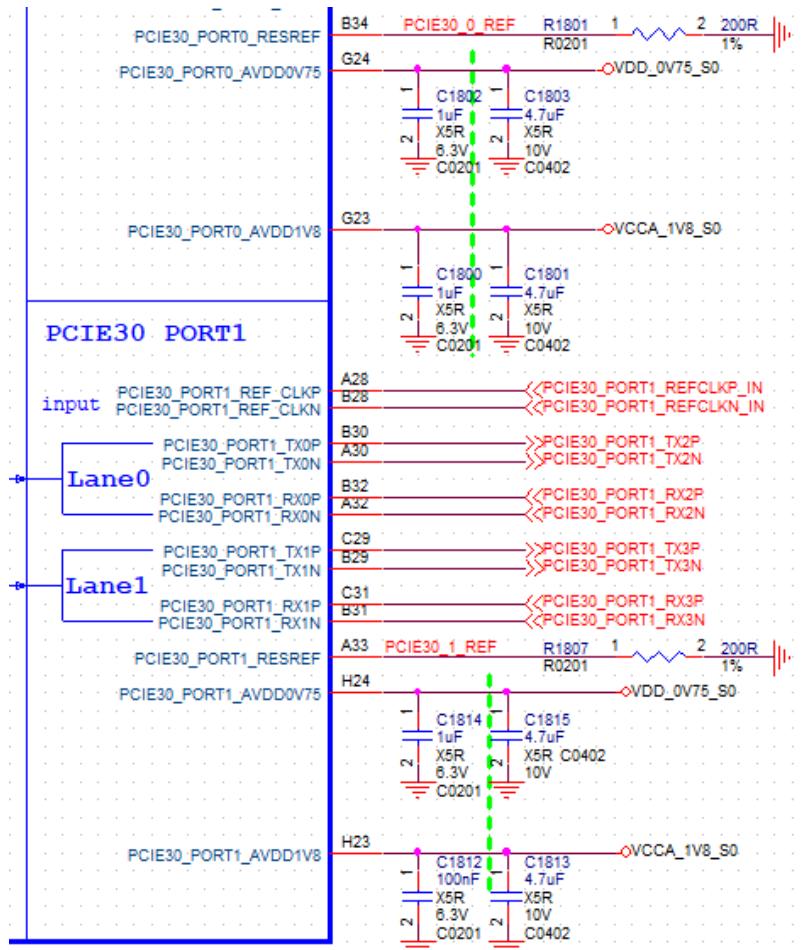


Figure 2-49 RK3588 PCIe3.0 PHY Power Pin

- PCIE30_PORT0/ PORT1_AVDD0V75: peak current 230mA
- PCIE30_PORT0/ PORT1_AVDD1V8: peak current 210mA

It is recommended to use LDO for power supply:

- 0.75V AC requirement: <20mV
- 1.8V AC requirement: <50mV

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

If none of the PCIe3.0 functions are used, then PCIE30_PORT0/1_AVDD0V75 and PCIE30_PORT0/1_AVDD1V8 can be left unpowered, left floating or grounded.

If PORT0 is used and PORT1 is not used, the 2-way power supply (0V75 and 1V8) of PORT1 must also be powered.

If PORT1 is used and PORT0 is not used, the 2-way power supply (0V75 and 1V8) of PORT0 must also be powered.

RK3588 PCIE Power		Port0, Not used Port1, Not used	Port0, used Port1, Not used	Port0, Not used Port1, used
Port0	PCIE30_PORT0_AVDD0V75	[X]	[]	[]
	PCIE30_PORT0_AVDD1V8	[X]	[]	[]
Port1	PCIE30_PORT1_AVDD0V75	[X]	[]	[]
	PCIE30_PORT1_AVDD1V8	[X]	[]	[]

2.2.2.17 MIPI CSI RX PHY Power Supply

RK3588 has two MIPI CSI RX interfaces. MIPI_CSI0_AVDD0V75, MIPI_CSI0_AVCC1V8 power supplies for MIPI CSI RX PHY. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic. As shown in the figure below, the capacitor layout on the left side of the green dotted line needs to be close to the chip pins. (The power of MIPI_CSI1 port is handled the same as MIPI_CSI0 port)

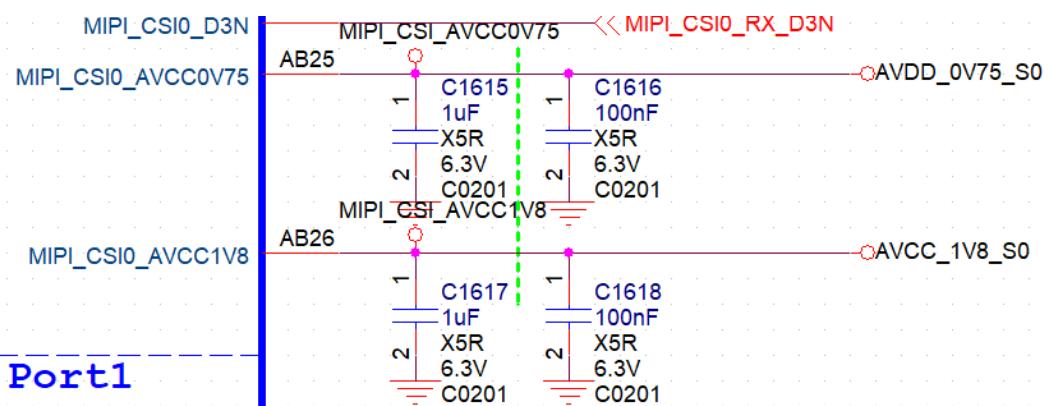


Figure 2-50 RK3588 MIPI CSI RX PHY0 Power Pin

- MIPI_CSI_RX_AVDD_0V9: peak current 10mA
- MIPI_CSI_RX_AVDD_1V8: peak current 3.3mA

It is recommended to use LDO for power supply:

- 0.75V AC requirement: <20mV
- 1.8V AC requirement: <50mV

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

If the MIPI CSI RX functions are not used, MIPI_CSI0/1_AVDD_0V75 and MIPI_CSI0/1_ACC1V8 can be power off. Grounding or Floating is ok.

2.2.2.18 MIPI D/C Combo PHY Power

RK3588 has two MIPI D/C PHY COMBO interfaces.

MIPI_D/C_PHY0_VDD, MIPI_D/C_PHY0_VDD_1V2, MIPI_D/C_PHY0_VDD_1V8 power supplies for MIPI D/C PHY. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic. The capacitor on the left of the green line in the figure below needs to be placed under the RK3588 chip, and the capacitor on the right should be placed as close to the chip as possible. (The power of phy1 port is handled the same as phy0 port)

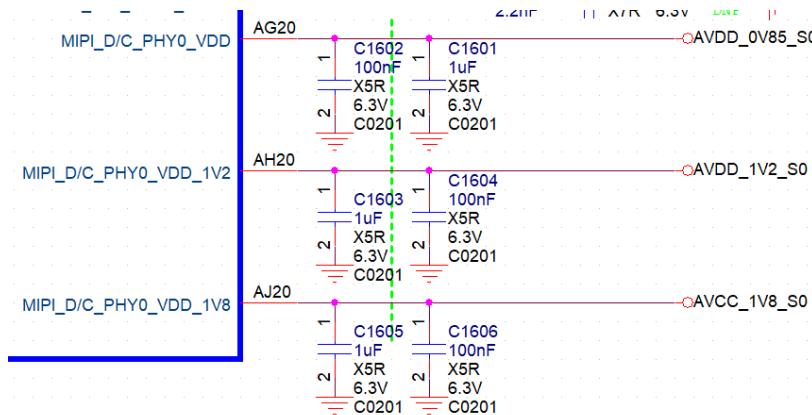


Figure 2-51 RK3588 MIPI D/C Combo PHY0 Power Pin

- MIPI_D/C_PHY_VDD: peak current 130mA
- MIPI_D/C_PHY_VDD_1V2: peak current 4mA
- MIPI_D/C_PHY_VDD_1V8: peak current 35mA

It is recommended to use LDO for power supply:

- 0.9V AC requirement: < 20mV
- 1.8V AC requirement: < 50mV

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

If the MIPI D/C PHY functions are not used, MIPI_D/C_PHY0/1_VDD, MIPI_D/C_PHY0/1_VDD_1V2, MIPI_D/C_PHY0/1_VDD_1V8 can be power off. Floating is ok.

2.2.2.19 HDMI2.1/eDP1.3 Combo Power Supply

RK3588 has two HDMI2.1/eDP Combo PHY interface.

HDMI/EDP_TX0_VDD_0V75, HDMI/EDP_TX0_AVDD_0V75, HDMI/EDP_TX0_VDD_IO_1V8, HDMI/EDP_TX0_VDD_CMN_1V8 power supply is for HDMI2.1/eDP Combo PHY, please do not delete the

decoupling capacitor in the RK3588 chip reference design schematic (the power supply of phy1 port is the same as that of phy0 treated like the mouth).

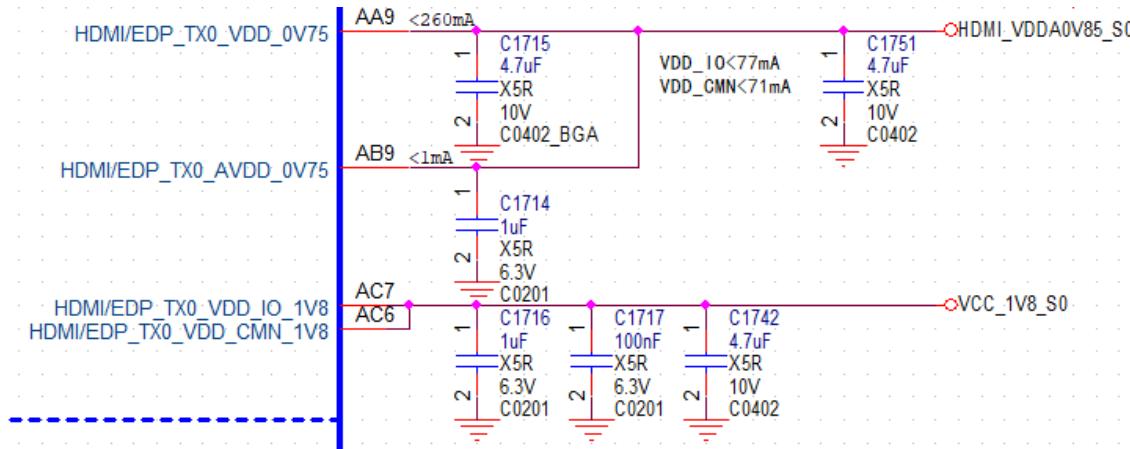


Figure 2-52 RK3588 HDMI2.1/EDP Combo PHY power pin

- HDMI/EDP_TX_VDD_0V75: peak current 440mA
- HDMI/EDP_TX_AVDD_0V75: peak current 1mA
- HDMI/EDP_TX_VDD_IO_1V8: peak current 100mA
- HDMI/EDP_TX_VDD_CMN_1V8: peak current 100mA

It is recommended to use LDO for power supply:

- 0.9V AC requirement: <20mV
- 1.8V AC requirement: <50mV

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

If the HDMI2.1/EDP1.3 TX functions are not used, HDMI/EDP_TX0_VDD_0V75, HDMI/EDP_TX0_AVDD_0V75, HDMI/EDP_TX0_VDD_IO_1V8/HDMI/EDP_TX0_VDD_CMN_1V8 can be power off. Grounding or Floating is ok.

2.2.2.20 SARADC/OTP Power Supply

RK3588 has 1 SARADC with 8 inputs. SARADC_AVDD_1V8 power supplies for SARADC and TSADC. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

- SARADC_AVDD_1V8: peak current 5mA

It is recommended to use LDO for power supply:

- 1.8V AC requirement: <50mV

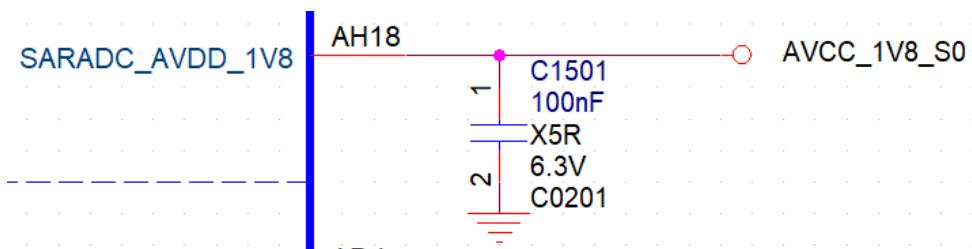


Figure 2-53 RK3588 SARADC Power Pin

RK3588 has 1 OTP. OTP_VCC18 power supplies for OTP. Do not delete the decoupling capacitor in the RK3588 chip reference design schematic.

- OTP_VDDOTP_0V75: peak current 1mA

The power supply can use LDO or DC/DC to supply power to OTP.

A stable power supply helps to improve the working stability of the chip, and the decoupling capacitors should be placed close to the pins. Please refer to the schematic diagram for the specific number and capacity of the capacitors. Please do not adjust it at will.

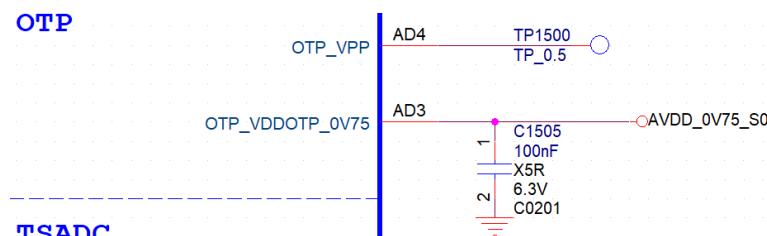


Figure 2-54 RK3588 SARADC Power Pin

2.2.3 RK806 Solution Introduction

2.2.3.1 RK806 Typical Application Diagram

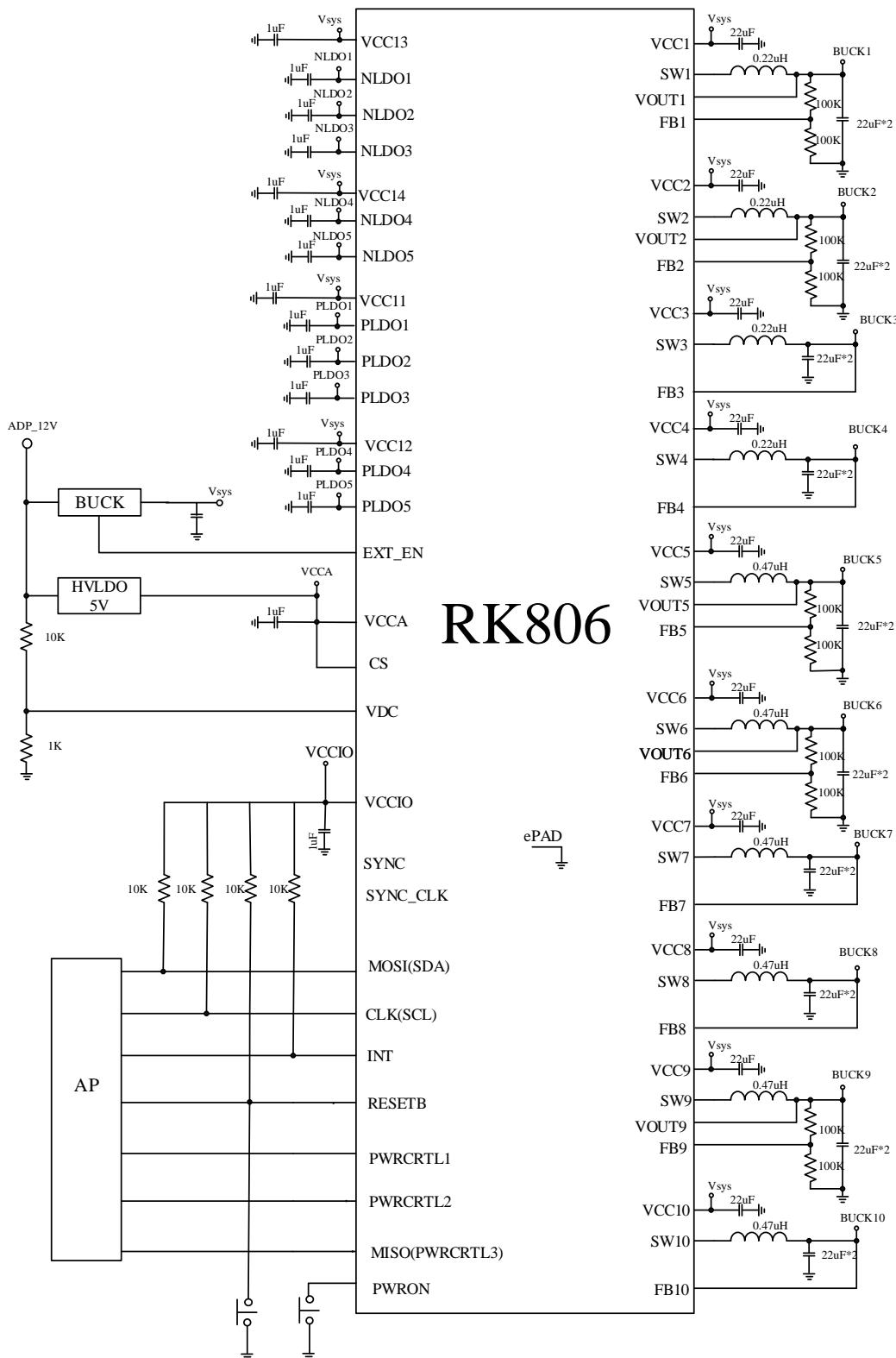


Figure 2-55 RK806 Typical Application Diagram of Single Chip

2.2.3.2 RK806 Features

- Input range: 2.7V-5.5V;
- Very low standby current: 10uA;
- Support I2C or SPI two communication protocol;
- Support dual-chip collaborative work;
- Ripple control architecture provides excellent transient response;
- Output level can be programmed via I2C or SPI;
- Optional power start sequence control;
- Power channels:
 - Buck1: 0.5V-3.4V output, 6.5A max;
 - Buck2/3/4: 0.5V-3.4V output, 5A max;
 - Buck5/6/7/8/9/10: 0.5V-3.4V output, 3.0A max;
 - NLDO1/2/5: 0.5V-3.4V output, 300mA max;
 - NLDO3/4: 0.5V-3.4V output, 500mA max;
 - PLDO1/4: 0.5V-3.4V output, 500mA max;
 - PLDO2/3/5/6: 0.5V-3.4V output, 300mA max.
- External Buck enable control;
- Package: 7mm x 7mm QFN68.

2.2.3.3 RK806 Notes

- RK806-2 can work with dual PMICs. When using it, one needs to be set as the master (EXT_EN is floating or only connected to the EN pin of the external BUCK), and the other is set as the slave (EXT_EN to VCCA), the power-on and power-off timings of the two chips are synchronized by SYNC and SYNC_CLK. When working, short-circuit the VDC, PWRON, and RESET of the two PMICs together.
Note: In single PMIC application, set PMIC to master mode through EXT_EN, and SYNC and SYNC_CLK can be left floating.

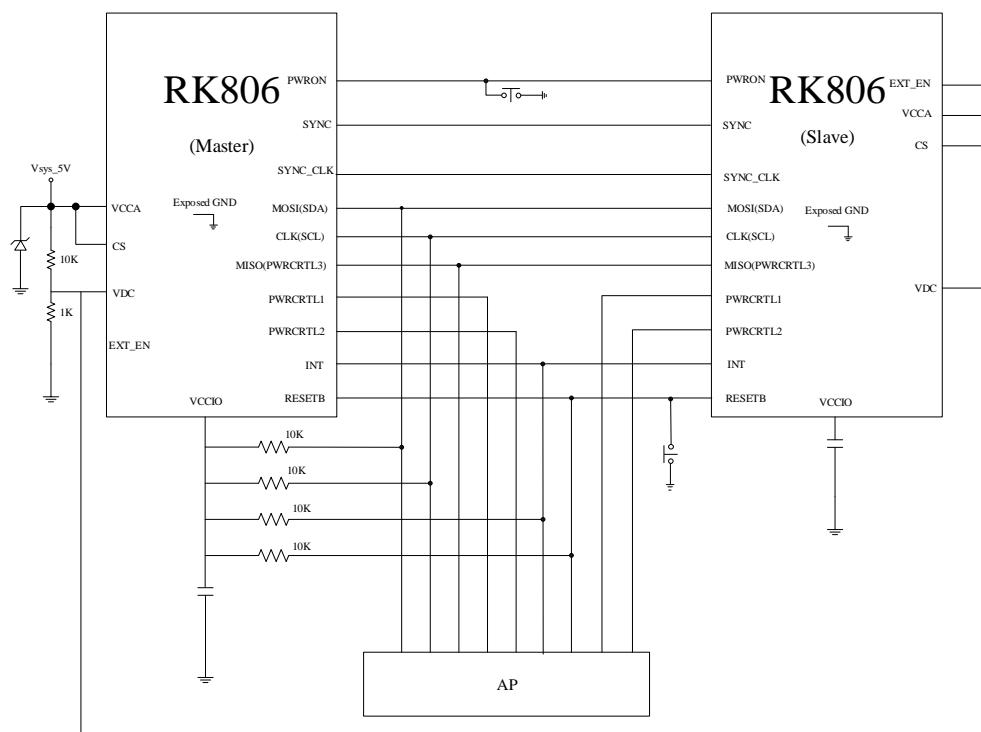


Figure 2-56 RK806 Dual Chip (I2C mode) Typical Application Diagram

- RK806 has two working modes: I2C and SPI. If the CS pin is connected to VCCA during power-up, it is in I2C mode; as long as the CS pin is not input high level at the moment when RK806 is powered on, it is in SPI mode. The figure below shows the dual PMIC working mode with SPI connection.

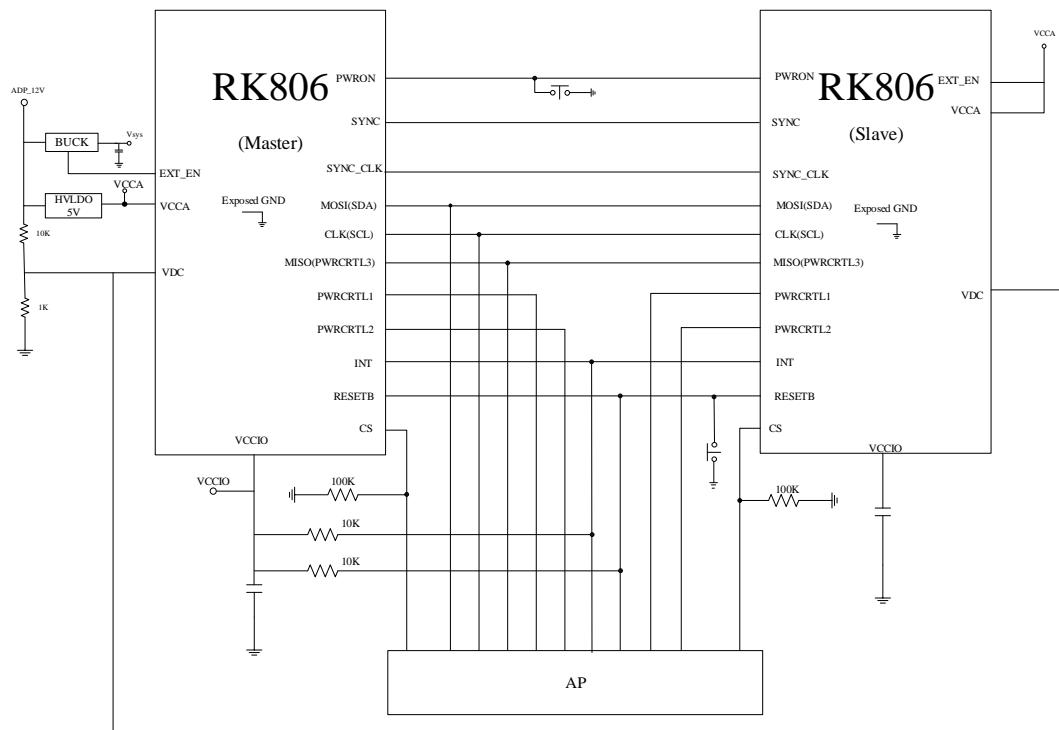


Figure 2-57 RK806 Dual Chip (SPI mode) Typical Application Diagram

- RK806-2 works together: the SYNC_CLK and SYNC of the two chips are interconnected. The main chip provides the SYNC_CLK clock (the frequency is close to 32K). SYNC provides the synchronization signal and generates the synchronization pulse to achieve: power on, power off, reset, power on and power off Timing.
 - Power on: The PWRON, VDC and RESET pin of the master and the slave are connected together, so the master and the slave can receive the same power-on signal. When the power-on signal is valid, the master will provide the SYNC_CLK clock to the slave and pull SYNC high. Respectively according to the master-slave timing of the on-chip OTP burned, using the SYNC_CLK clock as the counting clock, about 1ms as a step, turn on the LDO or BUCK according to the timing;
 - Normal shutdown or restart: RESET remains high and SYNC is pulled low (about 90us above 3clk);
 - Abnormal shutdown: SYNC and RESET are pulled down at the same time within 22us (the capacitance of the reset line cannot be greater than 0.3uF);
 - RESET pulls low to reset: SYNC is high and RESET is pulled low (about 2clk 60us).
- RK806 VCCA (Pin21): The power supply pin of RK806 chip internal digital logic and part of analog control. The design of this pin requires that the power supply voltage must be the highest voltage among all the power supply pins of RK806 or greater than Vmax-0.3V, so VCCA must be powered on first, or powered on together with other power supplies. It is not allowed that the VCCA is not powered on and other power supplies are powered on first.
- RK806 RESETB (Pin40): It is the reset signal output to the master control, and at the same time, it is also used as the external reset signal and the dual PMIC's synchronous shutdown signal input after the reset is pulled high. Because of the input function, a 100nF capacitor is required in the application to improve the anti-interference ability. But the total capacity of the line cannot exceed 0.3uF (because RESET has a synchronous shutdown function, when the capacitance of the RESET line is too large, the rising speed of the high level will slow down, resulting in abnormal detection of the dual PMIC synchronous shutdown sequence).
- The PLDO6 of RK806 supplies power to the VCCIO of these IOs: CS\ MOSI(SDA)\ CLK(SCL)\ MISO(SLEEP3)\ SLEEP2\ SLEEP1. It is recommended that the GPIO power domain that the master control connects to these IOs also use this power supply to achieve the purpose of level matching and synchronization of power-on and power-off.
- RK806 pin32 (VDC): It is used to automatically power on the external power supply. The high level of the VDC pin is 0.8V, and it is recommended that the voltage be greater than 1V and less than or equal to VCCA. When VCCA\ VCC1\ VCC2 is greater than 3.0V, if VDC detects a high level, RK806 will be powered on, and RK806 cannot be powered off while VDC is high (If you want to plug in an adapter to power on, you need to add RC delay to the VDC pin. As shown below).

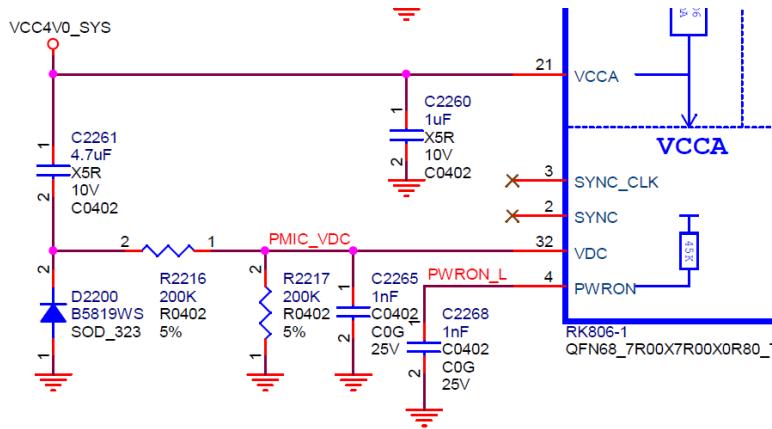


Figure 2-58 RK806 VDC Pin

- RK806 Pin 4 (PWRON): Connect the power button, there is a 45Kohm resistor inside this pin to pull up to VCCA. Pull down this pin for 20ms in the power-off state, and it will turn on if the voltage meets the power-on conditions. (Note: RK806-1 and RK806-2 default 20ms. If the PWRON is pulled down in the power-on state, a short press\long press and other interruptions will be issued to the main control. If it is pulled down for more than 6S, it will be forced to shut down (6S\8S\10S\12S software Optional)).
- RK806 has three PWRCTRL pins, which are PIN16\61\62 (PWRCTRL3\2\1). The functions are the same except that SLEEP3 is multiplexed with MISO. These pins can control RK806 into and out of SLEEP mode, and can also be used to control BUCK or LDO for fast voltage regulation or switch output by configuring the corresponding register.
- RK806 BUCK VOUT pin: VOUT is not only the ripple detection input of COT architecture BUCK, but also the feedback voltage input pin. Generally, it is directly connected to the positive terminal of the output capacitor (the VOUT line should be avoided by other signals as far as possible).
- BUCK1\2\5\6\9 has one more FB pin than other BUCKs. The BUCK with FB pin can choose the voltage feedback pin as VOUT pin or FB pin. The FB reference voltage is 0.5V. When selecting the FB pin, the voltage divider resistance is recommended to be between 10K ohm and 1M ohm. The calculation formula is $V_{out} = (R1/R2 + 1) * 0.5V$. When using external divider resistors, for better transient response of the system, it is recommended to connect a 100pF bypass capacitor in parallel with both ends of the upper divider resistor.

Note: Whether FB is enabled by default is set by OTP. Generally, only the power supply whose default voltage needs to be changed (such as VDD_DDR) will use FB to adjust the default voltage. After power-on, the register can be changed to achieve dynamic switching.

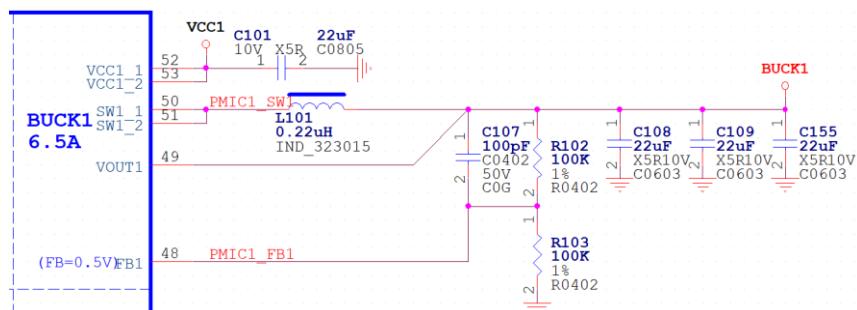


Figure 2-59 RK806 BUCK1

- RK806 BUCK1: The maximum output full load current is 6.5A, the input capacitance is 22uF, the output capacitance is 66uF, the switching frequency is 2MHz (typical), and the inductance is 0.22uH. The withstand voltage of the input and output capacitors is recommended to be twice the working voltage, and the inductor current ripple is about 30% of the full-load current (saturation current is above 8.1A), and the DCR is less than 15m ohm (in order to achieve better conversion efficiency, it is recommended to select DCR Around 10m ohm).
- RK806 BUCK2\3\4: The maximum output full load current is 5A, the input capacitance is 22uF, the output capacitance is 66uF, the switching frequency is 2MHz (typical), and the inductance is 0.22uH. The withstand voltage of the input and output capacitors is recommended to be twice the working voltage, and the inductor current ripple is about 30% of the full-load current (saturation current is above 6.5A), and the DCR is less than 20m ohm (in order to achieve better conversion efficiency, it is recommended to select DCR Around 15m ohm).
- RK806 BUCK5\6\7\8\9\10: The maximum output full load current is 3A, the input capacitance is 10uF, the output capacitance is 44uF, the switching frequency is 2MHz (typical), and the inductance is 0.47uH. The withstand voltage of the input and output capacitors is recommended to be twice the working voltage, and the inductor current ripple is about 30% of the full-load current (saturation current is above 4A), and the DCR is less than 40m ohm (in order to achieve better conversion efficiency, it is recommended to select DCR Around 20m ohm).
- RK806 PLDO: In addition to PLDO6 (VCCIO), RK806 also provides 3 PLDOs with a load capacity of 300mA and 2 PLDOs(PLDO1\PLDO4) with a load capacity of 500mA. The capacity of each input and output capacitor of PLDO should be 1uF or more. Among them, VCC11 is the power supply input pin of PLDO1\2\3, and VCC12 is the power supply input pin of PLDO4\5. To ensure that the PLDO can normalize the voltage regulation efficiency, the minimum input voltage of VCC11 and VCC12 is the maximum output voltage of the LDO +0.2V, and the minimum input voltage is not less than 2.0V.
- RK806 NLDO: NLDO is an LDO that uses an N tube for the adjustment tube. Its characteristic is that the input voltage of the adjustment tube can be very low (Unlike PLDO, there is no minimum 2.0V input voltage requirement). It only needs to meet the output voltage +0.2V, but the highest output voltage is required: the voltage should be 1.5V lower than VCCA (Pin21). NLDO also has two power supply pins VCC13 and VCC14, and it also provides 3 load capacity of 300mA and 2 load capacity of 500mA (NLDO3\NLDO4). The guaranteed capacity of each input and output capacitor of NLDO is 2.2uF or more. VCC13 is the power supply input pin of NLDO1\2\3, and VCC14 is the power supply input pin of NLDO4\5.
- RK806 power on and off condition:
 - VDC boot process
 - ◆ VCCA is powered;
 - ◆ VDC pin level higher than 0.8V, and the recommended value is about 1.0V;
 - ◆ EXT_EN outputs high level;
 - ◆ VCCA\VCC1\VCC2 voltage exceeds VB_LO_SEL voltage within 100mS of EXT_EN output high level (RK806-1/RK80602 value is 3.0V), otherwise it will not boot;
 - ◆ Start the power-on process, each DC/DC, LDO is powered on according to the sequence;
 - ◆ After starting up, VDC can be pulled down or kept at high level.

- Power Key boot process:
 - ◆ VCCA is powered;
 - ◆ PWRON pin voltage is pulled from high level (greater than VCCA*0.7) to low level (less than VCCA*0.3V), the time exceeds 20ms (20/500ms by OTP setting);
 - ◆ EXT_EN outputs high level;
 - ◆ VCCA\VCC1\VCC2 needs to exceed 3.0V within 100ms of EXT_EN outputs high level, otherwise it will not turn on;
 - ◆ Start the power-on process, each DC/DC, LDO is powered on according to the sequence.
- Power off method:
 - ◆ VCC9\VCC1\VCC2 voltage is lower than the under voltage setting value VB_UV_SEL;
 - ◆ VCC9\VCC1\VCC2 voltage is lower than the under voltage setting value VB_UV_SEL, and VB_LO_ACT=0;
 - ◆ I2C or SPI command write DEV_OFF=1;
 - ◆ Over temperature protection shutdown (140/160 degrees);
 - ◆ Press and hold Power Key for more than 6 seconds to force shutdown (6s/8s/10s/12s by set)
 - ◆ The other PMIC pulls down the SYNC and RESET pins to trigger a cooperative shutdown.
- Please refer to RK PMIC related design document "AN_RK806_V1.1" for detailed design instructions of RK806.

2.2.4 RK3588 and RK806-2 Dual PMIC Power Supply Solution Introduction

2.2.4.1 RK3588+RK806-2 Power Tree

Power Diagram

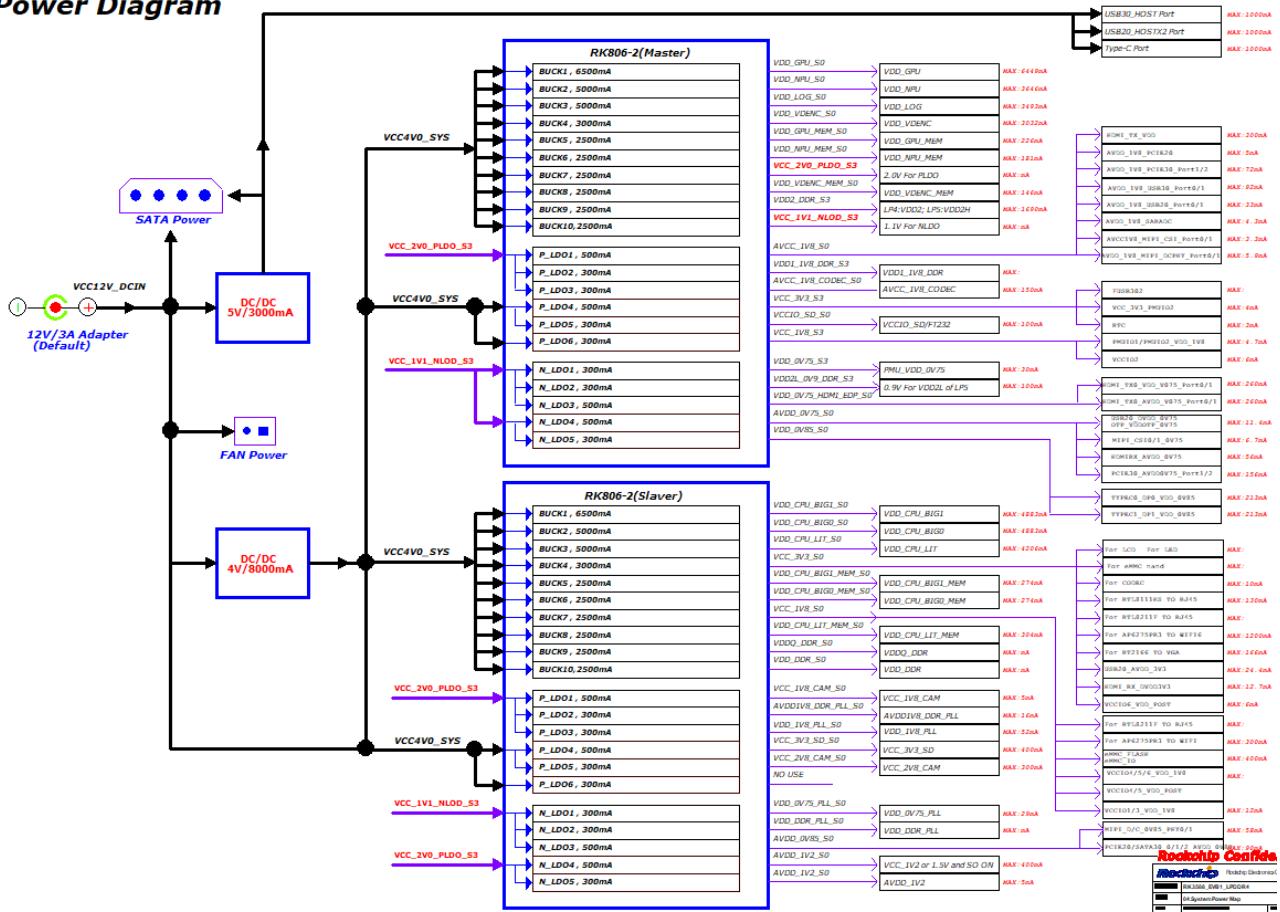


Figure 2-60 RK3588+RK806-2 Power Tree

2.2.4.2 RK806-2 Power on Sequence

RK806-2 contains two sets of power-on sequence of Master and Slave, and they have been solidified. Other models such as RK806-1 cannot be used to replace RK806-2. Similarly, RK806-1 with a single PMIC solution can not be replaced with RK806-2.

Master:

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	PMIC1_BUCK1	6.5A	VDD_GPU_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK2	5A	VDD_NPU_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK3	5A	VDD_LOG_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK4	3A	VDD_VDEC_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK5	2.5A	VDD_GPU_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK6	2.5A	VDD_NPU_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK7	2.5A	VCC_2V0_PLDO_S3		2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK8	2.5A	VDD_VDEC_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK9	2.5A	VDD2_DDR_S3		1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	PMIC1_BUCK10	2.5A	VCC_1V1_NLDO_S3		1.1V	ON	ON	TBD	TBD
	PMIC1_PLDO1	0.3A	AVCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC1_PLDO2	0.3A	VDD1_1V8_DDR_S3		1.8V	ON	ON	TBD	TBD
	PMIC1_PLDO3	0.5A	AVCC_1V8_CODEC_S0		1.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC1_PLDO4	0.5A	VCC_3V3_S3		3.3V	ON	ON	TBD	TBD
	PMIC1_PLDO5	0.3A	VCCIO_SD_S0		3.3V	ON	OFF	TBD	TBD
VCC4V0_VCCA	PMIC1_PLDO6	0.3A	VCC_1V8_S3		1.8V	ON	ON	TBD	TBD
	PMIC1_NLDO1	0.3A	VDD_0V75_S3		0.75V	ON	ON	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO2	0.3A	VDD2L_0V9_DDR_S3		0.9V	ON	ON	TBD	TBD
	PMIC1_NLDO3	0.5A	VDD_0V75_HDMI_EDP_S0		0.75V	ON	OFF	TBD	TBD
	PMIC1_NLDO4	0.5A	AVDD_0V75_S0		0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC1_NLDO5	0.3A	VDD_0V85_S0		0.85V	ON	OFF	TBD	TBD

Slave:

VCC4V0_SYS	PMIC2_BUCK1	6.5A	VDD_CPU_BIG1_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK2	5A	VDD_CPU_BIG0_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK3	5A	VDD_CPU_LIT_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK4	3A	VCC_3V3_S0		3.3V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK5	2.5A	VDD_CPU_BIG1_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK6	2.5A	VDD_CPU_BIG0_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK7	2.5A	VCC_1V8_S0		1.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK8	2.5A	VDD_CPU_LIT_MEM_S0		0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK9	2.5A	VDDQ_DDR_S0		0.6V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_BUCK10	2.5A	VDD_DDR_S0		0.85V	ON	OFF	TBD	TBD
	PMIC2_PLDO1	0.3A	VCC_1V8_CAM_S0		0V	OFF	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_PLDO2	0.3A	AVDD1V8_DDR_PLL_S0		1.8V	ON	OFF	TBD	TBD
	PMIC2_PLDO3	0.5A	VDD_1V8_PLL_S0		1.8V	ON	OFF	TBD	TBD
VCC4V0_SYS	PMIC2_PLDO4	0.5A	VCC_3V3_SD_S0		3.3V	ON	OFF	TBD	TBD
	PMIC2_PLDO5	0.3A	VCC_2V8_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_NLDO1	0.3A	VDD_0V75_PLL_S0		0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	PMIC2_NLDO2	0.3A	VDD_DDR_PLL_S0		0.85V	ON	OFF	TBD	TBD
	PMIC2_NLDO3	0.5A	AVDD_0V85_S0		0.85V	ON	OFF	TBD	TBD
VCC_2V0_PLDO	PMIC2_NLDO4	0.5A	VCC_1V2_CAM_S0		0V	OFF	OFF	TBD	TBD
	PMIC2_NLDO5	0.3A	AVDD_1V2_S0		1.2V	ON	OFF	TBD	TBD

Figure 2-61 RK806-2 Power On Sequence

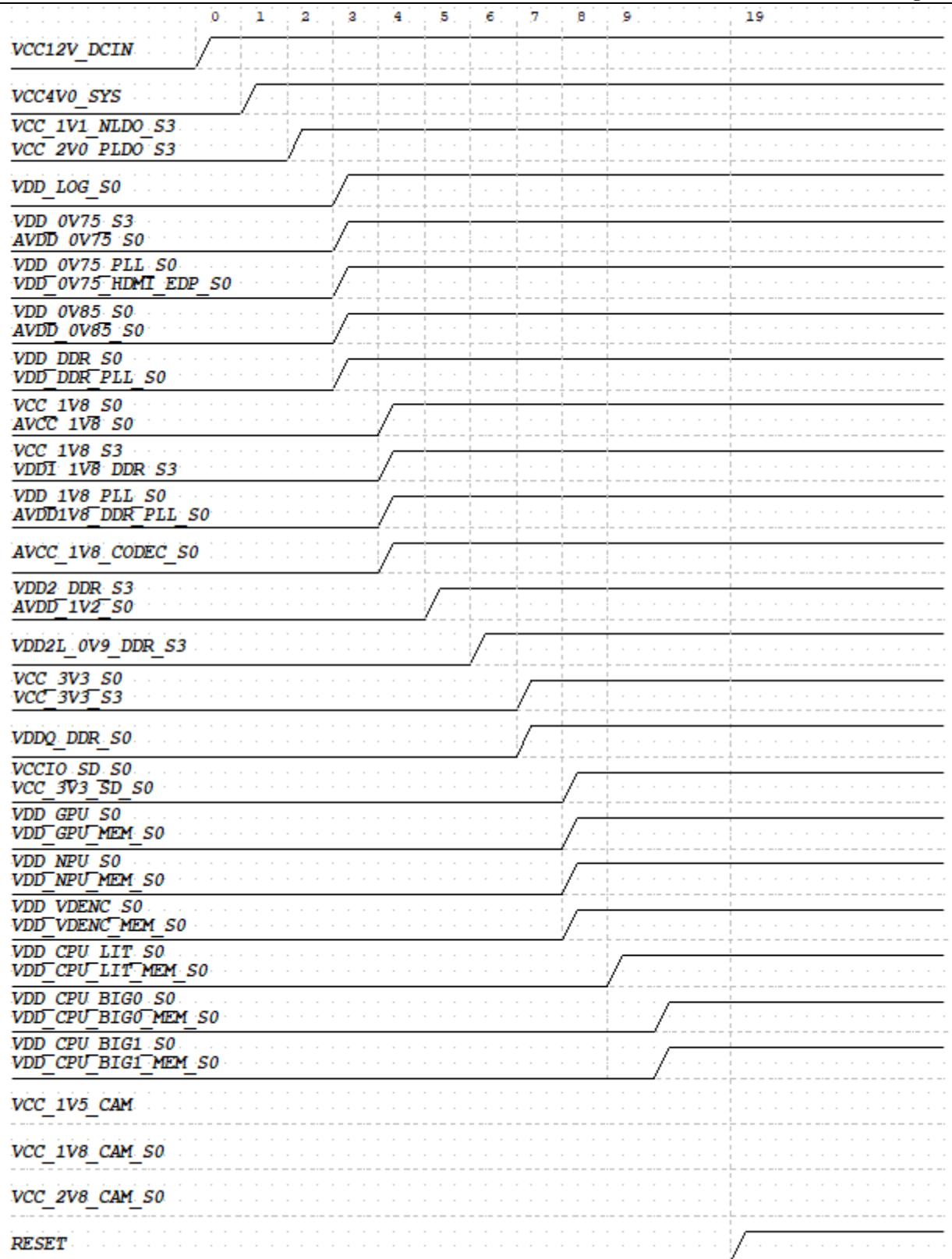


Figure 2-62 RK3588+RK806-2 Power On Sequence

2.2.5 RK3588 and RK806-1 Single PMIC Power Supply Solution Introduction

2.2.5.1 RK3588+RK806-1 Power Tree (AIOT REF)

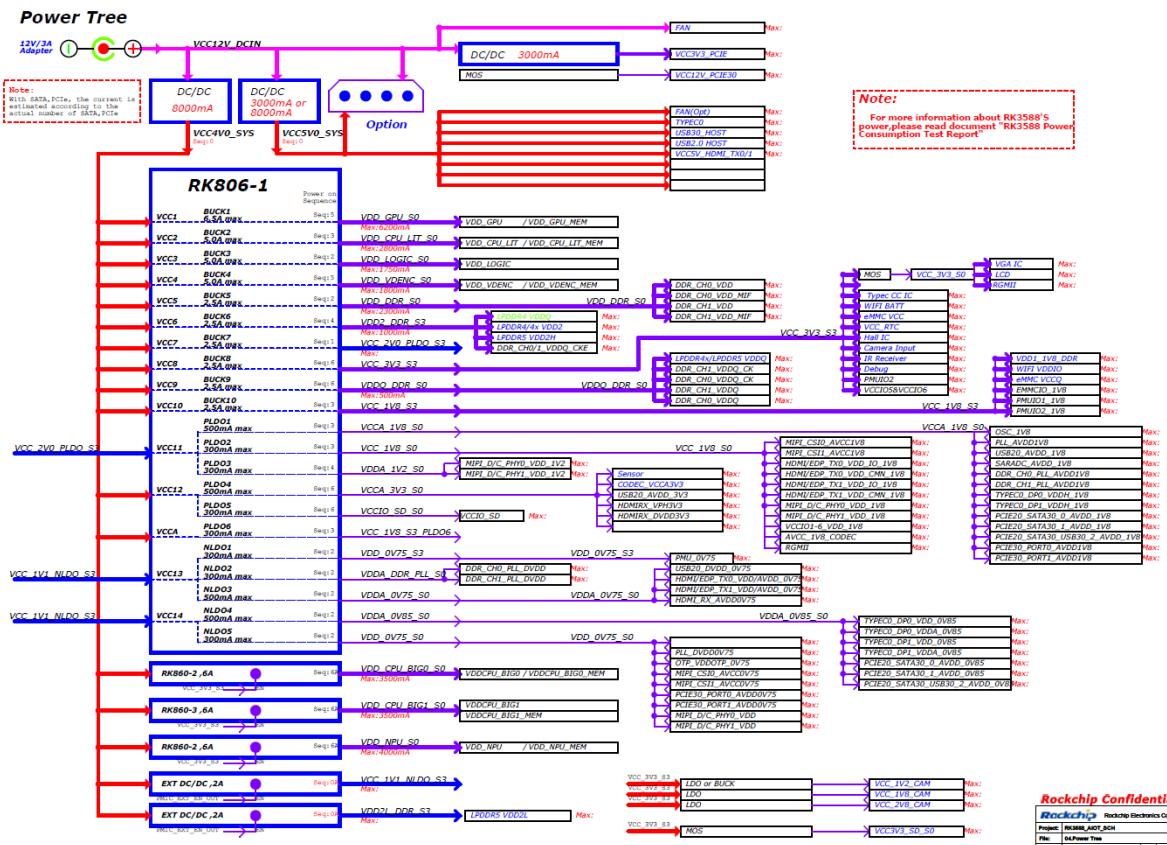


Figure 2-63 RK3588+RK806-1 Power Architect

2.2.5.2 RK806-1 Power On Sequence

When the RK3588 uses a single PMIC RK806-1, three external RK860s are required to provide auxiliary power for the NPU and two big CPUs of the RK3588. The part numbers of the three RK860s are RK860-2/RK860-3/RK860-2 respectively (hanging on two I2C buses respectively). The EN signals of the three RK860s are controlled by the VCC_3V3_S3 power supply. The BIG0 CPU, BIG1_CPU, and NPU (including their respective MEM power supplies) require the default power supply at startup.

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

Figure 2-64 RK3588+RK806-1 Power On Sequence Table

Power Sequence

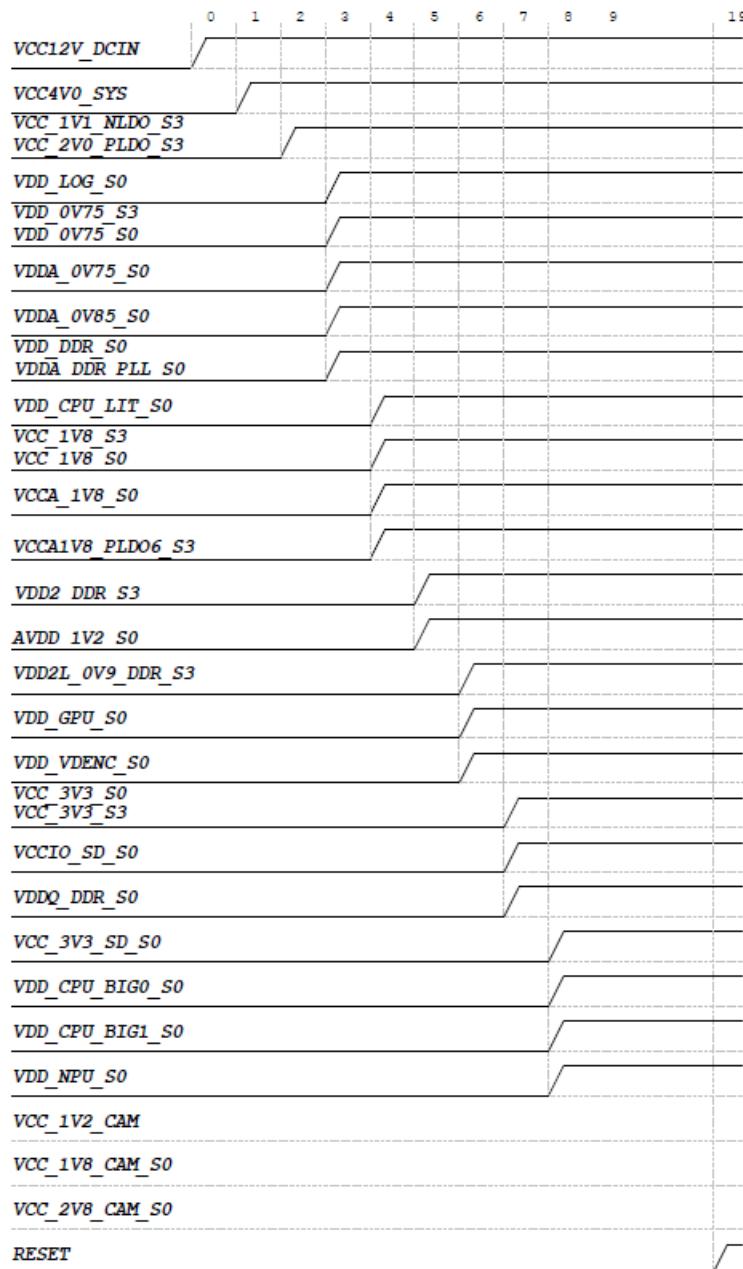


Figure 2-65 RK3588+RK806-1 Power On Sequence

2.2.5.3 Core Module Peak Circuit

The following data is the peak current of each core module, which is used for evaluating the power supply scheme and PCB layout, and is for reference only.

Note: It cannot be simply added up to calculate the peak current of the SOC. To evaluate the heat dissipation scheme, please conduct it according to the working average current of the actual scene.

Table 2-13 RK3588 Peak Current Table

RK3588 core module limit current (in high temperature)					
core module limit current	Power network	Voltage (V)	Peak current (A)	Peak power (W)	Note
	VDD_CPU_BIG0_S0	0.980	4.00	3.92	Frequency 2400MHz
	VDD_CPU_BIG1_S0	0.980	4.00	3.92	Frequency 2400MHz
	VDD_CPU_LIT_S0	0.950	3.00	2.85	Frequency 1800MHz
	VDD_LOG_S0	0.750	2.50	1.88	
	VDD_GPU_S0	0.850	6.50	5.53	Frequency 1000MHz
	VDD_NPU_S0	0.850	4.00	3.40	Frequency 1000MHz
	VDD_VDENC_S0	0.775	2.50	1.94	Frequency 750MHz
	VDD_DDR_S0	0.870	2.50	2.18	Frequency 2112MHz

2.3 Functional Interface Circuit Design Guide

2.3.1 SDMMC/SDIO

RK3588 integrates 1 SDMMC controller and 1 SDIO controller, and they all support SDIO3.0 protocol and MMC V4.51 protocol.

4-wire data bus width; supports SDR104 mode with a rate of 150MHz.

2.3.1.1 SDMMC Interface

- The SDMMC interface is multiplexed in the VCCIO2 power domain;
- Support System Boot, default allocation of SD card function;
- SDMMC is multiplexed with JTAG and other functions. The function selection is performed through the SDMMC_DET state by default. For details, please refer to the description in section 2.1.5;
- VCCIO2 power supply, need to provide external 3.3V or 1.8V power supply;
- When connecting to an SD card: If you only need to support SD2.0 mode, you can directly supply 3.3V power; if you want to support SD3.0 mode and be compatible with SD2.0 mode, 3.3V power is supplied by default. After negotiating with the SD card to run the SD3.0 mode, the power supply voltage needs to be switched to 1.8V. PLDO5 of RK806-2 or RK806-1 can power VCCIO2 alone to realize this process;

- When connected to SDIO device: 1.8V or 3.3V according to the peripherals and the actual operating mode;

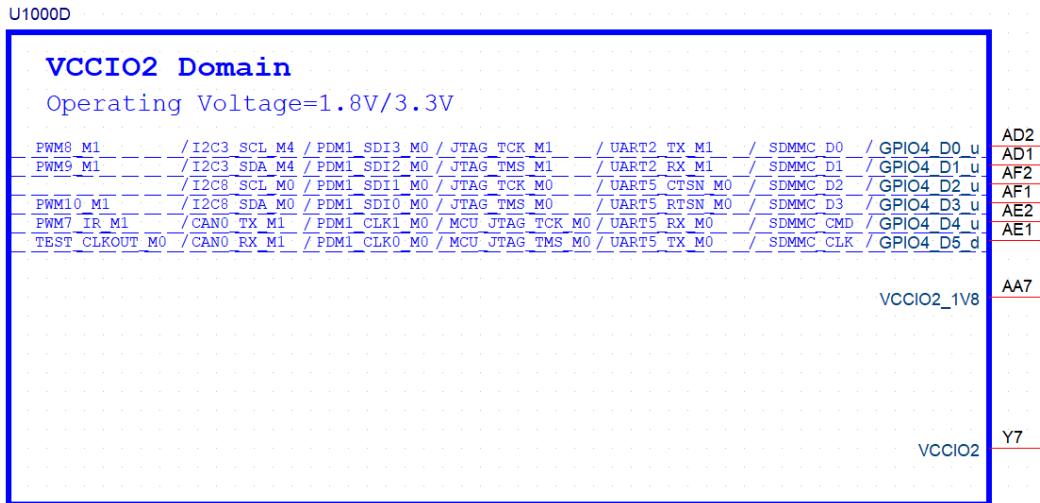


Figure 2-66 RK3588 SDMMC Interface Pin

- When realizing the board-to-board connection through the connector, it is recommended to connect a certain resistance resistor in series (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices;
- When using SD card, pay attention to the following items:
 - The supply voltage of VDD pin of the SD card is 3.3V, and the decoupling capacitors are not allowed to be deleted. Place them close to the connector when layout.
 - SDMMC0_D [3:0], SDMMC0_CMD, SDMMC0_CLK need to be connected to a 22ohm resistor in series, and SDMMC0_DET to be connected to a 100ohm resistor in series;
 - SDMMC_D[3:0], SDMMC_CMD, SDMMC_CLK, SDMMC_DET signals need to place ESD devices in the SD card position. To support the SD3.0 mode, the junction capacitance of the ESD device must be less than 1pF. If only the SD2.0 mode is required, the junction capacitance of the ESD device can be relaxed to 9pF.

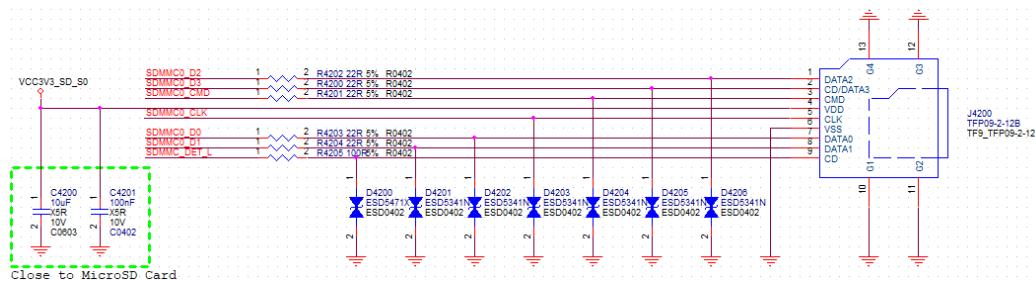


Figure 2-67 SD Card Interface Circuit

- SDMMC0 interface pull-up/down and matching design recommendations are shown in the table

Table 2-14 SDMMC0 Interface Design

Signal	Internal pull-up and pull-down	Connection mode	Description (chipset)
SDMMC0_D[3:0]	pull up	connect a 22ohm resistor in series, use the corresponding IO internal pull-up resistor	SD data send/receive
SDMMC0_CLK	pull down	connect a 22ohm resistor in series	SD clock send
SDMMC0_CMD	pull up	connect a 22ohm resistor in series, use the corresponding IO internal pull-up resistor	SD command send/receive
SDMMC0_DET	pull up	connect a 100ohm resistor in series, use the corresponding IO internal pull-up resistor	SD card insertion detection

2.3.1.2 SDIO Interfaces

- The SDIO interface is multiplexed in two locations: one in the VCCIO3 power domain and one in the VCCIO5 power domain. Only one of them can be used. Either all use the VCCIO3 power domain, or all use the VCCIO5 power domain, it does not support part of the VCCIO3 power domain, and some of the VCCIO5 power domain;
- Does not support System Boot;
- The power supply of VCCIO3 is 1.8V only; the power supply of VCCIO5 is 1.8V or 3.3V, and the corresponding voltage should be selected according to the needs of the peripheral. It should be kept consistent with the IO of the peripheral.

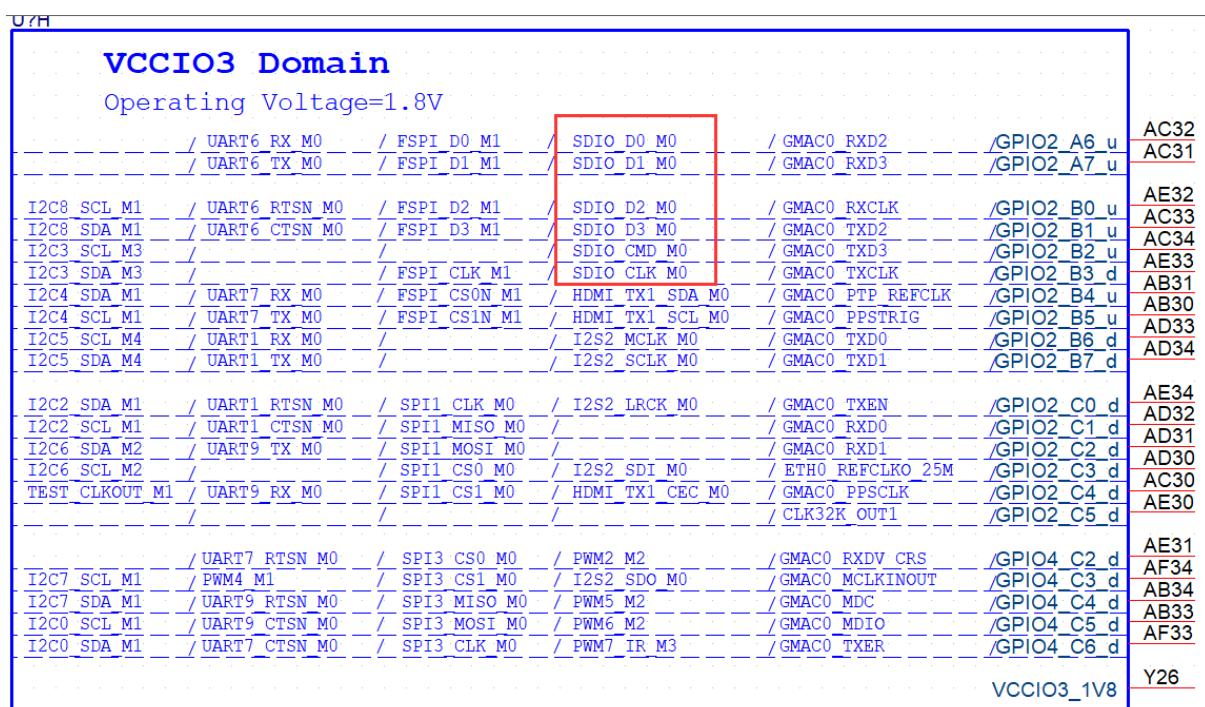


Figure 2-68 RK3588 SDIO Interface M0 Function Pin

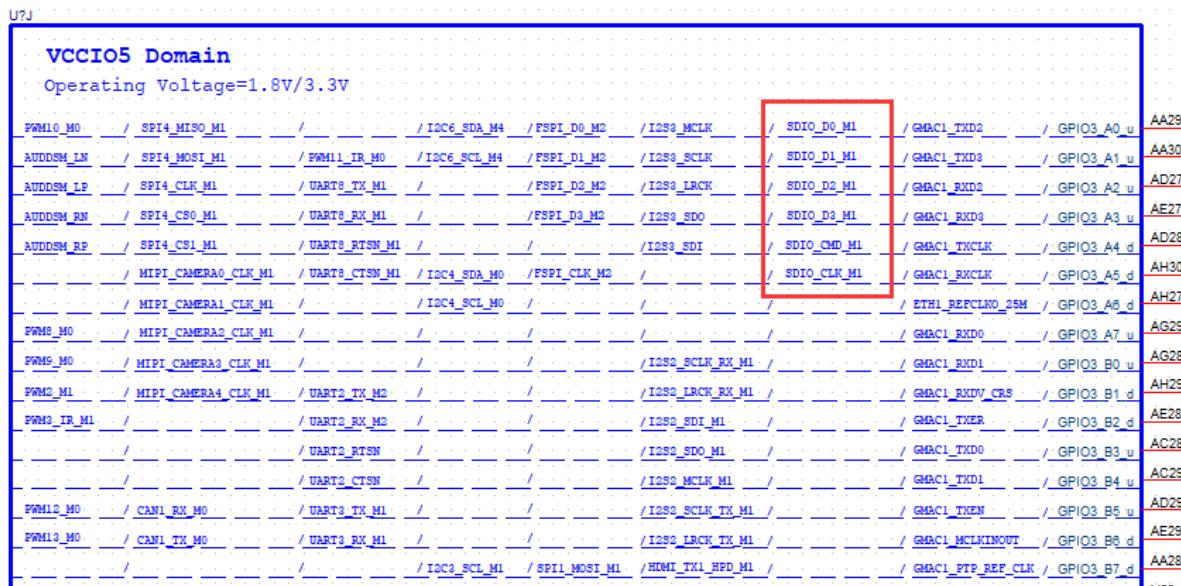


Figure 2-69 RK3588 SDIO Interface M1 Function Pin

- SDIO interface pull-up and pull-down and matching design recommendations are shown in the Table

Table 2-15 SDIO Interface Design

Signal	Internal pull-up and pull-down	Connection mode	Description (chipset)
SDIO_D[3:0]	pull up	22ohm resistor in series, delete when the trace is short Use the corresponding IO internal pull-up resistor	SD data send/receive
SDIO_CLK	pull down	22ohm resistor in series,	SD clock send
SDIO_CMD	pull up	22ohm resistor in series, delete when the trace is short Use the corresponding IO internal pull-up resistor	SD command send/receive

When realizing the board-to-board connection through the connector, it is recommended to connect a resistor with a certain resistance in series (between 22ohm and 100ohm, depending on the specific requirements that can meet the SI test), and reserve TVS devices.

2.3.1.3 Notes of When SDIO Connects to WIFI

- Please ensure that the IO level of the module is consistent with the IO level of the CPU, otherwise, level matching processing is required;
- The crystal load capacitance should be selected according to the CL capacitance value of the crystal actually used, and the frequency tolerance at room temperature should be controlled within 10ppm;
- The antenna reserves a π -type circuit for antenna matching adjustment;
- Confirm the connection direction of PCM and UART interface, such as IN and OUT, TXD and RXD;
- If you need to use a 32.768k clock input module, 32.768kohm pull-up resistor is required and you need to pay attention to the clock amplitude to meet the parameters of the WIFI module.

2.3.2 SARADC Circuit

RK3588 integrates a SARADC controller with a resolution of 12bit, with a speed of 1MS/s, an input voltage

range of 0-1.8V, and 8 SARADC inputs.

SARADC_IN0_BOOT is dedicated to the setting of the startup sequence of SYSTEM BOOT and cannot be used for other functions. The value obtained by sampling the voltage of the pull-up and pull-down resistor is used to determine which interface to BOOT. The settings are as follows: (Rup/Rdown represents the pull-up and pull-down resistors)

Item	Rup(ohm)	Rdown(ohm)	ADC	VOL(Unit:V)	BOOT MODE
LEVEL1	DNP	100K	0	0	USB (Maskrom Mode)
LEVEL2	100K	20K	682	0.3	SD Card→USB
LEVEL3	100K	51K	1365	0.6	EMMC→USB
LEVEL4	100K	100K	2047	0.9	FSPI_M0→USB
LEVEL5	100K	200K	2730	1.2	FSPI_M1→USB
LEVEL6	100K	499K	3412	1.5	FSPI_M2→USB
LEVEL7	100K	DNP	4095	1.8	FSPI_M2 → FSPI_M1 → FSPI_M0 → EMMC_SD Card→USB

If Rup=DNP, Rdown=100K, RK3588 device is connected to the USB, and power on at this time, the system can directly enter the Maskrom.

SARADC_VIN1 is used as the key value input sampling of the button, and reused as a Recovery mode button (cannot be modified).

SARADC_VIN1 is pulled up to VCCA_1V8_S0 through a 10Kohm pull-up resistor, and the default is high level (1.8V). Under the premise that there is no key action and the system has already burned the firmware, power on and enter the system directly. If the Recovery mode button is in the pressed state when the system starts, (that is, SARADC_VIN1 remains at low level (0V)), RK3588 enters Loader programming mode. When the PC recognizes the USB device, release the button to restore SARADC_VIN1 to a high level (1.8V), and then the firmware can be programmed. Therefore, when the product does not have a button, when SARADC_VIN1 is left floating, it will be unstable, which may affect booting. Therefore, the 10Kohm pull-up resistor of SARADC_VIN1 must be retained and cannot be deleted to ensure the default normal startup judgment. In order to facilitate development, SARADC_VIN1 is recommended to reserve button or reserve test point.

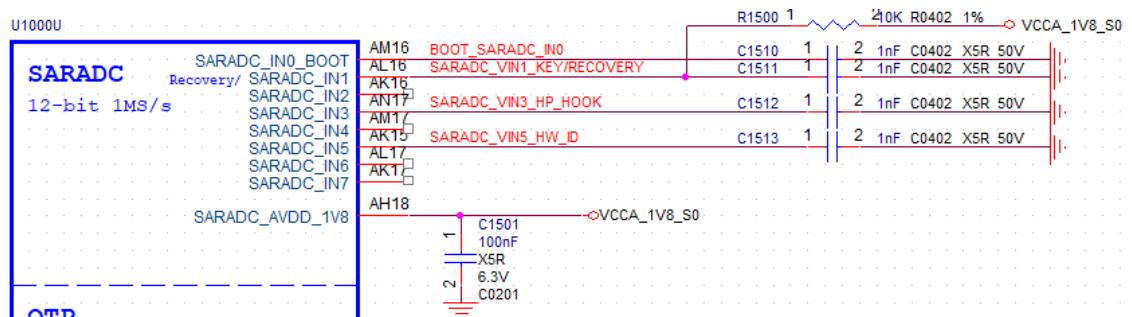


Figure 2-70 SARADC VIN0 Interface

On RK3588, the key array adopts the parallel type, and the input key value can be adjusted by adding or subtracting keys and adjusting the voltage divider resistance ratio to realize multi-key input to meet customer product requirements. In the design, it is recommended that the key value of any two keys must be greater than +/- 35, that is, the center voltage difference must be greater than 31mV.

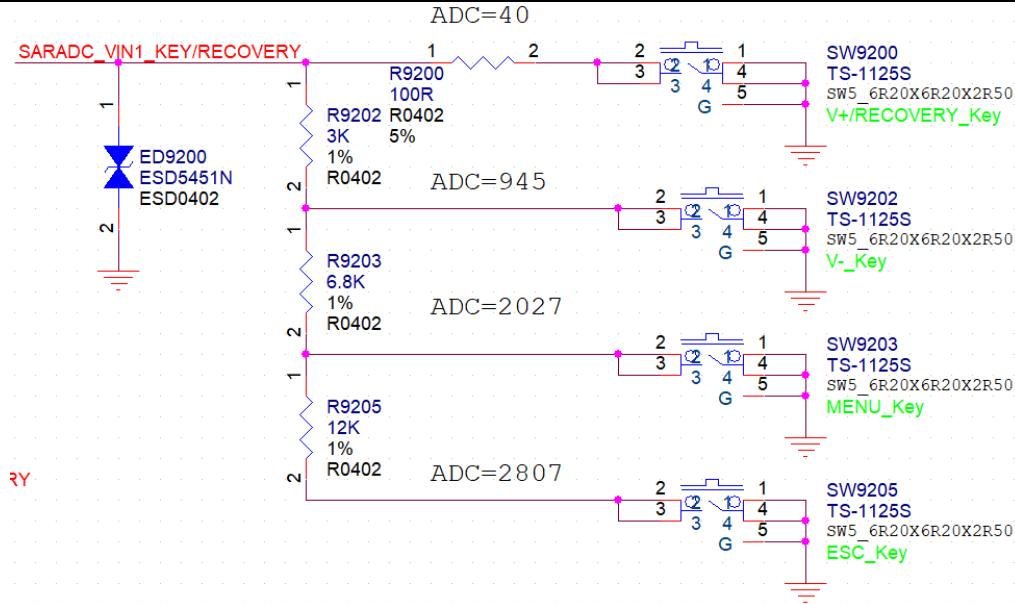


Figure 2-71 RK3588 SARADC Key Matrix Circuit

Some notes for RK3588 SARADC design:

- The decoupling capacitor of the SARADC_AVDD_1V8 power supply must be kept. During layout, place it close to the RK3588 pin;
- If SARADC_VIN[7:0] is used, a 1nF capacitor must be added close to the pin to eliminate jitter;
- When used for button collection, ESD protection must be done and close to the button, and a 100ohm resistor must be connected in series with 0 key value to enhance the anti-static surge capability (if there is only one button, ESD must be close to the button, first pass ESD 100ohm resistor 1nF Chip pin)

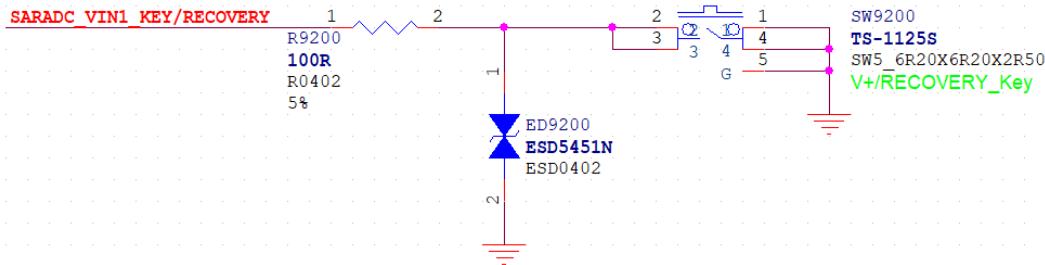


Figure 2-72 RK3588 SARADC Single Button Circuit

2.3.3 OTP Circuit

RK3588 has 32Kbit space and high 4Kbit address non-secure space for programming. Support write, read and idle modes, these modes OTP_VDDOTP_0V75 pins must be powered.

The decoupling capacitor of the OTP_VDDOTP_0V75 power supply must not be deleted, and should be placed close to the RK3588 pin during layout.

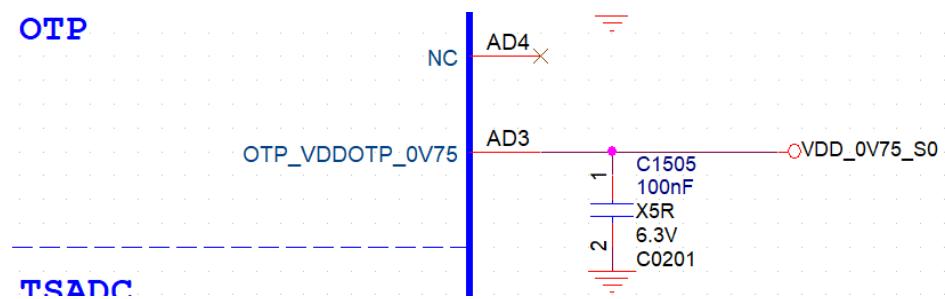


Figure 2-73 RK3588 OTP Power Pin

2.3.4 USB2.0/USB3.0 Circuit

RK3588 has built-in 2 USB3.0 OTG controllers (embedded with two USB2.0 OTG, as the green area in the figure below), 1 USB3.0 HOST controller, and 2 USB2.0 HOST controllers.

The internal multiplexing diagram of these controllers and PHY is as follows

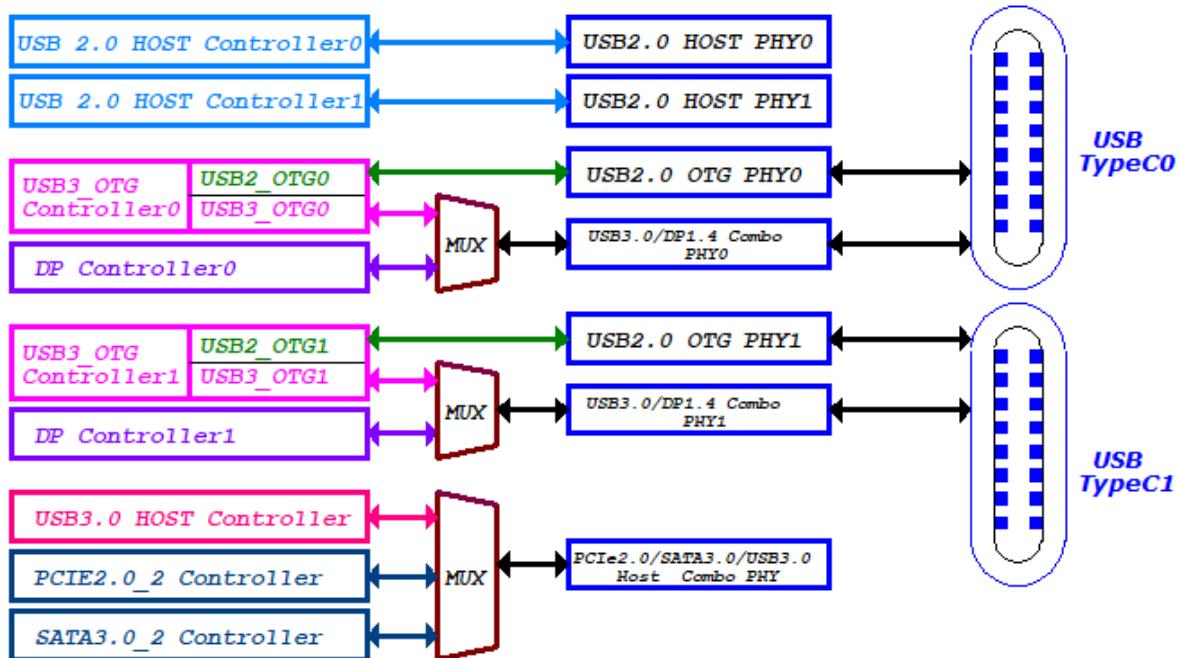


Figure 2-74 Multiplexing Relationship Between MULTI_PHY0/1and USB3.0 Controllers

The USB3.0 OTG0 controller supports SS/HS/FS/LS, the embedded USB2.0 (HS/FS/LS) signal adopts USB2.0 OTG PHY, the signal name is shown in the red box in the figure below; RK3588 currently only This interface supports Fireware Download, please be sure to reserve this interface in the application.

U1000L

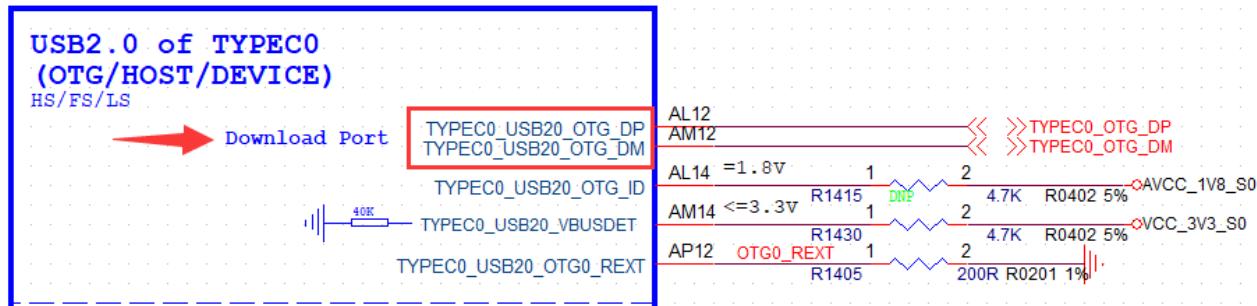


Figure 2-75 TYPEC0 USB2.0 OTG Pin


NOTE

Only TYPEC0_USB2.0_OTG_DP/TYPEC0_USB2.0_OTG_DM supports Download Firmware. If the product does not use this interface, it must be reserved during debugging and production. Note: USB3_OTG0_VBUSDET must also be connected!

The SS signal (5Gbps) of USB 3.0 is multiplexed with DP1.4, using the Combo PHY of USB/DP; the signal is in the red box as shown in the figure below.

U1000M

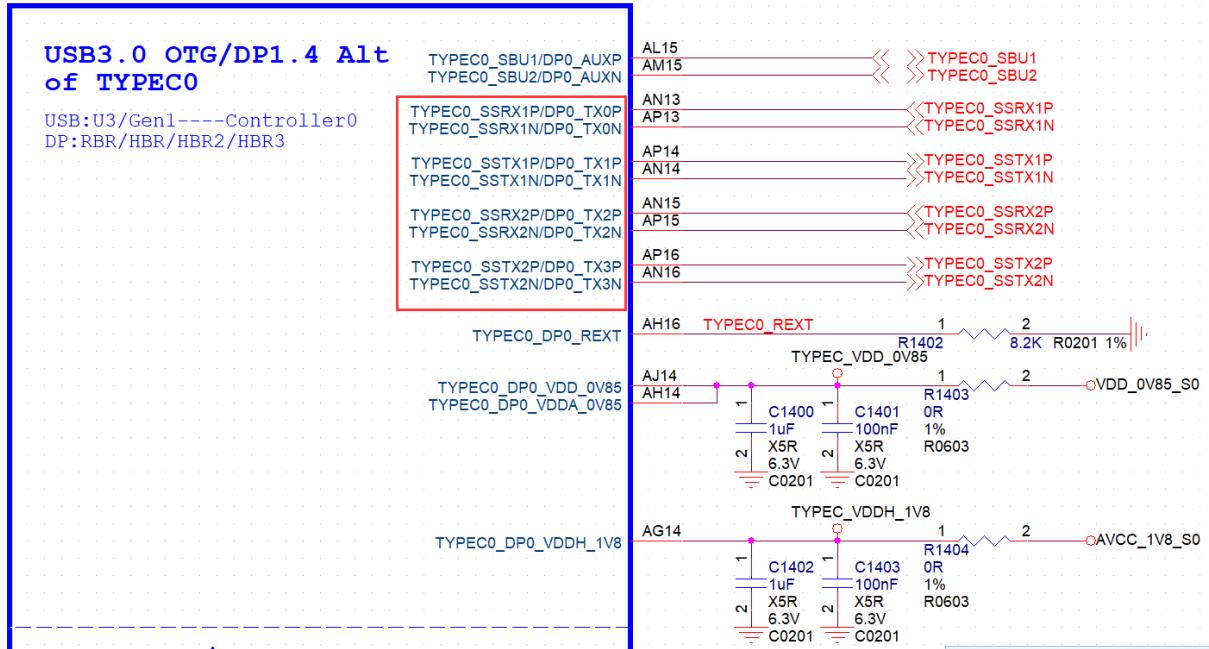


Figure 2-76 TYPEC0 USB3.0 OTG and DP Pins

Since USB3.0 OTG and USB2.0 OTG are the same USB3.0 controller, USB3.0 and USB2.0 OTG can only be used as Device or HOST at the same time, and USB3.0 OTG cannot be used as HOST. USB2.0 OTG is used as Device or USB3.0 OTG is used as Device and USB2.0 OTG is used as HOST.

USB3.0 Controller0 and DP1.4 Controller0 are combined into a complete TYPEC port through the Combo PHY0 of USB3.0/DP1.4. This Combo PHY supports Display Alter mode. Lane0 and Lane2 are used as TX in DP mode, and used as RX in USB mode. TX and RX share Lane0 and Lane2.

The TYPEC1 port composed of USB3.0 Controller1 and DP1.4 Controller1 is the same as the TYPEC0 port.

This USB3.0/DP1.4 Combo PHY supports the switching between Lanes (SWAP), so a TYPEC standard port have the following five configurations:

- Configuration 1: Type-C 4Lane(with DP function)

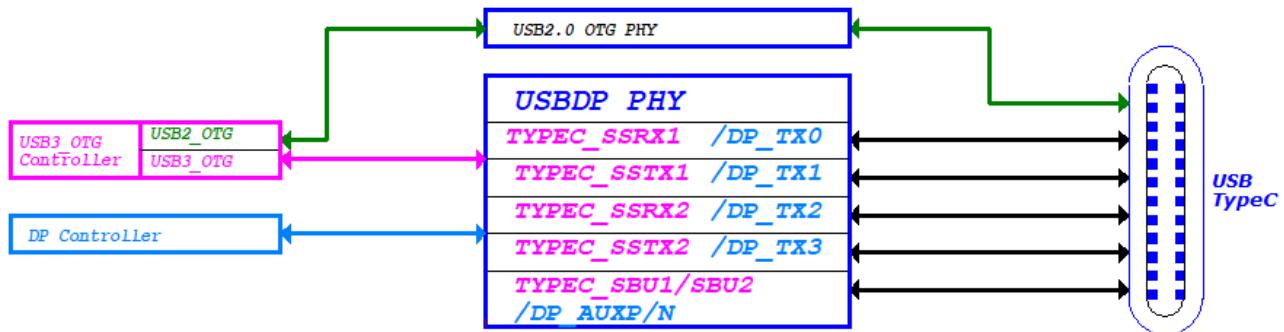


Figure 2-77 TYPEC0 4Lane and DP Connection Block Diagram

- Configuration 2: USB2.0 OTG+DP 4Lane (Swap OFF)

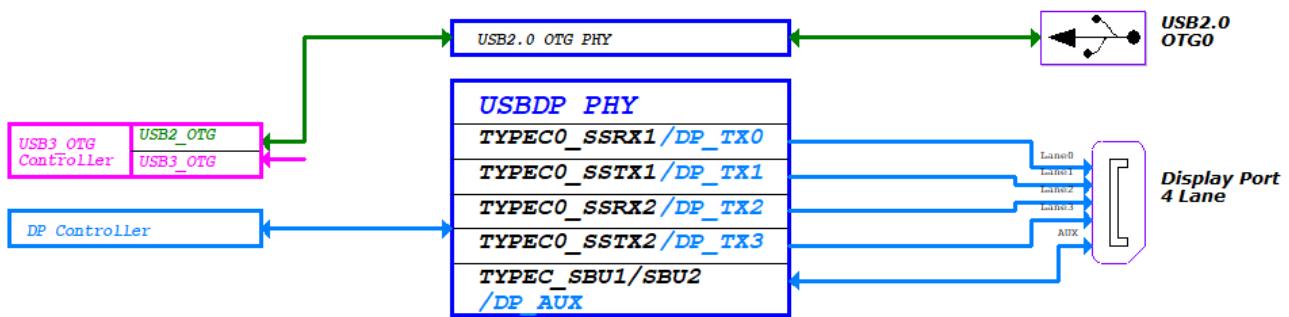


Figure 2-78 USB2.0 OTG+DP 4Lane Connection Block Diagram

- Configuration 3: USB2.0 OTG+DP 4Lane(Swap ON)

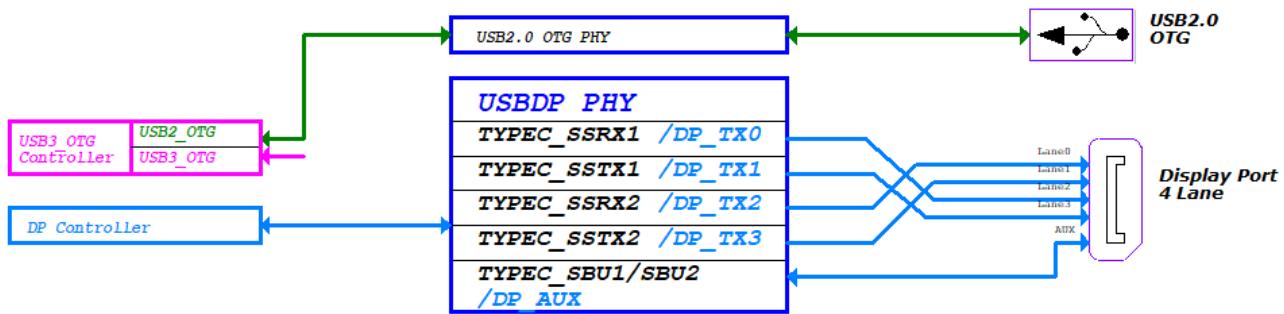


Figure 2-79 USB2.0 OTG+DP 4Lane (Swap ON) Connection Block Diagram

- Configuration 4: USB3.0 OTG0+DP 2Lane(Swap OFF)

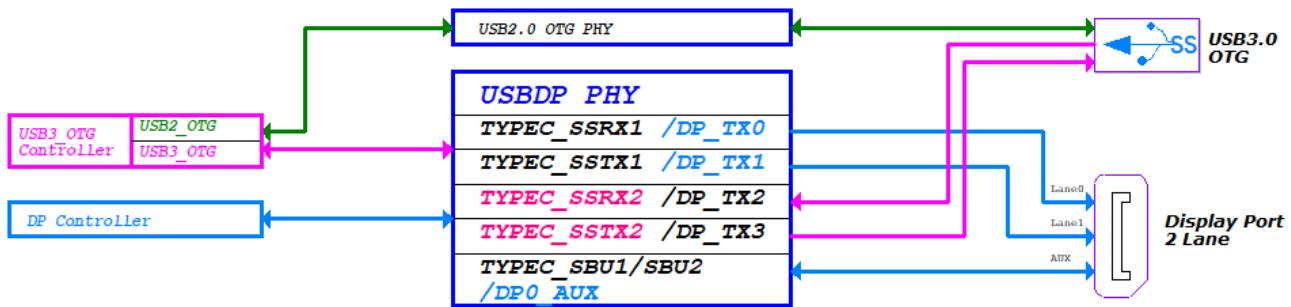


Figure 2-80 USB3.0 OTG0+DP 2Lane(Swap OFF) Connection Block Diagram

- Configuration 5: USB3.0 OTG+DP 2Lane (Swap ON)

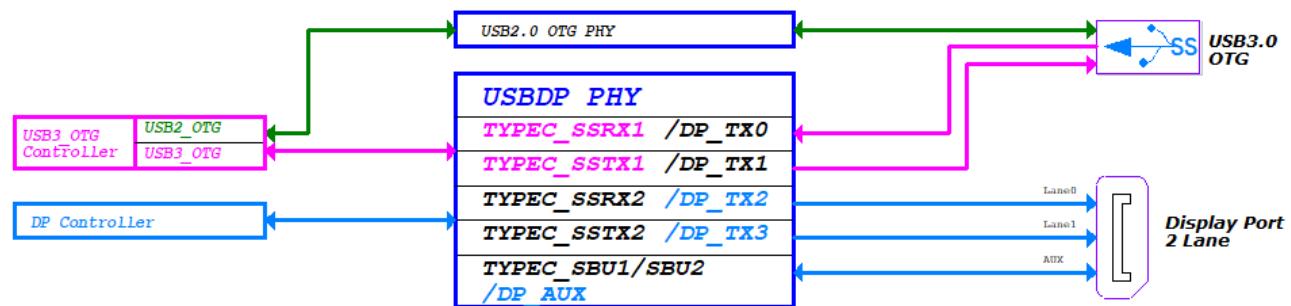


Figure 2-81 USB3.0 OTG0+DP 2Lane(Swap ON) Connection Block Diagram

For the pin assignments of the above configurations, see PAGE 07 of the **EVB schematic diagram** for details.

Since the USB3.0 HOST controller has only USB3.0 HOST and no embedded USB2.0, if you need to form a complete USB3.0 HOST interface, it needs to be the same as USB2.0 HOST Controller1 (configuration 2) or USB2.0 HOST Controller0 (Configuration 2) combine into a standard USB3.0 HOST. The internal connection diagram is as follows:

- Configuration 1: USB3.0 HOST2+USB2.0 HOST1

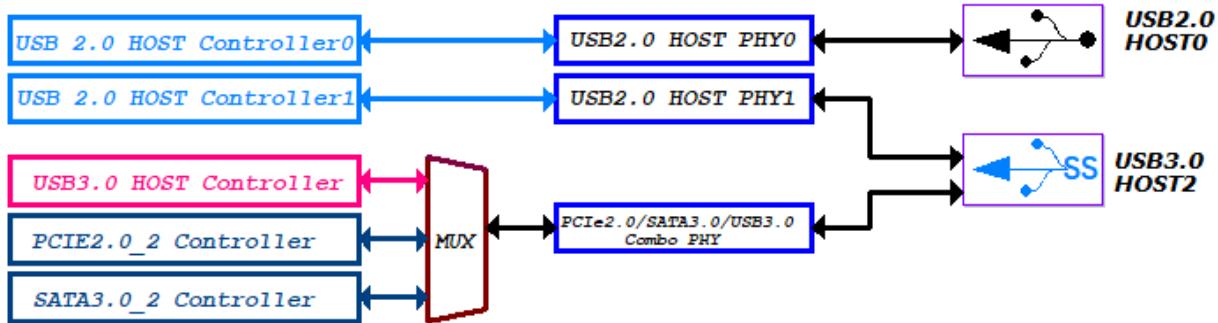


Figure 2-82 USB3.0 HOST2+USB2.0 HOST1 Connection Block Diagram

- Configuration 2: USB3.0 HOST2+USB2.0 HOST0

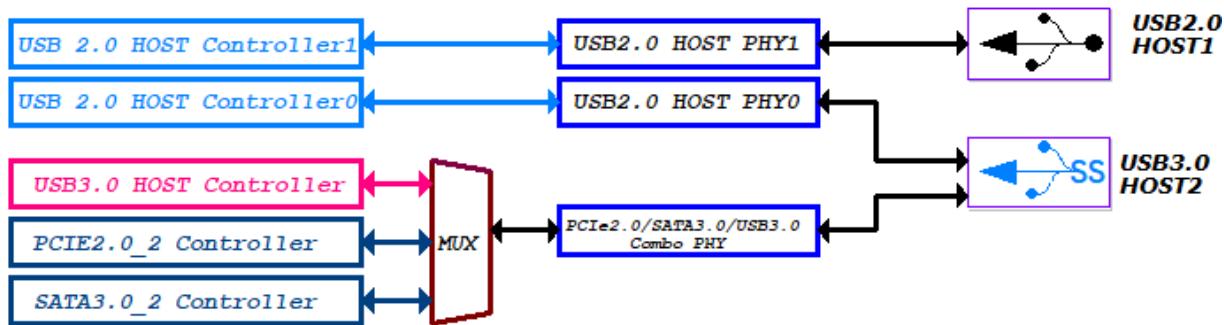


Figure 2-83 USB3.0 HOST2+USB2.0 HOST0 Connection Block Diagram

USB2.0 HOST0 controller, use USB2.0 HOST0 PHY. The signals in the red box below constitute the USB2.0 HOST0 interface:

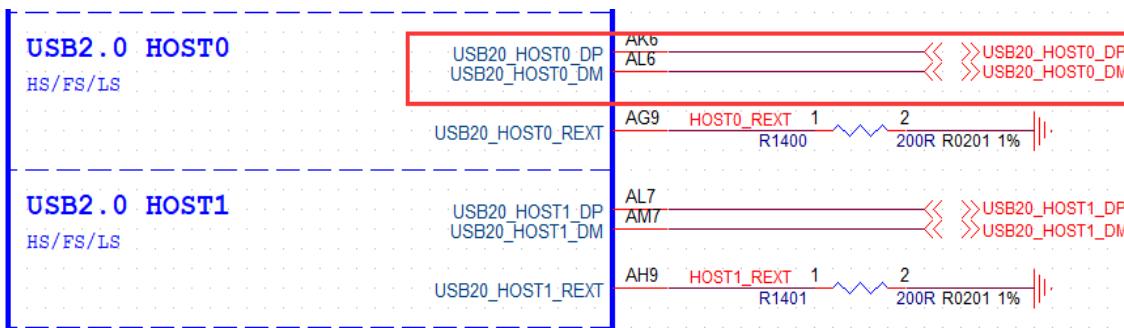


Figure 2-84 USB2.0 HOST0 Pin

USB2.0 HOST1 controller, use USB2.0 HOST1 PHY. The signals in the red box below constitute the USB2.0 HOST1 interface:

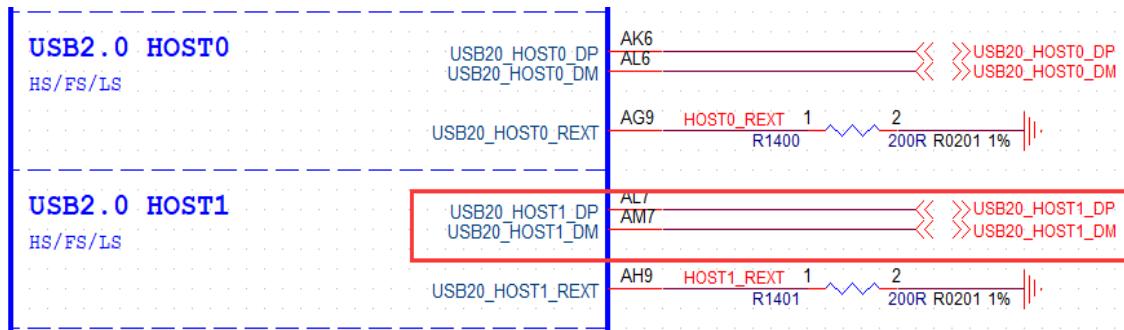


Figure 2-85 USB2.0 HOST1 Pin

The internal connection block diagram of USB2.0 Controller and PHY is as follows:

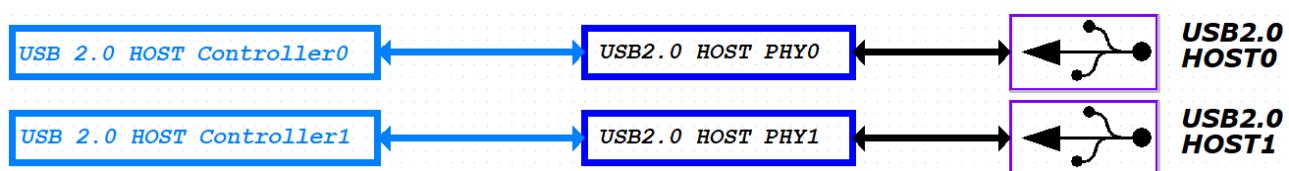


Figure 2-86 Connection Block Diagram of USB2.0 Controller and PHY

Please note in the USB2.0/USB3.0 design:

- TYPEC0_USB20_OTG_DP/TYPEC0_USB20_OTG_DM is the system firmware programming interface. If the product does not use this interface, this interface must be reserved during the debugging and production process, otherwise it will not be able to debug and produce the programming firmware;
- TYPEC_USB20_OTG0_ID has about 200Kohm resistor pulled up to USB20_AVDD_1V8;
- TYPEC_USB20_VBUSDET is the OTG and Device mode detection pin, high level is DEVICE device, 2.7-3.3V, TYP: 3.0V, it is recommended to place a 100nF capacitor on the pin.

OTG mode can set the following three modes:

- OTG mode: automatically switch between device mode or HOST mode according to the state of ID pin, ID high is device, ID is pulled low to HOST, when in device mode, it will also judge whether the VBUSDET pin is high (greater than 2.3V), if it is high , will pull up DP and start enumeration;
- Device mode: When set to this mode, no ID pin is needed, just judge whether the VBUSDET pin is high (greater than 2.3V), if it is high, it will pull up DP and start enumeration;
- HOST mode: When set to this mode, the ID and VBUSDET status do not need to be concerned. (If the product only needs HOST mode, but since only TYPEC0_USB20_OTG_DP/TYPEC0_USB20_OTG_DM is the system firmware programming port, this port needs to be used in the debugging and production process. When programming and adb debugging, it needs to be set to device mode, so the TYPEC_USB20/1_VBUSDET signal must also be received).

Before uboot is up, it defaults to device mode. After entering uboot, you can configure these three modes according to actual needs.

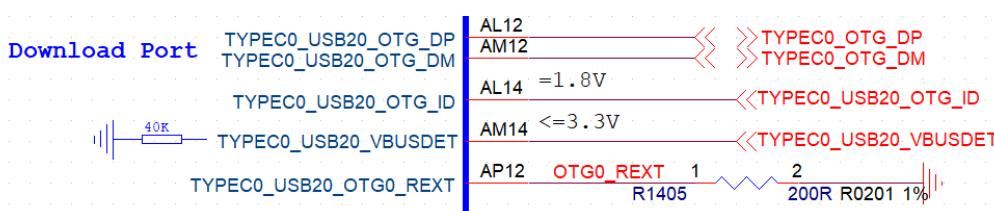


Figure 2-87 RK3588 TYPEC0_USB20_OTG Circuit

If the TYPEC interface is used, the Pin "TYPEC0_USB20_VBUSDET" can be connected to 3.3V through a 4.7K pull-up resistor; if the Micro USB2.0 interface is used, the following circuit is used:

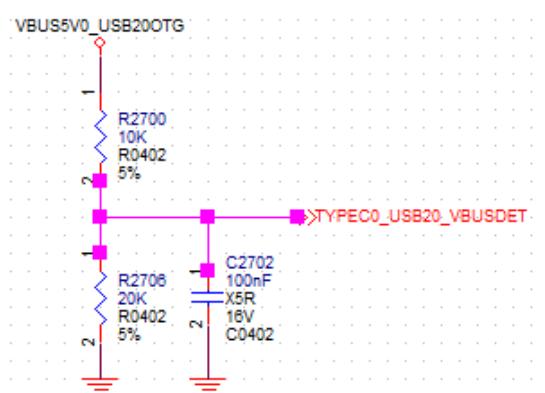


Figure 2-88 TYPEC0_USB20_VBUSDET Circuit

- In order to improve the USB performance, the decoupling capacitors of each PHY power supply can not be deleted, and place them close to the pins during layout;
- In order to strengthen the anti-static and surge capability, ESD devices must be reserved on the signal. The ESD parasitic capacitance of the USB2.0 signal can not exceed 3pF. In addition, the DP/DM of the USB2.0 signal is connected in series with a 2.2ohm resistor to strengthen the anti-static surge capability, and cannot be deleted. Take TYPEC0_OTG_DP/DMas an example, as shown in the figure below, other USB2.0 interfaces also need to be processed in the same way;

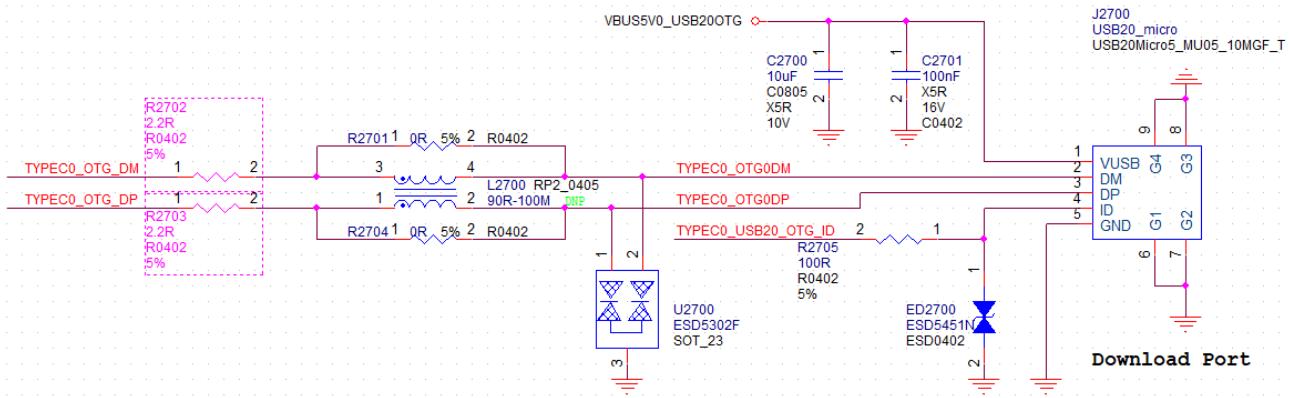


Figure 2-89 USB2.0 Signal Serially Connected with 2.2ohm Resistor Circuit

- In order to suppress electromagnetic radiation, you can consider reserving a common mode choke on the signal line, and choose to use a resistor or a common mode choke according to the actual situation during the debugging process, see the figure below, for example TYPEC0_OTG_DP/DM, other USB2. The 0 interface also needs the same treatment.

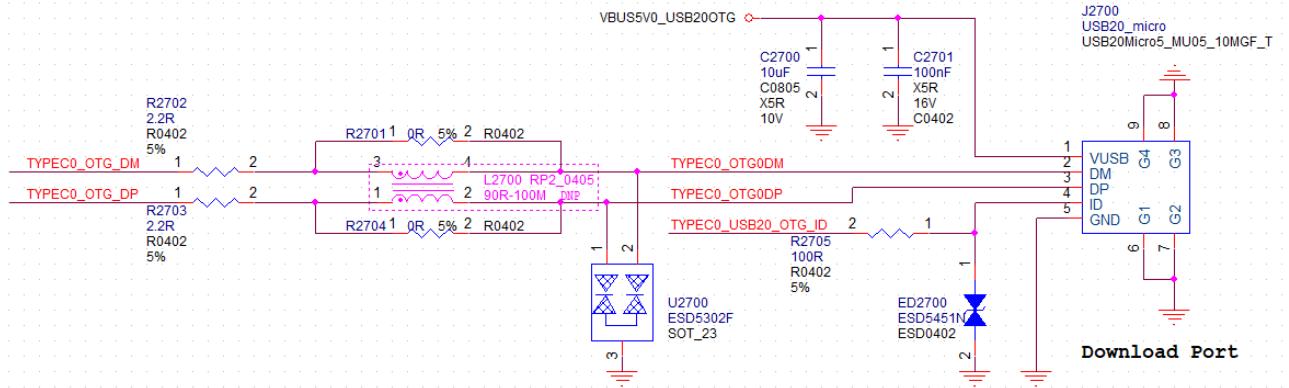


Figure 2-90 USB2.0 Signal Serial Connection Common Mode Inductance Circuit

If the TYPEC_USB20_OTG0/1_ID signal is used, in order to strengthen the anti-static and surge capability, an ESD device must be reserved on the signal, and a 100ohm resistor must be connected in series, and must not be deleted, see the figure below:

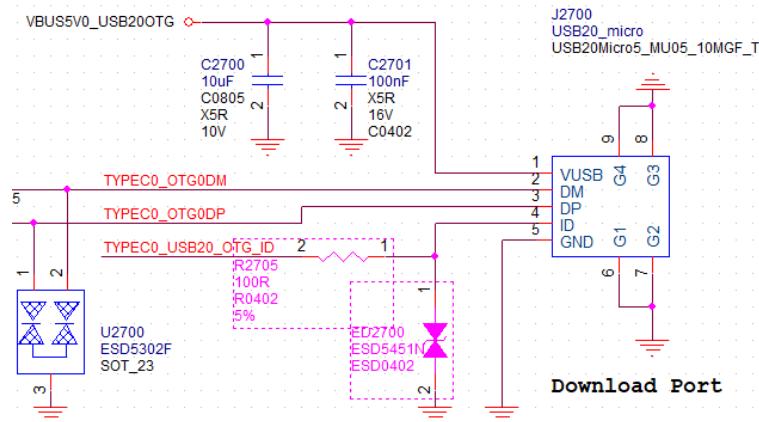


Figure 2-91 TYPEC_USB20_OTG0/1_ID Pin Circuit

When the HOST function is used, it is recommended to add a current limit switch to the 5V power supply. The current limit value can be adjusted according to the application needs. The current limit switch is controlled by 3.3V GPIO. Hard disk, Jianyi filter increases the capacitance to more than 100uF.

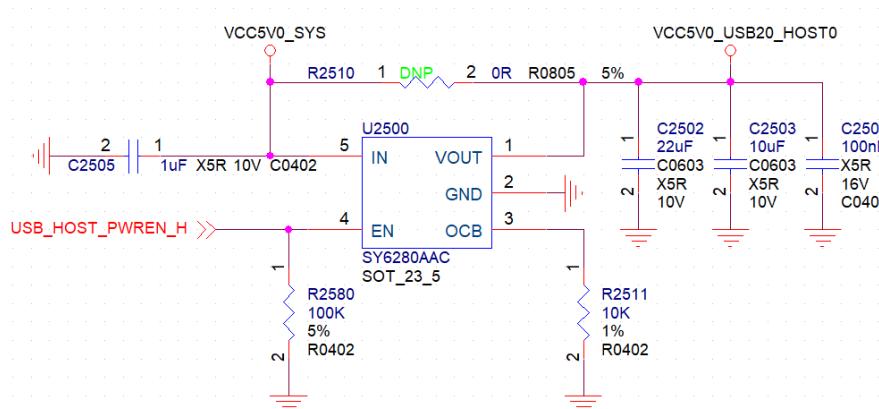


Figure 2-92 USB 5V Current –Limiting Circuit

The USB3.0 protocol requires a 100nF AC coupling capacitor to be added to the SSTXP/N line. The AC coupling capacitor is recommended to be packaged in 0201, with lower ESR and ESL, which can also reduce the impedance change on the line.

ESD devices must be added to all signals of the TYPEC socket and placed close to the USB connector during layout. For SSTXP/N, SSRXP/N signals, the ESD parasitic capacitance must not exceed 0.3pF.

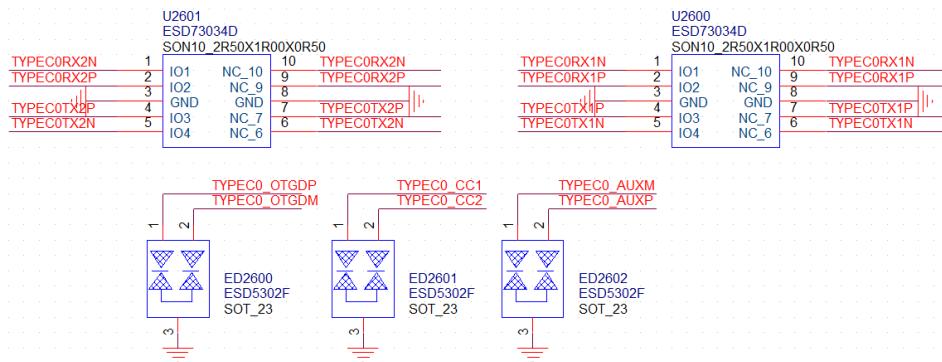


Figure 2-93 TYPEC Socket ESD Circuit

USB2.0/USB3.0 interface matching design recommendations are shown in the following Table:

Table 2-16 RK3588 USB2.0/USB3.0 Interface Design

Signal	Connection mode	Description
TYPEC0_USB20_OTG_DP/DM	Connect 2.2ohm resistor in series	data input and output in USB HS/FS/LS mode
TYPEC_SSTXP/SSTXN	Connect a 100nF capacitor in series (0201 package is recommended)	data output in USB SS mode
TYPEC_SSRXP/SSRXN	Connect 0ohm resistor in series	data input in USB SS mode
TYPEC_USB20_OTG_ID	Connect a 100ohm resistor in series (To pull up externally, the pull-up power supply needs to be connected to the same power supply as USB20_AVDD_1V8)	USB OTG ID recognition, required for Micro-USB interface
TYPEC_USB20_VBUSDET	Resistance voltage-dividing detection	USB OTG insertion detection
USB30_2_SSTXP/SSTXN	Connect a 100nF capacitor in series (0201 package is recommended)	data output in USB SS mode
USB30_2_SSRXP/SSRXN	Connect 0ohm resistor in series	data input in USB SS mode
HOST0_DP/DM	Connect 2.2ohm resistor in series	data input and output in USB HS/FS/LS mode
HOST1_DP/DM	Connect 2.2ohm resistor in series	data input and output in USB HS/FS/LS mode

2.3.5 SATA3.0 Circuit

RK3588 has 3 SATA3.0 controller, which reuse PIPE PHY0/1/2 with PCIe and USB3_HOST2 controllers. Please refer to the figure below for the specific path.

- Support SATA PM function, each port can support 5 devices;
- Support SATA 1.5Gb/s, SATA 3.0Gb/s, SATA 6.0Gb/s
- Support eSATA.

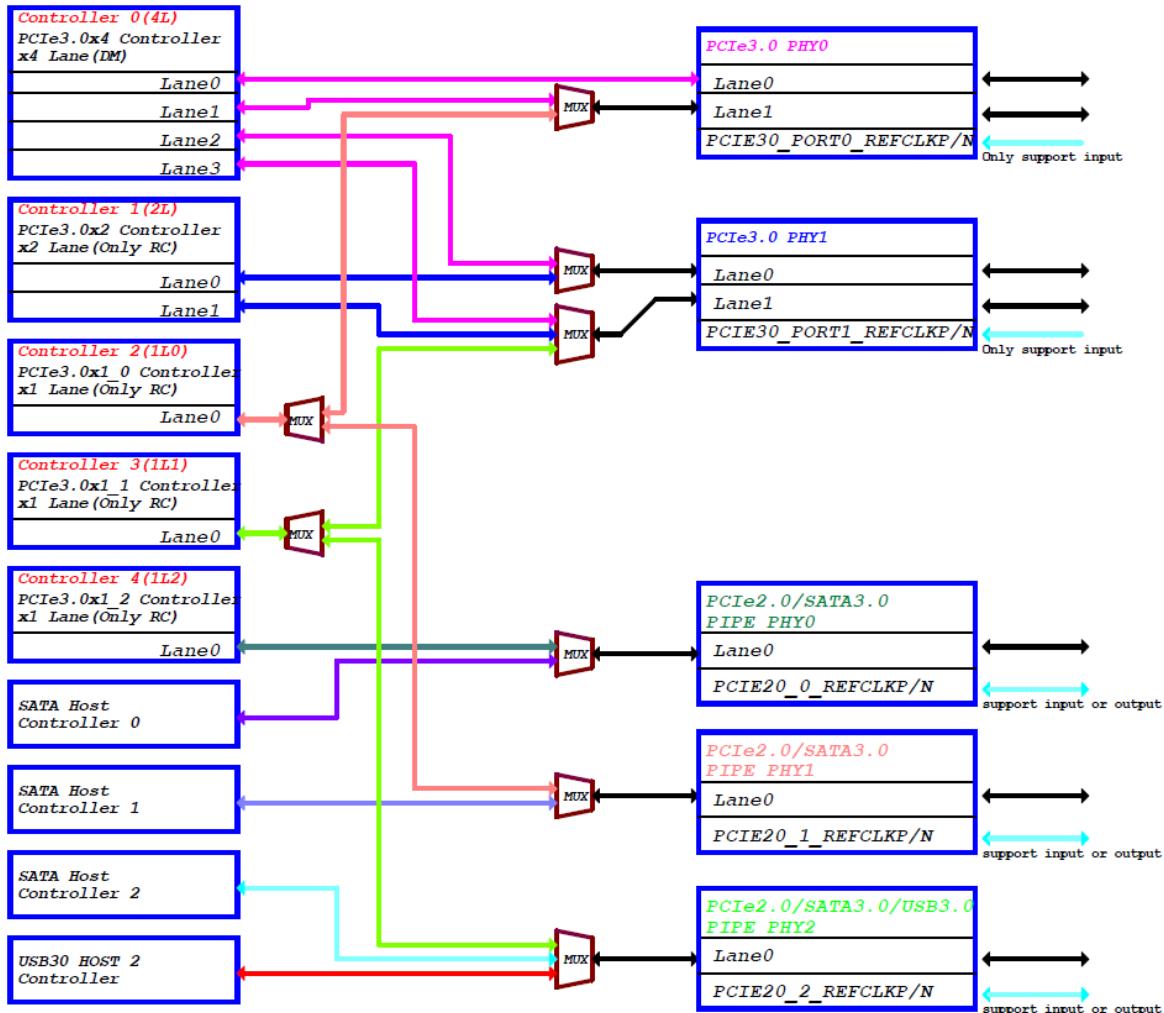
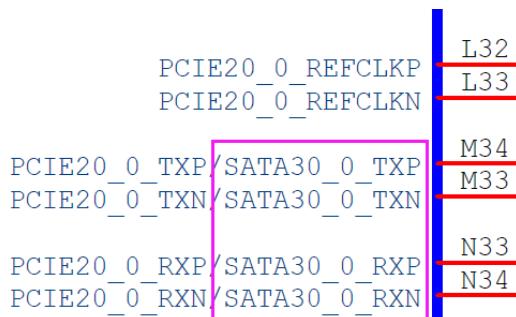
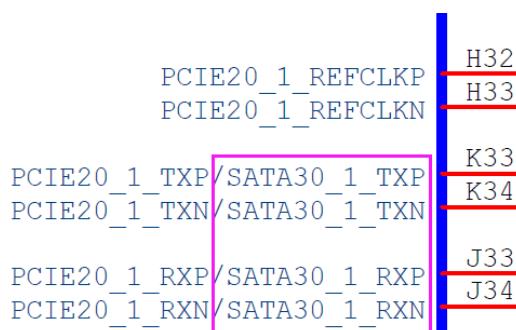


Figure 2-94 PIPE_PHY0/1/2 and SATA3.0 Controller Multiplexing Relationship

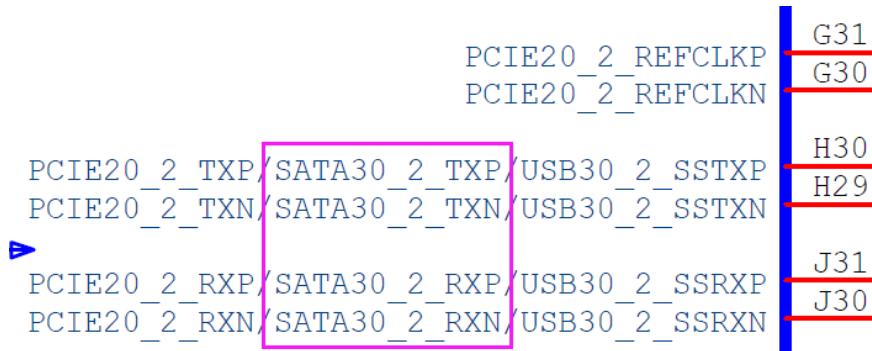
SATA0 controller use PIPE_PHY0 (Multiplexing with PCIe2.0x1_2 Controller).



SATA1 controller use PIPE_PHY1 (Multiplexing with PCIe2.0x1_0 Controller).



SATA2 controller with PIPE_PHY2 (Multiplexing with PCIe2.0x1_1 Controller and USB30 HOST2 Controller).



SATA0/1/2 controller related control IO has:

- SATA0_ACT_LED: LED blinking control output when SATA0 interface has data transmission;
- SATA1_ACT_LED: LED blinking control output when SATA1 interface has data transmission;
- SATA2_ACT_LED: LED blinking control output when SATA2 interface has data transmission;
- SATA_CP_DET: SATA hot-swappable device plug detection input;
- SATA_MP_SWITCH: SATA hot-swappable device switch detection input;
- SATA_CP POD: SATA hot-swappable device power switch output;
- SATA_CP_DET, SATA_MP_SWITCH, and SATA_CP POD are SATA0/1/2 common interfaces, which can be configured through registers to be SATA0, SATA1 or SATA2, in the PMUIO2 power domain;
- SATA0_ACT_LED, SATA1_ACT_LED, and SATA2_ACT_LED are multiplexed in two positions, one in the VCCIO6 power domain and one in the VCCIO4 power domain.

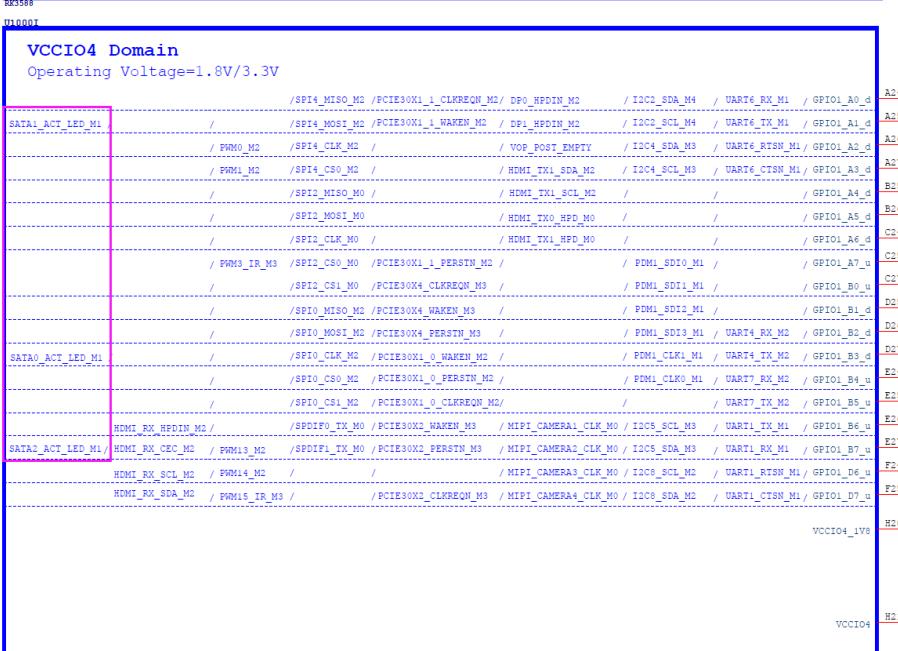
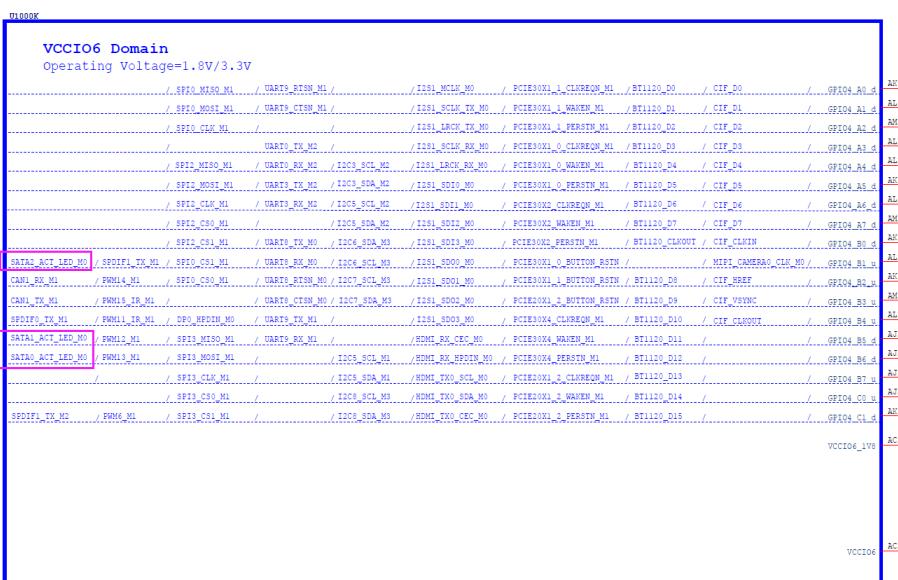
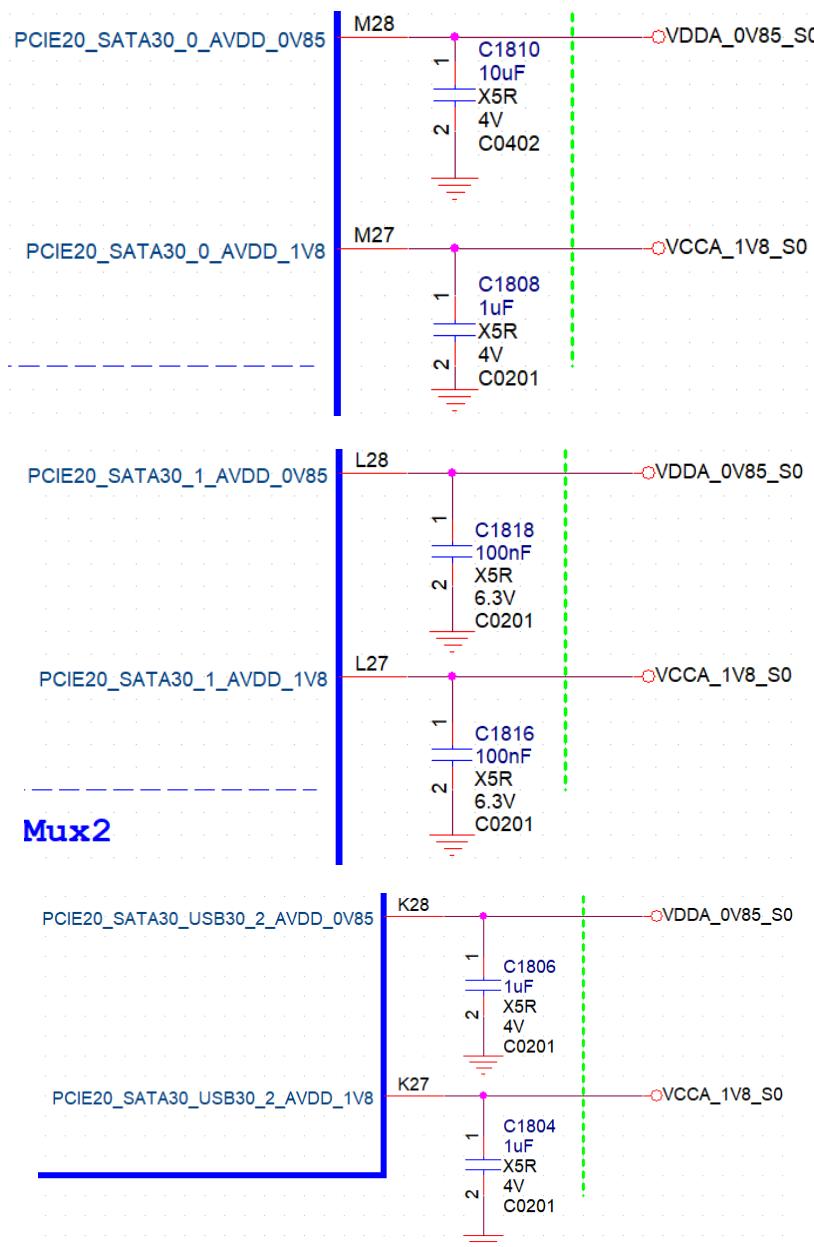


Figure 2-95 SATA0/1/2 Related Control IO Pins

Please pay attention to SATA design:

- During Slot design, Peripheral circuit and power supply need to meet Spec requirements;
- PCIE20_SATA30_0/1_AVDD_0V85/PCIE20_SATA30_USB30_2_AVDD_0V85 three-way combined power supply, need to place 1x10uF+1x1uF+1x100nF decoupling capacitors, and place them close to the RK3588 pins during layout.
- PCIE20_SATA30_0/1_AVDD_1V8/PCIE20_SATA30_USB30_2_AVDD_1V8 three-way combined power supply, need to place 2x1uF+1x100nF decoupling capacitors, and place them close to the RK3588 pins during layout.



- 10nF AC coupling capacitors connected in series on the TXP/N, RXP/N differential signals of the SATA interface. It is recommended to use the 0201 package for the AC coupling capacitors. Lower ESR and ESL can also reduce the impedance change on the line;
- All signals of the eSATA interface socket must be added with ESD devices, placed close to the socket during layout, and the ESD parasitic capacitance must not exceed 0.4pF;

- SATA interface matching design recommendations are shown in the following table:

Table 2-17 RK3588 SATA Interface Design

Signal	Connection mode	Description
SATA30_0_TXP/TXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data output
SATA30_0_RXP/RXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data input
SATA30_1_TXP/TXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data output
SATA30_1_RXP/RXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data input
SATA30_2_TXP/TXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data output
SATA30_2_RXP/RXN	Connect a 10nF capacitor in series (0201 package is recommended)	SATA data input

2.3.6 PCIe2.0 and PCIe3.0 Circuit

RK3588 has 5 PCIe3.0 controllers: (DM: Dual Mode, RC: Root Complex)

- Controller 0(4L), PCIe3.0x4 Controller x4 Lane (DM)
- Controller 1(2L), PCIe3.0x2 Controller x2 Lane (Only RC)
- Controller 2(1L0), PCIe3.0x1_0 Controller x1 Lane (Only RC)
- Controller 3(1L1), PCIe3.0x1_1 Controller x1 Lane (Only RC)
- Controller 4(1L2), PCIe3.0x1_2 Controller x1 Lane (Only RC)

2 PCIe3.0 PHY, data bit 2Lane, PCIe3.0 PHY0 and PCIe3.0 PHY1.

3 PCIe2.0 Combo PHY, data bit 1Lane, PCIe2.0/SATA3.0 Combo PHY0, PCIe2.0/SATA3.0 Combo PHY1 and PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2.

The mapping relationship between Controller and PHY as follow:

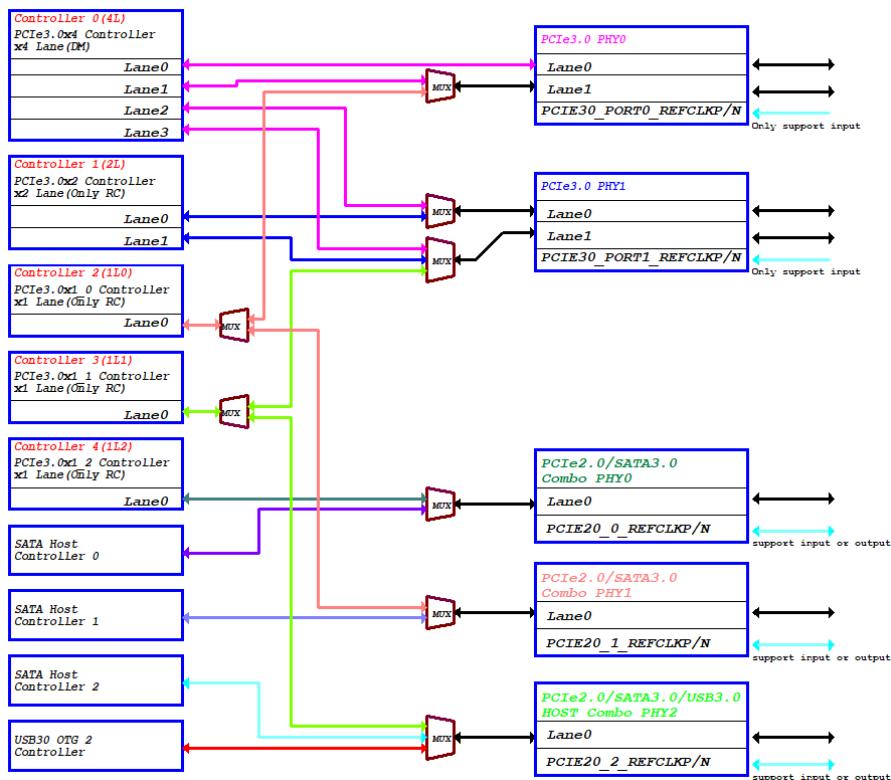


Figure 2-96 RK3588 PCIe 5 Controller and 5 PHY Mapping Relationship Diagram

- Controller 0(4L) Lane0 can only be combined with PCIe3.0 PHY0 Lane0;
- Controller 1(2L) Lane0 can only be combined with PCIe3.0 PHY1 Lane0;
- Controller 1(2L) + PCIe3.0 PHY1, form PCIe3.0 X2Lane RC mode of 2Lane. Compatible with PCIe3.0 X1Lane RC mode;

RK3588 PCIE Signal		PCIe3.0 X2Lane RC	PCIe3.0 X1Lane RC
Port1	PCIE30_PORT1_TX0P/N	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
	PCIE30_PORT1_RX0P/N	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
	PCIE30_PORT1_TX1P/N	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT1_RX1P/N	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT1_REFCLKP/N_IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

- Controller 0(4L) + PCIe3.0 PHY0 + PCIe3.0 PHY1, form PCIe3.0 X4Lane RC or EP mode of 4Lane. Compatible with PCIe3.0 X2Lane RC or EP mode, compatible with PCIe3.0 X1Lane RC or EP mode;

RK3588 PCIE Signal		PCIe3.0 X4Lane RC or EP	PCIe3.0 X2Lane RC or EP	PCIe3.0 X1Lane RC or EP
Port0	PCIE30_PORT0_TX0P/N	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
	PCIE30_PORT0_RX0P/N	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
	PCIE30_PORT0_TX1P/N	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT0_RX1P/N	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT0_REFCLKP/N_IN	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
Port1	PCIE30_PORT1_TX0P/N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT1_RX0P/N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT1_TX1P/N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT1_RX1P/N	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
	PCIE30_PORT1_REFCLKP/N_IN	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

- Controller 4(1L2))+ PCIe2.0/SATA3.0 Combo PHY0, form PCIe2.0 X1Lane RC mode of 1Lane;
 - The corresponding signals in this mode are:

RK3588 PCIE Signal		PCIe2.0 X1Lane RC
PCIe2.0/SATA3.0 Combo PHY0	PCIE20_0_TXP/N	<input checked="" type="checkbox"/>
	PCIE20_0_RXP/N	<input checked="" type="checkbox"/>
	PCIE20_0_REFCLKP/N	<input checked="" type="checkbox"/>

- Controller 2(1L0) + Lane1 of PCIe3.0 PHY0 form PCIe3.0 X1Lane RC of 1Lane, or Controller 2(1L0) + PCIe2.0/SATA3.0 Combo PHY1 form PCIe2.0 X1Lane RC, so these two modes cannot be used simultaneously;
 - The corresponding signals of PCIe3.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe3.0 X1Lane RC
Port0	PCIE30_PORT0_TX1P/N	<input checked="" type="checkbox"/>
	PCIE30_PORT0_RX1P/N	<input checked="" type="checkbox"/>
	PCIE30_PORT0_REFCLKP/N_IN	<input checked="" type="checkbox"/>

- The corresponding signals of PCIe2.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe2.0 X1Lane RC
PCIe2.0/SATA3.0 Combo PHY1	PCIE20_1_TXP/N	<input checked="" type="checkbox"/>
	PCIE20_1_RXP/N	<input checked="" type="checkbox"/>
	PCIE20_1_REFCLKP/N	<input checked="" type="checkbox"/>

- Controller 3(1L1) + Lane1 of PCIe3.0 PHY1 form PCIe3.0 X1Lane RC mode of 1Lane, or Controller 3(1L1) + PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2 form PCIe2.0 X1Lane RC mode, so the two modes cannot be used at the same time.

- The corresponding signals of PCIe3.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe3.0 X1Lane RC
Port1	PCIE30_PORT1_TXP/N	<input checked="" type="checkbox"/>
	PCIE30_PORT1_RXP/N	<input checked="" type="checkbox"/>
	PCIE30_PORT1_REFCLKP/N_IN	<input checked="" type="checkbox"/>

- The corresponding signals of PCIe2.0 X1Lane RC mode in this mode are:

RK3588 PCIE Signal		PCIe2.0 X1Lane RC
PCIe2.0/SATA3.0/USB HOST Combo PHY2	PCIE20_2_TXP/N	<input checked="" type="checkbox"/>
	PCIE20_2_RXP/N	<input checked="" type="checkbox"/>
	PCIE20_2_REFCLKP/N	<input checked="" type="checkbox"/>

Based on the above description, it can support multiple modes, so if all PCIe functions are used, RK3588 can support a combination of multiple PCIe modes, and up to 5 modes can be used at the same time.

eg1: 1 x PCIe3.0 X4Lane RC or EP
+ 3 x PCIe2.0 X1Lane RC

PCIe3.0 x4Lane	Controller 0 (4L) RC or EP	PCIe3.0 PHY0 Lane0+Lane1 + PCIe3.0 PHY1 Lane0+Lane1
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 Combo PHY0
+ PCIe2.0 x1Lane	Controller 2 (1L0) RC	PCIe2.0/SATA3.0 Combo PHY1
+ PCIe2.0 x1Lane	Controller 3 (1L1) RC	PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2

eg2: 1 x PCIe3.0 X2Lane RC or EP
+ 1 x PCIe3.0 X2Lane RC
+ 3 x PCIe2.0 X1Lane RC

PCIe3.0 x2Lane	Controller 0 (4L) RC or EP	PCIe3.0 PHY0 Lane0+Lane1
+ PCIe3.0 x1Lane	Controller 1 (2L) RC	PCIe3.0 PHY1 Lane0
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 Combo PHY0
+ PCIe2.0 x1Lane	Controller 2 (1L0) RC	PCIe2.0/SATA3.0 Combo PHY1
+ PCIe2.0 x1Lane	Controller 3 (1L1) RC	PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2

eg3: 1 x PCIe3.0 X2Lane RC or EP
+ 1 x PCIe3.0 X1Lane RC
+ 3 x PCIe2.0 X1Lane RC

PCIe3.0 x2Lane	Controller 0 (4L) RC or EP	PCIe3.0 PHY0 Lane0+Lane1
+ PCIe3.0 x1Lane	Controller 1 (2L) RC	PCIe3.0 PHY1 Lane0
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 Combo PHY0
+ PCIe2.0 x1Lane	Controller 2 (1L0) RC	PCIe2.0/SATA3.0 Combo PHY1
+ PCIe2.0 x1Lane	Controller 3 (1L1) RC	PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2

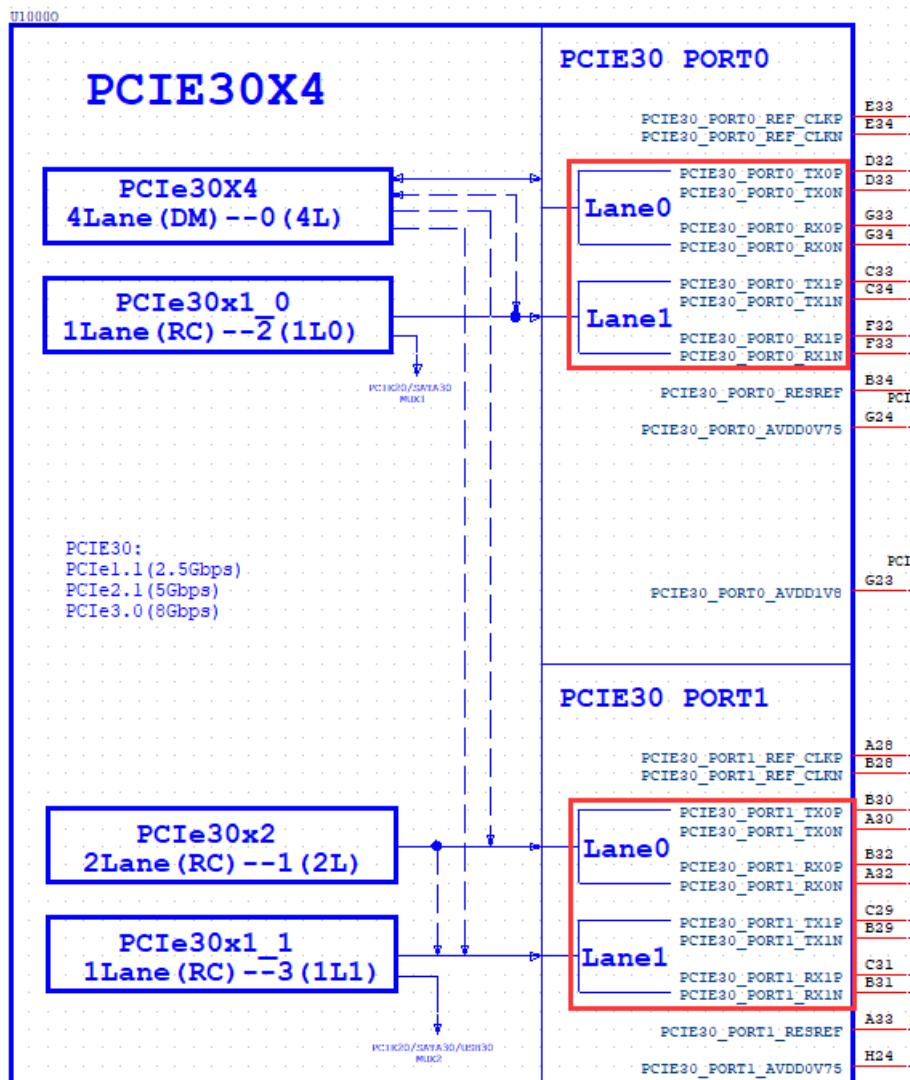
eg4: 4 x PCIe3.0 X1Lane RC
+ 1 x PCIe2.0 X1Lane RC

PCIe3.0 x1Lane	Controller 0 (4L) RC	PCIe3.0 PHY0 Lane0
+ PCIe3.0 x1Lane	Controller 2 (1L0) RC	PCIe3.0 PHY0 Lane1
+ PCIe3.0 x1Lane	Controller 1 (2L) RC	PCIe3.0 PHY1 Lane0
+ PCIe3.0 x1Lane	Controller 3 (1L1) RC	PCIe3.0 PHY1 Lane1
+ PCIe2.0 x1Lane	Controller 4 (1L2) RC	PCIe2.0/SATA3.0 HOST Combo PHY0

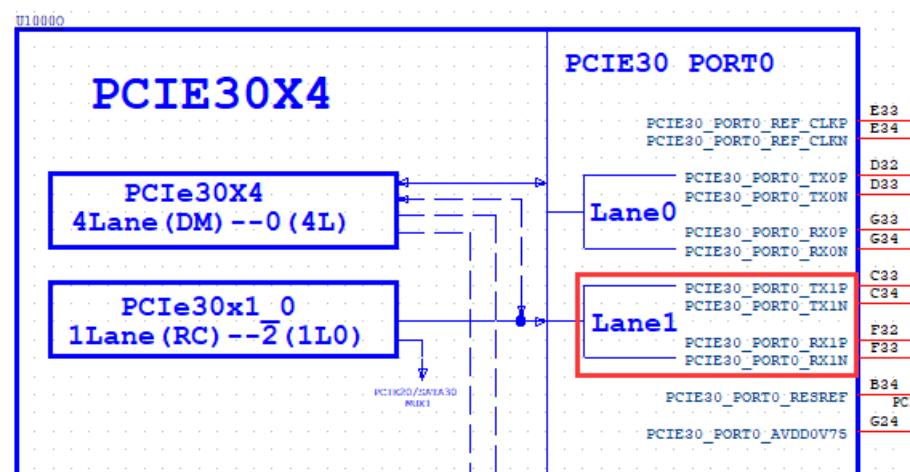
Figure 2-97 RK3588 PCIe Multiple Mode Combination Diagram

The combination of PCIe Controller and PHY is reflected on the schematic module as follows:

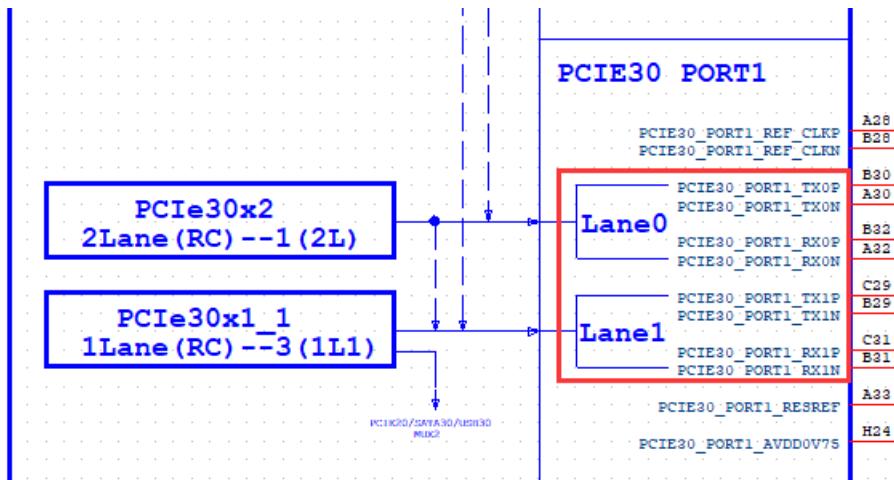
- PCIe3.0 controller Controller 0 (4L) can use PCIe3.0 PHY0 and PCIe3.0 PHY1;



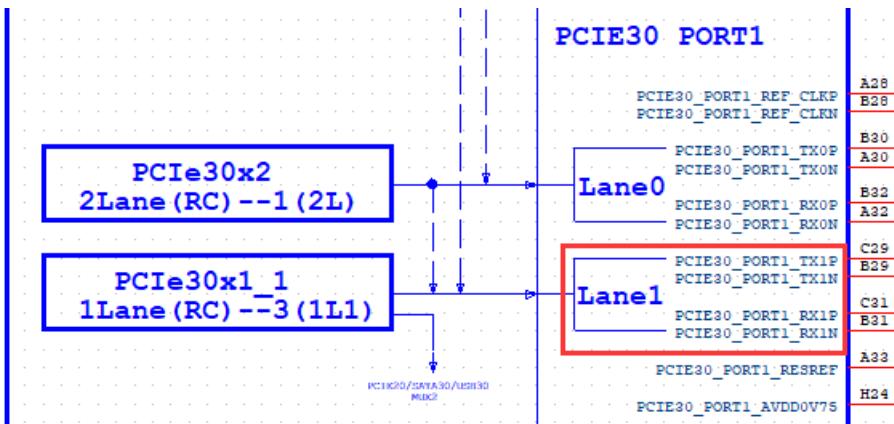
- PCIe3.0 Controller 2(1L0) can use PCIe3.0 PHY0 Lane1 channel;



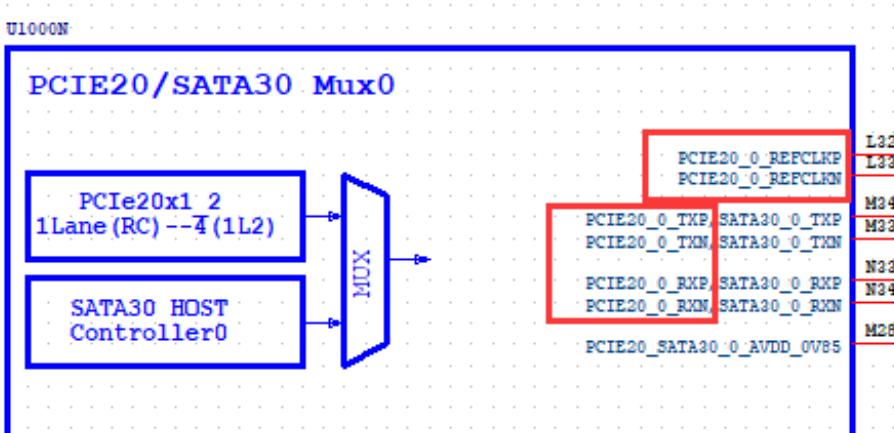
- PCIe3.0 Controller 1(2L) can use PCIe3.0 PHY1;



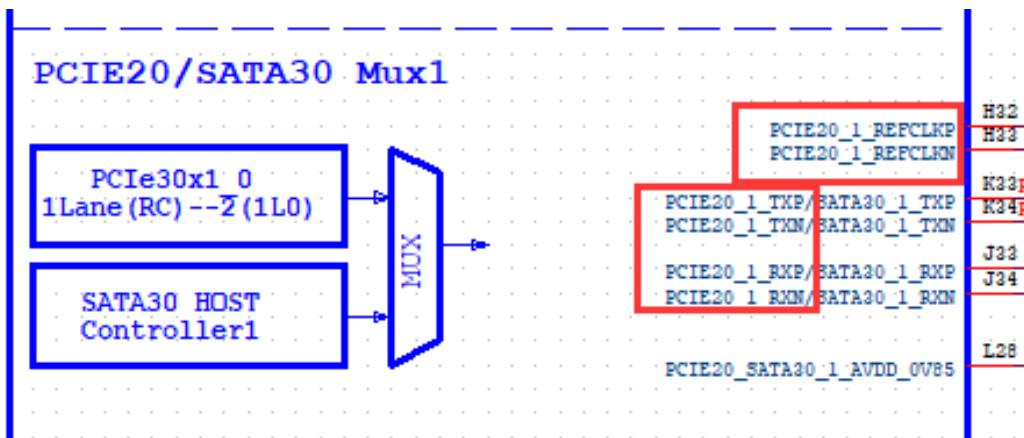
- PCIe3.0 Controller 3(1L1) can use Lane1 of PCIe3.0 PHY1;



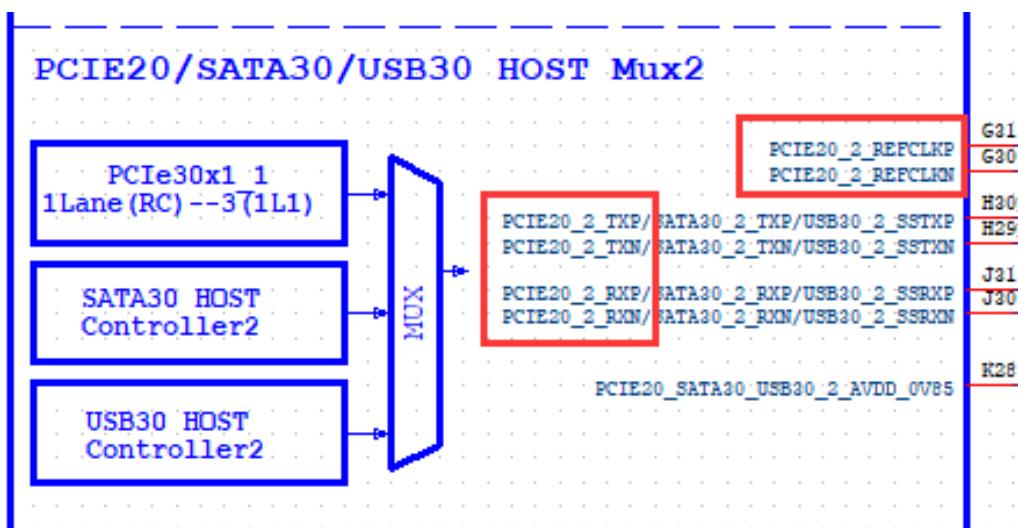
- PCIe3.0 Controller 4(1L2) use PCIe2.0/SATA3.0 Combo PHY0, multiplexed with SATA30 HOST Controller0;



- PCIe3.0 Controller 2(1L0) use PCIe2.0/SATA3.0 Combo PHY1, multiplexed with SATA30 HOST Controller1;



- PCIe3.0 Controller 3(1L1) use PCIe2.0/SATA3.0/USB3.0 HOST Combo PHY2, multiplexed with SATA30 HOST Controller2, USB30 OTG Controller2.



PCIE20_REFCLKP/N supports input and output, and output to EP device by default.

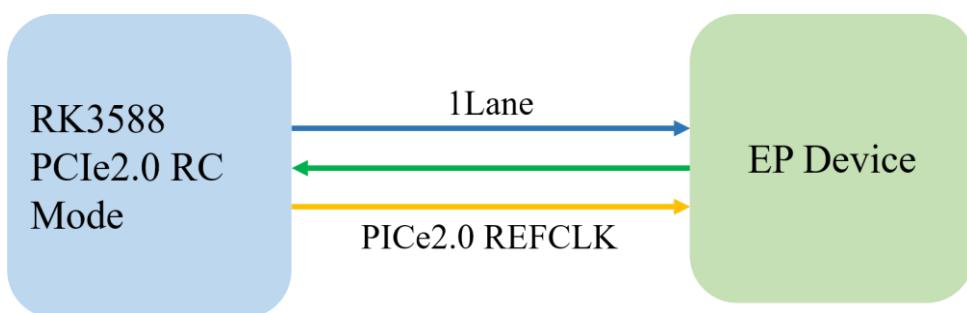


Figure 2-98 RK3588 Reference Clock Path Diagram in PCIe2.0 RC Mode

Please note the following items in PCIe2.0 design:

- When designing a slot, the peripheral circuit and power supply need to meet the Spec requirements;
- A 100nF AC coupling capacitor connected in series on the TXP/N differential signal of the PCIe2.0 interface, the AC coupling capacitor is recommended to use 0201 package, lower ESR and ESL, and can

also reduce the impedance change on the line;

- PCIE2.0_CLKREQn and PCIE20_WAKEEn must use function pins and cannot be replaced by GPIO. Special instructions: when selecting, you must select _M0 or _M1 or _M2, not one _M0 and one _M1;
- PCIE20_PERSTn can select function pins or GPIO instead. When selecting function pins, it must be the same group of _Mx as PCIE20_CLKREQn and PCIE20_WAKEEn;
- Standard PCIe Slot: PCIE20_CLKREQn, PCIE20_WAKEEn, PCIE20_PERSTn are 3.3V level;
- PCIE20_PRSNT is the Add In Card insertion detection pin, which can use GPIO;
- When using the PCIE20 function, the multiplexed SATA/USB30 function cannot be used, and the function module corresponding to SATA/USB30 is explained;
- The PCIe2.0 function module is not used, the data lines PCIE20_TXP/TXN, PCIE20_RXP/RXN and the reference clock line PCIE20_REFCLKP/REFCLKN can be left floating;
- The PCIe2.0 interface matching design recommendations are shown in the following table:

Table 2-18 RK3588 PCIe2.0 Interface Design

Signal	Connection mode	Description
PCIE20_0/1/2_TXP/TXN	Connect a 22ohm resistor in series (the 0201 package is recommended)	PCIe data output
PCIE20_0/1/2_RXP/RXN	Direct connection	PCIe data input
PCIE20_0/1/2_REFCLKP/CLKN	Direct connection	PCIe reference clock
PCIE20_CLKREQn	Connect a 0ohm resistor in series	PCIe reference clock request input (RC mode)
PCIE20_WAKEEn	Connect a 0ohm resistor in series	PCIe wake-up input(RC mode)
PCIE20_PERSTn	Connect a 0ohm resistor in series	PCIe global reset output(RC mode)
PCIE20_PRSNT	Connect a 0ohm resistor in series	Add In Card insert test input (RC mode)

PCIE30_REFCLKP/N only supports input:

- Need to provide HCSL level clock input;
- Must provide a clock that meets PCIe3.0 or higher requirements;
- RK3588 PCIe3.0 X4Lane RC mode. Compatible with PCIe3.0 X2Lane RC mode and compatible with PCIe3.0 X1Lane RC mode. The reference clock path is as follows:

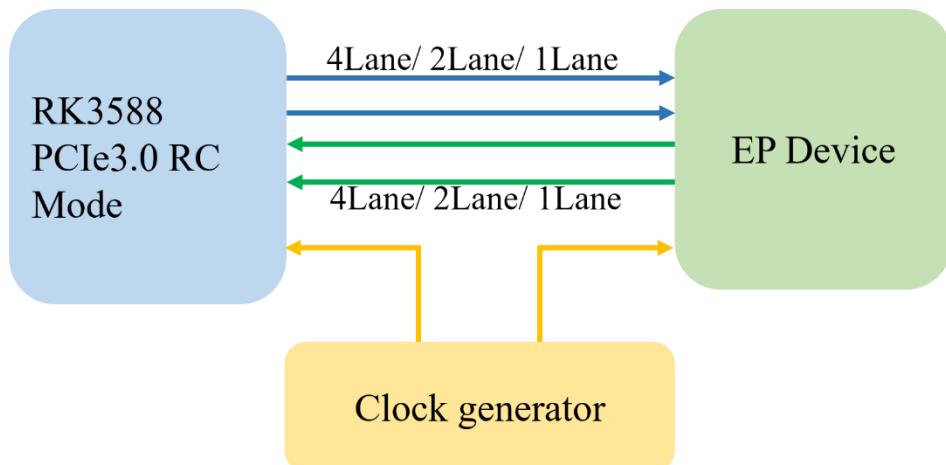


Figure 2-99 RK3588 Reference Clock Path in PCIe3.0 RC Mode

- In another case, if two RK3588 are cascaded, it is means the EP device in the above picture is also RK3588. The reference clock path is the same, data Lane TX is connected to RX, and RX is connected to TX;

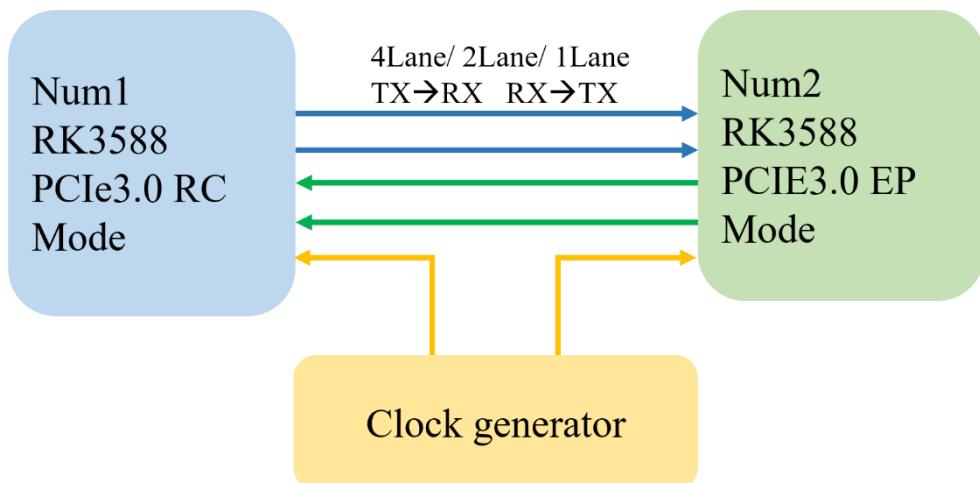


Figure 2-100 Reference Clock Path Diagram in RK3588 PCIe3.0 Cascade Docking Mode

- RK3588 PCIe3.0 x4 Lane EP mode, compatible with PCIe3.0 X2Lane EP mode, and compatible with PCIe3.0 X1Lane EO mode. The reference clock path is as follows:

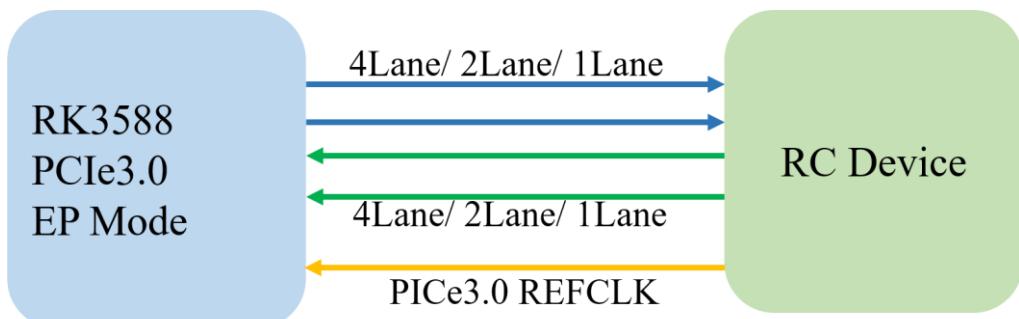


Figure 2-101 Reference Clock Path Diagram in RK3588 PCIe3.0 EP Mode

Please note the following items in PCIe3.0 design:

- In the design of slot, peripheral circuit and power supply should meet the requirements of Spec;
- A 220nF AC coupling capacitor connected in series to the TXP0P/N, TX1P/N differential signal of the PCIe3.0 interface. It is recommended to use the 0201 package for the AC coupling capacitor to obtain lower ESR and ESL and reduce impedance changes on the line;
- PCIE_RESREF is the external reference resistor pin of PCIe3.0 PHY. It is connected to an external 200ohm 1% resistor to the ground. The resistance value can not be changed. Place it close to the RK3588 chip pin during layout;

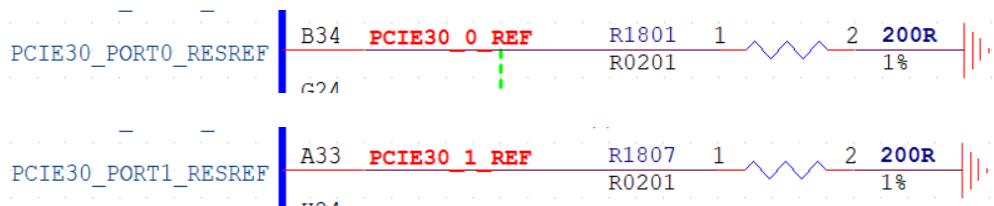


Figure 2-102 PCIe3.0 PHY RESREF Pin

- The corresponding relationship between PCIE30_CLKREQn, PCIE30_WAKEn, PCIE30_PERSTn, PCIE30X4_BUTTON_RSTN control signals and the controller is shown in the figure below

PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_TXX PCIE20_1_RXP PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_TXX PCIE20_2_RXP PCIE20_2_RXN	
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_TXX PCIE20_0_RXP PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:

PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

Note:

M*=Mean to M0 or M1, It's the same source, Just multiplex to M0 or M1, So, Only use one at the same time.

Figure 2-103 Matching Relationship between PCIe Controller and Control Signal

Table 2-19 PCIe Control Signal Multiplexing Situation and Corresponding Power Domain Distribution

PCIe control signal	Reuse	Multiplex power domain
PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M*	M0,M1,M2,M3	M0: PMUIO2 M1: VCCIO6 M2: VCCIO5 M3: VCCIO4
PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M*	M0,M1,M2,M3	M0: PMUIO2 M1: VCCIO6 M2: VCCIO5 M3: VCCIO4
PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M*	M0,M1,M2	M0: PMUIO2 M1: VCCIO6 M2: VCCIO4
PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M*	M0,M1,M2	M0: PMUIO2 M1: VCCIO6 M2: VCCIO4
PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M*	M0,M1	M0: VCCIO5 M1: VCCIO6

The distribution on the schematic is as follows:

- There are 4 IOMUX on the PMUIO2 power domain:

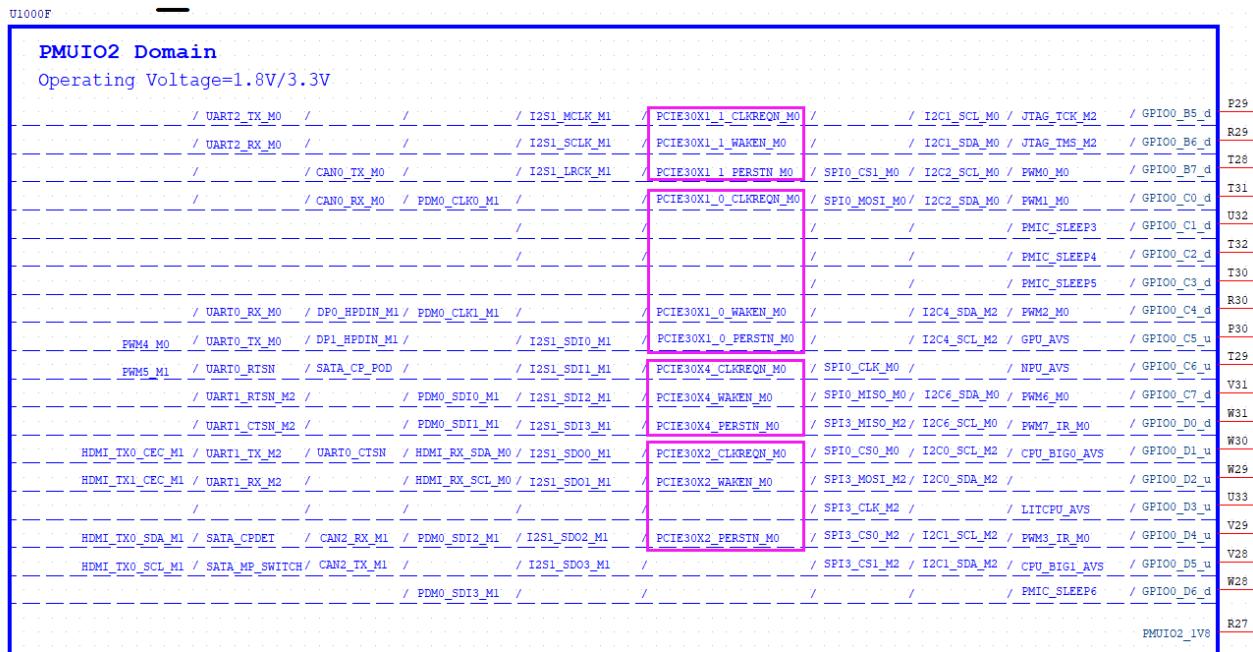


Figure 2-104 PCIE Control Signal Pin on PMUIO2

- There are 5 IOMUX on the VCCIO6 power domain:

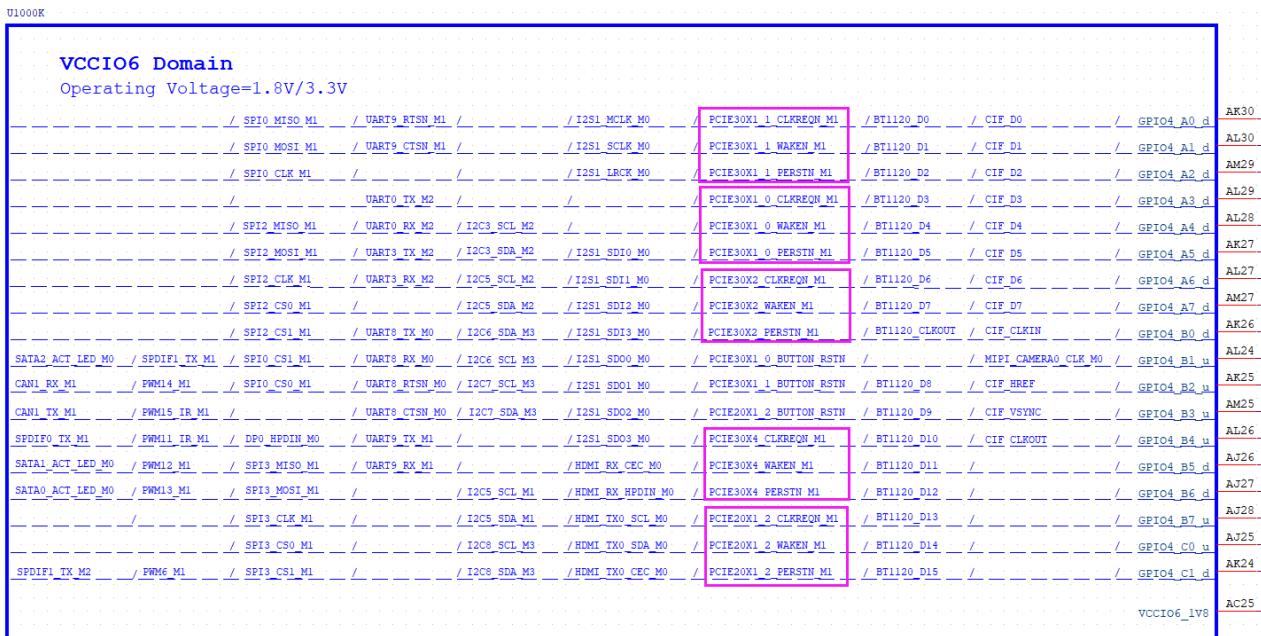


Figure 2-105 PCIE Control Signal Pin on VCCIO6

- There are 3 IOMUX on the VCCIO5 power domain:

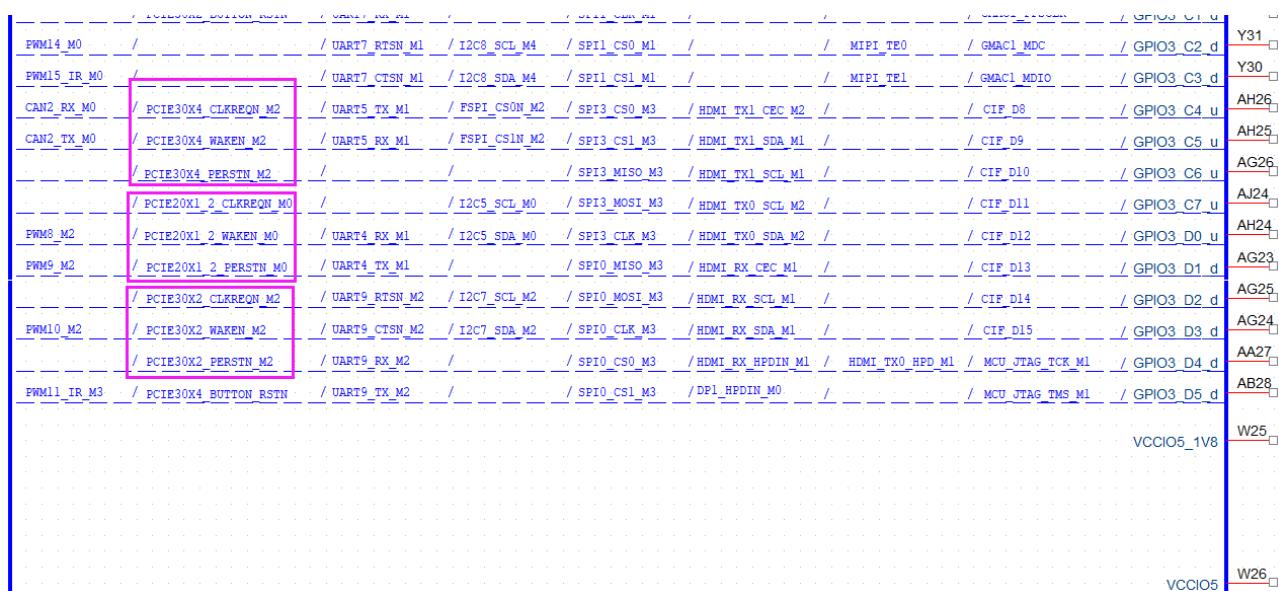


Figure 2-106 PCIE Control Signal Pin on VCCIO5

- There are 4 IOMUX on the VCCIO4 power domain:

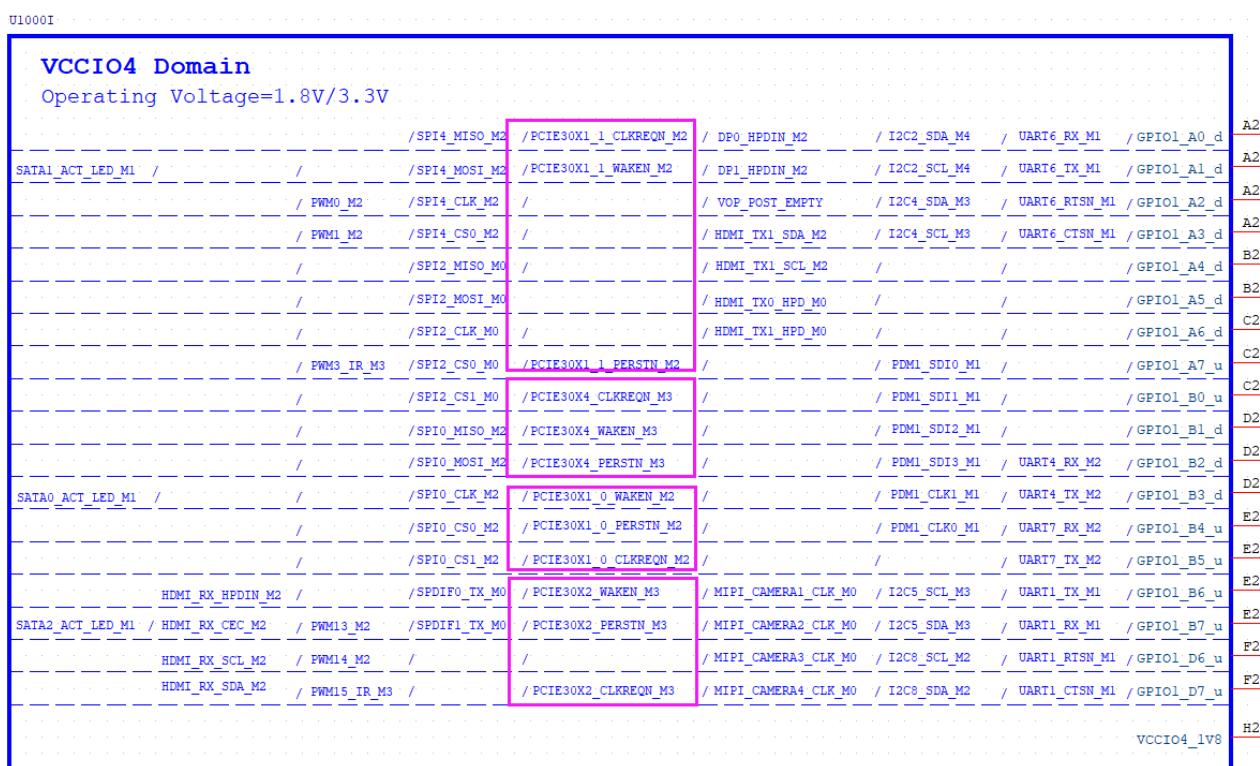


Figure 2-107 PCIE Control Signal Pin on VCCIO4

- PCIE30_CLKREQn and PCIE30_WAKEn must use function pins and cannot be replaced by GPIO. Special instructions: when selecting, you must select _M0 or _M1 or _M2, not one _M0 and one _M1;
 - PCIE30_PERSTn can select function pins or GPIO instead. When selecting function pins, it must be the same group of Mx as PCIE30_CLKREQn and PCIE30_WAKEn;

- Standard PCIe Slot: PCIE30X2_CLKREQn, PCIE30X1_WAKEn, PCIE30_PERSTn are 3.3V level;
- PCIE30_PRSNT is the Add In Card insertion detection pin, which can use GPIO;
- PCIE30_BUTTON_RSTN is the reset of the external hardware, reserved for use;
- 2 RK3588 PCIe are connected in cascade, and the data lines are cross-connected, namely TX→RX, RX→TX. The control signals PCIE30_CLKREQn and PCIE30_PERSTn are connected in one-to-one correspondence (for example: Num1 and Num2 represent two RK3588,
- Num1_PCIE30_CLKREQn connects to Num2_PCIE30_CLKREQn, and Num1_PCIE30_PERSTn connects to Num2_PCIE30_PERSTn). The three signals PCIE30_WAKEn, PCIE30_PRSNT and PCIE30_BUTTON_RSTN can be left floating;
- The PCIe30 function module is not used, the data lines PCIE30_TXP/TXN, PCIE30_RXP/RXN are floating, and the reference clock line PCIE30_REFCLKP/REFCLKN is grounded or floating;
- The REFCLKP/N of PCIe30 PHY and Slot peripheral must meet the same-source clock requirement. For example, the PHY0/PHY1 and Slot three-way REFCLKP/N of the reference design are output by the same clock generator.
- The PCIe3.0 interface matching design recommendations are shown in the following table:

Table 2-20 RK3588 PCIe3.0 Interface Design

Signal	Connection mode	Description
PCIE30_TX0P/TX0N	Connect a 22ohm resistor in series (the 0201 package is recommended)	PCIe data output
PCIE30_RX0P/RX0N	Direct connection	PCIe data input
PCIE30_TX1P/TX1N	Connect a 22ohm resistor in series (the 0201 package is recommended)	PCIe data output
PCIE30_RX1P/RX1N	Direct connection	PCIe data input
PCIE30_REFCLKP_IN/ PCIE30_REFCLKN_IN	Direct connection	PCIe reference clock input
PCIE30_RESREF	Grounding with 200 Ω/1% resistance	External reference resistor of PCIe3.0 PHY
PCIE30_CLKREQn	Connect a 0ohm resistor in series	PCIe reference clock request input (RC mode) PCIe reference clock request output (EP mode)
PCIE30_WAKEn	Connect a 0ohm resistor in series	PCIe wake-up input (RC mode) PCIe wake-up output (EP mode)
PCIE30_PERSTn	Connect a 0ohm resistor in series	PCIe global reset output (RC mode) PCIe global reset input (EP mode)
PCIE30_PRSNT	Connect a 0ohm resistor in series	‘Add In Card’-insert test input (RC mode)
PCIE30_BUTTON_RSTN	Connect a 0ohm resistor in series	PCIe external hardware reset output (RC mode) PCIe external hardware reset intput (EP mode)

2.3.7 Video Input Interface Circuit

2.3.7.1 MIPI DPHY CSI RX Interface (**This interface is preferred**)

RK3588 has two MIPI DPHY CSI RX, both support MIPI V1.2, and the maximum data transmission rate of each channel is 2.5Gbps.

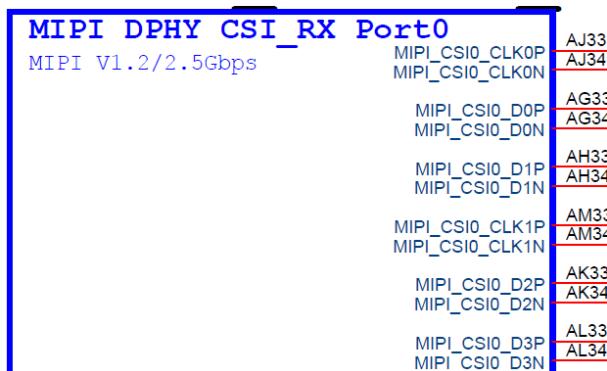


Figure 2-108 RK3588 MIPI CSI0 RX Signal Pin

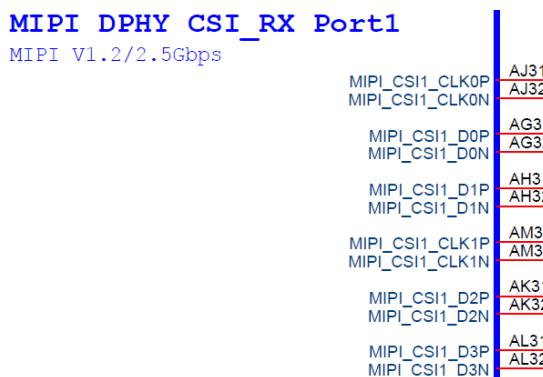


Figure 2-109 RK3588 MIPI CSI1 RX Signal Pin

MIPI CSI0 RX interface mode support:

- Support x4Lane mode, MIPI_CSI0_D[3:0] data refer to MIPI_CSI0_CLK0;
- Support x2Lane+x2Lane mode:
 - MIPI0_CSI_D[1:0] data refer to MIPI_CSI0_CLK0;
 - MIPI0_CSI_D[3:2] data refer to MIPI_CSI0_CLK1.

<i>option1</i>	<i>Sensor1 x4Lane</i>	<i>MIPI_CSI_RX_D0-3</i> <i>MIPI_CSI_RX_CLK0</i>
<i>option2</i>	<i>Sensor1 x2Lane</i>	<i>MIPI_CSI_RX_D0-1</i> <i>MIPI_CSI_RX_CLK0</i>
	<i>+ Sensor2 x2Lane</i>	<i>MIPI_CSI_RX_D2-3</i> <i>MIPI_CSI_RX_CLK1</i>

Figure 2-110 RK3588 MIPI CSI0 Working Mode and Data and Clock Distribution

MIPI CSI1 RX interface mode support:

- Support x4Lane mode, MIPI_CSI1_D[3:0] data refer to MIPI_CSI1_CLK0;
- Support x2Lane+x2Lane mode:
 - MIPI1_CSI_D[1:0] data refer to MIPI_CSI1_CLK0;
 - MIPI1_CSI_D[3:2] data refer to MIPI_CSI1_CLK1;

<i>Option1</i>	<i>Sensor1 x4Lane</i>	<i>MIPI_CSI_RX_D0-3</i> <i>MIPI_CSI_RX_CLK0</i>
<i>Option2</i>	<i>Sensor1 x2Lane</i>	<i>MIPI_CSI_RX_D0-1</i> <i>MIPI_CSI_RX_CLK0</i>
	<i>Sensor2 x2Lane</i>	<i>MIPI_CSI_RX_D2-3</i> <i>MIPI_CSI_RX_CLK1</i>

Figure 2-111 RK3588 MIPI CSI1 Working Mode and Data and Clock Distribution

Pay attention to the design of MIPI CSI0/1 RX:

- To improve MIPI CSI0/1 RX performance, the decoupling capacitors of every PHY power supply cannot be deleted, and they should be placed close to power pins when layout.

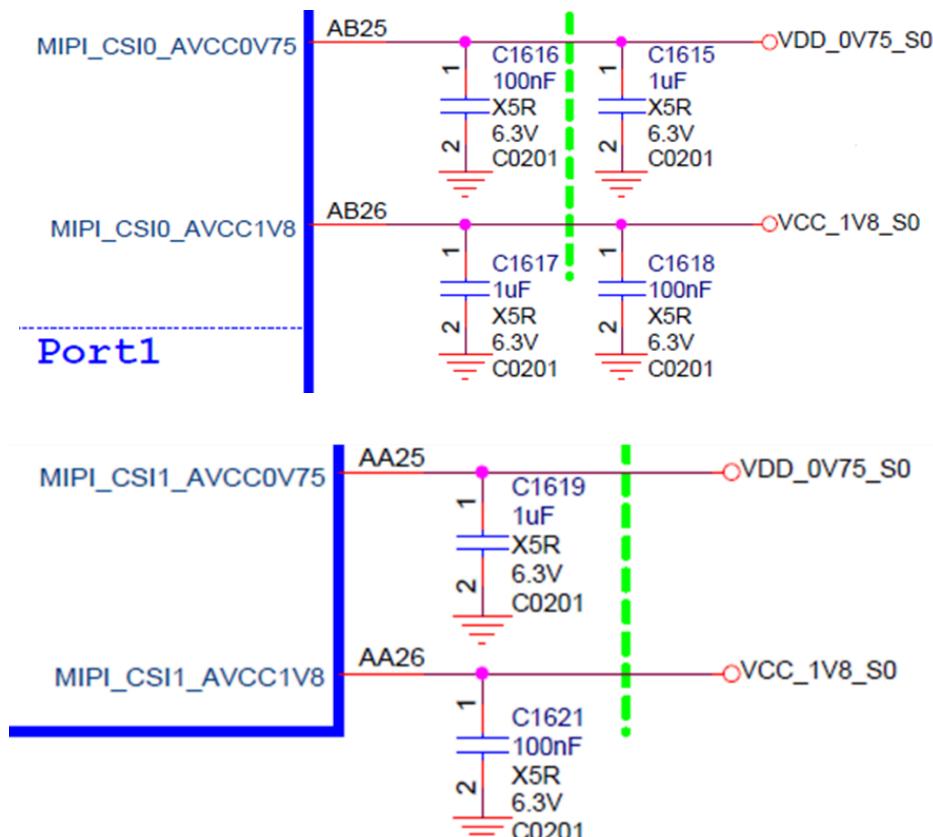


Figure 2-112 MIPI CSI0/1 RX PHY Power Supply Decoupling Capacitor

- The MIPI CSI0/1 RX interface matching design recommendation is shown in the following table

Table 2-21 RK3588 MIPI CSI0/1 RX Interface Design

Signal	Connection mode	Description
MIPI_CSIO_D0P/D0N	Direct connection	MIPI CSI0 data Lane0 input
MIPI_CSIO_D1P/D1N	Direct connection	MIPI CSI0 data Lane1 input
MIPI_CSIO_D2P/D2N	Direct connection	MIPI CSI0 data Lane2 input
MIPI_CSIO_D3P/D3N	Direct connection	MIPI CSI0 data Lane3 input
MIPI_CSIO_CLK0P/CLK0N	Direct connection	MIPI CSI0 clock 0 input
MIPI_CSIO_CLK1P/CLK1N	Direct connection	MIPI CSI0 clock 1 input
MIPI_CSII_D0P/D0N	Direct connection	MIPI CSI1 data Lane0 input
MIPI_CSII_D1P/D1N	Direct connection	MIPI CSI1 data Lane1 input
MIPI_CSII_D2P/D2N	Direct connection	MIPI CSI1 data Lane2 input
MIPI_CSII_D3P/D3N	Direct connection	MIPI CSI1 data Lane3 input
MIPI_CSII_CLK0P/CLK0N	Direct connection	MIPI CSI1 clock 0 input
MIPI_CSII_CLK1P/CLK1N	Direct connection	MIPI CSI1 clock 1 input

2.3.7.2 MIPI_D/CPHY_RX Interface

RK3588 has two PHYs of MIPI D-PHY/C-PHY CSI RX Combo, supports V1.2 version, D-PHY mode has 0/1/2/3 Lane and 2 lines per Lane, maximum transmission rate is 2.5Gbps /Lane;

1. It is recommended to use 1 Lane or 2Lane mode.
 2. Skew calibration function is not supported. In the case of mipi bitrate $\geq 1.5\text{Gbps/lane}$, the influence of PCB on the skew between each data lane and clk lane needs to be considered more strictly.
 3. It is not recommended to use the 4Lane mode when it is not necessary. If it must be used, there are strict requirements on the timing of the Camera, and the following conditions must be met:
 - T₄ > T₁ > T₄ - 2 > T₁ - 2

T_lane0 \equiv T_lane1 \equiv T_lane2 \equiv T_lane3;

T_lane* The time point of the arrow in the following figure is for reference:

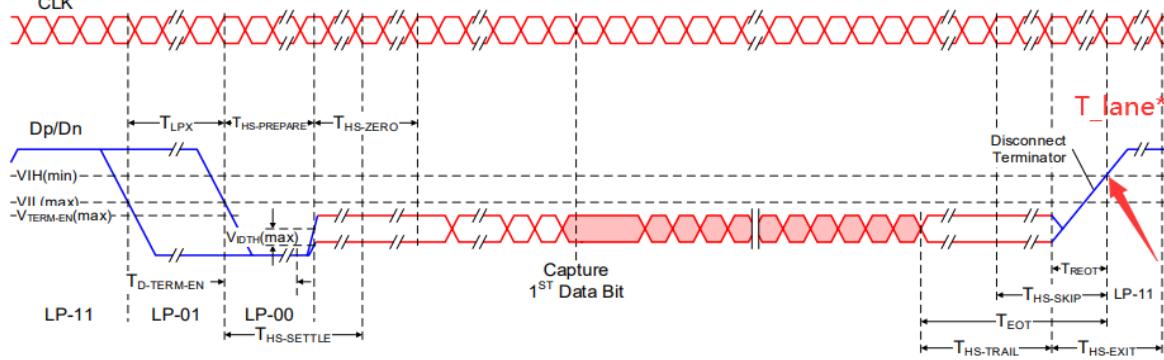


Figure 2-113 High-Speed Data Transmission in Bursts

- C-PHY supports V1.1 version, C-PHY mode has 0/1/2 Trio, each Trio A/B/C 3 lines, the maximum transmission rate is 5.7Gbps/Trio.

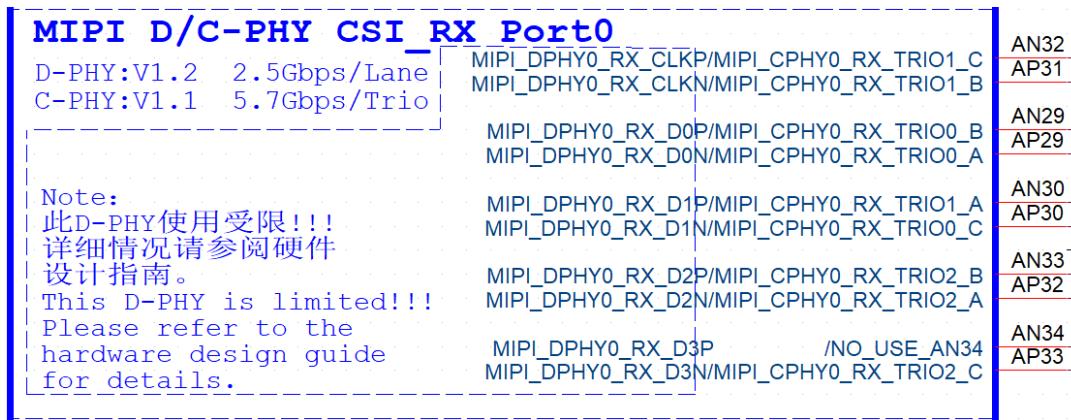


Figure 2-114 RK3588 MIPI D/C-PHY0 RX Signal Pin

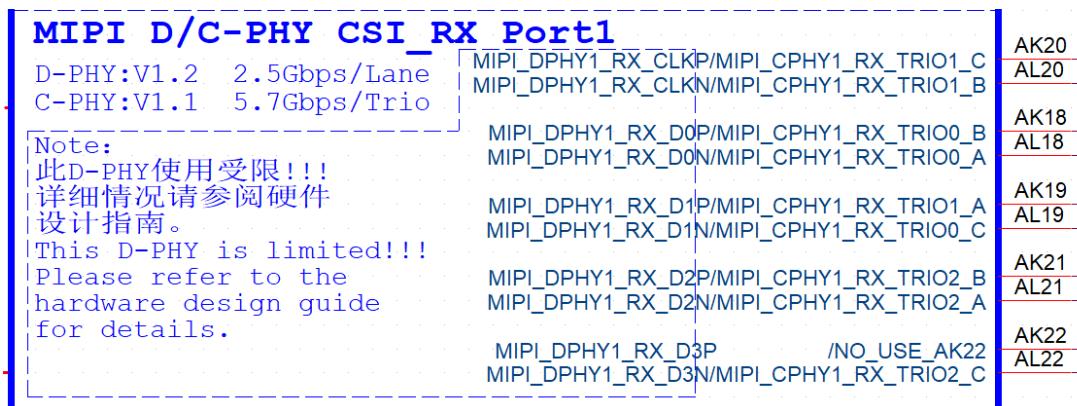


Figure 2-115 RK3588 MIPI D/C-PHY1 RX Signal Pin

DPHY and CPHY configuration support:

- The TX and RX of MIPI D-PHY/C-PHY Combo PHY0 can only be configured as DPHY0 TX, DPHY0 RX mode at the same time, or configured as CPHY0 TX, CPHY0 RX mode at the same time. Does not support one configured as DPHY0 TX and one configured as CPHY0 RX;
- The TX and RX of MIPI D-PHY/C-PHY Combo PHY1 can only be configured as DPHY1 TX, DPHY1 RX mode at the same time, or configured as CPHY1 TX, CPHY1 RX mode at the same time. Does not support one configured as DPHY1 TX and one configured as CPHY1 RX;

Mode support situation when MIPI D/C-PHY0 works in D-PHY:

- Support x4Lane mode (**not recommend**), MIPI_DPHY0_RX_D[3:0] data refer to MIPI_DPHY0_RX_CLK;
- Splitting into x2Lane+x2Lane mode is not supported.

Mode support situation when MIPI D/C-PHY0 works in C-PHY:

- Support 0/1/2 Trio, each Trio has 3 A/B/C lines: MIPI_CPHY0_RX_TRIO[2:0]_A, MIPI_CPHY0_RX_TRIO[2:0]_B, MIPI_CPHY0_RX_TRIO[2:0]_C.

Mode support situation when MIPI D/C-PHY1 works in D-PHY:

- Support x4Lane mode (**not recommend**), MIPI_DPHY1_RX_D[3:0] data refer to MIPI_DPHY1_RX_CLK;
- Splitting into x2Lane+x2Lane mode is not supported.

Mode support situation when MIPI D/C-PHY1 works in C-PHY:

- Support 0/1/2 Trio, 3 lines per Trio A/B/C, MIPI_CPHY1_RX_TRIO[2:0]_A, MIPI_CPHY1_RX_TRIO[2:0]_B, MIPI_CPHY1_RX_TRIO[2:0]_C.

Pay attention to MIPI D-PHY/C-PHY CSI RX Combo PHY0/1 design:

- In order to improve the performance of MIPI D-PHY/C-PHY CSI RX Combo PHY0/1, the decoupling capacitors of each power supply of PHY must not be deleted. Please place them close to the pins during layout (note that MIPI D-PHY/C-PHY CSI RX and MIPI D-PHY/C-PHY DSI TX power supply is combined in the same way);

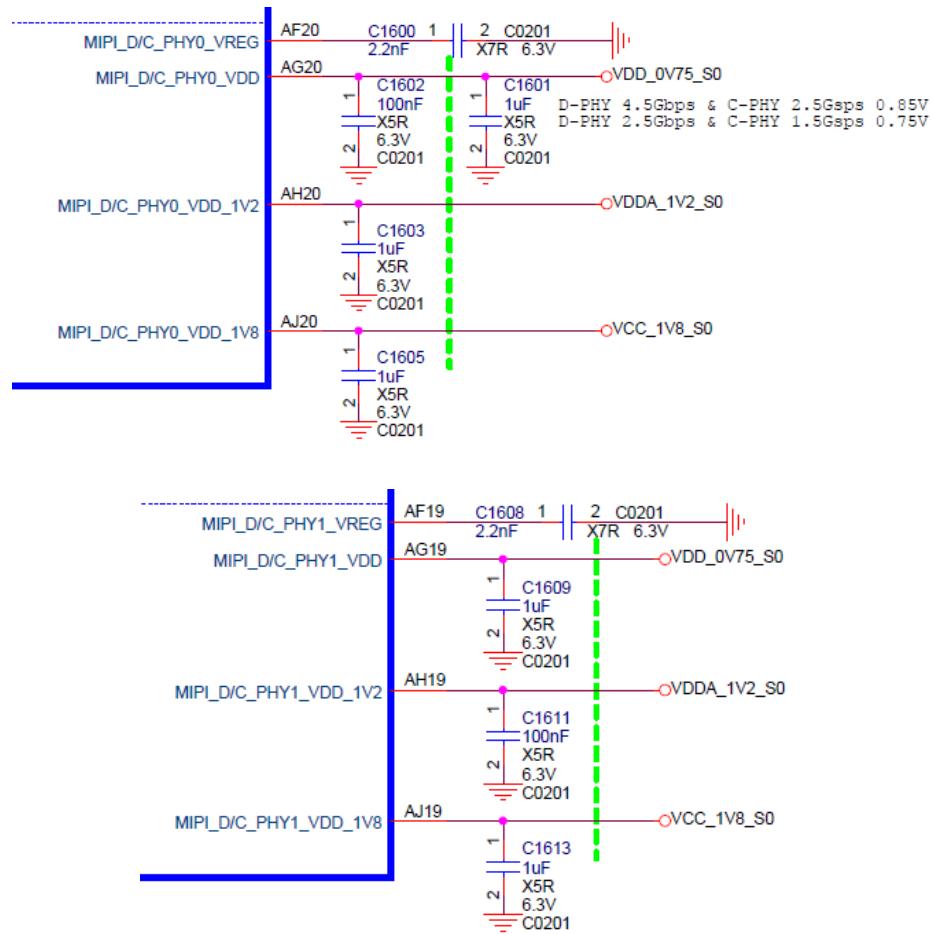


Figure 2-116 MIPI D-PHY/C-PHY CSI RX Combo PHY0/1 Power Decoupling Capacitor

- MIPI D-PHY/C-PHY Combo PHY0/1 RX matching design recommendations are shown in the following table:

Table 2-22 RK3588 MIPI D-PHY/C-PHY CSI RX Combo PHY0/1 Interface Design

Signal	Connection mode	Description
MIPI_DPHY0_RX_D0P/D0N	Direct connection	MIPI_DPHY0_RX data Lane0 input
MIPI_DPHY0_RX_D1P/D1N	Direct connection	MIPI_DPHY0_RX data Lane1 input
MIPI_DPHY0_RX_D2P/D2N	Direct connection	MIPI_DPHY0_RX data Lane2 input
MIPI_DPHY0_RX_D3P/D3N	Direct connection	MIPI_DPHY0_RX data Lane3 input
MIPI_DPHY0_RX_CLKP/CLKN	Direct connection	MIPI_DPHY0_RX clock input
MIPI_CPHY0_RX_TRIO0_A/B/C	Direct connection	MIPI_CPHY0_RX_TRIO0 input
MIPI_CPHY0_RX_TRIO1_A/B/C	Direct connection	MIPI_CPHY0_RX_TRIO1 input
MIPI_CPHY0_RX_TRIO2_A/B/C	Direct connection	MIPI_CPHY0_RX_TRIO2 input
MIPI_DPHY1_RX_D0P/D0N	Direct connection	MIPI_DPHY1_RX data Lane0 input
MIPI_DPHY1_RX_D1P/D1N	Direct connection	MIPI_DPHY1_RX data Lane1 input
MIPI_DPHY1_RX_D2P/D2N	Direct connection	MIPI_DPHY1_RX data Lane2 input
MIPI_DPHY1_RX_D3P/D3N	Direct connection	MIPI_DPHY1_RX data Lane3 input
MIPI_DPHY1_RX_CLKP/CLKN	Direct connection	MIPI_DPHY1_RX clock input
MIPI_CPHY1_RX_TRIO0_A/B/C	Direct connection	MIPI_CPHY1_RX_TRIO0 input
MIPI_CPHY1_RX_TRIO1_A/B/C	Direct connection	MIPI_CPHY1_RX_TRIO1 input
MIPI_CPHY1_RX_TRIO2_A/B/C	Direct connection	MIPI_CPHY1_RX_TRIO2 input

2.3.7.3 CIF Interface

The CIF interface is distributed in two power domains, namely VCCIO5 and VCCIO6. In actual product design, you need to select the corresponding power supply according to the actual IO power supply requirements (1.8V or 3.3V) of the product Camera (the two power domains need to be synchronized) At the same time, the I2C pull-up level must be consistent with it, otherwise it will cause the Camera to work abnormally or fail to work.

VCCIO6 Domain		Operating Voltage=1.8V/3.3V								
/ SPI0_MISO_M1	/ UART9_RTSN_M1	/ I2S1_MCLK_M0	/ PCIE30X1_1_CLKREQN_M1	/ BT1120_D0	CIF_D0	/ GPIO4_A0_d	AK30			
/ SPI0_MOSI_M1	/ UART9_CTSN_M1	/ I2S1_SCLK_RX_M0	/ PCIE30X1_1_WAKEN_M1	/ BT1120_D1	CIF_D1	/ GPIO4_A1_d	AL30			
/ SPI0_CLK_M1	/	/ I2S1_LRCK_RX_M0	/ PCIE30X1_1_PERSTN_M1	/ BT1120_D2	CIF_D2	/ GPIO4_A2_d	AM29			
/	UART0_TX_M2	/ I2S1_SCLK_RX_M0	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D3	CIF_D3	/ GPIO4_A3_d	AL29			
/ SPI2_MISO_M1	/ UART0_RX_M2	/ I2C3_SDA_M2	/ I2S1_LRCK_RX_M0	/ PCIE30X1_0_WAKEN_M1	/ BT1120_D4	CIF_D4	/ GPIO4_A4_d	AL28		
/ SPI2_MOSI_M1	/ UART0_RX_M2	/ I2C3_SDA_M2	/ I2S1_SD0_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D5	CIF_D5	/ GPIO4_A5_d	AK27		
/ SPI2_CLK_M1	/ UART0_RX_M2	/ I2C3_SDA_M2	/ I2S1_SD1_M0	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D6	CIF_D6	/ GPIO4_A6_d	AL27		
/ SPI2_CS0_M1	/	/ I2C5_SDA_M2	/ I2S1_SD2_M0	/ PCIE30X2_WAKEN_M1	/ BT1120_D7	CIF_D7	/ GPIO4_A7_d	AM27		
/ SPI2_CS1_M1	/ UART8_TX_M0	/ I2C6_SDA_M3	/ I2S1_SD3_M0	/ PCIE30X2_PERSTN_M1	/ BT1120_CLKOUT	CIF_CLKIN	/ GPIO4_B0_d	AK26		
SATA2_ACT_LED_M0	/ SPOIFI1_TX_M1	/ SPI0_CS1_M1	/ UART8_RX_M0	/ I2C6_SCL_M3	/ I2S1_SD0_M0	/ PCIE30X1_0_BUTTON_RSTN	/ MIPI_CAMERA0_CLK_M0	GPIO4_B1_u	AL24	
CANL_RX_M1	/ PWM14_M1	/ SPI0_CS0_M1	/ UART8_RTSN_M0	/ I2C7_SDA_M3	/ I2S1_SD1_M0	/ PCIE30X1_1_BUTTON_RSTN	/ BT1120_D8	CIF_HREF	GPIO4_B2_u	AK25
CANL_RX_M1	/ PWM15_IR_M1	/	/ UART8_CTSN_M0	/ I2C7_SDA_M3	/ I2S1_SD2_M0	/ PCIE30X1_2_BUTTON_RSTN	/ BT1120_D9	CIF_VSYNC	/ GPIO4_B3_u	AM25
SPDIF0_RX_M1	/ PWM11_IR_M1	/ DPO_HEDIN_M0	/ UART8_TX_M1	/	/ I2S1_SD3_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D10	CIF_CLKOUT	/ GPIO4_B4_u	AJ26
SATA1_ACT_LED_M0	/ PWM12_M1	/ SPI3_MISO_M1	/ UART8_RX_M1	/	/ HDMI_RX_CEC_M0	/ PCIE30X4_WAKEN_M1	/ BT1120_D11	/	/ GPIO4_B5_d	AJ26
SATD0_ACT_LED_M0	/ PWM13_M1	/ SPI3_MOSI_M1	/	/ I2C5_SCL_M1	/ HDMI_RX_HPDIN_M0	/ PCIE30X4_PERSTN_M1	/ BT1120_D12	/	/ GPIO4_B6_d	AJ27
/	/ SPI3_CLK_M1	/	/ I2C6_SDA_M1	/ HDMI_RX_SCL_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D13	/	/ GPIO4_B7_u	AJ28	
/	/ SPI3_CS0_M1	/	/ I2C8_SDA_M3	/ HDMI_RX_SDA_M0	/ PCIE30X1_2_WAKEN_M1	/ BT1120_D14	/	/ GPIO4_C0_u	AJ25	
SPDIF1_RX_M2	/ PWM6_M1	/ SPI3_CS1_M1	/	/ I2C8_SDA_M3	/ HDMI_RX_CEC_M0	/ PCIE30X1_2_PERSTN_M1	/ BT1120_D15	/	/ GPIO4_C1_d	AK24

VCCIO5 Domain		Operating Voltage=1.8V/3.3V							
PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_DO_M2	/ I2S3_MCLK	/ SDIO_D0_M1	/ GMAC1_TXD2	/ GPIO3_A0_u	AA29
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_DI_M2	/ I2S3_SCLK	/ SDIO_D1_M1	/ GMAC1_TXD3	/ GPIO3_A1_u	AA30
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_TX_M1	/	/ FSPI_D2_M2	/ I2S3_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u	AD27
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S3_SD0	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u	AE27
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S3_SD1	/ SDIO_CMD_M1	/ GMAC1_RXCLK	/ GPIO3_A4_d	AD28
/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	AH30	
/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLK0_25M	/ GPIO3_A6_d	AH27	
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXD0	/ GPIO3_A7_u	AG29
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_RXD1	/ GPIO3_B0_u	AG28
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART3_RX_M2	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	AH29
PWM3_IR_M1	/	/ UART3_RX_M2	/	/	/ I2S2_SD1_M1	/	/ GMAC1_RXER	/ GPIO3_B2_d	AE28
/	/ UART3_RTSN	/	/	/ I2S2_SD0_M1	/	/ GMAC1_RXD0	/ GPIO3_B3_u	AC28	
/	/ UART3_CTSN	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_RXD1	/ GPIO3_B4_u	AC29	
PWM12_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_RXEN	/ GPIO3_B5_u	AD29
PWM13_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_MCLNINOUT	/ GPIO3_B6_d	AE29
/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_RX1_HPD_M1	/	/ GMAC1_PTP_REF_CLK	/ GPIO3_B7_d	AA28	
/	/ UART7_RX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d	Y29	
/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPCLK	/ GPIO3_C1_d	Y27	
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d	Y31
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d	Y30
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_RX_M1	/ FSPI_CS0_M2	/ SPI3_CS0_M3	/ HDMI_RX1_CEC_M2	/	CIF_D8	/ GPIO3_C4_u	AH26
CAN2_RX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1_M2	/ SPI3_CS1_M3	/ HDMI_RX1_SDA_M1	/	CIF_D9	/ GPIO3_C5_u	AH25
/	/ PCIE30X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_RX1_SCL_M1	/	CIF_D10	/ GPIO3_C6_u	AG26
/ PCIE30X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_RX0_SCL_M2	/	CIF_D11	/ GPIO3_C7_u	AJ24	
PWM8_M2	/ PCIE30X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_RX0_SDA_M2	/	CIF_D12	/ GPIO3_D0_u	AH24
PWM9_M2	/ PCIE30X1_2_PERSTN_M0	/ UART4_RX_M1	/	/ SPI0_MISO_M3	/ HDMI_RX_CEC_M1	/	CIF_D13	/ GPIO3_D1_d	AG23
/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SDA_M2	/ SPI0_MOSI_M3	/ HDMI_RX_SCL_M1	/	CIF_D14	/ GPIO3_D2_d	AG25	
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/ HDMI_RX_SDA_M1	/	CIF_D15	/ GPIO3_D3_d	AG24
/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M3	/ HDMI_RX_HPDIN_M1	/ HDMI_RX_HPD_M1	/ MCU_JTAG_TCK_M1	/ GPIO3_D4_d	AA27	
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART9_RX_M2	/	/ SPI0_CS1_M3	/ DPL_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

Figure 2-117 RK3588 CIF Function Pin

The CIF interface supports the following formats:

- Support BT601 YCbCr 422 8bit input
- Support BT656 YCbCr 422 8bit input
- Support RAW 8/10/12bit input
- Support BT1120 YCbCr 422 8/16bit input, single/dual-edge sampling
- Support 2/4 mixed BT656/BT1120 YCbCr 422 8/16bit input
- Support YUYV sequence configuration

The corresponding relationship of 8/10/12/16bit data of CIF[15:0] is as shown in the table below, using high-order alignment.

Mode	16bit	12bit	10bit	8bit
<i>CIF_D0</i>	<i>D0</i>	--	--	--
<i>CIF_D1</i>	<i>D1</i>	--	--	--
<i>CIF_D2</i>	<i>D2</i>	--	--	--
<i>CIF_D3</i>	<i>D3</i>	--	--	--
<i>CIF_D4</i>	<i>D4</i>	<i>D0</i>	--	--
<i>CIF_D5</i>	<i>D5</i>	<i>D1</i>	--	--
<i>CIF_D6</i>	<i>D6</i>	<i>D2</i>	<i>D0</i>	--
<i>CIF_D7</i>	<i>D7</i>	<i>D3</i>	<i>D1</i>	--
<i>CIF_D8</i>	<i>D8</i>	<i>D4</i>	<i>D2</i>	<i>D0</i>
<i>CIF_D9</i>	<i>D9</i>	<i>D5</i>	<i>D3</i>	<i>D1</i>
<i>CIF_D10</i>	<i>D10</i>	<i>D6</i>	<i>D4</i>	<i>D2</i>
<i>CIF_D11</i>	<i>D11</i>	<i>D7</i>	<i>D5</i>	<i>D3</i>
<i>CIF_D12</i>	<i>D12</i>	<i>D8</i>	<i>D6</i>	<i>D4</i>
<i>CIF_D13</i>	<i>D13</i>	<i>D9</i>	<i>D7</i>	<i>D5</i>
<i>CIF_D14</i>	<i>D14</i>	<i>D10</i>	<i>D8</i>	<i>D6</i>
<i>CIF_D15</i>	<i>D15</i>	<i>D11</i>	<i>D9</i>	<i>D7</i>

Figure 2-118 RK3588 CIF Data Data Correspondence

Data relationship in BT1120 16bit mode is shown as follows, and supports YC Swap.

Table 2-23 RK3588 Data Relationship in BT1120 16bit Mode

Pin Name	Default mode		Swap is enabled	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
CIF_D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
CIF_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
CIF_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
CIF_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
CIF_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
CIF_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
CIF_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
CIF_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
CIF_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
CIF_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
CIF_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
CIF_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
CIF_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
CIF_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
CIF_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
CIF_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]

Table 2-24 RK3588 CIF Interface Design

Signal	Pull up/down Inside	Connection, Mode	Description (chip end)
CIF_D[15:0]	Pull-down	Direct connection, it's recommended to reserve a series resistor near device end.	CIF data input
CIF_HREF	Pull-down	Direct connection, it's recommended to reserve a series resistor near device end.	CIF row synchronous input
CIF_VSYNC	Pull-down	Direct connection, it's recommended to reserve a series resistor near device end.	CIF field synchronous input
CIF_CLKIN	Pull-down	Connect 22ohm resistor in series, close to the device	CIF clock input
CIF_CLKOUT	Pull-down	Connect 22ohm resistor in series, close to the chip	CIF clock output, provide MCLK work clock for device.

When realizing the board-to-board connection through the connector, it is recommended to connect a resistor in series (between 22ohm and 100ohm, depending on the specific requirements that can meet the SI test), and reserve TVS devices.

Note when designing MIPI CSI RX/CIF:

- DVDD power supply of Camera is 1.2V/1.5V/1.8V, etc. Please provide accurate power supply according to the specifications of Camera. The reference circuit is 1.2V by default;
- DVDD current of some Cameras is relatively large, if the current is more than 100mA, it is suggested to use DCDC for power supply;
- Several power supplies of Camera require the power on sequence, please adjust the power on sequence according to the specifications of Camera, the default power on sequence in the schematic design is 1.8V→1.2V→2.8V;
- When using the Camera with CIF interface, you should pay attention that DOVDD (IO power supply) of Camera must use the same voltage as VCCIO5, VCCIO6 power supply;
- When using two Cameras, the power supply can be separated or combined according to the actual requirements. The power supply in schematic design is separated by default.
- For cameras with AF function, VCC2V8_AF needs to supply the power separately or shares supply with AVCC2V8_DVP which should be separated by magnetic beads;
- The decoupling capacitors of all power supplies of Camera should not be deleted, they must be reserved and placed close to the connector;
- PWDN signal of Camera must be controlled by GPIO, and GPIO level must match with Camera IO level;
- Reset signal of Camera is suggested to be controlled by GPIO, and GPIO level must match with Camera IO level. The 100nF capacitors of Reset signal should not be deleted and placed near the connector to enhance anti ESD capability;
- MCLK of Camera can be got from:
 - 1) CIF_CLKOUT
 - 2) MIPI_CAMERA0_CLK
 - 3) MIPI_CAMERA1_CLK
 - 4) MIPI_CAMERA2_CLK
 - 5) MIPI_CAMERA3_CLK
 - 6) MIPI_CAMERA4_CLK

Note: clock level must match with Camera IO level, if not, level conversion or resistor divider must be performed to match the level;

- If two Cameras are the same model, note that whether I2C addresses are the same or not. If the address as the same, then two I2C buses are required.

2.3.7.4 HDMI2.0 RX Interface

RK3588 chip supports HDMI2.0 RX, backward compatible with HDMI1.4b; supports RGB/YUV444/YUV422/YUV420 formats; and can support up to 4K@60Hz input.

(This HDMI2.0 RX interface has low probability anomalies, such as splash screen and restart, in scenarios such as frequent plug and pull, high and low resolution switching, etc. The probability is between 0.1% and 1%. We are still trying to debug and solve these problems.

If the user will frequently use various peripherals to insert this HDMI2.0 RX interface, it is recommended to use external bridges connecting chips to improve compatibility to avoid affecting product production.)

The HDMI RX TMDS signal is as shown in the figure below. It is required to reserve a 2.2ohm resistor close

to the HDMI RX socket, which must not be deleted to strengthen the anti-static surge capability.

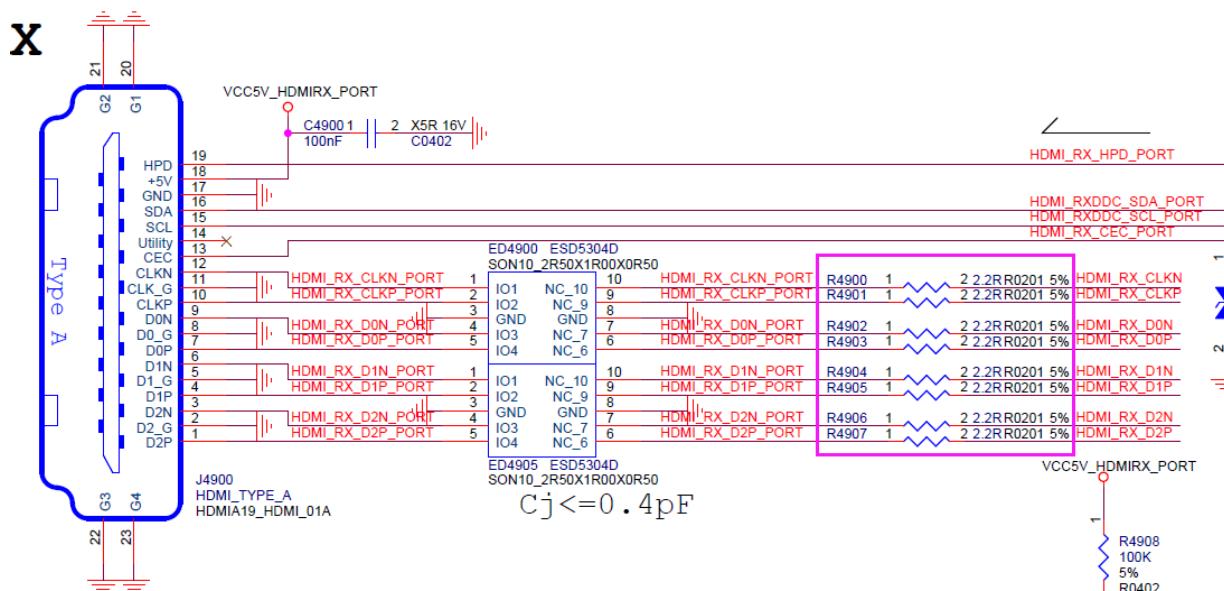


Figure 2-119 RK3588 HDMI RX PHY Pin

HDMI RX PHY power pins need to place 1uF and 100nF decoupling capacitors, which cannot be deleted. Place them close to the RK3588 pin during layout.

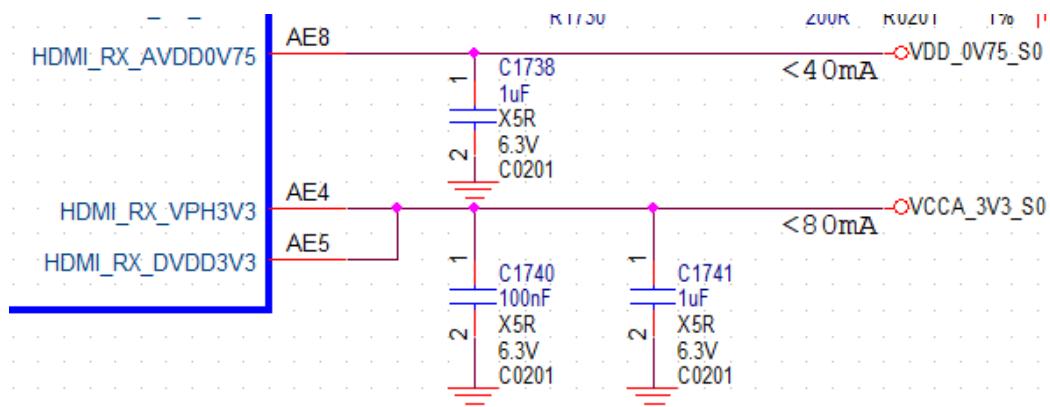


Figure 2-120 RK3588 HDMI RX PHY Power Decoupling Capacitor

HDMI RX REXT is an external reference resistor pin of HDMI RX PHY. It is connected to a 200ohm resistor with an accuracy of 1% to the ground. The resistance value must not be changed. Place it close to the RK3588 chip pin during layout.



Figure 2-121 RK3588 HDMI RX REXT Pin

HDMI_RX_HPD is the function of HDMI RX controller multiplexing to common GPIO, and the level varies with the voltage of the power domain.

HDMI_RX_HPD is multiplexed in three different power domains, one on the IO of the VCCIO6 power domain, one on the IO of the VCCIO5 power domain, and one on the IO of the VCCIO4 power domain.

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

/ SPI0_MISO_M1 /	/ UART9_PTSN_M1 /	/ I2S1_MCLK_M0 /	/ PCIE30X1_1_CLKREQN_M1 /	/ BT1120_D0 /	/ CIF_D0 /	/ GPIO4_A0_d /	AK30		
/ SPI0_MOSI_M1 /	/ UART9_CTSN_M1 /	/ I2S1_SCLK_M0 /	/ PCIE30X1_1_WAKEN_M1 /	/ BT1120_D1 /	/ CIF_D1 /	/ GPIO4_A1_d /	AL30		
/ SPI0_CLK_M1 /	/	/ I2S1_LRCK_M0 /	/ PCIE30X1_1_PERSTN_M1 /	/ BT1120_D2 /	/ CIF_D2 /	/ GPIO4_A2_d /	AM29		
/	/UART0_RX_M2 /	/	/ PCIE30X1_0_CLKREQN_M1 /	/ BT1120_D3 /	/ CIF_D3 /	/ GPIO4_A3_d /	AL29		
/ SPI2_MISO_M1 /	/UART0_RX_M2 /	/ I2C3_SCL_M2 /	/ PCIE30X1_0_WAKEN_M1 /	/ BT1120_D4 /	/ CIF_D4 /	/ GPIO4_A4_d /	AL28		
/ SPI2_MOSI_M1 /	/UART3_RX_M2 /	/ I2C3_SDA_M2 /	/ I2S1_SD10_M0 /	/ PCIE30X1_0_PERSTN_M1 /	/ BT1120_D5 /	/ CIF_D5 /	/ GPIO4_A5_d /	AK27	
/ SPI2_CLK_M1 /	/UART3_RX_M2 /	/ I2C5_SCL_M2 /	/ I2S1_SD11_M0 /	/ PCIE30X2_CLKREQN_M1 /	/ BT1120_D6 /	/ CIF_D6 /	/ GPIO4_A6_d /	AL27	
/ SPI2_C80_M1 /	/	/ I2C5_SDA_M2 /	/ I2S1_SD12_M0 /	/ PCIE30X2_WAKEN_M1 /	/ BT1120_D7 /	/ CIF_D7 /	/ GPIO4_A7_d /	AM27	
/ SPI2_C81_M1 /	/UART6_RX_M0 /	/ I2C6_SDA_M3 /	/ I2S1_SD13_M0 /	/ PCIE30X2_PERSTN_M1 /	/ BT1120_CLKOUT /	/ CIF_CLKIN /	/ GPIO4_B0_d /	AK26	
SATA0_ACT_LED_M0 /	/SPDIF1_TX_M1 /	/ SPI0_C81_M1 /	/UART7_RX_M0 /	/ I2C6_SCL_M3 /	/ I2S1_SD00_M0 /	/ PCIE30X1_0_BUTTON_RSTN /	/ MIPI_CAMERA0_CLK_M0 /	GPIO4_B1_u	
CAN1_RX_M1 /	/ PWM14_M1 /	/ SPI1_C80_M1 /	/UART7_PTSN_M0 /	/ I2C7_SCL_M3 /	/ I2S1_SD01_M0 /	/ PCIE30X1_1_BUTTON_RSTN /	/ BT1120_D8 /	/ CIF_HREF /	GPIO4_B2_u
CAN1_RX_M1 /	/ PWM15_IR_M1 /	/	/UART8_CTSN_M0 /	/ I2C7_SDA_M3 /	/ I2S1_SD02_M0 /	/ PCIE30X1_2_BUTTON_RSTN /	/ BT1120_D9 /	/ CIF_VSYNC /	GPIO4_B3_u
SPDIF0_RX_M1 /	/ PWM11_IR_M1 /	/ DPO_HPDIN_M0 /	/UART8_RX_M1 /	/	/ I2S1_SD03_M0 /	/ PCIE30X4_CLKREQN_M1 /	/ BT1120_D10 /	/ CIF_CLKOUT /	GPIO4_B4_u
SATA0_ACT_LED_M0 /	/ PWM12_M1 /	/ SPI1_MISO_M1 /	/UART8_RX_M1 /	/	/HDMI_RX_CEC_M0 /	/ PCIE30X4_WAKEN_M1 /	/ BT1120_D11 /	/	GPIO4_B5_d
SATA0_ACT_LED_M0 /	/ PWM13_M1 /	/ SPI1_MOSI_M1 /	/	/ I2C5_SCL_M1 /	/HDMI_RX_HPDOUT_M0 /	/ PCIE30X4_PERSTN_M1 /	/ BT1120_D12 /	/	GPIO4_B6_d
/	/ SPI1_CLK_M1 /	/	/	/ I2C5_SDA_M1 /	/HDMI_RX_SCL_M0 /	/ PCIE30X1_2_CLKREQN_M1 /	/ BT1120_D13 /	/	GPIO4_B7_u
/	/ SPI1_C80_M1 /	/	/	/ I2C8_SCL_M3 /	/HDMI_RX_SDA_M0 /	/ PCIE30X1_2_WAKEN_M1 /	/ BT1120_D14 /	/	GPIO4_C0_u
SPDIF1_RX_M2 /	/ PWM46_M1 /	/ SPI1_C81_M1 /	/	/ I2C8_SDA_M3 /	/HDMI_RX_CEC_M0 /	/ PCIE30X1_2_PERSTN_M1 /	/ BT1120_D15 /	/	GPIO4_C1_d

Figure 2-122 RK3588 HDMI_RX_HPD M0 Function Pin

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM0_M0 /	/ SPI4_MISO_M1 /	/	/ I2C6_SDA_M4 /	/FSPI_D0_M2 /	/ I2S2_MCLK /	/ SDIO_D0_M1 /	/ GMAC1_TxD2 /	/ GPIO3_A0_u /	AA29
AUDDSM_LN /	/ SPI4_MOSI_M1 /	/ PWM11_IR_M0 /	/ I2C6_SCL_M4 /	/FSPI_DL_M2 /	/ I2S2_SCLK /	/ SDIO_D1_M1 /	/ GMAC1_TxD3 /	/ GPIO3_A1_u /	AA30
AUDDSM_LP /	/ SPI4_CLK_M1 /	/UART8_RX_M1 /	/	/FSPI_D2_M2 /	/ I2S2_LRCK /	/ SDIO_D2_M1 /	/ GMAC1_RXD2 /	/ GPIO3_A2_u /	AD27
AUDDSM_RN /	/ SPI4_C80_M1 /	/UART8_RX_M1 /	/	/FSPI_D3_M2 /	/ I2S2_SDO /	/ SDIO_D3_M1 /	/ GMAC1_RXD3 /	/ GPIO3_A3_u /	AE27
AUDDSM_RP /	/ SPI4_C81_M1 /	/UART8_PTSN_M1 /	/	/	/ I2S2_SD1 /	/ SDIO_CMD_M1 /	/ GMAC1_RXCLK /	/ GPIO3_A4_d /	AD28
/	/ MIPI_CAMERA0_CLK_M1 /	/UART8_CTSN_M1 /	/ I2C4_SDA_M0 /	/FSPI_CLK_M2 /	/	/ SDIO_CLK_M1 /	/ GMAC1_RXCLK /	/ GPIO3_A5_d /	AH30
/	/ MIPI_CAMERA1_CLK_M1 /	/	/ I2C4_SCL_M0 /	/	/	/	/ETH1_REFCLK0_25M /	/ GPIO3_A6_d /	AH27
PWM0_M0 /	/ MIPI_CAMERA2_CLK_M1 /	/	/	/	/	/	/ GMAC1_RXD0 /	/ GPIO3_A7_u /	AG29
PWM0_M0 /	/ MIPI_CAMERA3_CLK_M1 /	/	/	/	/	/	/ GMAC1_RXD1 /	/ GPIO3_B0_u /	AG28
PWM2_M1 /	/ MIPI_CAMERA4_CLK_M1 /	/UART2_RX_M2 /	/	/	/	/	/ GMAC1_RXDV_CRS /	/ GPIO3_B1_d /	AH29
PWM3_IR_M1 /	/	/UART3_RX_M2 /	/	/	/ I2S2_SD1_M1 /	/	/ GMAC1_RXER /	/ GPIO3_B2_d /	AE28
/	/UART3_PTSN /	/	/	/	/ I2S2_SDO_M1 /	/	/ GMAC1_TxD0 /	/ GPIO3_B3_u /	AC28
/	/UART2_CTSN /	/	/	/	/ I2S2_MCLK_M1 /	/	/ GMAC1_TxD1 /	/ GPIO3_B4_u /	AC29
PWM12_M0 /	/ CAN1_RX_M0 /	/UART3_RX_M1 /	/	/	/ I2S2_SCL_M1 /	/	/ GMAC1_TxEN /	/ GPIO3_B5_u /	AD29
PWM13_M0 /	/ CAN1_RX_M0 /	/UART3_RX_M1 /	/	/	/ I2S2_LRCK_M1 /	/	/ GMAC1_MCLKINOUT /	/ GPIO3_B6_d /	AE29
/	/	/ I2C3_SCL_M1 /	/ SPI1_MOSI_M1 /	/HDMI_RX_HPD_M1 /	/	/ GMAC1_PTB_REF_CLK /	/ GPIO3_B7_d /	AA28	
/	/UART7_RX_M1 /	/ I2C8_SDA_M1 /	/ SPI1_MISO_M1 /	/	/	/ GMAC1_PPSTRIG /	/ GPIO3_C0_d /	Y29	
/	/ PCIE30X2_BUTTON_RSTN /	/UART7_RX_M1 /	/	/ SPI1_CLK_M1 /	/	/	/ GMAC1_PPCLK /	/ GPIO3_C1_d /	Y27
PWM14_M0 /	/	/UART7_RSH_M1 /	/ I2C8_SCL_M4 /	/ SPI1_C80_M1 /	/	/ MIPI_TE0 /	/ GMAC1_MDC /	/ GPIO3_C2_d /	Y31
PWM15_IR_M0 /	/	/UART7_CTSN_M1 /	/ I2C8_SDA_M4 /	/ SPI1_C81_M1 /	/	/ MIPI_TE1 /	/ GMAC1_MDIO /	/ GPIO3_C3_d /	Y30
CAN2_RX_M0 /	/ PCIE30X4_CLKREQN_M2 /	/UART5_RX_M1 /	/FSPI_CS0_M2 /	/ SPI2_C80_M3 /	/HDMI_RX_CEC_M2 /	/	/ CIF_D8 /	/ GPIO3_C4_u /	AH26
CAN2_RX_M0 /	/ PCIE30X4_WAKEN_M2 /	/UART5_RX_M1 /	/FSPI_CS1_M2 /	/ SPI2_C81_M3 /	/HDMI_RX_SDA_M1 /	/	/ CIF_D8 /	/ GPIO3_C5_u /	AH25
/	/ PCIE30X4_PERSTN_M2 /	/	/	/ SPI2_MISO_M3 /	/HDMI_RX_SCL_M1 /	/	/ CIF_D10 /	/ GPIO3_C6_u /	AG26
/	/ PCIE30X1_2_CLKREQN_M0 /	/	/ I2C5_SCL_M0 /	/ SPI3_MOSI_M3 /	/HDMI_RX_SCL_M1 /	/	/ CIF_D11 /	/ GPIO3_C7_u /	AJ24
PWM8_M2 /	/ PCIE30X1_2_WAKEN_M0 /	/UART4_RX_M1 /	/ I2C8_SDA_M0 /	/ SPI3_CLK_M3 /	/HDMI_RX_SDA_M1 /	/	/ CIF_D12 /	/ GPIO3_D0_u /	AH24
PWM9_M2 /	/ PCIE30X1_2_PERSTN_M0 /	/UART4_RX_M1 /	/	/ SPI0_MISO_M3 /	/HDMI_RX_CEC_M1 /	/	/ CIF_D13 /	/ GPIO3_D1_d /	AG23
/	/ PCIE30X2_CLKREQN_M2 /	/UART9_PTSN_M2 /	/ I2C7_SCL_M2 /	/ SPI0_MOSI_M3 /	/HDMI_RX_SCL_M1 /	/	/ CIF_D14 /	/ GPIO3_D2_d /	AG25
PWM10_M2 /	/ PCIE30X2_WAKEN_M2 /	/UART9_CTSN_M2 /	/ I2C7_SDA_M2 /	/ SPI0_CLK_M3 /	/HDMI_RX_SDA_M1 /	/	/ CIF_D15 /	/ GPIO3_D3_d /	AG24
/	/ PCIE30X2_PERSTN_M2 /	/UART9_RX_M2 /	/	/ SPI0_C80_M3 /	/HDMI_RX_HPDOUT_M1 /	HDMI_RX_HPD_M1 /	/MCU_JTAG_TMS_M1 /	/ GPIO3_D4_d /	AA27
PWM11_IR_M0 /	/ PCIE30X4_BUTTON_RSTN /	/UART9_RX_M2 /	/	/ SPI0_C81_M3 /	/DPI_HPDIN_M0 /	/	/ MCU_JTAG_TMS_M1 /	/ GPIO3_D5_d /	AB28

Figure 2-123 RK3588 HDMI_RX_HPD M1 Function Pin

VCCIO4 Domain	
Operating Voltage=1.8V/3.3V	
/SPI4_MISO_M2 /PCIE30X1_1_CLKREQN_M2/ DP0_HPDIN_M2	/I2C2_SDA_M4 / UART6_RX_M1 /GPIO1_A0_d A24
SATA1_ACT_LED_M1 / / SPI4_MOSI_M2 /PCIE30X1_1_WAKEN_M2 / DP1_HPDIN_M2	/I2C2_SCL_M4 / UART6_TX_M1 /GPIO1_A1_d A25
/PWM0_M2 /SPI4_CLK_M2 / / VOP_POST_EMPTY	/I2C4_SDA_M3 /UART6_RTSN_M1 /GPIO1_A2_d A26
/PWM1_M2 /SPI4_C80_M2 / / HDMI_TX1_SDA_M2	/I2C4_SCL_M3 /UART6_CTSN_M1 /GPIO1_A3_d A27
/ /SPI2_MISO_M0 / / HDMI_TX1_SCL_M2	/ / / /GPIO1_A4_d B25
/ /SPI2_MOSI_M0 / / HDMI_TX0_HPD_M0	/ / / /GPIO1_A5_d B26
/ /SPI2_CLK_M0 / / HDMI_TX1_HPD_M0	/ / / /GPIO1_A6_d C24
/ PWM3_IR_M3 /SPI2_C80_M0 /PCIE30X1_1_PERSTN_M2 /	/PDM1_SDIO_M1 / /GPIO1_A7_u C25
/ /SPI2_C81_M0 /PCIE30X4_CLKREQN_M3 /	/PDM1_SDII_M1 / /GPIO1_B0_u C27
/ /SPI0_MISO_M2 /PCIE30X4_WAKEN_M3 /	/PDM1_SDII2_M1 / /GPIO1_B1_d D25
/ /SPI0_MOSI_M2 /PCIE30X4_PERSTN_M3 /	/PDM1_SDIII_M1 /UART4_RX_M2 /GPIO1_B2_d D26
SATA0_ACT_LED_M1 / /SPI0_CLK_M2 /PCIE30X1_0_WAKEN_M2 /	/PDM1_CLK1_M1 /UART4_TX_M2 /GPIO1_B3_d D27
/ /SPI0_C80_M2 /PCIE30X1_0_PERSTN_M2 /	/PDM1_CLK0_M1 /UART7_RX_M2 /GPIO1_B4_u E24
/ /SPI0_C81_M2 /PCIE30X1_0_CLKREQN_M2/	/ / / /UART7_TX_M2 /GPIO1_B5_u E25
HDMI_RX_HPDOUT_M2 / /SPDIFO_RX_M0 /PCIE30X2_WAKEN_M3 / MIPI_CAMERA1_CLK_M0 /I2C5_SCL_M3 /UART1_RX_M1 /GPIO1_B6_u E26	
SATA2_ACT_LED_M1 /HDMI_RX_CEC_M2 / PWM13_M2 /SPDIFI1_RX_M0 /PCIE30X2_PERSTN_M3 / MIPI_CAMERA2_CLK_M0 /I2C5_SDA_M3 /UART1_RX_M1 /GPIO1_B7_u E27	
HDMI_RX_SCL_M2 / PWM14_M2 / / / /MIPI_CAMERA3_CLK_M0 /I2C8_SCL_M2 /UART1_RTSN_M1 /GPIO1_D6_u F24	
HDMI_RX_SDA_M2 / PWM15_IR_M3 / / / /PCIE30X2_CLKREQN_M3 / MIPI_CAMERA4_CLK_M0 /I2C8_SDA_M2 /UART1_CTSN_M1 /GPIO1_D7_u F25	

Figure 2-124 RK3588 HDMI_RX_HPD M2 Function Pin

Since the HDMI RX controller does not support hardware detection of Source insertion and removal, it can only be detected in software. The hardware circuit is as follows:

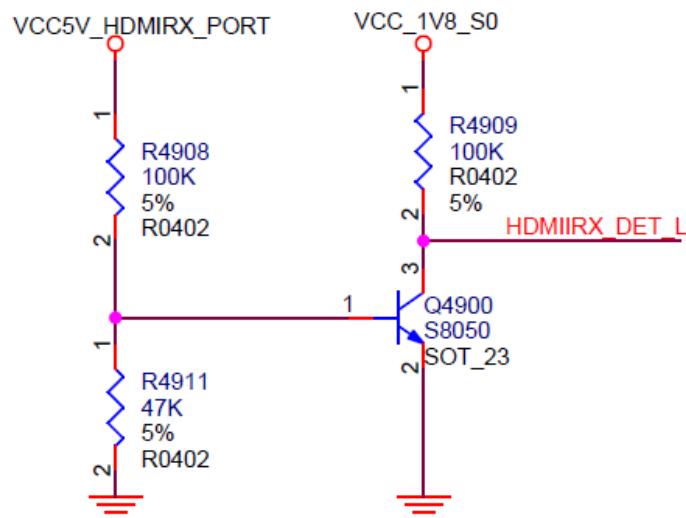


Figure 2-125 RK3588 HDMI_RX_DET Circuit

After detecting the HDMI RX DET pull down action, HDMI RX HPD outputs a high level, Q4900 is turned on, VCC5V_HDMIRX_PORT sends 5V voltage to HDMI RX HPD Port to complete the handshake action with the Source end.

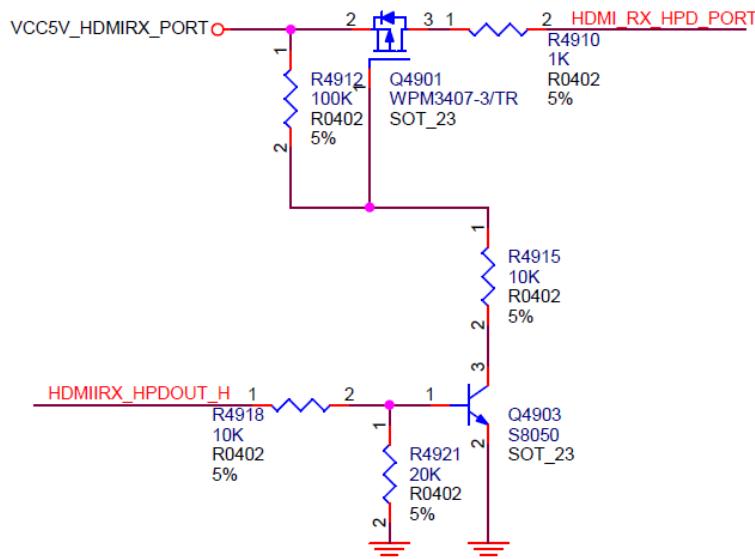


Figure 2-126 RK3588 HDMI_RX_HPD Circuit

HDMI_RX_CEC is that the CEC function of the HDMI controller is multiplexed onto the ordinary GPIO function. The level varies with the voltage of the power domain. If the power supply voltage of the power domain changes, the pull-up resistor power supply of the peripheral circuit must also be adjusted synchronously.

HDMI_RX_CEC multiplexes 3 positions respectively, one is on the IO of the VCCIO6 power domain, one is on the IO of the VCCIO5 power domain, and one is on the IO of the VCCIO4 power domain.

VCCIO6 Domain	
Operating Voltage=1.8V/3.3V	
/ SPI0_MISO_M1	/UART5_RTSN_M1 /
/ SPI0_MOSI_M1	/UART5_CTSN_M1 /
/ SPI0_CLK_M1	/
/	/UART0_TX_M2 /
/ SPI2_MISO_M1	/UART0_RX_M2 / I2C3_SCL_M2 / I2S1_LRCK_RX_M0 / PCIE30X1_0_WAKEN_M1 / BT1120_D0 / CIP_D0 / GPIO4_A0_d
/ SPI2_MOSI_M1	/UART3_RX_M2 / I2C3_SDA_M2 / I2S1_SD0_M0 / PCIE30X1_1_WAKEN_M1 / BT1120_D1 / CIP_D1 / GPIO4_A1_d
/ SPI2_CLK_M1	/UART3_RX_M2 / I2C5_SCL_M2 / I2S1_SD1_M0 / PCIE30X1_2_WAKEN_M1 / BT1120_D2 / CIP_D2 / GPIO4_A2_d
/	/I2S1_SD0_RX_M0 / PCIE30X1_0_CLKREQN_M1 / BT1120_D3 / CIP_D3 / GPIO4_A3_d
/ SPI2_CS0_M1	/I2C5_SDA_M0 / I2S1_SD2_M0 / PCIE30X1_0_PERSTN_M1 / BT1120_D4 / CIP_D4 / GPIO4_A4_d
/ SPI2_CS1_M1	/UART0_RX_M0 / I2C6_SDA_M3 / I2S1_SD3_M0 / PCIE30X2_WAKEN_M1 / BT1120_D5 / CIP_D5 / GPIO4_A5_d
SATA2_ACT_LED_M0	/SPDIF1_TX_M1 / SPI0_CS1_M1 / UART5_RX_M0 / I2C6_SCL_M3 / I2S1_SD0_M0 / PCIE30X1_0_BUTTON_RSTN / BT1120_CLKOUT / CIP_CLKIN / GPIO4_B0_d
CAN1_RX_M1	/PWMI4_M1 / SPI0_CS0_M1 / UART5_RTSN_M0 / I2C7_SCL_M3 / I2S1_SD1_M0 / PCIE30X1_1_BUTTON_RSTN / BT1120_D8 / CIP_HREF / GPIO4_B1_u
CAN1_TX_M1	/PWMI5_IR_M1 /
SPDIFO_RX_M1	/PWMI1_IR_M1 / DPO_HEDIN_M0 / UART5_RX_M1 /
SATA1_ACT_LED_M0	/SPDIF1_M1 / SPI1_MISO_M1 / UART5_RX_M1 / /HDMI_RX_CEC_M0 / PCIE30X4_WAKEN_M1 / BT1120_D11 / CIP_D11 / GPIO4_B5_d
SATA0_ACT_LED_M0	/PWMI3_M1 / SPI3_MOSI_M1 / /I2C5_SCL_M1 / HDMI_RX_HPDIN_M0 / PCIE30X4_PERSTN_M1 / BT1120_D12 / CIP_D12 / GPIO4_B6_d
/	/SPI3_CLK_M1 / /I2C5_SDA_M1 / HDMI_RX_SCL_M0 / PCIE30X1_2_CLKREQN_M1 / BT1120_D13 / CIP_D13 / GPIO4_B7_u
SPDIFO_TX_M2	/PWMI6_M1 / SPI3_CS1_M1 / /I2C8_SDA_M3 / HDMI_RX_CEC_M0 / PCIE30X1_2_PERSTN_M1 / BT1120_D15 / CIP_D15 / GPIO4_C0_u

Figure 2-127 RK3588 HDMI_RX_CEC M0 Function Pin

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S8_MCLK	/ SDIO_D0_M1	/ GMAC1_TXD2	/ GPIO3_A0_u	AA29	
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_D1_M2	/ I2S8_SCLK	/ SDIO_D1_M1	/ GMAC1_RXD3	/ GPIO3_A1_u	
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_RX_M1	/	/ FSPI_D2_M2	/ I2S8_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u	
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S8_SDO	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u	
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S8_SDI	/ SDIO_CMD_M1	/ GMAC1_TXCLK	/ GPIO3_A4_d	
	/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	
	/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLK0_25M	/ GPIO3_A6_d	
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXDO	/ GPIO3_A7_u	
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_RXDI	/ GPIO3_B0_u	
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_RX_M2	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d	
	/	/ UART2_RTSN	/	/	/ I2S2_SDO_M1	/	/ GMAC1_TXDO	/ GPIO3_B3_u	
	/	/ UART2_CTSN	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_TXDI	/ GPIO3_B4_u	
PWM12_M0	/ CAN1_RX_M0	/ UART3_RX_M1	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_TXEN	/ GPIO3_B5_u	
PWM13_M0	/ CAN1_TX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d	
	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_RX1_HPD_M1	/	/ GMAC1_PTP_REF_CLK	/ GPIO3_B7_d	AA28	
	/	/ UART7_RX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/ GMAC1_PPSTTRIG	/ GPIO3_C0_d	Y29	
	/ PCIE30X1_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPCLK	/ GPIO3_C1_d	Y27
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d	Y31
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d	Y30
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_RX_M1	/ FSPI_CS0N_M2	/ SPI3_CS0_M3	/ HDMI_RX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u	AH26
CAN2_RX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1N_M2	/ SPI3_CS1_M3	/ HDMI_RX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u	AH25
	/ PCIE30X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_RX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AG26
	/ PCIE30X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_RX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AJ24
PWM8_M2	/ PCIE30X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_RX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u	AH24
PWM9_M2	/ PCIE30X1_2_PERSTN_M0	/ UART4_RX_M1	/	/ SPI0_MISO_M3	HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d	AG23
	/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M3	/ HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d	AG25
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d	AG24
	/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M3	/ HDMI_RX_HPDIN_M1	/ HDMI_RX_HPD_M1	/ MCU_JTAG_TCK_M1	/ GPIO3_D4_d	AA27
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART9_RX_M2	/	/ SPI0_CS1_M3	/ DP1_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

Figure 2-128 RK3588 HDMI_RX_CEC M1 Function Pin

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

	/ SPI4_MISO_M2	/ PCIE30X1_1_CLKREQN_M2	/ DP0_HPDIN_M2	/ I2C2_SDA_M4	/ UART6_RX_M1	/ GPIO1_A0_d	A24		
SATA1_ACT_LED_M1	/	/ SPI4_MOSI_M2	/ PCIE30X1_1_WAKEN_M2	/ DP1_HPDIN_M2	/ I2C2_SCL_M4	/ UART6_TX_M1	/ GPIO1_A1_d	A25	
	/ PWM0_M2	/ SPI4_CLK_M2	/	/ VOP_POST_EMPTY	/ I2C4_SDA_M3	/ UART6_RTSN_M1	/ GPIO1_A2_d	A26	
	/ PWM1_M2	/ SPI4_CS0_M2	/	/ HDMI_RX1_SDA_M2	/ I2C4_SCL_M3	/ UART6_CTSN_M1	/ GPIO1_A3_d	A27	
	/	/ SPI4_MISO_M0	/	/ HDMI_RX1_SCL_M2	/	/	/ GPIO1_A4_d	B25	
	/	/ SPI4_MOSI_M0	/	/ HDMI_RX0_HPD_M0	/	/	/ GPIO1_A5_d	B26	
	/	/ SPI2_CLK_M0	/	/ HDMI_RX1_HPD_M0	/	/	/ GPIO1_A6_d	C24	
	/ PWM3_IR_M3	/ SPI2_CS0_M0	/ PCIE30X1_1_PERSTN_M2	/	/ PDM1_SD10_M1	/	/ GPIO1_A7_u	C25	
	/	/ SPI2_CS1_M0	/ PCIE30X4_CLKREQN_M3	/	/ PDM1_SD11_M1	/	/ GPIO1_B0_u	C27	
	/	/ SPI0_MISO_M2	/ PCIE30X4_WAKEN_M3	/	/ PDM1_SD12_M1	/	/ GPIO1_B1_d	D25	
	/	/ SPI0_MOSI_M2	/ PCIE30X4_PERSTN_M3	/	/ PDM1_SD13_M1	/ UART4_RX_M2	/ GPIO1_B2_d	D26	
SATA0_ACT_LED_M1	/	/ SPI0_CLK_M2	/ PCIE30X1_0_WAKEN_M2	/	/ PDM1_CLK1_M1	/ UART4_TX_M2	/ GPIO1_B3_d	D27	
	/	/ SPI0_CS0_M2	/ PCIE30X1_0_PERSTN_M2	/	/ PDM1_CLK0_M1	/ UART7_RX_M2	/ GPIO1_B4_u	E24	
	/	/ SPI0_CS1_M2	/ PCIE30X1_0_CLKREQN_M2	/	/	/ UART7_TX_M2	/ GPIO1_B5_u	E25	
HDMI_RX_HPDIN_M2	/	/ SPDIFO_RX_M0	/ PCIE30X2_WAKEN_M3	/ MIPI_CAMERA1_CLK_M0	/ I2C5_SCL_M3	/ UART1_TX_M1	/ GPIO1_B6_u	E26	
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	/ PWM13_M2	/ SPDIFI_RX_M0	/ PCIE30X2_PERSTN_M3	/ MIPI_CAMERA2_CLK_M0	/ I2C5_SDA_M3	/ UART1_RX_M1	/ GPIO1_B7_u	E27
HDMI_RX_SCL_M2	/ PWM14_M2	/	/	/ MIPI_CAMERA3_CLK_M0	/ I2C8_SCL_M2	/ UART1_RTSN_M1	/ GPIO1_D6_u	F24	
HDMI_RX_SDA_M2	/ PWM15_IR_M3	/	/ PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0	/ I2C8_SDA_M2	/ UART1_CTSN_M1	/ GPIO1_D7_u	F25	

Figure 2-129 RK3588 HDMI_RX_CEC M2 Function Pin

The CEC protocol stipulates that it is 3.3V level. If the selected IO belongs to 3.3V IO, then due to the protocol requirements, add 3.3V voltage to the CEC pin through a 56K resistor, and the leakage is not allowed to exceed 1.8uA, and the MOS tube cannot be omitted.

Test ID 7-15: CEC Line Degradation

Reference	Requirement
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device). Maximum CEC line leakage current must be $\leq 1.8\mu A$

Figure 2-130 HDMI CEC Protocol Requirements

When the RK3588 IO Domain is not powered on, if there is voltage on the IO, the IO will have leakage current. For example, the RK3588 has been powered off, and the HDMI cable is still connected to the Source. Leakage to RK3588 IO through HDMI cable will cause CEC leakage to exceed 1.8uA, so an isolation circuit needs to be added externally. Equivalently, if the junction capacitance is too large, it will not only affect the work, but also fail to pass the certification.

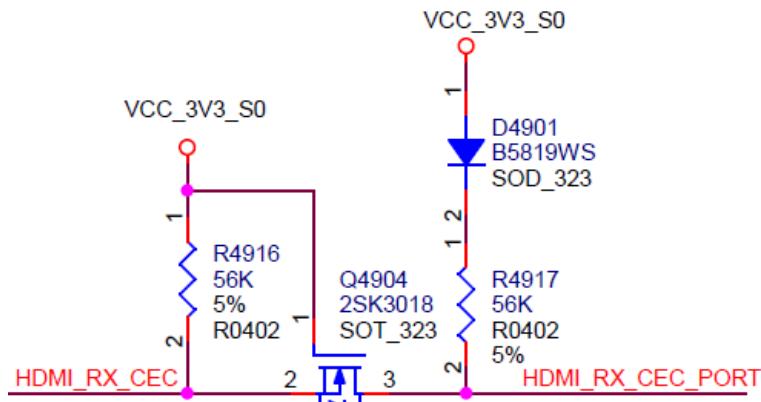


Figure 2-131 HDMI RX CEC Isolation Circuit

HDMI_RX_DDC_SCL/DDC_SDA is the I2C/DDC bus of the HDMI RX controller. The functions are multiplexed to the IO of the PMUIO2, VCCIO5, and VCCIO4 power domains. Resistive power supplies must also be adjusted synchronously.

The DDC_SCL/DDC_SDA protocol stipulates that the level is 5V. The RK3588 IO does not support the 5V level. The level conversion circuit must be added and must not be deleted. The MOS tube level conversion is used by default. The MOS model selects 2SK3018 by default. The capacitance must be equivalent. If the junction capacitance is too large, it will not only affect the work, but also fail to pass the certification.

The pull-up resistor is recommended to refer to the default value and cannot be modified at will.

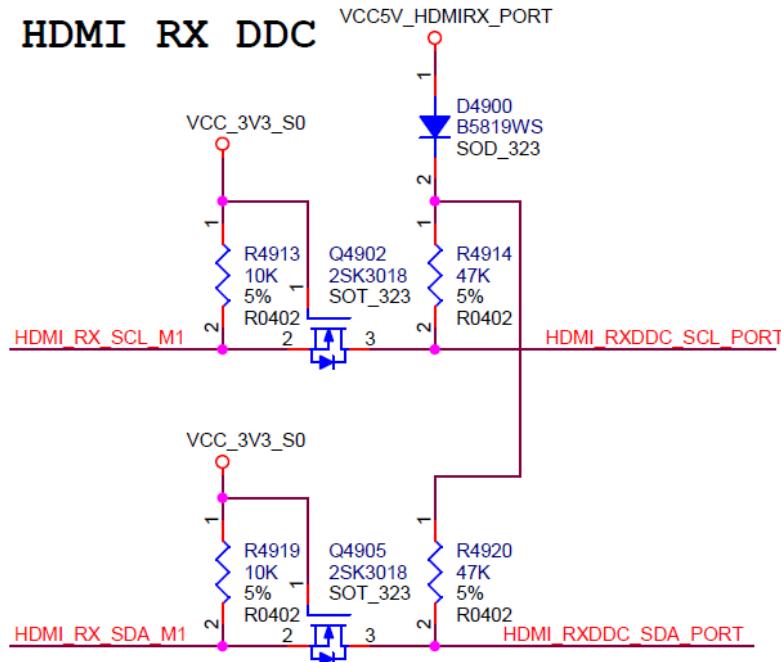


Figure 2-132 HDMI RX DDC Level Conversion Circuit

It is recommended to place a 0.1uF decoupling capacitor on the Pin18 pin of the HDMI socket, and place it close to the HDMI socket pin during layout. In order to strengthen the anti-static ability, ESD devices must be reserved on the signal. The ESD parasitic capacitance of HDMI2.0 signal should not exceed 0.4pF, and the ESD parasitic capacitance of other signals should not exceed 1pF.

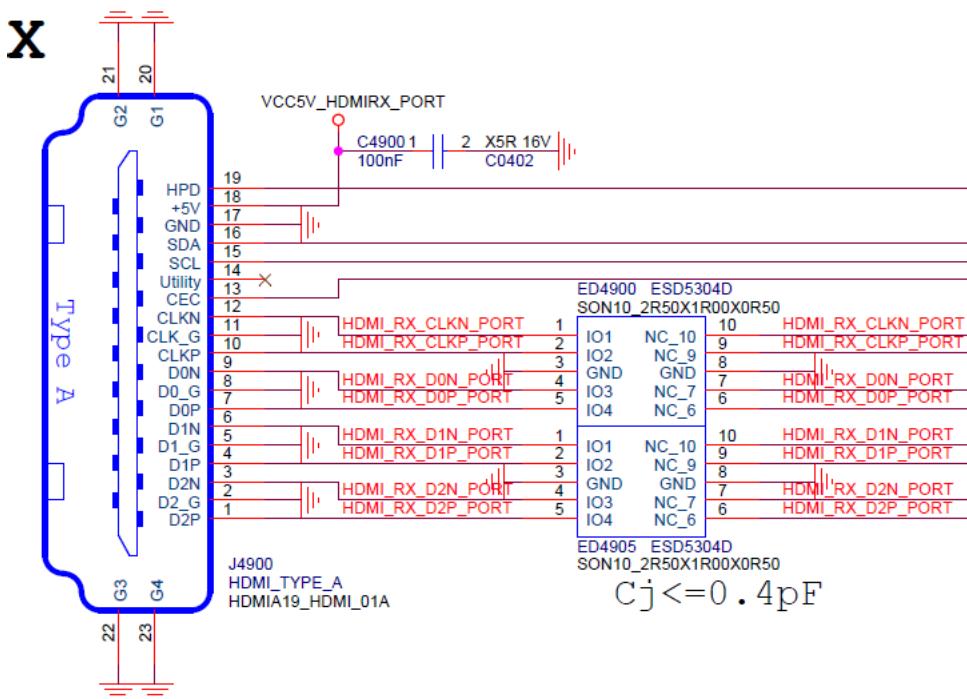


Figure 2-133 HDMI RX Socket ESD Circuit

HDMI RX interface matching design recommendations are shown in the following table:

Table 2-25 RK3588 HDMI RX Interface Design

Signal	Connection method	Description
HDMI_RX_D0P/D0N	2.2ohm resistor in series	TMDS data Lane0 input
HDMI_RX_D1P/D1N	2.2ohm resistor in series	TMDS data Lane1 input
HDMI_RX_D2P/D2N	2.2ohm resistor in series	TMDS data Lane2 input
HDMI_RX_D3P/D3N	2.2ohm resistor in series	TMDS clock input
HDMI_RX_RECT	200ohm 1% resistance to ground	HDMI_RX PHY external reference resistance
HDMI_RX_HPD	MOS control circuit	HDMI HPD output
HDMI_RX_CEC	MOS isolation circuit	HDMI CEC signal
HDMI_RX_SCL	MOS level conversion	HDMI DDC clock
HDMI_RX_SDA	MOS level conversion	HDMI DDC data input and output

2.3.8 Video Output Interface Circuit

The VOP controller of the RK3588 chip has 4 Port outputs and supports DP0/DP1/HDMI0/eDP0/HDMI1/eDP1/MIPI DSI0/MIPI DSI1/BT656/BT1120 video interface output.

A maximum of standard 4 different displays are allowed, such as 4K+4K+4K+2K. If you want to support 8K, then only 8K+4K+2K is supported (8K is implemented through the combination of Post Process0+Post Process1).

VOP and video interface output path diagram:

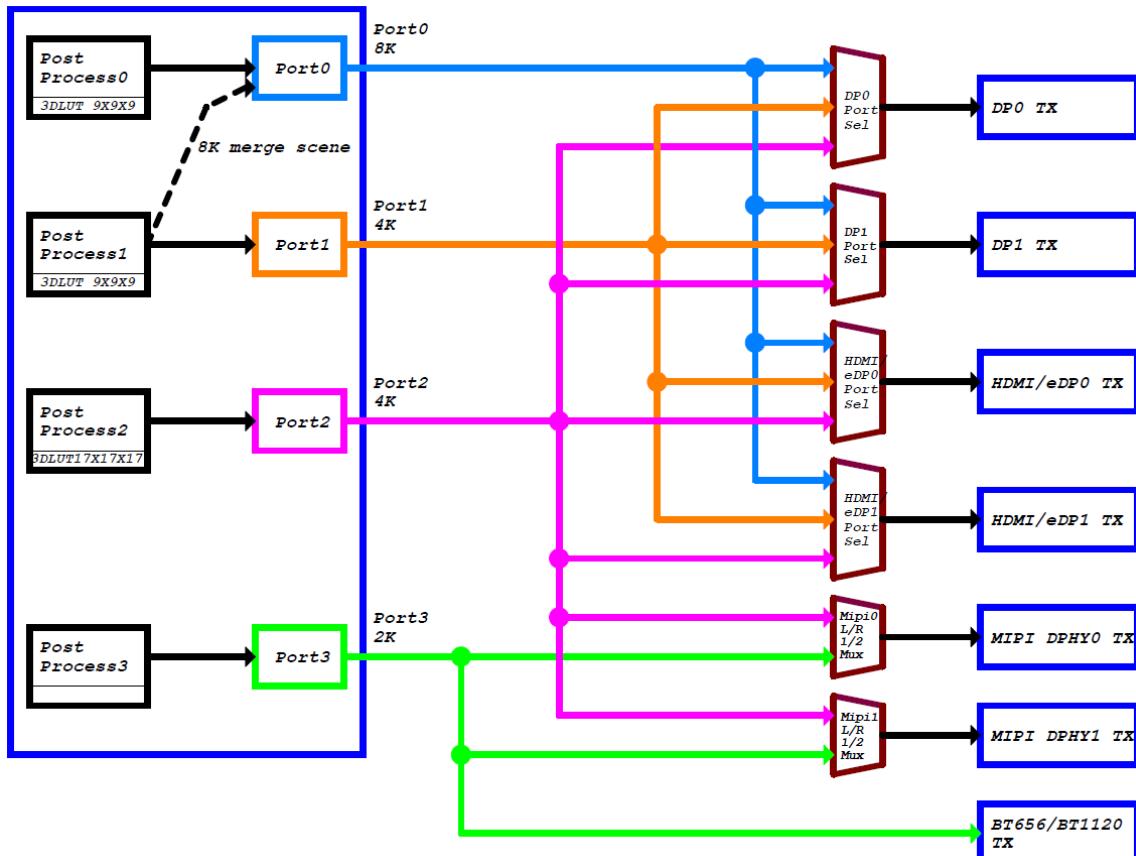


Figure 2-134 RK3588 VOP and Video Interface Output Path Diagram

2.3.8.1 HDMI2.1/eDP TX Interface

RK3588 has build in 2 HDMI/eDP TX Combo PHY.

HDMI/eDP TX Combo PHY support the following two modes:

- HDMI TX mode: Maximum resolution support 8K@60Hz, support RGB/YUV444/YUV420 (Up to 10bit) format;
- eDP TX mode: Maximum resolution support 4K@60Hz, support RGB/YUV422(Up to 10bit) format.

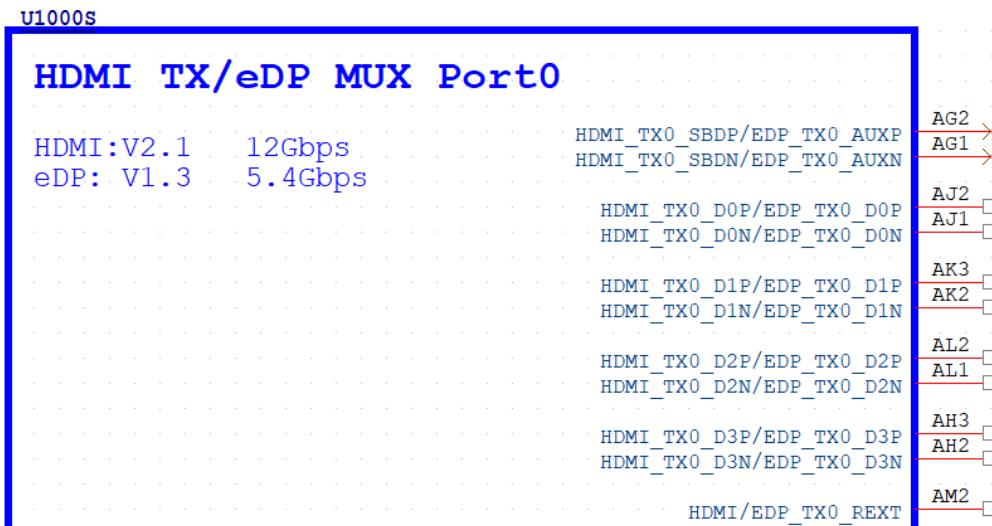


Figure 2-135 RK3588 HDMI/eDP Combo PHY0 Pin

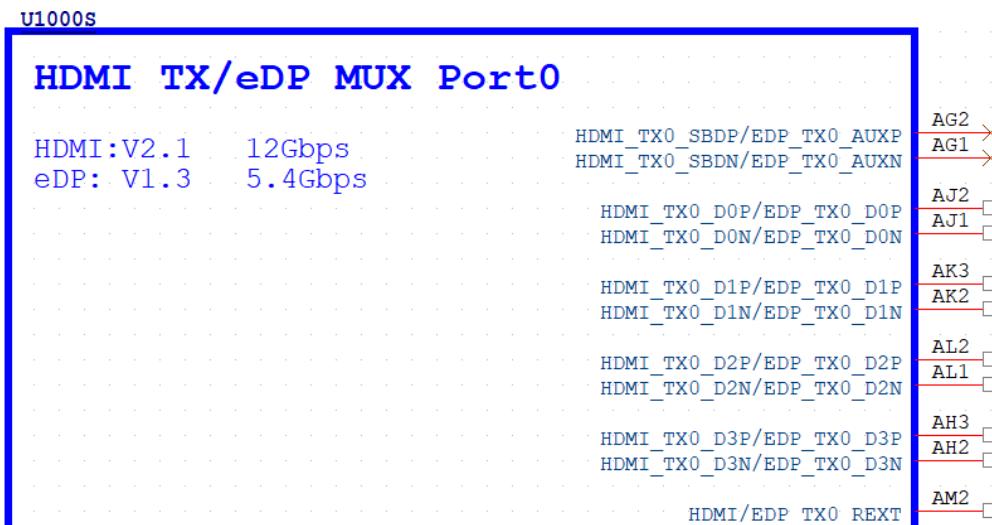


Figure 2-136 RK3588 HDMI/eDP Combo PHY1 Pin

HDMI/eDP Combo PHY0/1 power pins need to placed 4.7uF, 1uF and 100nF decoupling capacitors, which cannot be deleted. Place them close to the RK3588 pin during layout.

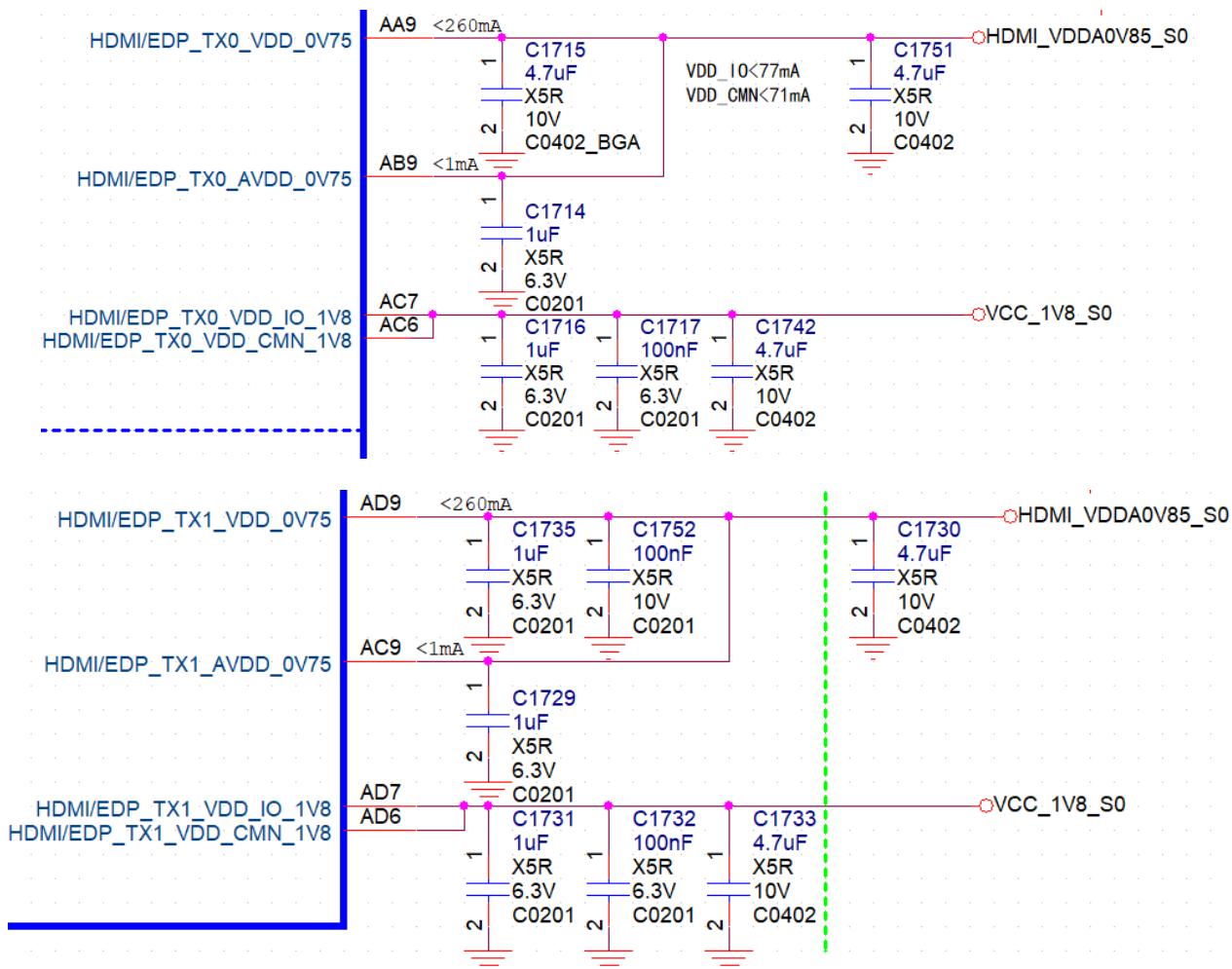


Figure 2-137 HDMI/eDP Combo PHY0/1 Power Decoupling Capacitor

HDMI/EDP_TX0_REXT/HDMI/EDP_TX1_REXT is the external reference resistor pin of HDMI/eDP Combo PHY0/1. It is an external 8200ohm resistor with an accuracy of 1% to ground. The resistor value should not be changed. It should be placed close to the RK3588 chip pin during layout.

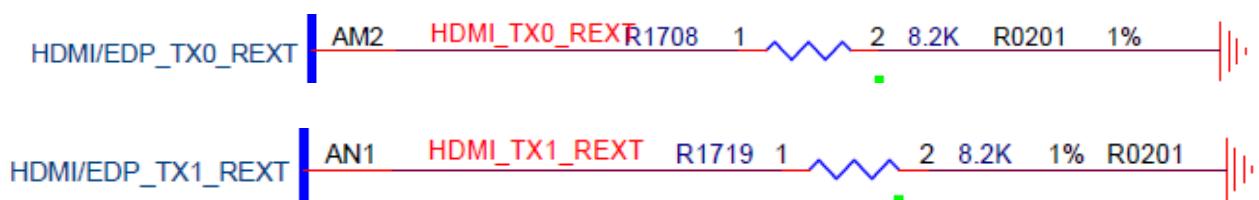


Figure 2-138 RK3588 HDMI/EDP_TX0_REXT/HDMI/EDP_TX1_REXT Pin

- HDMI2.1 TX mode

RK3588 supports HDMI2.1 and is backward compatible with HDMI2.0 and HDMI1.4. Since HDMI2.1 works in FRL mode, when switching to HDMI2.0 and below modes, it works in TMDS mode, and AC-coupled voltage mode driver should be used.

As shown in the figure below, the capacitance value of the AC coupling capacitor is 220nF and cannot be changed arbitrarily. It is recommended to use the 0201 package for the AC coupling capacitor. The lower ESR and

ESL can also reduce the impedance change on the line.

Take HDMI TX0 as an example, HDMI TX1 and HDMI TX0 are the same.

- Working in HDMI2.1 mode, HDMI0_TX_ON_H is configured as low level, Q5003, Q5004, Q5006, and Q5007 are non-conducting.
- When working in HDMI2.0 and below mode, HDMI0_TX_ON_H is configured to high level. At this mode, only Q5003 is required, and the other three Q5004, Q5005, Q5006 can not be welded, welded with R5040, R5041, R5042. The 590ohm resistance of the ground and the 50ohm resistance on the Sink end to form a DC bias, about 3V.

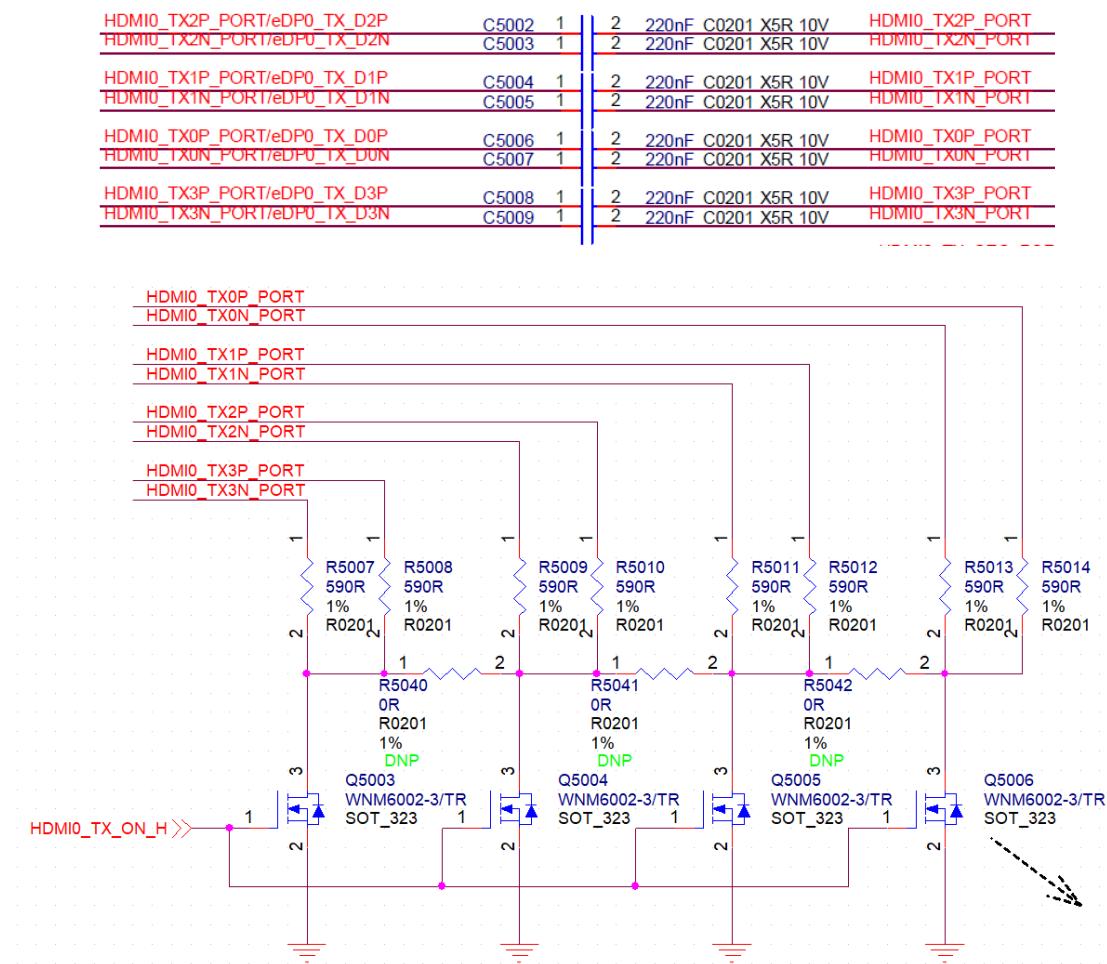


Figure 2-139 RK3588 HDMI TX Mode Peripheral Circuit



Note

1: If you only need to support HDMI2.0 and below modes, Q5007, Q5004, Q5005, Q5006 cannot be omitted. It is necessary to ensure that the tube cannot be turned on when the machine is not turned on, because HDMI CTS Test ID 7-3 TMDS Voff test item requirements. When the DUT is not powered on, the Voff voltage must be within AVcc+-10mV, otherwise this test item will fail.

2: The Coss of the control MOS tube should not be too large, otherwise it will affect the signal quality. It is recommended to refer to the model of the reference diagram or the corresponding Coss value.

FRL mode: Under the traditional TMDS architecture, an independent channel is used to transmit the Clock, but in the FRL architecture, the Clock is embedded in the Data channel, and the Clock is parsed out through Clock Recovery on the sink side.

Table 2-26 FRL Rate and Channel Relationship

Channel rate	Channel quantity
3Gbps	3
6Gbps	3
6Gbps	4
8Gbps	4
10Gbps	4
12Gbps	4

The HPD signal on the HDMI2.1 connector is multiplexed with HDMI0_TX_SBDN. When the HDMI device is detected, HDMITX0_HPDIN_M0 outputs a high level to RK3588, and RK3588 starts the initial work of HDMI.

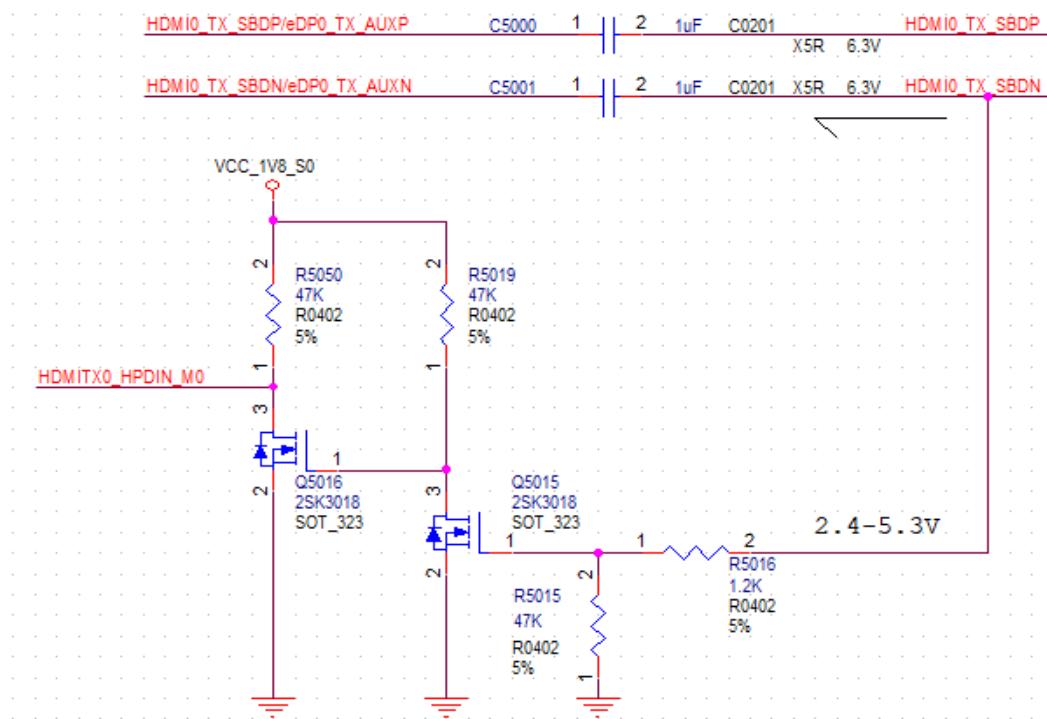


Figure 2-140 RK3588 HDMI TX0 HPD Circuit

HDMI_TX0_HPD is the function of multiplexing the HDMI TX controller to the common GPIO. The level varies with the voltage of the power supply domain, the power supply voltage of the power supply domain changes, and the pull-up resistor power supply of the peripheral circuit must also be adjusted synchronously.

HDMI_TX0/1_HPD are multiplexed in two different power domains, one is on the IO of the VCCIO4 power domain, and the other is on the IO of the VCCIO5 power domain.

VCCIO4 Domain		Operating Voltage=1.8V/3.3V			
SATA1_ACT_LED_M1 /	/	/SPI4_MISO_M2 /PCIE30X1_1_CLKREQN_M2 / DP0_HPDIN_M2	/I2C2_SDA_M4 /UART6_RX_M1	/GPIO1_A0_d	A2
	/	/SPI4_MOSI_M2 /PCIE30X1_1_WAKEN_M2 / DP1_HPDIN_M2	/I2C2_SCL_M4 /UART6_TX_M1	/GPIO1_A1_d	A2
	/	/PWM0_M2 /SPI4_CLK_M2 /	/VOP_POST_EMPTY /I2C4_SDA_M3	/UART6_RTSN_M1 /GPIO1_A2_d	A2
	/	/PWM1_M2 /SPI4_CSO_M2 /	/HDMI_TX1_SDA_M2 /I2C4_SCL_M3	/UART6_CTSN_M1 /GPIO1_A3_d	A2
	/	/SPI2_MISO_M0 /	/HDMI_TX1_SCL_M2 /	/	/GPIO1_A4_d
	/	/SPI2_MOSI_M0	HDMI_TX0_HPD_M0	/	/GPIO1_A5_d
	/	/SPI2_CLK_M0 /	HDMI_TX1_HPD_M0	/	/GPIO1_A6_d
	/	/PWM3_IR_M3 /SPI2_CSO_M0 /PCIE30X1_1_PERSTN_M2 /	/PDM1_SD10_M1 /	/GPIO1_A7_u	C2
	/	/SPI2_CS1_M0 /PCIE30X4_CLKREQN_M3 /	/PDM1_SD11_M1 /	/GPIO1_B0_u	C2
	/	/SPI0_MISO_M2 /PCIE30X4_WAKEN_M3 /	/PDM1_SD12_M1 /	/GPIO1_B1_d	D2
	/	/SPI0莫斯I_M2 /PCIE30X4_PERSTN_M3 /	/PDM1_SD13_M1 /UART4_RX_M2	/GPIO1_B2_d	D2
SATA0_ACT_LED_M1 /	/	/SPI0_CLK_M2 /PCIE30X1_0_WAKEN_M2 /	/PDM1_CLK1_M1 /UART4_TX_M2	/GPIO1_B3_d	D2
	/	/SPI0_CSO_M2 /PCIE30X1_0_PERSTN_M2 /	/PDM1_CLK0_M1 /UART7_RX_M2	/GPIO1_B4_u	E2
	/	/SPI0_CS1_M2 /PCIE30X1_0_CLKREQN_M2 /	/	/UART7_TX_M2	/GPIO1_B5_u
	HDMI_RX_HPDIN_M2 /	/SPDIFI0_TX_M0 /PCIE30X2_WAKEN_M3	/MIPI_CAMERA1_CLK_M0 /I2C5_SCL_M3	/UART1_RX_M1	/GPIO1_B6_u
SATA2_ACT_LED_M1 /	HDMI_RX_CEC_M2 /	PWM13_M2 /SPDIFI1_TX_M0 /PCIE30X2_PERSTN_M3	/MIPI_CAMERA2_CLK_M0 /I2C5_SDA_M3	/UART1_RX_M1	/GPIO1_B7_u
	HDMI_RX_SCL_M2 /	PWM14_M2 /	/MIPI_CAMERA3_CLK_M0 /I2C8_SCL_M2	/UART1_RTSN_M1 /GPIO1_D6_u	F2
	HDMI_RX_SDA_M2 /	PWM15_IR_M3 /PCIE30X2_CLKREQN_M3	/MIPI_CAMERA4_CLK_M0 /I2C8_SDA_M2	/UART1_CTSN_M1 /GPIO1_D7_u	F2

Figure 2-141 RK3588 HDMI_TX0/1_HPD M0 Function Pin

VCCIO5 Domain									
Operating Voltage=1.8V/3.3V									
PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S3_MCLK	/ SDIO_D0_M1	/ GMAC1_RXD2	/ GPIO3_A0_u	AA29
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_D1_M2	/ I2S3_SCLK	/ SDIO_D1_M1	/ GMAC1_TXD3	/ GPIO3_A1_u	AA30
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_RX_M1	/	/ FSPI_D2_M2	/ I2S3_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u	AD27
AUDDSM_RP	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S3_SD0	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u	AE27
AUDDSM_PP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S3_SDI	/ SDIO_CMD_M1	/ GMAC1_RXCLK	/ GPIO3_A4_d	AD28
	/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	AH30
	/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLK_25M	/ GPIO3_A6_d	AH27
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXD0	/ GPIO3_A7_u	AG29
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_RXD1	/ GPIO3_B0_u	AG28
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_RX_M2	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	AH29
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d	AE28
	/	/ UART2_RTSN	/	/	/ I2S2_SD0_M1	/	/ GMAC1_RXD0	/ GPIO3_B3_u	AC28
	/	/ UART2_CTSN	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_RXD1	/ GPIO3_B4_u	AC29
PWM12_M0	/ CAN1_RX_M0	/ UART8_RX_M1	/	/	/ I2S2_SCLK_RX_M1	/	/ GMAC1_TXEN	/ GPIO3_B5_u	AD29
PWM13_M0	/ CAN1_TX_M0	/ UART8_RX_M1	/	/	/ I2S2_LRCK_RX_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d	AE29
	/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_TX1_HPD_M1	/	/ GMAC1_PTF_REF_CLK	/ GPIO3_B7_d	AA28
	/	/	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d	Y29
	/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPSCLK	/ GPIO3_C1_d	Y27
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C3_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d	Y31
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDI0	/ GPIO3_C3_d	Y30
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_RX_M1	/ FSPI_CS0N_M2	/ SPI3_CS0_M3	/ HDMI_TX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u	AH26
CAN2_TK_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1N_M2	/ SPI3_CS1_M3	/ HDMI_TX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u	AH25
	/ PCIE30X4_PERTSN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_TX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AG26
	/ PCIE20X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_TX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AJ24
PWM8_M2	/ PCIE20X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_TX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u	AH24
PWM9_M2	/ PCIE20X1_2_PERTSN_M0	/ UART4_RX_M1	/	/ SPI3_MISO_M3	/ HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d	AG23
	/ PCIE30X2_CLKREQN_M2	/ UART8_RTSN_M2	/ I2C7_SCL_M2	/ SPI10_MOSI_M3	/ HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d	AG25
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART8_CTSN_M2	/ I2C7_SDA_M2	/ SPI10_CLK_M3	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d	AG24
	/ PCIE30X2_PERTSN_M2	/ UART8_RX_M2	/	/ SPI10_CS0_M3	/ HDMI_RX_HPDIN_M1	/ HDMI_TX0_HPD_M1	/ MCU_JTAG_TCK_M1	/ GPIO3_D4_d	AA27
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART8_RX_M2	/	/ SPI10_CS1_M3	/ DPL_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

Figure 2-142 RK3588 HDMI_TX0/1_HPD M1 Function Pin

HDMI_TX0_CEC is the function of multiplexing the CEC function of the HDMI controller to the ordinary GPIO. The level varies with the voltage of the power supply domain, the power supply voltage of the power supply domain changes, and the pull-up resistor power supply of the peripheral circuit must also be adjusted synchronously.

HDMI_TX0_CEC multiplexes two positions, one is on the IO of the VCCIO6 power domain, and the other is on the IO of the PMUIO2 power domain.

HDMI_TX1_CEC multiplexes three positions, one on the IO of the VCCIO3 power domain, one on the IO of the PMUIO2 power domain, and one on the IO of the VCCIO5 power domain.

VCCIO6 Domain	
Operating Voltage=1.8V/3.3V	
/ SPI0_MISO_M1	/ UART5_RTSN_M1 /
/ SPI0_MOSI_M1	/ UART5_CTSN_M1 /
/ SPI0_CLK_M1	/
/	UART0_TX_M2 /
/ SPI2_MISO_M1	/ UART0_RX_M2 / I2C3_SCL_M2
/ SPI2_MOSI_M1	/ UART3_TX_M2 / I2C3_SDA_M2
/ SPI2_CLK_M1	/ UART3_RX_M2 / I2C5_SCL_M2
/ SPI2_CS0_M1	/
/ SPI2_CS1_M1	/ UART5_RX_M0 / I2C6_SDA_M3
SATA2_ACT_LED_M0	/ SPDIF1_TX_M1 / SPI0_CS1_M1
CANL_RX_M1	/ PWM14_M1 / SPI0_CS0_M1
CANL_TX_M1	/ PWM15_IR_M1 /
SPDIFO_RX_M1	/ PWM11_IR_M1 / DPO_HPDIN_M0
SATA1_ACT_LED_M0	/ PWM12_M1 / SPI3_MISO_M1
SATA0_ACT_LED_M0	/ PWM13_M1 / SPI3_MOSI_M1
/	/ SPI3_CLR_M1 /
/	/ SPI3_CS0_M1 /
SPDIF1_RX_M2	/ PWM6_M1 / SPI3_CS1_M1 /
	/ I2S1_MCLK_M0 / PCIE30X1_1_CLKREQN_M1 / BT1120_D0 / CIF_D0 / GPIO4_A0_d
	/ I2S1_SCLK_RX_M0 / PCIE30X1_1_WAKEN_M1 / BT1120_D1 / CIF_D1 / GPIO4_A1_d
	/ I2S1_LRCK_RX_M0 / PCIE30X1_1_PERSTN_M1 / BT1120_D2 / CIF_D2 / GPIO4_A2_d
	/ I2S1_SCLK_RX_M0 / PCIE30X1_0_CLKREQN_M1 / BT1120_D3 / CIF_D3 / GPIO4_A3_d
	/ I2S1_LRCK_RX_M0 / PCIE30X1_0_WAKEN_M1 / BT1120_D4 / CIF_D4 / GPIO4_A4_d
	/ I2S1_SD10_M0 / PCIE30X1_0_PERSTN_M1 / BT1120_D5 / CIF_D5 / GPIO4_A5_d
	/ I2S1_SD11_M0 / PCIE30X2_CLKREQN_M1 / BT1120_D6 / CIF_D6 / GPIO4_A6_d
	/ I2S1_SD12_M0 / PCIE30X2_WAKEN_M1 / BT1120_D7 / CIF_D7 / GPIO4_A7_d
	/ I2S1_SD13_M0 / PCIE30X2_PERSTN_M1 / BT1120_CLKOUT / CIF_CLKIN / GPIO4_B0_d
	/ I2S1_SD00_M0 / PCIE30X1_0_BUTTON_RSTN / MIPI_CAMERA0_CLK_M0 / GPIO4_B1_u
	/ I2S1_SD01_M0 / PCIE30X1_1_BUTTON_RSTN / BT1120_D8 / CIF_HREF / GPIO4_B2_u
	/ I2S1_SD02_M0 / PCIE30X1_2_BUTTON_RSTN / BT1120_D9 / CIF_VSYNC / GPIO4_B3_u
	/ I2S1_SD03_M0 / PCIE30X4_CLKREQN_M1 / BT1120_D10 / CIF_CLKOUT / GPIO4_B4_u
	/ HDMI_RX_CEC_M0 / PCIE30X4_WAKEN_M1 / BT1120_D11 /
	/ I2C5_SCL_M1 / HDMI_RX_HPDIN_M0 / PCIE30X4_PERSTN_M1 / BT1120_D12 /
	/ I2C5_SDA_M1 / HDMI_RX0_SCL_M0 / PCIE30X1_0_CLKREQN_M1 / BT1120_D13 /
	/ I2C8_SDA_M3 / HDMI_RX0_SDA_M0 / PCIE30X1_0_WAKEN_M1 / BT1120_D14 /
	/ I2C8_SCL_M3 / HDMI_RX0_CEC_M0 / PCIE30X1_0_PERSTN_M1 / BT1120_D15 /

Figure 2-143 RK3588 HDMI_TX0_CEC M0 Function Pin

VCCIO3 Domain	
Operating Voltage=1.8V	
/ UART6_RX_M0	/ FSPI_D0_M1 / SDIO_D0_M0 / GMAC0_RXD2 / GPIO2_A6_u
/ UART6_TX_M0	/ FSPI_D1_M1 / SDIO_D1_M0 / GMAC0_RXD3 / GPIO2_A7_u
I2C8_SCL_M1	/ UART6_RTSN_M0 / FSPI_D2_M1 / SDIO_D2_M0 / GMAC0_RXCLK / GPIO2_B0_u
I2C8_SDA_M1	/ UART6_CTSN_M0 / FSPI_D3_M1 / SDIO_D3_M0 / GMAC0_TXD2 / GPIO2_B1_u
I2C3_SCL_M3	/
I2C3_SDA_M3	/ FSPI_CLK_M1 / SDIO_CMD_M0 / GMAC0_TXD3 / GPIO2_B2_u
I2C4_SDA_M1	/ UART7_RX_M0 / FSPI_CS0_M1 / HDMI_TX1_SDA_M0 / GMAC0_PTP_REFCLK / GPIO2_B4_u
I2C4_SCL_M1	/ UART7_TX_M0 / FSPI_CS1_M1 / HDMI_TX1_SCL_M0 / GMAC0_PPSTRIK / GPIO2_B5_u
I2C3_SCL_M4	/ UART1_RX_M0 / I2S2_MCLK_M0 / GMAC0_TXD0 / GPIO2_B6_d
I2C5_SDA_M4	/ UART1_TX_M0 / I2S2_SCLK_TX_M0 / GMAC0_TXD1 / GPIO2_B7_d
I2C2_SDA_M1	/ UART1_RTSN_M0 / SPI1_CLK_M0 / I2S2_LRCK_RX_M0 / GMAC0_TXEN / GPIO2_C0_d
I2C2_SCL_M1	/ UART1_CTSN_M0 / SPI1_MISO_M0 / I2S2_SCLK_RX_M0 / GMAC0_RXDO / GPIO2_C1_d
I2C6_SDA_M2	/ UART9_RX_M0 / SPI1_MOSI_M0 / I2S2_LRCK_RX_M0 / GMAC0_RXDI / GPIO2_C2_d
I2C6_SCL_M2	/
TEST_CLKOUT_M1	/ UART9_RX_M0 / SPI1_CS1_M0 / HDMI_TX1_CEC_M0 / GMAC0_PPCLK / GPIO2_C3_d
/	/ CLK32K_OUT1 /
/ UART7_RTSN_M0	/ SPI3_CS0_M0 / PWM2_M2 / GMAC0_RXDV_CRS / GPIO4_C2_d
I2C7_SCL_M1	/ PWM4_M1 / SPI3_CS1_M0 / I2S2_SDO_M0 / GMAC0_MCLKINOUT / GPIO4_C3_d
I2C7_SDA_M1	/ UART9_RTSN_M0 / SPI3_MISO_M0 / PWM5_M2 / GMAC0_MDC / GPIO4_C4_d
I2C0_SCL_M1	/ UART9_CTSN_M0 / SPI3_MOSI_M0 / PWM6_M2 / GMAC0_MDIO / GPIO4_C5_d
I2C0_SDA_M1	/ UART7_CTSN_M0 / SPI3_CLK_M0 / PWM7_IR_M3 / GMAC0_TXER / GPIO4_C6_d

VCCIO3_1V8

Figure 2-144 RK3588 HDMI_TX1_CEC M0 Function Pin

PMUIO2 Domain

Operating Voltage=1.8V/3.3V

/UART2_RX_M0	/	/	/I2S1_MCLK_M1	/PCIE30X1_1_CLKREQN_M0	/I2C1_SCL_M0	/JTAG_TCK_M2	/GPIO0_B5_d	P29	
/UART2_RX_M0	/	/	/I2S1_SCLK_TX_M1	/PCIE30X1_1_WAKEN_M0	/I2C1_SDA_M0	/JTAG_TMS_M2	/GPIO0_B6_d	R29	
/CAN0_RX_M0	/	/	/I2S1_LRCK_TX_M1	/PCIE30X1_1_PERSTN_M0	/SPI0_CS1_M0	/I2C2_SCL_M0	/PWR0_M0	T28	
CAN0_RX_M0	/	/	/I2S1_SCLK_RX_M1	/PCIE30X1_0_CLKREQN_M0	/SPI0_MOSI_M0	/I2C2_SDA_M0	/PWR1_M0	/GPIO0_C0_d	
/CAN0_RX_M0	/	/	/	/	/	/	/PMIC_SLEEP3	U32	
/CAN0_RX_M0	/	/	/	/	/	/	/PMIC_SLEEP4	/GPIO0_C1_d	
/CAN0_RX_M0	/	/	/	/	/	/	/PMIC_SLEEP5	/GPIO0_C3_d	
/UART0_RX_M0	/DP0_HPDIN_M1	/PD0_CLK1_M1	/I2S1_LRCK_RX_M1	/PCIE30X1_0_WAKEN_M0	/I2C4_SDA_M2	/PWR2_M0	/GPIO0_C4_d	R30	
PWR4_M0	/UART0_RX_M0	/DP1_HPDIN_M1	/I2S1_SDIO_M1	/PCIE30X1_0_PERSTN_M0	/I2C4_SCL_M2	/GPU_AVIS	/GPIO0_C5_u	P30	
PWR5_M1	/UART1_RTSN	/SATA_C_POD	/I2S1_SD1_M1	/PCIE30X4_CLKREQN_M0	/SPI0_CLK_M0	/NPV_AVIS	/GPIO0_C6_u	T29	
/UART1_RTSN_M2	/	/PD0_MSDIO_M1	/I2S1_SD2_M1	/PCIE30X4_WAKEN_M0	/SPI0_MISO_M0	/I2C6_SDA_M0	/PWR4_M0	/GPIO0_C7_d	
HDMI_TX0_CEC_M1	UART1_RX_M2	/UART0_CTSN	/HDMI_RX_SDA_M0	/I2S1_SD0_M1	/PCIE30X2_CLKREQN_M0	/SPI0_CS0_M0	/I2C0_SCL_M2	/CPU_B10_AVIS	/GPIO0_D1_u
HDMI_TX1_CEC_M1	UART1_RX_M2	/	/HDMI_RX_SCL_M0	/I2S1_SD01_M1	/PCIE30X2_WAKEN_M0	/SPI3_MOSI_M2	/I2C0_SDA_M2	/	/GPIO0_D2_u
/	/	/	/	/	/	/SPI3_CLK_M2	/	/LITCPU_AVIS	/GPIO0_D3_u
HDMI_TX0_SDA_M1	/SATA_C_PDET	/CAN2_RX_M1	/PD0_MSD12_M1	/I2S1_SD02_M1	/PCIE30X2_PERSTN_M0	/SPI3_CS0_M2	/I2C1_SCL_M2	/PWR3_IR_M0	/GPIO0_D4_u
HDMI_TX0_SCL_M1	/SATA_MP_SWITCH	/CAN2_RX_M1	/	/I2S1_SD03_M1	/	/SPI3_CS1_M2	/I2C1_SDA_M2	/CPU_B10_AVIS	/GPIO0_D5_u
/	/PD0_SD13_M1	/	/	/	/	/	/PMIC_SLEEP6	/GPIO0_D6_d	W28

Figure 2-145 RK3588 HDMI_TX0/1_CEC M1 Function Pin

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/SPI4_MISO_M1	/	/I2C6_SDA_M4	/FSPI_D0_M2	/I2S3_MCLK	/SDIO_D0_M1	/GMAC1_TKD1	/GPIO3_A0_u	AA29
AUDDSM_LN	/SPI4_MOSI_M1	/PWN11_IR_M0	/I2C6_SCL_M4	/FSPI_D1_M2	/I2S3_SCLK	/SDIO_D1_M1	/GMAC1_TKD3	/GPIO3_A1_u	AA30
AUDDSM_LP	/SPI4_CLK_M1	/UART8_RX_M1	/	/FSPI_D2_M2	/I2S3_LRCK	/SDIO_D2_M1	/GMAC1_RXD2	/GPIO3_A2_u	AD27
AUDDSM_RM	/SPI4_CS0_M1	/UART8_RX_M1	/	/FSPI_D3_M2	/I2S3_SDO	/SDIO_D3_M1	/GMAC1_RXD3	/GPIO3_A3_u	AE27
AUDDSM_RF	/SPI4_CS1_M1	/UART8_RTSN_M1	/	/	/I2S3_SDI	/SDIO_CMD_M1	/GMAC1_RXCLK	/GPIO3_A4_d	AD28
/	/MIPI_CAMERA0_CLK_M1	/UART8_CTSN_M1	/I2C4_SDA_M0	/FSPI_CLK_M2	/	/SDIO_CLK_M1	/GMAC1_RXCLK	/GPIO3_A5_d	AH30
/	/MIPI_CAMERA1_CLK_M1	/	/I2C4_SCL_M0	/	/	/	/ETH1_REFCLKO_25M	/GPIO3_A6_d	AH27
PWN8_M0	/MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/GMAC1_RXD0	/GPIO3_A7_u	AG29
PWN8_M0	/MIPI_CAMERA3_CLK_M1	/	/	/	/I2S2_SCLK_RX_M1	/	/GMAC1_RXD1	/GPIO3_B0_u	AG28
PWN2_M1	/MIPI_CAMERA4_CLK_M1	/UART2_RX_M2	/	/	/I2S2_LRCK_RX_M1	/	/GMAC1_RXDV_CRS	/GPIO3_B1_d	AH29
PWN3_IR_M1	/	/UART2_RX_M2	/	/	/I2S2_SDI_M1	/	/GMAC1_RXER	/GPIO3_B2_d	AE28
/	/UART2_RTSN	/	/	/I2S2_SDO_M1	/	/GMAC1_RXD0	/GPIO3_B3_u	AC28	
/	/UART2_CTSN	/	/	/I2S2_MCLK_M1	/	/GMAC1_TKD1	/GPIO3_B4_u	AC29	
PWN12_M0	/CAN1_RX_M0	/UART3_RX_M1	/	/I2S2_SCLK_RX_M1	/	/GMAC1_TKD_N	/GPIO3_B5_u	AD29	
PWN13_M0	/CAN1_RX_M0	/UART3_RX_M1	/	/I2S2_LRCK_RX_M1	/	/GMAC1_MCLKINOUT	/GPIO3_B6_d	AE29	
/	/	/I2C3_SCL_M1	/SPI1_MOSI_M1	/HDMI_RX1_HPD_M1	/	/GMAC1_PTP_REF_CLK	/GPIO3_B7_d	AA28	
/	/UART7_RX_M1	/I2C3_SDA_M1	/SPI1_MISO_M1	/	/	/GMAC1_PPSTRIG	/GPIO3_C0_d	Y29	
/	/PCIE30X2_BUTTON_RSTN	/UART7_RX_M1	/	/SPI1_CLK_M1	/	/	/GMAC1_PPCLK	/GPIO3_C1_d	Y27
PWN14_M0	/	/UART7_RTSN_M1	/I2C8_SCL_M4	/SPI1_CS0_M1	/	/MIPI_TE0	/GMAC1_MDC	/GPIO3_C2_d	Y31
PWN15_IR_M0	/	/UART7_CTSN_M1	/I2C8_SDA_M4	/SPI1_CS1_M1	/	/MIPI_TE1	/GMAC1_MDIO	/GPIO3_C3_d	Y30
CAN2_RX_M0	/PCIE30X4_CLKREQN_M2	/UART5_RX_M1	/FSPI_CS0N_M2	/SPI3_CS0_M3	HDMI_RX1_CEC_M1	/	/CIF_D8	/GPIO3_C4_u	AH26
CAN2_RX_M0	/PCIE30X4_WAKEN_M2	/UART5_RX_M1	/FSPI_CS1N_M2	/SPI3_CS1_M3	/HDMI_RX1_SDA_M1	/	/CIF_D9	/GPIO3_C5_u	AH25
/	/PCIE30X4_PERSTN_M2	/	/	/SPI3_MISO_M3	/HDMI_RX1_SCL_M1	/	/CIF_D10	/GPIO3_C6_u	AG26
/	/PCIE20X2_CLKREQN_M0	/	/I2C5_SCL_M0	/SPI3_MOSI_M3	/HDMI_RX0_SCL_M2	/	/CIF_D11	/GPIO3_C7_u	AJ24
PWN8_M2	/PCIE20X2_WAKEN_M0	/UART4_RX_M1	/I2C5_SDA_M0	/SPI3_CLK_M3	/HDMI_RX0_SDA_M2	/	/CIF_D12	/GPIO3_D0_u	AH24
PWN8_M2	/PCIE20X1_2_PERSTN_M0	/UART4_RX_M1	/	/SPI0_MISO_M3	/HDMI_RX_CEC_M1	/	/CIF_D13	/GPIO3_D1_d	AG23
/	/PCIE30X2_CLKREQN_M2	/UART9_RTSN_M2	/I2C7_SCL_M0	/SPI0_MOSI_M3	/HDMI_RX_SCL_M1	/	/CIF_D14	/GPIO3_D2_d	AG25
PWN10_M2	/PCIE30X2_WAKEN_M2	/UART9_CTSN_M2	/I2C7_SDA_M2	/SPI0_CLK_M3	/HDMI_RX_SDA_M1	/	/CIF_D15	/GPIO3_D3_d	AG24
/	/PCIE30X2_PERSTN_M2	/UART9_RX_M2	/	/SPI0_CS0_M3	/HDMI_RX_HPDIN_M1	/HDMI_RX_HPD_M1	/MCU_JTAG_TCK_M1	/GPIO3_D4_d	AA27
PWN11_IR_M3	/PCIE30X4_BUTTON_RSTN	/UART9_RX_M2	/	/SPI0_CS1_M3	/DP1_HPDIN_M0	/	/MCU_JTAG_TMS_M1	/GPIO3_D5_d	AB28

Figure 2-146 RK3588 HDMI_TX1_CEC M2 Function Pin

The CEC protocol stipulates that the level is 3.3V, but the protocol requires that 3.3V voltage is connected to the CEC pin through a 27K resistor, and the leakage is not allowed to exceed 1.8uA.

Test ID 7-15: CEC Line Degradation

Reference	Requirement
[HDMI: Table 4-40] CEC line Electrical Specifications for all Configurations	<p>A device with power removed (from the CEC circuitry) shall not degrade communication between other CEC devices (e.g. the line shall not be pulled down by the powered off device).</p> <p>Maximum CEC line leakage current must be $\leq 1.8\mu A$</p>

Figure 2-147 HDMI CEC Protocol Requirements

When the RK3588 IO Domain is not powered on, if there has voltage on the IO, there will be leakage in the IO. For example, the RK3588 has been powered off, and the HDMI cable is still connected to the sink (TV or monitor). Leakage of electricity to RK3588 IO through HDMI cable will cause CEC leakage to exceed 1.8uA. Therefore, an isolation circuit needs to be added externally. R5017 resistance cannot be modified at will. It needs to use 27Kohm. Q5002 defaults to 2SK3018. If you want to change to other models, the junction capacitance must be Quite, if the junction capacitance used is too large, it will not only affect the work, but also fail the certification.

HDMI TX CEC

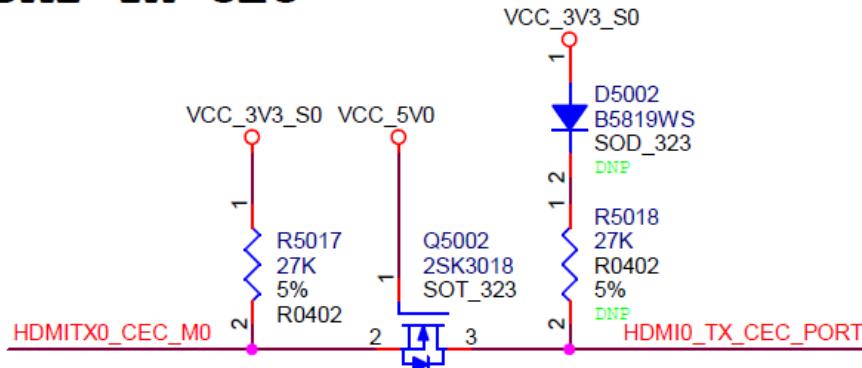


Figure 2-148 HDMI TX CEC Isolation Circuit

HDMI_TX0/1 DDC_SCL/DDC_SDA is the I2C/DDC bus of the HDMI TX0/1 controller. The function is multiplexed to the IO of the VCCIO3, VCCIO5, and VCCIO4 power domains. The level varies with the voltage of the power domain. When The power domain power supply voltage changes, the circuit's pull-up resistor power supply must also be adjusted simultaneously.

The DDC_SCL/DDC_SDA protocol stipulates that it is 5V level, but RK3588 IO does not support 5V level. So a level conversion circuit must be added and cannot be deleted. The MOS tube level conversion is used by default, and the MOS model is 2SK3018 by default. If you want to change to other models, the junction capacitance must be equivalent. If the junction capacitance is too large, effect timing,it will not only affect the work, but also fail the certification.

It is recommended to refer to the default value of the pull-up resistor and cannot be modified at will.

The D5000 diode must not be deleted to prevent the sink terminal from leaking to VCC_5V0.

Due to overlapping rising edges of SDA and SCL signals,it is not meet setup、hold time spec,So pull a 1K resistor in series between the MOS gate and the power supply of the SDA signal level conversion, and a 100pF

between the MOS gate and the source to improve the timing, it is so do, the signals is can meet the spec.

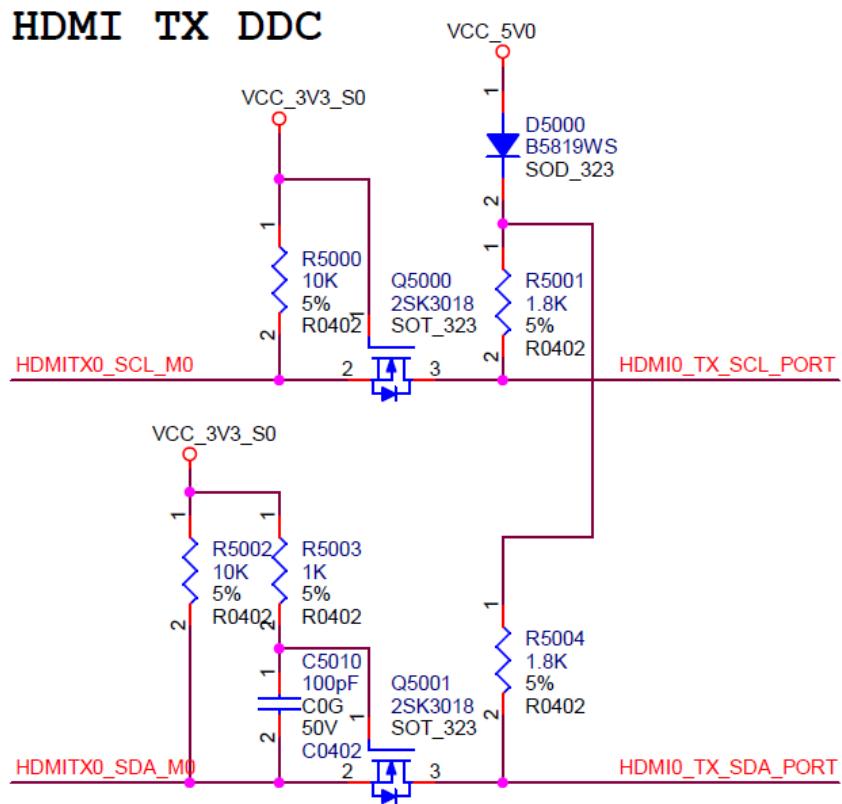


Figure 2-149 HDMI TX DDC Level Conversion Circuit

The Pin18 voltage of the HDMI socket must be guaranteed to be between 4.8-5.3V, and a 1uF decoupling capacitor must be placed on the pin. It must not be deleted. During layout, place it close to the HDMI socket pin.

In order to strengthen the anti-static ability, ESD devices must be reserved on the signal. The ESD parasitic capacitance of HDMI2.1 signals should not exceed 0.2pF, and the ESD parasitic capacitance of other signals should not exceed 1pF.

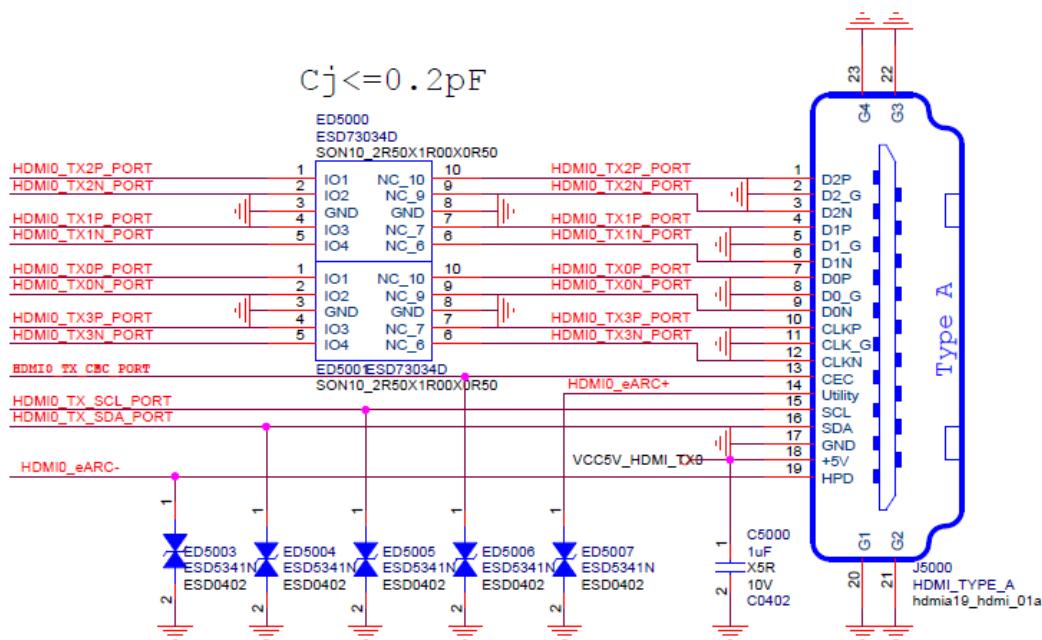


Figure 2-150 HDMI TX Socket ESD Circuit

The HDMI TX interface matching design recommendation is shown in the following table.

Table 2-27 RK3588 HDMI TX Interface Design

Signal	Connection method	Description
HDMI_TX0_D0P/D0N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane0/TMDS data Lane0 output
HDMI_TX0_D1P/D1N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane1/TMDS data Lane1 output
HDMI_TX0_D2P/D2N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane2/TMDS data Lane2 output
HDMI_TX0_D3P/D3N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane3/TMDS clock output
HDMI_TX0_SBDP/SBDN	1uF pacitor (0201 package) in series	ARC/eARC channel (This feature is not currently supported)
HDMI/EDP_TX0_REXT	8200ohm 1% resistance to ground	HDMI/EDP_TX0 PHY external reference resistance
HDMI_TX0_HPD	diode	HDMI insert detection
HDMI_TX0_CEC	MOS isolated conversion	HDMI CEC signal
HDMI_TX0_SCL	MOS level conversion	HDMI DDC clock
HDMI_TX0_SDA	MOS level conversion	HDMI DDC data input and output
HDMI_TX1_D0P/D0N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane0/TMDS data Lane0 output
HDMI_TX1_D1P/D1N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane1/TMDS data Lane1 output
HDMI_TX1_D2P/D2N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane2/TMDS data Lane2 output
HDMI_TX1_D3P/D3N	220nF capacitor (0201 package) in series 590ohm resistance to ground	RFL mode Lane3/TMDS clock output
HDMI_TX1_SBDP/SBDN	1uF pacitor (0201 package) in series	ARC/eARC channel (This feature is not currently supported)
HDMI/EDP_TX1_REXT	8200ohm 1% resistance to ground	HDMI/EDP_TX0 PHY external reference resistance

Signal	Connection method	Description
HDMI_TX1_HPD	diode	HDMI insert detection
HDMI_TX1_CEC	MOS isolated conversion	HDMI CEC signal
HDMI_TX1_SCL	MOS level conversion	HDMI DDC clock
HDMI_TX1_SDA	MOS level conversion	HDMI DDC data input and output

- eDP TX mode

Supports eDP V1.3 version, a total of 4 Lanes, eDP TX maximum output resolution can reach 4K@60Hz.

- Each Lane rate can support 1.62/2.7/5.4Gbps;
- Support 1Lane or 2Lane or 4Lane mode;
- Support AUX channel, the rate can reach 1Mbps.

Take eDP TX0 as example. eDP TX1 and eDP TX0 are the same.

eDP_TX0_D0P/D0N, eDP_TX0_D1P/D1N, eDP_TX0_D2P/D2N, eDP_TX0_D3P/D3N need to be connected in series with 220nF AC coupling capacitors. It is recommended to use the 0201 package for the AC coupling capacitors, which can get lower ESR and ESL and reduce impedance changes on the line. During layout, place it close to the RK3588 pin.

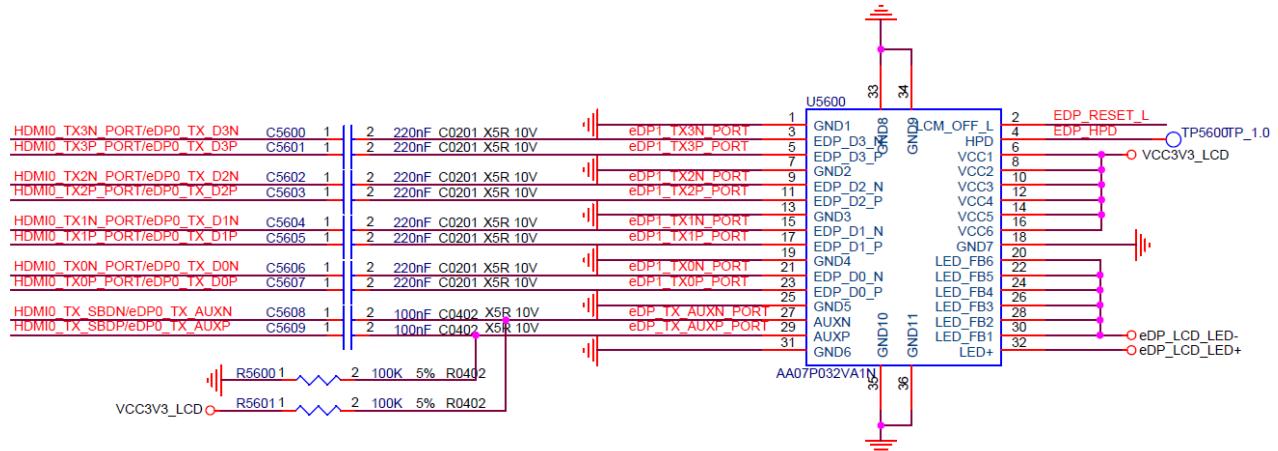


Figure 2-151 RK3588 eDP TX0 Signal AC Coupling Capacitor

eDP_TX0_AUXP/AUXN needs to connect a 100nF AC coupling capacitor in series near the interface end, AUXP needs to reserve a 100Kohm resistor to ground, and AUXN reserves a 100K resistor to pull up to 3.3V.

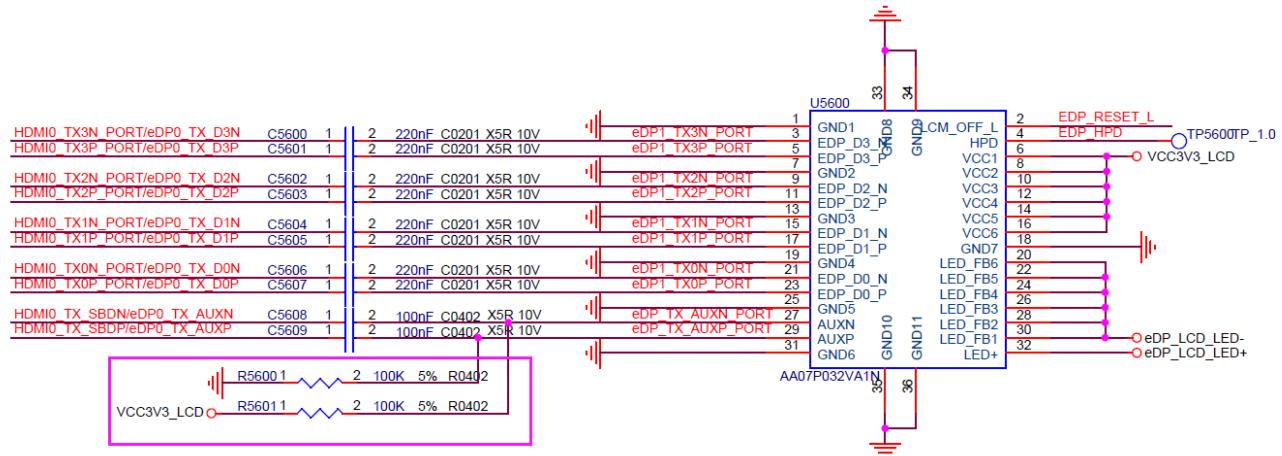


Figure 2-152 RK3588 eDP TX0 AUX AC Coupling Capacitor

The recommended design of eDP TX0/1 PHY interface matching is shown in the following table:

Table 2-28 RK3588 eDP TX0/1 PHY Interface Design

Signal	Connection method	Description
eDP_TX0_D0P/D0N	220nF capacitor (0201 package) in series	eDPdataLane0output
eDP_TX0_D1P/D1N	220nF capacitor (0201 package) in series	eDPdataLane1output
eDP_TX0_D2P/D2N	220nF capacitor (0201 package) in series	eDPdataLane2output
eDP_TX0_D3P/D3N	220nF capacitor (0201 package) in series	eDPdataLane3output
eDP_TX0_AUXP/AUXN	100nF capacitor in series	eDP AUXchannel
eDP_TX1_D0P/D0N	220nF capacitor (0201 package) in series	eDPdataLane0output
eDP_TX1_D1P/D1N	220nF capacitor (0201 package) in series	eDPdataLane1output
eDP_TX1_D2P/D2N	220nF capacitor (0201 package) in series	eDPdataLane2output
eDP_TX1_D3P/D3N	220nF capacitor (0201 package) in series	eDPdataLane3output
eDP_TX1_AUXP/AUXN	100nF capacitor in series	eDP AUXchannel

2.3.8.2 MIPI_D/CPHY_TX Interface

RK3588 has two MIPI D-PHY/C-PHY Combo PHY TX:

- D-PHY supports V2.0, D-PHY has 0/1/2/3 Lane, each Lane has 2 lines. The maximum data transmission rate is 4.5Gbps;
- C-PHY supports V1.1, C-PHY mode has 0/1/2 Trio, each Trio has A/B/C 3 lines. The maximum data transmission rate is 5.7Gbps/Trio.

U1000Q

MIPI D/C-PHY DS1_TX Port0	
D-PHY:V2.0	4.5Gbps/Lane
C-PHY:V1.1	5.7Gbps/Trio
MIPI_DPHY0_TX_CLKP	MIPI_CPHY0_TX_TRIO1_C
MIPI_DPHY0_TX_CLKN	MIPI_CPHY0_TX_TRIO1_B
MIPI_DPHY0_TX_D0P	MIPI_CPHY0_TX_TRIO0_B
MIPI_DPHY0_TX_D0N	MIPI_CPHY0_TX_TRIO0_A
MIPI_DPHY0_TX_D1P	MIPI_CPHY0_TX_TRIO1_A
MIPI_DPHY0_TX_D1N	MIPI_CPHY0_TX_TRIO0_C
MIPI_DPHY0_TX_D2P	MIPI_CPHY0_TX_TRIO2_B
MIPI_DPHY0_TX_D2N	MIPI_CPHY0_TX_TRIO2_A
MIPI_DPHY0_TX_D3P	/NO_USE_AN28
MIPI_DPHY0_TX_D3N	MIPI_CPHY0_TX_TRIO2_C
	AN26 AP26
	AN24 AP24
	AN25 AP25
	AN27 AP27
	AN28 AP28

Figure 2-153 RK3588 MIPI D/C-PHY0 TX Signal Pin

U1000R

MIPI D/C-PHY DS1_TX Port1	
D-PHY:V2.0	4.5Gbps/Lane
C-PHY:V1.1	5.7Gbps/Trio
MIPI_DPHY1_TX_CLKP	MIPI_CPHY1_TX_TRIO1_C
MIPI_DPHY1_TX_CLKN	MIPI_CPHY1_TX_TRIO1_B
MIPI_DPHY1_TX_D0P	MIPI_CPHY1_TX_TRIO0_B
MIPI_DPHY1_TX_D0N	MIPI_CPHY1_TX_TRIO0_A
MIPI_DPHY1_TX_D1P	MIPI_CPHY1_TX_TRIO1_A
MIPI_DPHY1_TX_D1N	MIPI_CPHY1_TX_TRIO0_C
MIPI_DPHY1_TX_D2P	MIPI_CPHY1_TX_TRIO2_B
MIPI_DPHY1_TX_D2N	MIPI_CPHY1_TX_TRIO2_A
MIPI_DPHY1_TX_D3P	/NO_USE_AN22
MIPI_DPHY1_TX_D3N	MIPI_CPHY1_TX_TRIO2_C
	AN20 AP20
	AN18 AP18
	AN19 AP19
	AN21 AP21
	AN22 AP22

Figure 2-154 RK3588 MIPI D/C-PHY1 TX Signal Pin

DPHY and CPHY configuration support:

- The TX and RX of MIPI D-PHY/C-PHY Combo PHY0 can only be configured as DPHY0 TX, DPHY0 RX mode at the same time, or configured as CPHY0 TX, CPHY0 RX mode at the same time. Does not support one configured as DPHY0 TX and one configured as CPHY0 RX;
- The TX and RX of MIPI D-PHY/C-PHY Combo PHY1 can only be configured as DPHY1 TX, DPHY1 RX mode at the same time, or configured as CPHY1 TX, CPHY1 RX mode at the same time. Does not support one configured as DPHY1 TX and one configured as CPHY1 RX;

Mode support situation when MIPI D/C-PHY0 works in D-PHY:

- Support x4Lane mode, MIPI_DPHY0_TX_D[3:0] data refer to MIPI_DPHY0_TX_CLK.

Mode support situation when MIPI D/C-PHY0 works in C-PHY:

- Support 0/1/2 Trio, each Trio has A/B/C 3 lines: MIPI_CPHY0_TX_TRIO[2:0]_A, MIPI_CPHY0_TX_TRIO[2:0]_B, MIPI_CPHY0_TX_TRIO[2:0]_C

Mode support situation when MIPI D/C-PHY1 works in D-PHY:

- Support x4Lane mode, MIPI_DPHY1_TX_D[3:0] data refer to MIPI_DPHY1_TX_CLK.

Mode support situation when MIPI D/C-PHY1 works in C-PHY:

- Support 0/1/2 Trio, each Trio has A/B/C 3 lines, MIPI_CPHY1_TX_TRIO[2:0]_A, MIPI_CPHY1_TX_TRIO[2:0]_B, MIPI_CPHY1_TX_TRIO[2:0]_C.

Please note in MIPI D-PHY/C-PHY Combo PHY0/1 TX design:

- In order to improve the performance of MIPI D-PHY/C-PHY Combo PHY0/1 RX, the decoupling capacitors of each PHY power supply must not be deleted. Please place it close to the pins during layout (RX and TX power supplies are the same).

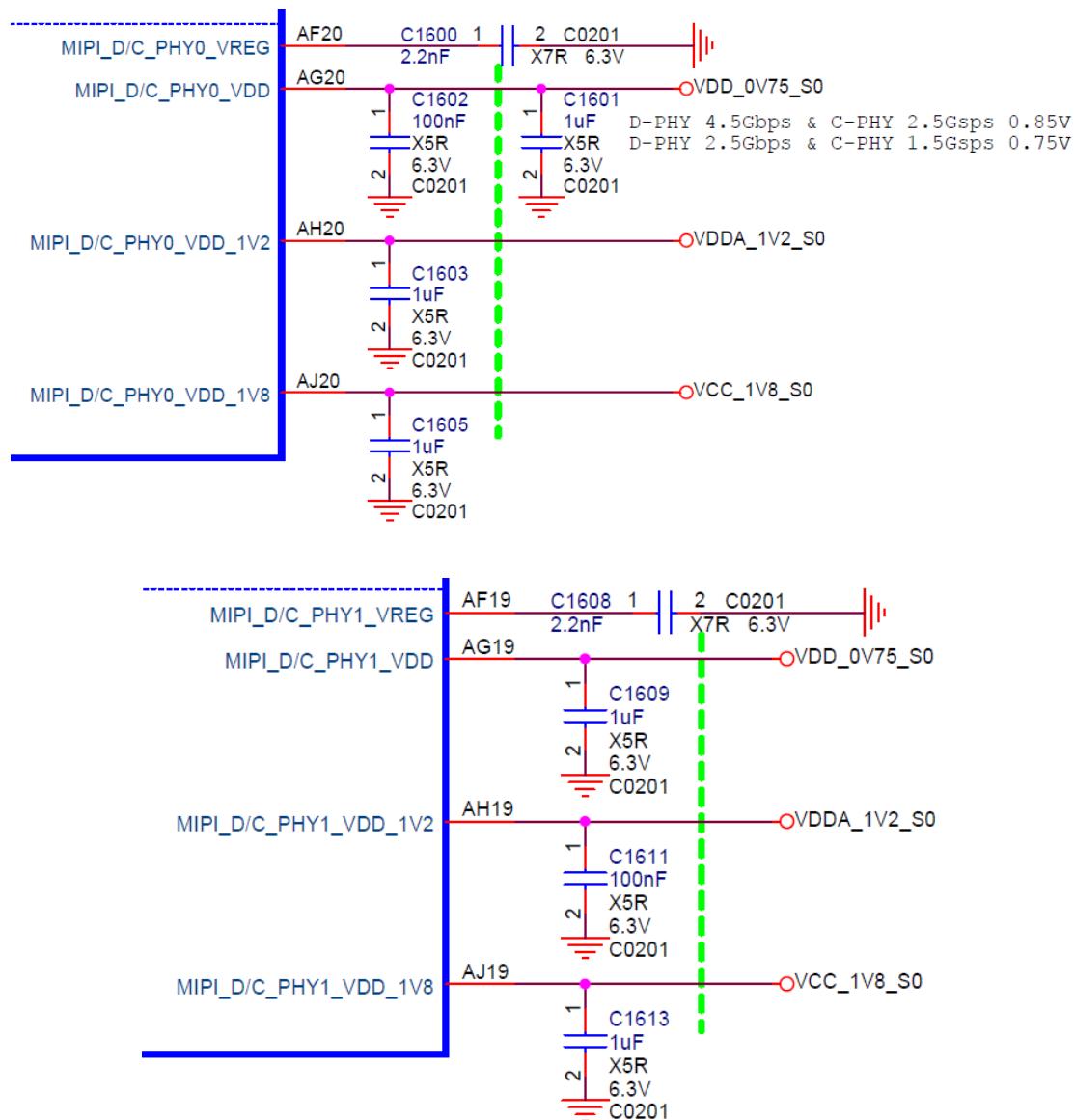


Figure 2-155 MIPI D-PHY/C-PHY Combo PHY0/1 TX Power Decoupling Capacitor

MIPI D-PHY/C-PHY Combo PHY0/1 TX matching design recommendations are shown in the following table:

Table 2-29 RK3588 MIPI D-PHY/C-PHY Combo PHY0/1 TX Interface Design

Signal	Connection method	Description
MIPI_DPHY0_TX_D0P/D0N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY0_TX data Lane0 output
MIPI_DPHY0_TX_D1P/D1N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY0_TX data Lane1 output
MIPI_DPHY0_TX_D2P/D2N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY0_TX data Lane2 output
MIPI_DPHY0_TX_D3P/D3N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY0_TX data Lane3 output
MIPI_DPHY0_TX_CLKP/CLKN	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY0_TX clock output
MIPI_CPHY0_TX_TRIO0_A/B/C	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_CPHY0_TX_TRIO0 output
MIPI_CPHY0_TX_TRIO1_A/B/C	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_CPHY0_TX_TRIO1 output
MIPI_CPHY0_TX_TRIO2_A/B/C	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_CPHY0_TX_TRIO2 output
MIPI_DPHY1_TX_D0P/D0N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY1_TX data Lane0 output
MIPI_DPHY1_TX_D1P/D1N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY1_TX data Lane1 output
MIPI_DPHY1_TX_D2P/D2N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY1_TX data Lane2 output
MIPI_DPHY1_TX_D3P/D3N	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY1_TX data Lane3 output
MIPI_DPHY1_TX_CLKP/CLKN	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_DPHY1_TX clock output
MIPI_CPHY1_TX_TRIO0_A/B/C	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_CPHY1_TX_TRIO0 output
MIPI_CPHY1_TX_TRIO1_A/B/C	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_CPHY1_TX_TRIO1 output
MIPI_CPHY1_TX_TRIO2_A/B/C	Direct connection. Reserve common mode inductance to suppress electromagnetic radiation	MIPI_CPHY1_TX_TRIO2 output

2.3.8.3 DP TX Interface

RK3588 supports 2 DP1.4 TX PHY (and USB3.0 Combo), the maximum output resolution can reach 8K@30Hz.

- Each Lane rate can support 1.62/2.7G/5.4/8.1Gbps;

- Support 1Lane or 2Lane or 4Lane mode;
- Support RGB/YUV (Up to 10bit) format;
- Support Single Stream Transport (SST).

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

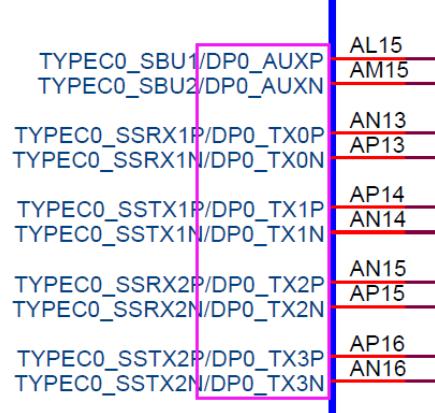


Figure 2-156 RK3588 DP0 TX Pin

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

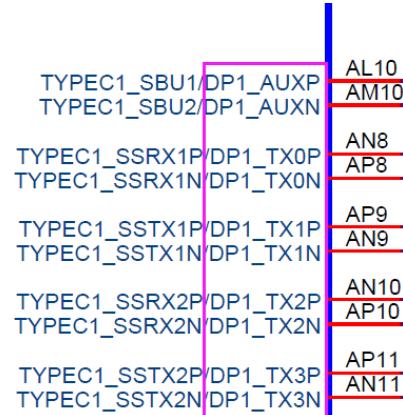


Figure 2-157 RK3588 DP1 TX Pin

Please pay attention to DP0/1 TX PHY design:

- In order to improve the performance of DP0/1 TX PHY, the decoupling capacitors of each power supply of PHY should not be deleted, and should be placed close to the pins during layout. Among them, TYPEC0_DP0_VDD_0V85, TYPEC0_DP0_VDDA_0V85, and TYPEC0_DP0_VDDH_1V8 must supply power even if the TYPEC0 function is not used;

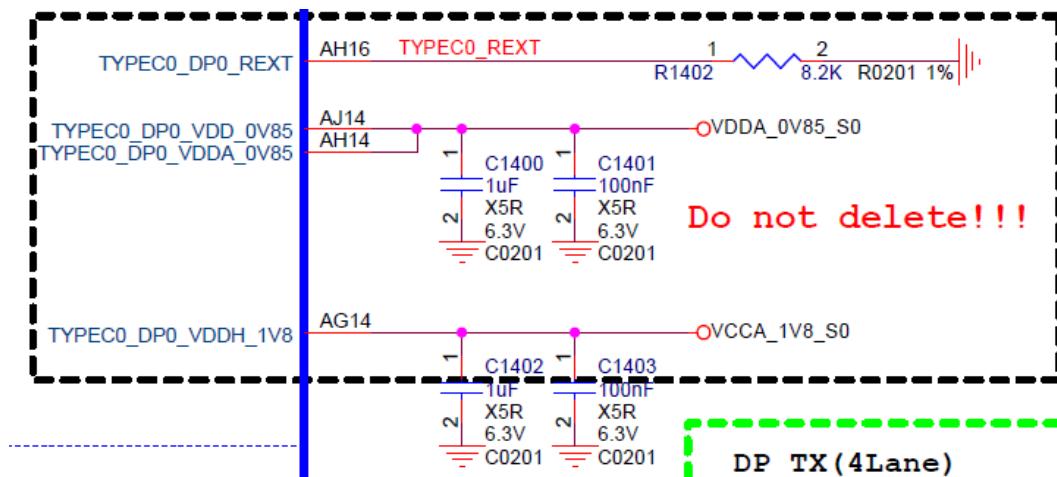


Figure 2-158 RK3588 DP0 TX PHY Power Decoupling Capacitor

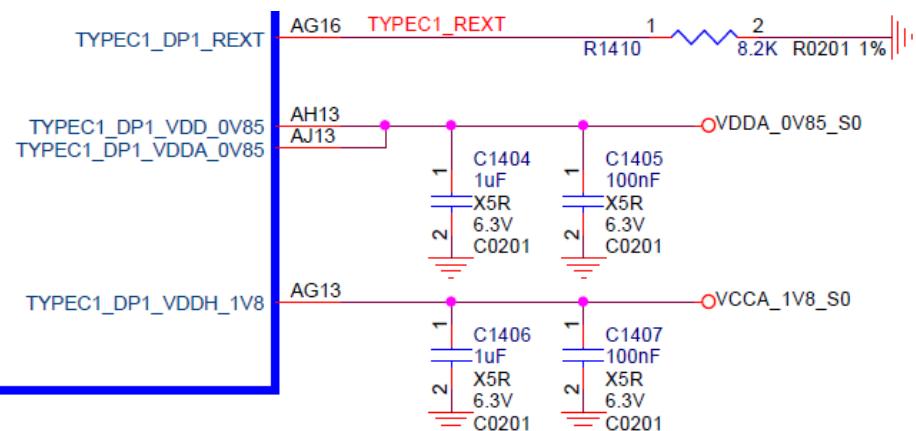


Figure 2-159 RK3588 DP1 TX PHY Power Decoupling Capacitor

- DP0_TX_D0P/D0N, DP0_TX_D1P/D1N, DP0_TX_D2P/D2N, DP0_TX_D3P/D3N, DP1_TX_D0P/D0N, DP1_TX_D1P/D1N, DP1_TX_D2P/D2N, DP1_TX_D3P/D3N need to be connected in series with 100nF AC coupling capacitors. It is recommended to use 0201 package for AC coupling capacitors, which can get lower ESR and ESL and reduce impedance changes on the line. During layout, place it close to the RK3588 pin;

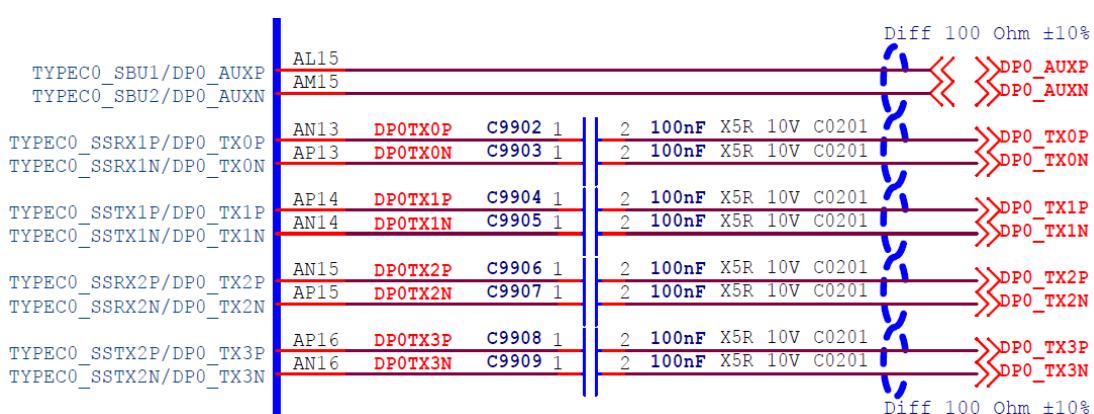


Figure 2-160 RK3588 DP0 TX Signal AC Coupling Capacitor

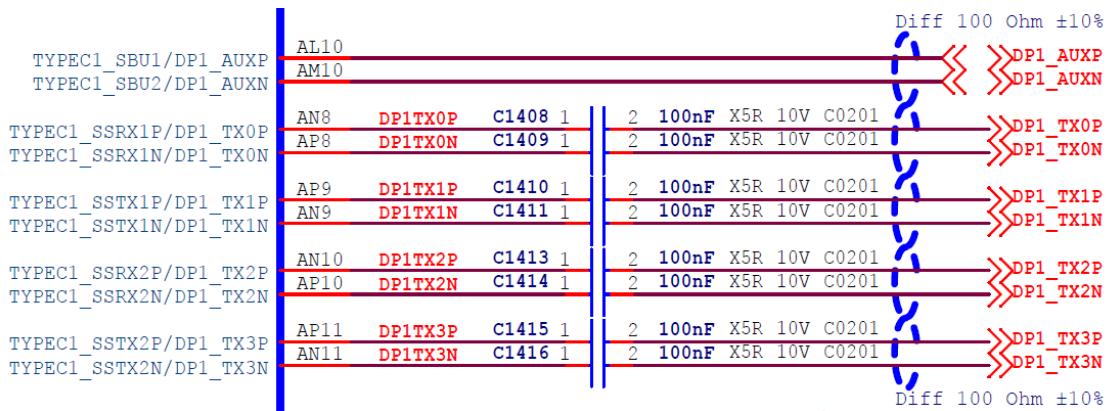


Figure 2-161 RK3588 DP1 TX Signal AC Coupling Capacitor

- TYPEC0_DP0_REXT and TYPEC1_DP1_REXT are the external reference resistor pins of USB DP Combo PHY0/1. They are externally connected to 8200ohm resistors with an accuracy of 1%. The resistance value should not be changed. They should be placed close to the RK3588 chip pins during layout. The resistance of the TYPEC0_DP0_REXT pin must be connected even if the TYPEC0 function is not used.



Figure 2-162 RK3588 DP0_TX_REXT Pin



Figure 2-163 RK3588 DP1_TX_REXT Pin

DP0/1 TX PHY interface matching design recommendations are shown in the following table:

Table 2-30 RK3588 DP0/1 TX PHY Interface Design

Signal	Connection method	Description
DP0_TX_D0P/D0N	a 100nF capacitor in series (0201 package is recommended)	DP0 data Lane0 output
DP0_TX_D1P/D1N	a 100nF capacitor in series (0201 package is recommended)	DP0 data Lane1 output
DP0_TX_D2P/D2N	a 100nF capacitor in series (0201 package is recommended)	DP0 data Lane2 output
DP0_TX_D3P/D3N	a 100nF capacitor in series (0201 package is recommended)	DP0 data Lane3 output
DP0_TX_AUXP/AUXN	a 100nF capacitor in series	DP0 AUX channel
TYPEC0_DP0_REXT	8200 ohm resistance to ground with an accuracy of 1%	External reference resistor for USB/DP0 PHY
DP1_TX_D0P/D0N	a 100nF capacitor in series (0201 package is recommended)	DP1 data Lane0 output
DP1_TX_D1P/D1N	a 100nF capacitor in series (0201 package is recommended)	DP1 data Lane1 output
DP1_TX_D2P/D2N	a 100nF capacitor in series (0201 package is recommended)	DP1 data Lane2 output
DP1_TX_D3P/D3N	a 100nF capacitor in series (0201 package is recommended)	DP1 data Lane3 output
DP1_TX_AUXP/AUXN	a 100nF capacitor in series	DP1 AUX channel
TYPEC1_DP1_REXT	8200 ohm resistance to ground with an accuracy of 1%	External reference resistor for USB/DP1 PHY

2.3.8.4 BT1120 TX Interface

RK3588 supports 16bit BT1120 output interface, the maximum output resolution can reach 1920X1080@60Hz; compatible with 8bit BT656 interface, support PAL and NTSC.

VCCIO6 Domain		Operating Voltage=1.8V/3.3V			
/ SPI0_MISO_M1	/ UART9_RTSN_M1 /	/ I2S1_MCLK_M0	/ PCIE30X1_1_CLKREQN_M1	/ BT1120_D0	/ CIP_D0 / GPIO4_A0_d AK30
/ SPI0_MOSI_M1	/ UART9_CTSN_M1 /	/ I2S1_SCLK_TX_M0	/ PCIE30X1_1_WAKEN_M1	/ BT1120_D1	/ CIP_D1 / GPIO4_A1_d AL30
/ SPI0_CLK_M1	/	/ I2S1_LRCK_TX_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D2	/ CIP_D2 / GPIO4_A2_d AM29
/	UART0_RX_M2 /	/ I2S1_SCLK_RX_M0	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D3	/ CIP_D3 / GPIO4_A3_d AL29
/ SPI2_MISO_M1	/ UART0_RX_M2 / I2C3_SCL_M2	/ I2S1_LRCK_RX_M0	/ PCIE30X1_0_WAKEN_M1	/ BT1120_D4	/ CIP_D4 / GPIO4_A4_d AL28
/ SPI2_MOSI_M1	/ UART3_TX_M2 / I2C3_SDA_M2	/ I2S1_SDIO_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D5	/ CIP_D5 / GPIO4_A5_d AK27
/ SPI2_CLK_M1	/ UART3_RX_M2 / I2C5_SCL_M2	/ I2S1_SD1_M0	/ PCIE30X2_CLKREQN_M1	/ BT1120_D6	/ CIP_D6 / GPIO4_A6_d AL27
/ SPI2_CS0_M1	/	/ I2C5_SDA_M2	/ I2S1_SD1_M0	/ PCIE30X2_WAKEN_M1	/ BT1120_D7 / CIP_D7 / GPIO4_A7_d AM27
/ SPI2_CS1_M1	/ UART8_RX_M0 / I2C6_SDA_M3	/ I2S1_SD13_M0	/ PCIE30X2_PERSTN_M1	/ BT1120_CLKOUT	/ CIP_CLKIN / GPIO4_B0_d AK26
SATA2_ACT_LED_M0	/ SPDIF1_TX_M1 / SPI0_CS1_M1	/ UART8_RX_M0 / I2C6_SCL_M3	/ I2S1_SD00_M0	/ PCIE30X1_0_BUTTON_RSTN	/ / MIPI_CAMERA0_CLK_M0 / GPIO4_B1_u AL24
CAN1_RX_M1	/ PWM14_M1 / SPI0_CS0_M1	/ UART8_RTSN_M0 / I2C7_SCL_M3	/ I2S1_SD01_M0	/ PCIE30X1_1_BUTTON_RSTN	/ BT1120_D8 / CIP_HREF / GPIO4_B2_u AK25
CAN1_TX_M1	/ PWM15_IR_M1 /	/ UART8_CTSN_M0 / I2C7_SDA_M3	/ I2S1_SD02_M0	/ PCIE30X1_2_BUTTON_RSTN	/ BT1120_D9 / CIP_VSYNC / GPIO4_B3_u AM25
SPDIF0_RX_M1	/ PWM11_IR_M1 / DP0_HPDIN_M0	/ UART9_RX_M1 /	/ I2S1_SD03_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D10 / CIP_CLKOUT / GPIO4_B4_u AL26
SATA1_ACT_LED_M0	/ PWM12_M1 / SPI1_MISO_M1	/ UART9_RX_M1 /	/ HDMI_RX_CEC_M0	/ PCIE30X4_WAKEN_M1	/ BT1120_D11 / / GPIO4_B5_d AJ26
SATA0_ACT_LED_M0	/ PWM13_M1 / SPI1_MOSI_M1 /	/ I2C5_SCL_M1	/ HDMI_RX_HPDIN_M0	/ PCIE30X4_PERSTN_M1	/ BT1120_D12 / / GPIO4_B6_d AJ27
/	/ SPI1_CLK_M1 /	/ I2C5_SDA_M1	/ HDMI_RX_TXO_SCL_M0	/ PCIE30X1_2_CLKREQN_M1	/ BT1120_D13 / / GPIO4_B7_u AJ28
/	/ SPI1_CS0_M1 /	/ I2C8_SCL_M3	/ HDMI_RX_TXO_SDA_M0	/ PCIE30X1_2_WAKEN_M1	/ BT1120_D14 / / GPIO4_C0_u AJ25
SPDIF1_RX_M2	/ PWM6_M1 / SPI1_CS1_M1 /	/ I2C8_SDA_M3	/ HDMI_RX_CEC_M0	/ PCIE30X1_2_PERSTN_M1	/ BT1120_D15 / / GPIO4_C1_d AK24

Figure 2-164 RK3588 VOP BT1120 Function Pin

The multiplexing relationship between BT1120 and BT656 is as follows:

Table 2-31 RK3588 BT1120 and BT656 Relationship Table

Pin name	BT656(8bit)	BT1120(16bit)
BT1120_CLKOUT	CLKOUT	CLKOUT
BT1120_D15		D15
BT1120_D14		D14
BT1120_D13		D13
BT1120_D12		D12
BT1120_D11		D11
BT1120_D10		D10
BT1120_D9		D9
BT1120_D8		D8
BT1120_D7	D7	D7
BT1120_D6	D6	D6
BT1120_D5	D5	D5
BT1120_D4	D4	D4
BT1120_D3	D3	D3
BT1120_D2	D2	D2
BT1120_D1	D1	D1
BT1120_D0	D0	D0

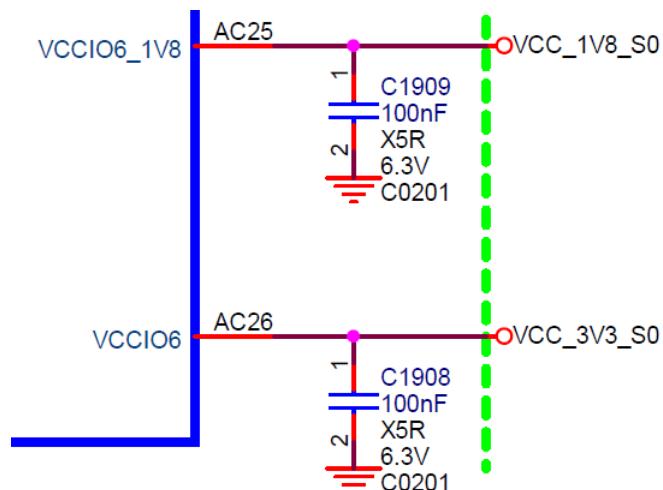
BT1120 output interface data corresponding relationship, support YC Swap.

Table 2-32 RK3588 BT1120 Output Format List

Pin Name	Default mode		Swap open	
	Pixel #0	Pixel #1	Pixel #0	Pixel #1
BT1120_D0	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]
BT1120_D1	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]
BT1120_D2	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]
BT1120_D3	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]
BT1120_D4	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]
BT1120_D5	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]
BT1120_D6	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]
BT1120_D7	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]
BT1120_D8	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]
BT1120_D9	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]
BT1120_D10	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]
BT1120_D11	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]
BT1120_D12	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]
BT1120_D13	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]
BT1120_D14	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]
BT1120_D15	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]

Please pay attention to the design of BT1120 output interface:

- BT1120 output interface power domain is VCCIO6 power supply. In actual product design, the corresponding power supply needs to be selected according to the actual IO power supply requirements (1.8V or 3.3V) of the peripherals, which must be consistent;
- In order to improve the performance of the BT1120 output interface, the decoupling capacitor of the VCCIO6 power supply must not be deleted. Please place it close to the pins during layout.



BT1120 output interface pull-up and pull-down and matching design recommendations are shown in the table:

Table 2-33 RK3588 BT1120 Output Interface Design

Signal	Pull up/down inside	Connection mode	Description (chip end)
BT1120_D[15:0]	Pull-down	Direct connection, it's recommended to reserve a series resistor near chip end.	BT1120 data output
BT1120_CLK	Pull-down	Connect a 22ohm resistor in series near device end.	BT1120 clock output

- When realizing the board-to-board connection through the connector, it is recommended to connect a resistor with a certain resistance in series (between 22ohm and 100ohm, depending on the specific requirements that can meet the SI test), and reserve TVS devices.

2.3.8.5 Some Attention Points When Designing LCD Screens and Touch Screens

- For the current limiting resistor on the FB side of the LED backlight boost IC, please select a 1% precision resistor and choose a suitable package size according to the power requirement;
- EN/PWM pin of LED backlight boost IC, select internal pull-down GPIO, external pull-down resistor, to avoid flickering when powering on;
- For LED backlight drive voltage output, please select a filter capacitor with a suitable rated voltage;
- For the Schottky diode of the LED backlight boost circuit, please select the appropriate model according to the working current, and pay attention to the reverse breakdown voltage of the diode to avoid reverse breakdown when there is no load;
- Please match the inductance, saturation current, DCR, etc. of the LED backlight boost circuit according to the actual model;
- The signal level of the screen and touch screen should match the IO drive level of the chip, such as RST/Stand by signals;
- The power supply of the screen must be controllable, and it is not provided by default when it is powered on;
- The decoupling capacitance of the screen and touch screen must not be deleted and must be retained;
- The I2C bus of TP must be pulled up to the VCC3V3_TP power supply by 2.2K. It is recommended not to share the bus with other devices. If it must be shared, pay attention to whether the pull-up power supply conflicts with the address;
- For TP IC with charge pump, please pay attention to the rated voltage of the capacitor;
- For the screen, when connecting to the board through FPC, it is recommended to connect a resistor with a certain resistance in series (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices;
- It is recommended to reserve common mode inductance at the interface of the serial interface screen;

2.3.8.6 Some Attention Points when Designing VGA Interface

RK3588 itself does not support direct VGA OUT, and requires an external conversion chip. HDMI, MIPI, eDP and other interfaces can be choosed to convert to VGA output. Here are the relevant points of attention based on IT6516BFN:

- The decoupling capacitors of each power supply pin must not be deleted and must be retained;
- Pay attention to the power-on sequence requirements;
- The LVTTL signal level of VGADDCSDA and VGADDCCCLK of IT6516BFN Pin12 and Pin13 is 5V, which needs to be pulled up to 5V level;
- For the HPD signal of IT6516BFN Pin26, the default ground resistance cannot be deleted or the default pull-down GPIO is used;
- The IT6516BFN peripheral circuit must directly refer to the reference design circuit;
- IVDDO (Pin25) outputs 1.8V for the Regulator, which provides power to the chip's I/O, DP Analog front-end, and DAC/Voltage.
- VGA_R/G/B needs to be connected with a pull-down 75ohm resistor, the accuracy is 1%, and must not be deleted;
- VGA_R/G/B filter circuit needs to refer to the requirements of each conversion chip;
- All signals of the VGA socket must increase the TVS tube, and the TVS device should be placed as close as possible to the VGA connector.

2.3.9 Audio Circuit Design

RK3588 provides a total of 11 sets of I2S interfaces, 2 sets of PDM interfaces, 6 SPDIF TX interfaces, 3 SPDIF RX interfaces and 1 set of DSM PWM Audio interfaces.

Among them, 4 sets of standard I2S interfaces, 2 sets of PDM interfaces, 2 SPDIF TX interfaces, and 1 set of DSM PWM Audio interfaces are provided externally. The multiplexing of IO domains of these interfaces and their power domains are shown in the following table for users to flexibly allocate and choose .

Table 2-34 RK3588 External Audio Interface and IO Multiplexing Situation

External Interface	First multiplex (M0)	Second multiplex (M1)	Third multiplex (M2)	Internal power domain
I2S0	VCCIO1	-	-	PD_AUDIO
I2S1	VCCIO6	PMUIO2	-	PD_PMUI
I2S2	VCCIO3	VCCIO5	-	PD_AUDIO
I2S3	VCCIO5	-	-	PD_AUDIO
PDM0	VCCIO1	PMUIO2	-	PD_PMUI
PDM1	VCCIO2	VCCIO4	-	PD_AUDIO
SPDIFO_TX	VCCIO4 GPIO1_B6	VCCIO6 GPIO4_B4	-	PD_AUDIO
SPDIF1_TX	VCCIO4 GPIO1_B7	VCCIO6 GPIO4_B1	VCCIO6 GPIO4_C1	PD_AUDIO
DSM PWM Audio	VCCIO5	-	-	PD_AUDIO

The remaining unlead audio interfaces are used for supporting the use of video input/output interfaces, and their internal distribution and correspondence are shown in the block diagram in chapter 2.3.9.1. The subordination of the internal power domains of these audio interfaces is as follows, which is consistent with the power domains of the corresponding video interfaces:

- I2S4 and I2S8 belong to PD_VO0;
- I2S5, I2S6, I2S7, I2S9, I2S10 belong to PD_VO1;
- SPDIF2_TX and SPDIF5_TX belong to PD_VO0;
- SPDIF3_TX and SPDIF4_TX belong to PD_VO1;
- SPDIF_RX0, SPDIF_RX1, SPDIF_RX2 belong to PD_VO1.

2.3.9.1 Audio Subsystem Block Diagram

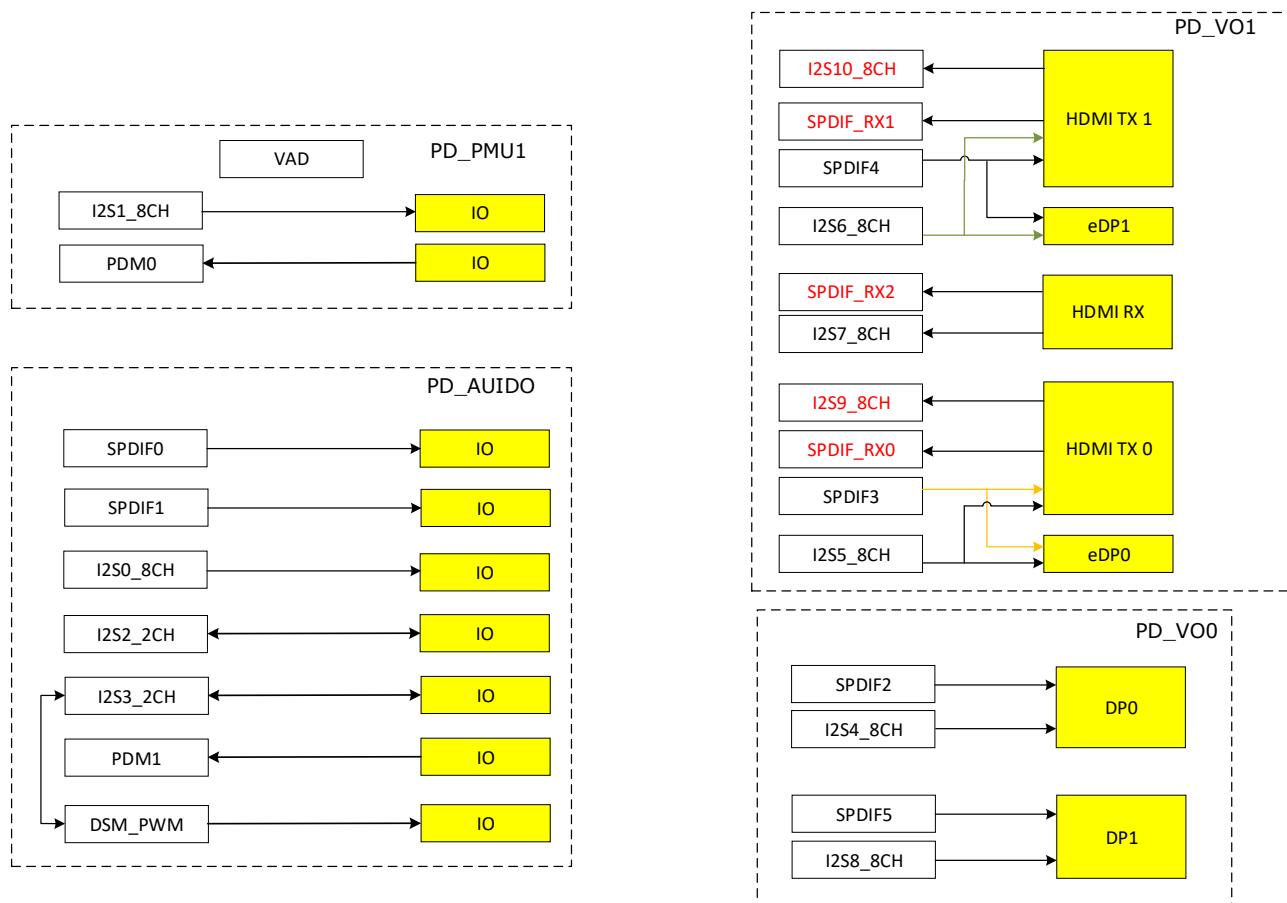


Figure 2-165 Audio Subsystem Block Diagram

2.3.9.2 I2S Digital Audio Interface

RK3588 provides a total of 11 groups of I2S interfaces, of which 4 groups can be connected to external interfaces. As the most widely used digital audio interface, I2S can be used for the communication of audio ADC, audio DAC, audio Codec, DSP and other peripherals. It can also provide integrated audio input and output support for video input/output interfaces.

Among them, I2S0 and I2S1 are standard I2S interfaces that support 8-channel input/output capabilities, and support I2S/PCM/TDM mode; I2S2, I2S3 are standard I2S interfaces that support 2-channel input/output capabilities, and support I2S/PCM mode. The format and timing of these modes can be described in detail in the TRM document.

These four groups of I2S interfaces can support master-slave mode, with a bit width of 16 to 32 bits, and a sampling rate of up to 192kHz.

2.3.9.2.1 I2S0 Digital Audio Interface

The I2S0 interface includes independent 8-channel output and 8-channel input. For output data SDOx and input data SDIx, refers to the same set of bit/frame clock SCLK/LRCK.

The I2S0 interface supports a master-slave working mode, which is configurable by software. Supports 3 I2S formats (regular, left-justified, right-justified); supports 4 PCM formats (early, late1, late2, late3); supports 5 TDM formats (regular, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift).

This group of I2S pins has only one multiplexing. In VCCIO1, two of the SDOx and SDIx signals have multiplexing conflicts. Pay attention to the pin assignment. At the same time, the IO level of the I2S peripheral needs to be checked to match the power supply of the corresponding IO power domain.

I2S0 interface pull-up and pull-down and matching design recommendations are shown in the table.

Table 2-35 RK3588 I2S0 Interface Signal Description

Signal	Default method	Connection method	Description(chip end)
I2S0_MCLK	pull down	22ohm resistor in series	I2S system clock output
I2S0_SCLK	pull down	22ohm resistor in series	I2S continuous serial clock, bit clock
I2S0_LRCK	pull down	22ohm resistor in series	I2S frame clock for channel selection
I2S0_SDO0	pull down	Direct connection	I2S serial data 0 output
I2S0_SDO1	pull down	Direct connection	I2S serial data 1 output
I2S0_SDO2/I2S0_SDI3	pull down	Direct connection	I2S serial data 2 output/serial data 3 input
I2S0_SDO3/I2S0_SDI2	pull down	Direct connection	I2S serial data 3 output/serial data 2 input
I2S0_SDI0	pull down	Direct connection	I2S serial data 0 input
I2S0_SDI1	pull down	Direct connection	I2S serial data 1 input

- In order to improve the performance of the I2S interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.2.2 I2S1 Digital Audio Interface

The I2S1 interface includes independent 8-channel output and 8-channel input. For output data SDOx and input data SDIx, refers to the same set of bit/frame clock SCLK/LRCK.

The I2S1 interface supports the master-slave working mode, and the software is configurable. Supports 3 I2S formats (regular, left-justified, right-justified); supports 4 PCM formats (early, late1, late2, late3); supports 5 TDM formats (regular, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift).

This group of I2S pins are multiplexed in two different power domains, I2S1_M0 is multiplexed in VCCIO6, and I2S1_M1 is multiplexed in PMUIO2, and all signals can be derived from the entire group at both locations. The two multiplexing cannot be used at the same time, only one of them can be used at a time. The IO level of the I2S peripheral needs to be checked to match the power supply of the corresponding IO power domain.

I2S1 interface pull-up and pull-down and matching design recommendations are shown in the table:

Table 2-36 RK3588 I2S1 Interface Signal Description

Signal	Default method	Connection method	Description(chip end)
I2S1_MCLK_M0	pull down	22ohm resistor in series	I2S system clock output
I2S1_SCLK_M0	pull down	22ohm resistor in series	I2S continuous serial clock, bit clock
I2S1_LRCK_M0	pull down	22ohm resistor in series	I2S frame clock for channel selection
I2S1_SDO0_M0	pull up	Direct connection	I2S serial data 0 output
I2S1_SDO1_M0	pull up	Direct connection	I2S serial data 1 output
I2S1_SDO2_M0	pull up	Direct connection	I2S serial data 2 output
I2S1_SDO3_M0	pull up	Direct connection	I2S serial data 3 output
I2S1_SDI0_M0	pull down	Direct connection	I2S serial data 0 input
I2S1_SDI1_M0	pull down	Direct connection	I2S serial data 1 input
I2S1_SDI2_M0	pull down	Direct connection	I2S serial data 2 input
I2S1_SDI3_M0	pull down	Direct connection	I2S serial data 3 input
I2S1_MCLK_M1	pull down	22ohm resistor in series	I2S system clock output
I2S1_SCLK_M1	pull down	22ohm resistor in series	I2S continuous serial clock, bit clock
I2S1_LRCK_M1	pull down	22ohm resistor in series	I2S frame clock for channel selection
I2S1_SDO0_M1	pull up	Direct connection	I2S serial data 0 output
I2S1_SDO1_M1	pull up	Direct connection	I2S serial data 1 output
I2S1_SDO2_M1	pull up	Direct connection	I2S serial data 2 output
I2S1_SDO3_M1	pull up	Direct connection	I2S serial data 3 output
I2S1_SDI0_M1	pull up	Direct connection	I2S serial data 0 input
I2S1_SDI1_M1	pull up	Direct connection	I2S serial data 1 input
I2S1_SDI2_M1	pull down	Direct connection	I2S serial data 2 input
I2S1_SDI3_M1	pull down	Direct connection	I2S serial data 3 input

- In order to improve the performance of the I2S interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.2.3 I2S2 Digital Audio Interface

The I2S2 interface includes independent 2-channel output and 2-channel input. For output data SDOx and input data SDIx, refers to the same set of bit/frame clock SCLK/LRCK.

The I2S2 interface supports the master-slave working mode, and the software is configurable. Support 3 kinds of I2S formats (regular, left-justified, right-justified); support 4 kinds of PCM formats (early, late1, late2, late3).

This group of I2S pins are multiplexed in two different power domains, I2S2_M0 is multiplexed in VCCIO3, I2S2_M1 is multiplexed in VCCIO5, and the entire group can be used to lead out all signals in both locations. The two multiplexing cannot be used at the same time, only one of them can be used at a time. The IO level of the I2S peripheral needs to be checked to match the power supply of the corresponding IO power domain.

I2S2 interface pull-up and pull-down and matching design recommendations are shown in the table:

Table 2-37 RK3588 I2S2 Interface Signal Description

Signal	Default method	Connection method	Description(chip end)
I2S2_MCLK_M0	pull down	22ohm resistor in series	I2S system clock output
I2S2_SCLK_M0	pull down	22ohm resistor in series	I2S continuous serial clock, bit clock
I2S2_LRCK_M0	pull down	22ohm resistor in series	I2S frame clock for channel selection
I2S2_SDO_M0	pull down	Direct connection	I2S serial data 0 output
I2S2_SDIX_M0	pull down	Direct connection	I2S serial data 0 input
I2S2_MCLK_M1	pull up	22ohm resistor in series	I2S system clock output
I2S2_SCLK_M1	pull up	22ohm resistor in series	I2S continuous serial clock, bit clock
I2S2_LRCK_M1	pull down	22ohm resistor in series	I2S frame clock for channel selection
I2S2_SDO_M1	pull up	Direct connection	I2S serial data 0 output
I2S2_SDIX_M1	pull down	Direct connection	I2S serial data 0 input

- In order to improve the performance of the I2S interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.2.4 I2S3 Digital Audio Interface

The I2S3 interface includes independent 2-channel output and 2-channel input. For output data SDOx and input data SDIx, refer to the same set of bit/frame clock SCLK/LRCK.

The I2S3 interface supports the master-slave working mode, and the software is configurable. Support 3 kinds of I2S formats (regular, left-justified, right-justified); support 4 kinds of PCM formats (early, late1, late2, late3).

There is only one multiplexed I2S pin in this group, which is VCCIO5. The IO level of the I2S peripheral needs to be checked to match the power supply of the corresponding IO power domain.

I2S3 interface pull-up and pull-down and matching design recommendations are shown in the table:

Table 2-38 RK3588 I2S3 Interface Design

Signal	Default method	Connection method	Description(chip end)
I2S3_MCLK	pull up	22ohm resistor in series	I2S system clock output
I2S3_SCLK	pull up	22ohm resistor in series	I2S continuous serial clock, bit clock
I2S3_LRCK	pull up	22ohm resistor in series	I2S frame clock for channel selection
I2S3_SDO	pull up	Direct connection	I2S serial data 0 output
I2S3_SDIX	pull down	Direct connection	I2S serial data 0 input

- In order to improve the performance of the I2S interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.3 PDM Digital Audio Interface

RK3588 provides a total of 2 sets of PDM interfaces, all of which can be connected to external interfaces.

Both sets of PDMS work in master receive mode (RK3588 provides PDM clock and receives data) and supports 8-channel input capabilities, a bit width of 16 to 32 bits, and a sampling rate of up to 192kHz.

The PDM interface is usually used to connect to a digital microphone, or to record an analog microphone through the analog audio ADC of the PDM interface.

The following figure shows the data format of the PDM interface. PDM_DATA consists of Data(R) and Data(L). PDM is a 1-bit sampling interface. The Data(L) and Data(R) are sampled on the rising and falling edges of CLK respectively. That is, each PDM_SDIX data line can transmit two channels of audio data.

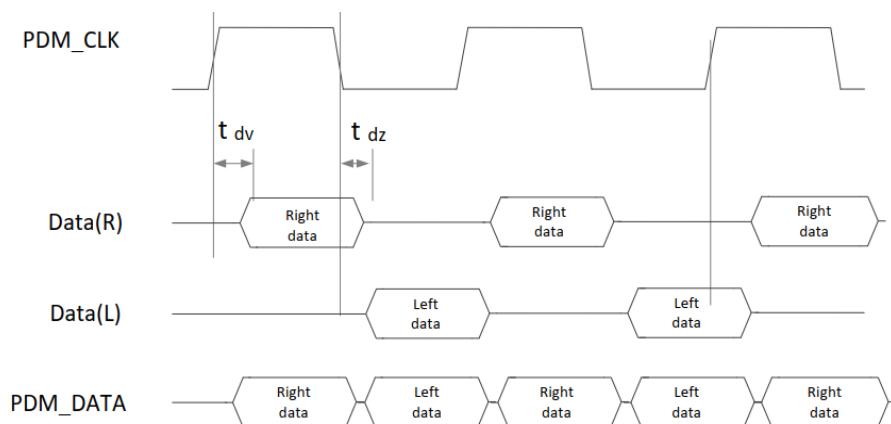


Figure 2-166 RK3588 PDM Interface Data Format

The corresponding relationship between common sampling rate and PDM_CLK is as follows, which can be referred during hardware commissioning:

Table 2-39 RK3588 PDM_CLK Frequency and Sampling Rate Comparison Table

PDM_CLK frequency	Sampling rate
3.072MHz	12kHz, 24kHz, 48kHz, 96kHz, 192kHz
2.8224MHz	11.025kHz, 22.05kHz, 44.1kHz, 88.2kHz, 176.4kHz
2.048MHz	8kHz, 16kHz, 32kHz, 64kHz, 128kHz

2.3.9.3.1 PDM0 Digital Audio Interface

PDM0 pins are multiplexed in two different power domains, PDM0_M0 is multiplexed in VCCIO1, and PDM0_M1 is multiplexed in PMUIO2. The two multiplexing cannot be used at the same time, only one of them can be used at a time. It is necessary to check the IO level of the PDM peripheral to match the power supply of the corresponding IO power domain.

PDM0 interface pull-up and pull-down and matching design recommendations are shown in the table. In order to improve the influence of PCB wiring on the clock, two PDM clocks of the same origin and phase are provided, PDM_CLK0 and PDM_CLK1, which can be allocated and used according to the layout wiring requirements to avoid the influence of branching in the case of a single CLK wiring.

Table 2-40 RK3588 PDM0 Interface Signal Description

Signal	Default method	Connection method	Description(chip end)
PDM0_CLK0_M0	pull down	22ohm resistor in series	PDM clock 0
PDM0_CLK1_M0	pull down	22ohm resistor in series	PDM clock 1
PDM0_SDIO_M0	pull down	Direct connection	PDM data input0
PDM0_SDII_M0	pull down	Direct connection	PDM data input1
PDM0_SDII_M0	pull down	Direct connection	PDM data input2
PDM0_SDIII_M0	pull down	Direct connection	PDM data input3
PDM0_CLK0_M1	pull down	22ohm resistor in series	PDM clock 0
PDM0_CLK1_M1	pull down	22ohm resistor in series	PDM clock 1
PDM0_SDIO_M1	pull down	Direct connection	PDM data input0
PDM0_SDII_M1	pull down	Direct connection	PDM data input1
PDM0_SDII_M1	pull up	Direct connection	PDM data input2
PDM0_SDIII_M1	pull down	Direct connection	PDM data input3

- In order to improve the performance of the PDM interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.3.2 PDM1 Digital Audio Interface

PDM1 pins are multiplexed in two different power domains, PDM1_M0 is multiplexed in VCCIO2, and PDM1_M1 is multiplexed in VCCIO4. The two multiplexing cannot be used at the same time, only one of them can be used at a time. It is necessary to check the IO level of the PDM peripheral to match the power supply of the corresponding IO power domain.

PDM1 interface pull-up and pull-down and matching design recommendations are shown in the table. In order to improve the influence of PCB wiring on the clock, two PDM clocks of the same origin and phase are provided, PDM_CLK0 and PDM_CLK1, which can be allocated and used according to the layout wiring requirements to avoid the influence of branching in the case of a single CLK wiring.

Table 2-41RK3588 PDM1 Interface Signal Description

Signal	Default method	Connection method	Description(chip end)
PDM1_CLK0_M0	pull down	22ohm resistor in series	PDM clock 0
PDM1_CLK1_M0	pull up	22ohm resistor in series	PDM clock 1
PDM1_SDIO_M0	pull up	Direct connection	PDM data input 0
PDM1_SDII_M0	pull up	Direct connection	PDM data input 1
PDM1_SDII_M0	pull up	Direct connection	PDM data input 2
PDM1_SDIII_M0	pull up	Direct connection	PDM data input 3
PDM1_CLK0_M1	pull up	22ohm resistor in series	PDM clock 0
PDM1_CLK1_M1	pull down	22ohm resistor in series	PDM clock 1

Signal	Default method	Connection method	Description(chip end)
PDM1_SDI0_M1	pull up	Direct connection	PDM data input 0
PDM1_SDI1_M1	pull up	Direct connection	PDM data input 1
PDM1_SDI2_M1	pull down	Direct connection	PDM data input 2
PDM1_SDI3_M1	pull down	Direct connection	PDM data input 3

- In order to improve the performance of the PDM interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.4 SPDIF TX Digital Audio Interface

2.3.9.4.1 SPDIF0_TX Digital Audio Interface

SPDIF0_TX pin is multiplexed in two different power domains, SPDIF0_TX_M0 is multiplexed in VCCIO4, GPIO1_B6; SPDIF0_TX_M1 is multiplexed in VCCIO6, GPIO4_B4. Need to check the IO level of the SPDIF_TX peripheral to match the power supply of the corresponding IO power domain.

SPDIF interface pull-down and matching design recommendations are shown in the table:

Table 2-42 RK3588 SPDIF0_TX Interface Signal Description

Signal and multiplexing situation	Default method	Connection method	Power domain
SPDIF0_TX_M0	Pull up	22ohm resistor in series	VCCIO5
SPDIF0_TX_M1	Pull up	22ohm resistor in series	VCCIO6

- In order to improve the performance of the SPDIF interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.4.2 SPDIF1_TX Digital Audio Interface

The SPDIF1_TX pin is multiplexed in three places, respectively in two different power domains, SPDIF1_TX_M0 is multiplexed in VCCIO4, GPIO1_B7; SPDIF1_TX_M1 is multiplexed in VCCIO6, GPIO4_B1; SPDIF1_TX_M2 is multiplexed in VCCIO6, GPIO4_C1. Need to check the IO level of the SPDIF_TX peripheral to match the power supply of the corresponding IO power domain.

SPDIF interface pull-down and matching design recommendations are shown in the table:

Table 2-43 RK3588 SPDIF1_TX Interface Signal Description

Signal and multiplexing situation	Default method	Connection method	Power domain
SPDIF1_TX_M0	Pull up	22ohm resistor in series	VCCIO5
SPDIF1_TX_M1	Pull up	22ohm resistor in series	VCCIO6
SPDIF1_TX_M2	Pull down	22ohm resistor in series	VCCIO6

- In order to improve the performance of the SPDIF interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.5 DSM PWM Audio Audio Interface

DSM PWM Audio refers to the 1-bit signal stream data converted and outputted by Direct Stream Digital encoding of audio PCM data. In a design that is not equipped with a high-performance audio DAC and requires a voice and audio output, this interface can be used. The audio signal is obtained by the first-order RC low-pass filtering process, as shown in the figure below, the output digital signal is filtered to obtain the audio signal.

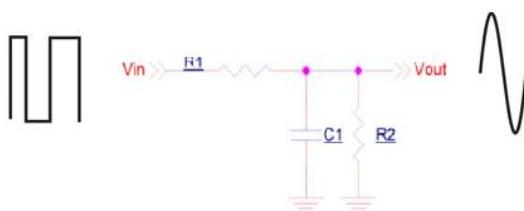


Figure 2-167 Schematic diagram of RK3588 DSM PWM Audio low-pass filter

This group of interfaces provides two pairs of differential outputs to meet the needs of stereo. For detailed introduction of the interface and calculation of RC low-pass filter parameters, please refer to the document "DSMAUDIO Audio Interface Circuit Design".

Table 2-44 RK3588 DSM PWM Audio Interface Signal Description

Signal and multiplexing situation	Default method	Connection method	Power domain
AUDDSM_LN	pull up	RC low-pass filter in series	VCCIO5
AUDDSM_LP	pull up	RC low-pass filter in series	VCCIO5
AUDDSM_RN	pull up	RC low-pass filter in series	VCCIO5
AUDDSM_RP	Pull down	RC low-pass filter in series	VCCIO5

- In order to improve the performance of the DSM PWM Audio interface, the decoupling capacitor corresponding to the VCCIO power domain can not be deleted. Please place it close to the pins during layout;
- When the board-to-board connection is realized through the connector, it is recommended that the clock/control/signal are connected in series with a certain resistance resistor (between 22ohm-100ohm, specific to meet the SI test), and reserve TVS devices.

2.3.9.6 Design Reference for Audio Peripherals

In most cases, the digital audio interface mentioned above cannot be used directly, and specific audio capabilities can be realized by supporting related peripherals. This chapter gives design suggestions for commonly used audio scenes, and users can refer to them.

2.3.9.6.1 Playback Equipment, Earphones, Speakers

For speaker playback requirements, the implementation plan is as follows. RK3588 connects audio DAC through I2S to achieve analog output, and then uses audio amplifier to achieve power amplification to drive the speaker:

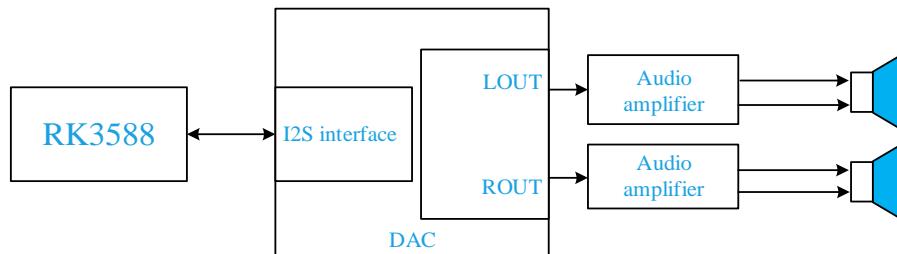


Figure 2-168 RK3588 Speaker Output Diagram

For scenarios with low sound quality and strict costs requirements, the output path through DSM PWM Audio is shown as follows. It is recommended to evaluate the audio quality before using this solution, for example, for simple voice broadcast and other purposes:

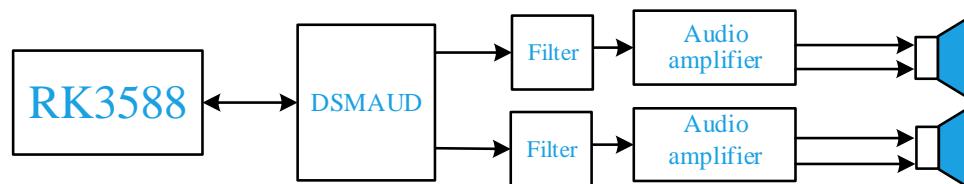


Figure 2-169 RK3588 Low-Cost Speaker Output Schematic Diagram

2.3.9.6.2 Recording Equipment, Microphone

In application scenarios such as tablets and laptops, in addition to playback, there is also a need for recording. At this time, Codec with integrated ADC and DAC is usually used to implement related functions. As shown in the figure below. For more complex functional design reference, such as 4G calls and Bluetooth calls, please contact RK at this stage to obtain:

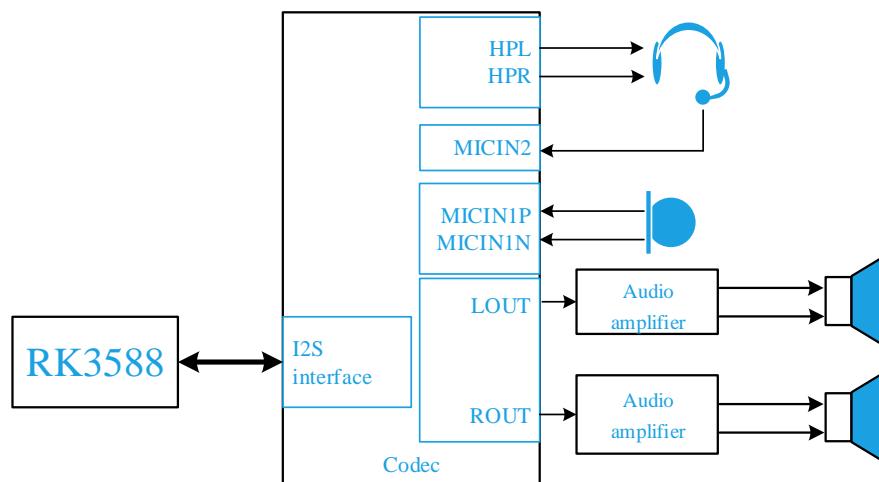


Figure 2-170 Schematic Diagram of RK3588 Typical Audio Solution

2.3.9.6.3 Introduction to the Multi-Microphone Solution

For scenarios with multiple microphone inputs (microphone array, far-field recognition), more microphones need to be connected at this time. There are three common expansion schemes as follows. If none of them can meet the specific needs, you can contact RK to discuss the feasibility:

- Method 1: Realize the input collection of multiple microphones and speakers loopback through the Codec of the I2S interface;
- Method 2: Realize the input collection of multiple microphones and speakers loopback through the Codec of the PDM interface;
- Method 3: Realize recording through the microphone of the PDM interface, and realize the input collection of the speaker loopback through the Codec of the PDM interface;

If there are insufficient channels, it can use multiple SDI signal lines to achieve multiple groups of inputs, or implement cascaded inputs through the TDM mode of the I2S interface. Simply stack the same circuits on the hardware.

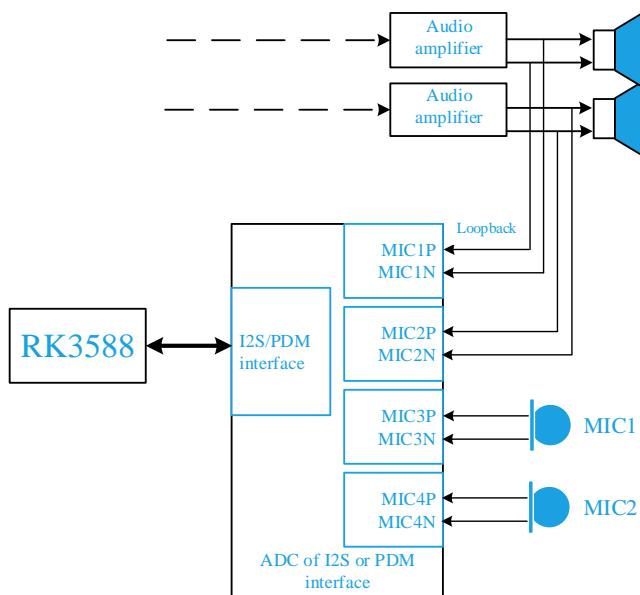


Figure 2-171 Schematic Diagram of RK3588 Multi-Microphone Solution

2.3.10 GMAC Interface Circuit

RK3588 has 2 GMAC controllers, providing RMII or RGMII interface to connect to external Ethernet PHY. The GMAC controller supports the following functions:

- RGMII interface supporting 10/100/1000 Mbps data transmission rate;
- RMII interface supporting 10/100 Mbps data transmission rate.

The RGMII/RMII interface of GMAC0 is multiplexed in the VCCIO3 power domain.

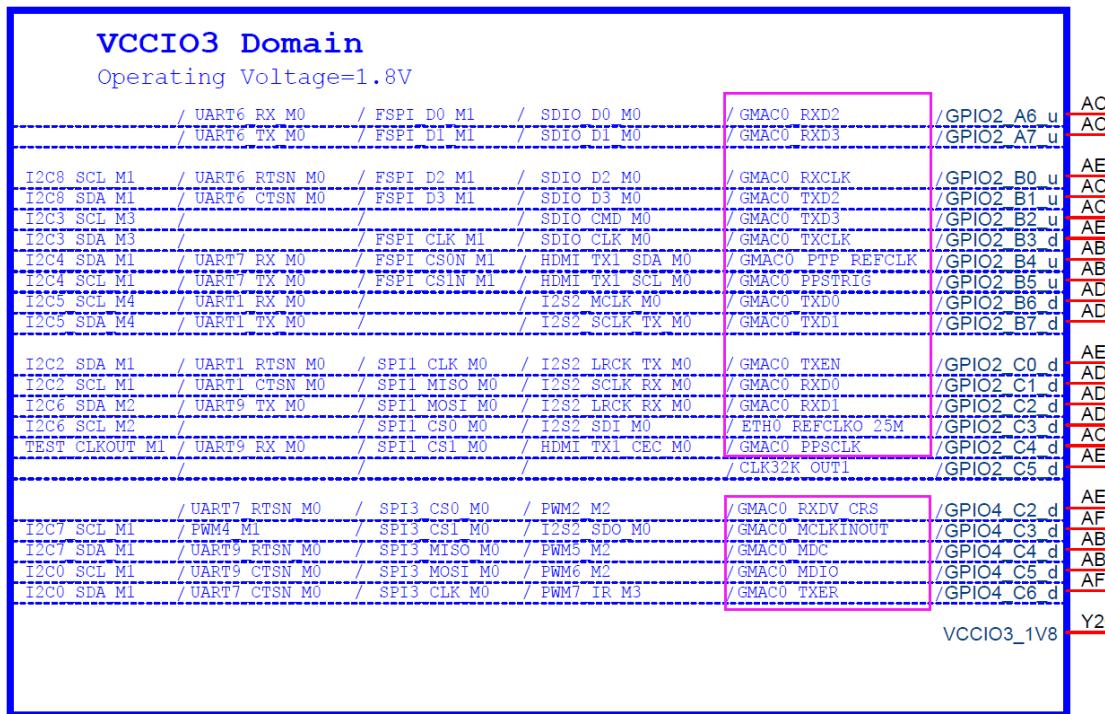


Figure 2-172 RK3588 GMAC0 Function Pin

The RGMII/RMII interface of GMAC1 is multiplexed in the VCCIO5 power domain.

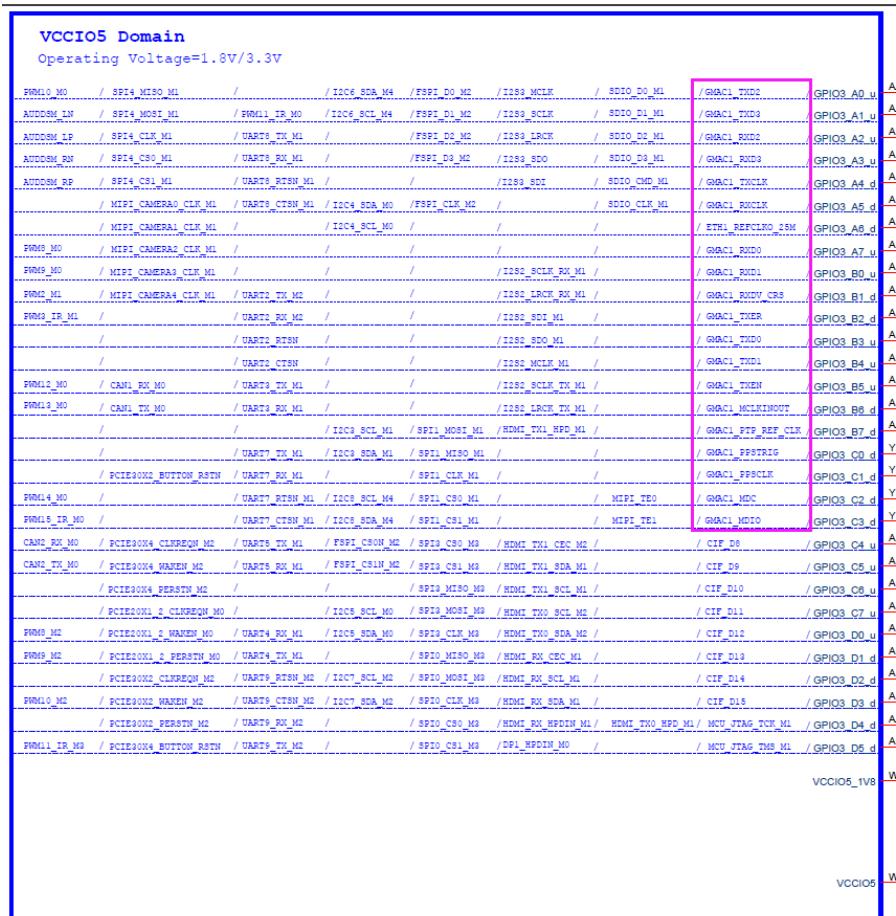


Figure 2-173 RK3588 GMAC1 Function Pin

Please pay attention to the RGMII/RMII interface design:

- GMAC0 multiplexed in the VCCIO3 power domain only supports 1.8V level;
- GMAC1 is multiplexed in the VCCIO5 power domain and can support 1.8V or 3.3V level, which is determined by VCCIO5 (Pin W26). When Pin W26 is connected to 1.8V power supply, it is 1.8V power level, when Pin W26 is connected to 3.3V power supply, it is 3.3V power supply. (Note that Pin W25 is fixedly connected to 1.8V power supply);
- If conditions permit, it is recommended that RGMII/RMII use 1.8V level to obtain better signal quality;
- In order to improve the performance of the RGMII/RMII interface, the decoupling capacitor of the VCCIOx power supply must not be deleted, and please place it close to the pins during layout;
- ETH0_REFCLKO_25M needs to reserve a 0 ohm resistor in series at the RK3588 end to improve the signal quality according to the actual situation;
- ETH1_REFCLKO_25M needs to reserve a 0 ohm resistor in series at the RK3588 end to improve the signal quality according to the actual situation;
- TXD0-TXD3, TXCLK, TXEN need to reserve a 0 ohm resistor in series at the RK3588 end to improve the signal quality according to the actual situation;
- RXD0-RXD3, RXCLK, RXDV need to connect 22 ohm resistor in series at the PHY end to improve the signal quality;
- RGMII/RMII interface pull-up and pull-down and matching design recommendations are shown in the table:

Table 2-45 RK3588 RGMII Interface Design

Signal	IO type (chip end)	Connection method	RGMII interface	Description
GMACx_TXD[3:0]	output	A 0ohm resistor in series, close to RK3588 end	RGMIIx_TXD[3:0]	Data sent
GMACx_TXCLK	output	A 0ohm resistor in series, close to RK3588 end	RGMIIx_TXCLK	Data sent reference clock
GMACx_TXEN	output	A 0ohm resistor in series, close to RK3588 end	RGMIIx_TXEN	Data sent enable (rising) and data sent error (falling)
GMACx_RXD[3:0]	input	A 22ohm resistor in series, close to PHY end	RGMIIx_RXD[3:0]	Data receive
GMACx_RXCLK	input	A 22ohm resistor in series, close to PHY end	RGMIIx_RXCLK	Data receive reference clock
GMACx_RXDV	input	A 22ohm resistor in series, close to PHY end	RGMIIx_RXDV	Data reception valid (rising) and receiving error (falling edge)
GMACx_MCLKINOUT	input/ output	Output mode: A 22ohm resistor in series, close to RK3588 end Input mode: A 22ohm resistor in series, close to PHY end	RGMIIx_MCLKIN_125M	PHY sends 125MHz to MAC, optional
ETHx_REFCLKO_25M	output	A 22ohm resistor in series, close to RK3588 end	ETHx_REFCLKO_25M	RK3588 provides 25MHz clock instead of PHY crystal
GMACx_MDC	output	A 22ohm resistor in series, close to RK3588 end	RGMIIx_MDC	Manage data clock
GMACx_MDIO	input/ output	A 22ohm resistor in series and pull up 1.5K-1.8Kohm resistor externally	RGMIIx_MDIO	Manage data output/input

Table 2-46 RK3588 RMII Interface Design

Signal	IO type (chip end)	Connection method	RMII interface	Description
GMACx_TXD[3:0]	output	A 22ohm resistor in series, close to RK3588 end	RMIIx_TXD[1:0]	Data sent
GMACx_RXCLK	output	A 22ohm resistor in series, close to RK3588 end	--	--
GMACx_TXEN	output	A 22ohm resistor in series, close to RK3588 end	RMIIx_TXEN	Data sent using signal
GMACx_RXD[3:0]	input	A 22ohm resistor in series, close to PHY end	RMIIx_RXD[1:0]	Data receive
GMACx_RXCLK	input	A 22ohm resistor in series, close to PHY end	--	--
GMACx_RXDV	input	A 22ohm resistor in series, close to PHY end	RMIIx_RXDV_CRS	Effective data receive and carrier sense
GMACx_MCLKINOUT	input/ output	Output mode: A 22ohm resistor in series, close to RK3588 end Input mode: A 22ohm resistor in series, close to PHY end	RMII_MCLKIN_50M or RMII_MCLKOUT_50M	RMII data sent and data receive reference clock
ETHx_REFCLKO_25M	output	A 22ohm resistor in series, close to RK3588 end	ETHx_REFCLKO_25M	RK3588 provides 25MHz clock instead of PHY crystal
GMACx_MDC	output	A 22ohm resistor in series, close to RK3588 end	RMIIx_MDC	Manage data clock
GMACx_MDIO	input/ output	A 22ohm resistor in series and pull up 1.5K-1.8Kohm resistor externally	RMIIx_MDIO	Manage data output/input

- When the board-to-board connection is realized through the connector, it is recommended to connect a resistor in series with the resistance value between 22ohm-100ohm, and the specific requirements shall be subject to the SI test. And reserve TVS devices;
- RGMII connection diagram 1 is as follows, please refer to the reference diagram for the specific circuit (GEPHY working clock uses an external 25MHz crystal):

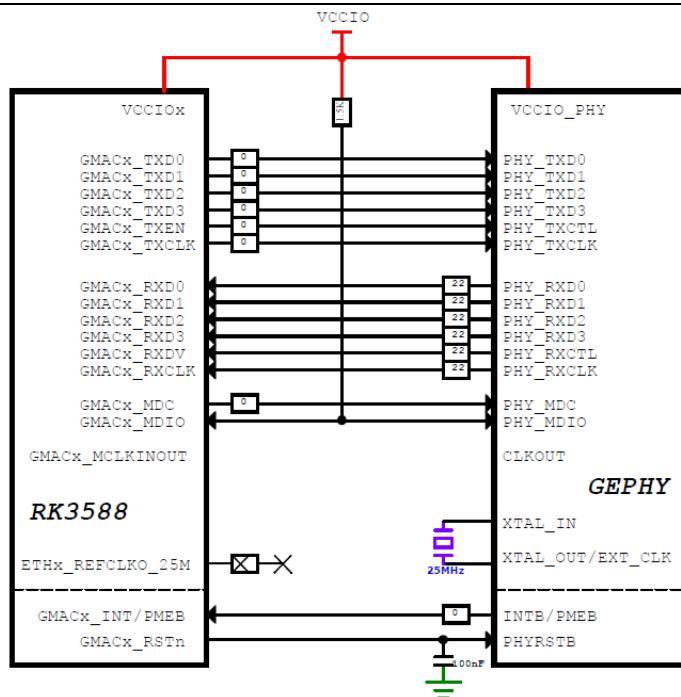


Figure 2-174 RGMII Connection Diagram 1

- RGMII connection diagram 2 is as follows (Take RTL8211F as an example), please refer to the reference diagram for the specific circuit (GEPHY working clock uses 25MHz provided by RK3588):

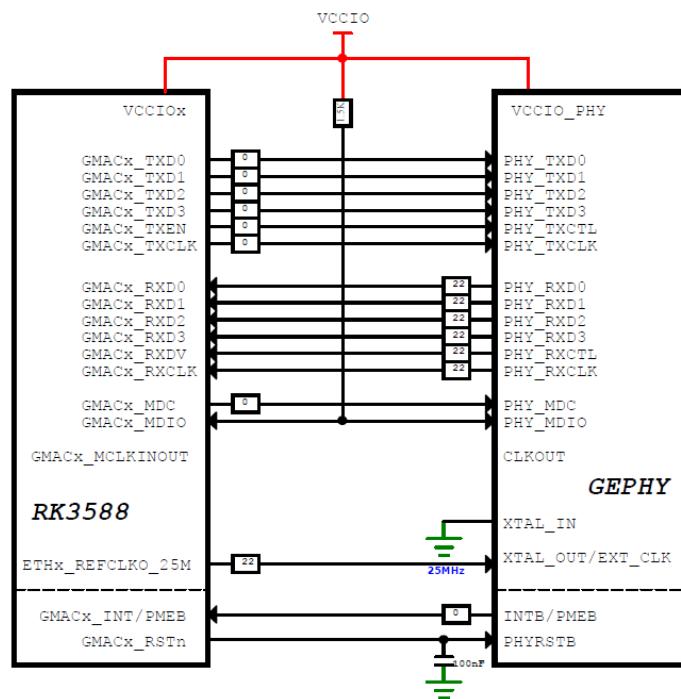


Figure 2-175 RGMII Connection Diagram 2

- RMII connection diagram 1 is as follows (Take RTL8201F as an example), please refer to the reference diagram for the specific circuit (GMACx_MCLKINOUT adopts the output mode, that is, when the FEPHY working clock is also used as the reference clock of the RMII interface. Please note some FEPHY does not support this mode):

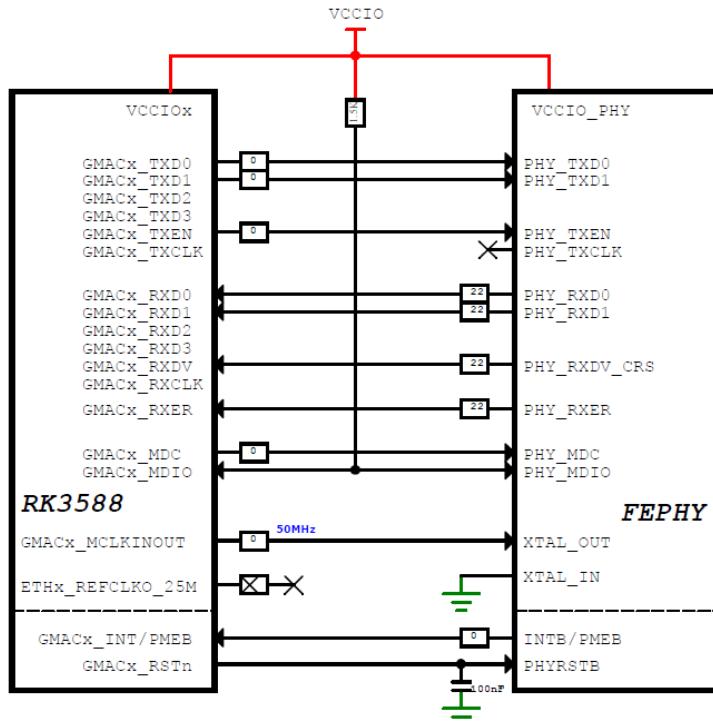


Figure 2-176 RMII Connection Diagram 1

- RMII connection diagram 2 is as follows, see the reference diagram for the specific circuit (FEPHY working clock uses 25MHz crystal, GMACx_MCLKINOUT adopts output mode, when RMII interface reference clock, FEPHY TXCLK needs to be configured as input mode):

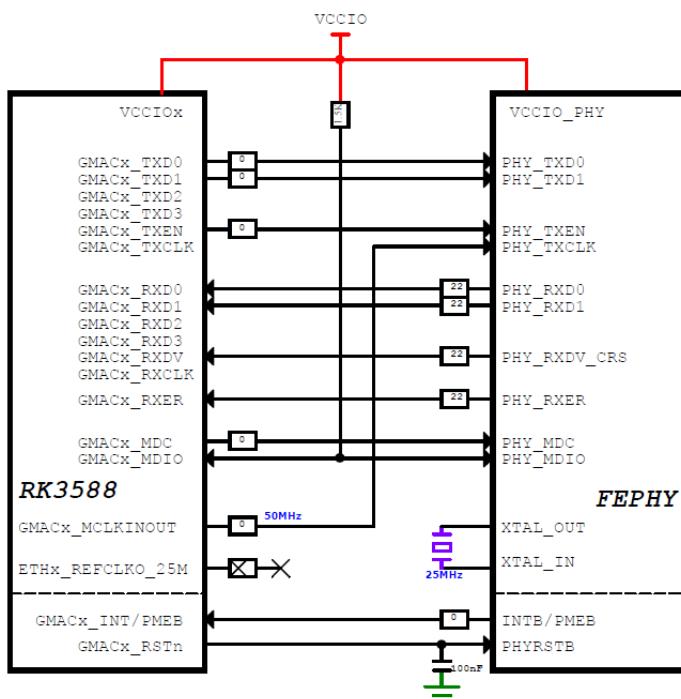


Figure 2-177 RMII Connection Diagram 2

- RMII connection diagram 3 is as follows (Take RTL8201F as an example), please refer to the reference diagram for the specific circuit (use the 25MHz provided by RK3588 to replace the FEPHY crystal, GMACx_MCLKINOUT adopts the output mode, when the RMII interface is the reference clock, the

FEPHY TXCLK needs to be configured as the input mode):

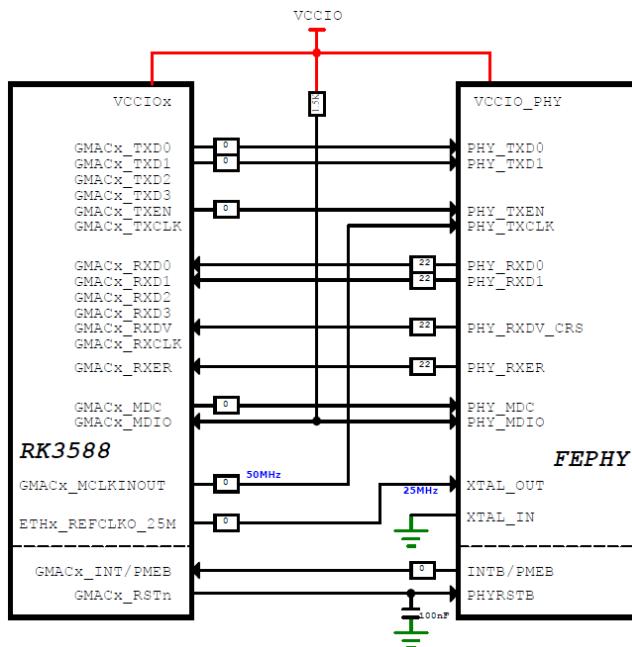


Figure 2-178 RMII Connection Diagram 3

- RMII connection diagram 4 is as follows, please refer to the reference diagram for the specific circuit (FEPHY working clock uses an external 25MHz crystal, GMACx_MCLKINOUT uses input mode, RMII interface reference clock is provided by FEPHY, and FEPHY TXCLK needs to be configured as output mode):

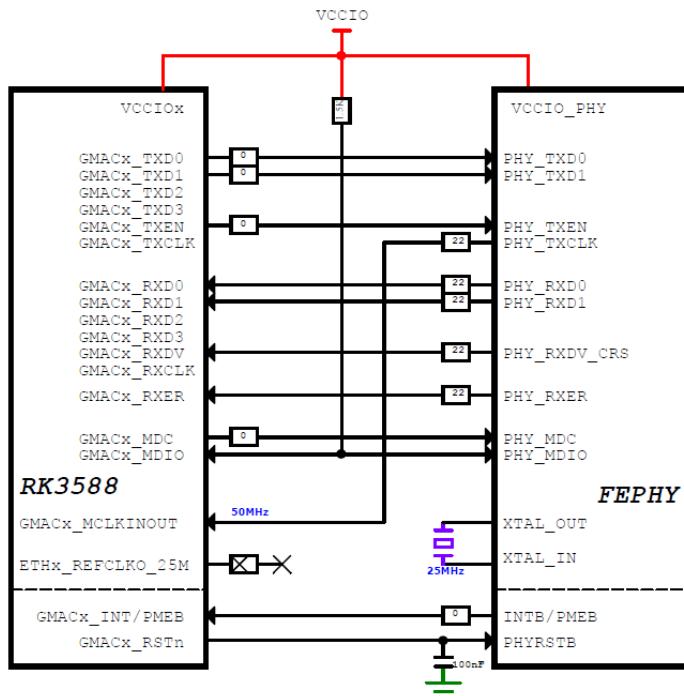


Figure 2-179 RMII Connection Diagram 4

- RMII connection diagram 5 is as follows (Take RTL8201F as an example), please refer to the reference diagram for the specific circuit (use the 25MHz provided by RK3588 to replace the FEPHY crystal, GMACx_MCLKINOUT adopts the input mode, the reference clock of the RMII interface is provided by

FEPHY, and the TXCLK of FEPHY needs to be configured as output mode):

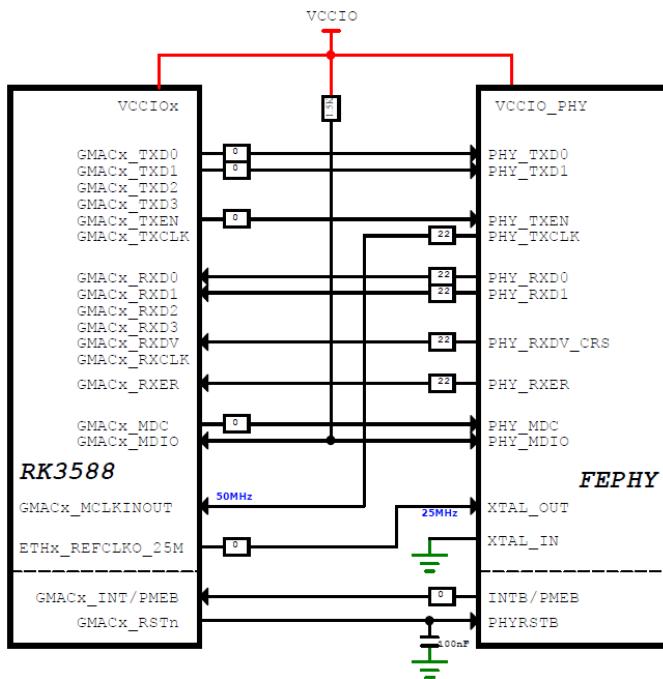


Figure 2-180 RMII Connection Diagram 5

- In RGMII mode, the TX/RX clock path inside the RK3588 chip integrates a delayline, which supports adjustment. The default configuration of the reference diagram is: the timing between TXCLK and data is controlled by MAC, and the timing between RXCLK and data is controlled by PHY (if RTL8211F/FI is used, that is, RXCLK turns on 2nS delay by default, other PHYs should pay attention to this configuration);
- The reset signal of the Ethernet PHY needs to be controlled by GPIO. The GPIO level must match the PHY IO level. A 100nF capacitor must be added close to the PHY pin to strengthen the antistatic ability.
Note: The reset pin of RTL8211F/FI only supports 3.3V power;
- The INTB/PMEB of RTL8211F/FI is an open-drain output, and an external pull-up resistor must be added;
- When using an external crystal for PHY, please select the crystal capacitance according to the load capacitance value of the crystal actually used, and control the frequency deviation within +/-20ppm;
- The external resistance of the RSET pin of RTL8211F/FI is 2.49KOHM, the accuracy is 1%, and it cannot be modified at will;
- MDIO must be externally connected with a pull-up resistor, 1.5-1.8Kohm is recommended, and the pull-up power supply must be consistent with the IO power supply;
- The connection of the center tap of the transformer of RTL8211F/FI must be connected according to the reference diagram. If you change to another Ethernet PHY, then the connection of the center tap of the transformer is recommended to refer to the reference design of each Ethernet PHY manufacturer, because different PHY manufacturers have different connection methods;
- It is recommended to use high-voltage safety capacitors for 1000pF isolation capacitors, with sufficient electrical clearance to ensure the safety of lightning strikes;
- The 75ohm resistor on the high voltage side of the network transformer is recommended to be packaged with a package of 0805 or more;

- When the lightning protection level reaches 4KV or higher, an anti-detoner is needed. Ordinary isolation transformers can only meet the requirements of 2KV;
- If there is a lightning differential test requirement, TVS tubes need to be added between MDI differential pairs;
- Be sure to confirm whether the RJ45 package is consistent with the schematic. RJ45 has Tab down and Tab up, and the signal sequence is just the opposite. If you use RTL8211F/FI, it is recommended to use Tab down, and the MDI sequence is straight;
- The initial hardware configuration of the PHY must match the actual requirements.

2.3.11 UART Interface Circuit

The RK3588 chip has 10 UART controllers and supports the following functions:

- Both contain two 64-byte FIFOs for data reception and transmission;
- Support 115.2Kbps, 460.8Kbps, 921.6Kbps, 1.5Mbps, 3Mbps, 4Mbps;
- Support programmable baud rate, support non-integer clock divider;
- Support interrupt-based or DMA-based mode;
- Support 5-8bit width transmission.

Considering the application flexibility of different products, 10 UARTs are multiplexed in several different power domains, and the suffixes _M0/_M1/_M2 are used to distinguish different multiplexing positions. _M0/_M1/_M2 cannot be used at the same time. You can only select one of them when assigning. You cannot select M0 for some signals, M1 for some, and M2 for some, such situation is not supported.

RK3588 UART interface distribution:

Table 2-47 RK3588 UART Interface Distribution

UART No.	multiplex	Multiplex power domain
UART0	M0,M1,M2	M0:PMUIO2 M1:PMUIO1 M2:VCCIO6
UART1	M0,M1,M2	M0:VCCIO3 M1:VCCIO4 M2:PMUIO2
UART2	M0,M1,M2	M0:PMUIO2 M1:VCCIO2 M2:VCCIO5
UART3	M0,M1,M2	M0:VCCIO1 M1:VCCIO5 M2:VCCIO6
UART4	M0,M1,M2	M0:VCCIO1 M1:VCCIO5 M2:VCCIO4
UART5	M0,M1,M2	M0:VCCIO2 M1:VCCIO5 M2:EMMCIO
UART6	M0,M1,M2	M0:VCCIO3 M1:VCCIO4 M2:VCCIO1
UART7	M0,M1,M2	M0:VCCIO3 M1:VCCIO5 M2:VCCIO4

UART No.	multiplex	Multiplex power domain
UART8	M0,M1	M0:VCCIO6 M1:VCCIO5
UART9	M0,M1,M2	M0:VCCIO3 M1:VCCIO6 M2:VCCIO5

Table 2-48 RK3588 UART Flow Control Interface Distribution

UART No.	multiplex	Multiplex power domain
UART0_RTSN UART0_CTSN	None	None
UART1_RTSN UART1_CTSN	M0,M1,M2	M0:VCCIO3 M1:VCCIO4 M2:PMUIO2
UART2_RTSN UART2_CTSN	None	VCCIO5
UART3_RTSN UART3_CTSN	None	VCCIO1
UART4_RTSN UART4_CTSN	None	VCCIO1
UART5_RTSN UART5_CTSN	M0,M1	M0:VCCIO2 M1:EMMCIO
UART6_RTSN UART6_CTSN	M0,M1	M0:VCCIO3 M1:VCCIO4
UART7_RTSN UART7_CTSN	M0,M1	M0:VCCIO3 M1:VCCIO5
UART8_RTSN UART8_CTSN	M0,M1	M0:VCCIO6 M1:VCCIO5
UART9_RTSN UART9_CTSN	M0,M1,M2	M0:VCCIO3 M1:VCCIO6 M2:VCCIO5

Among them, UART2 M0 is the Debug UART of RK3588 by default.

According to the IO level of the UART peripheral, adjust the power supply of the corresponding power domain, which must be consistent.

UART interface pull-down and matching design recommendations are shown in the table:

Table 2-49 RK3588 UART Interface Design

Signal	Connection method	Description (chip end)
UARTx_RX	Direct connection	UART data input
UARTx_TX	Direct connection	UART data output
UARTx_CTSn	Direct connection	UART allows to send signals
UARTx_RTStn	Direct connection	UART request to send signal

When realizing board-to-board connection through connectors, please reserve TVS devices.

2.3.12 SPI Interface Circuit

In addition to the FSPI controller, the RK3588 also has 5 general-purpose SPI controllers that support the following functions:

- Support two modes of master and slave;
- Support 4, 8, 16 bit serial data transmission;
- Support full-duplex and half-duplex mode transmission.

Considering the application flexibility of different products, these SPIs are multiplexed in several different power domains, and the suffix _M0/_M1/_M2/_M3 is used to distinguish different multiplexing positions. _M0/_M1/_M2/_M3 cannot be used at the same time, only one of them can be selected when assigning, and M0 cannot be selected for some signals, and M1 for some signals.

RK3588 SPI interface distribution:

Table 2-50 RK3588 SPI Interface Distribution

SPI No.	multiplex	Multiplex power domain
SPI0	M0, M1, M2, M3	M0: PMUIO2 M1: VCCIO6 M2: VCCIO4 M3: VCCIO5
SPI1	M0, M1, M2	M0: VCCIO3 M1: VCCIO5 M2: VCCIO1
SPI2	M0, M1, M2	M0: VCCIO4 M1: VCCIO6 M2: PMUIO1
SPI3	M0, M1, M2, M3	M0: VCCIO3 M1: VCCIO6 M2: PMUIO2 M3: VCCIO5
SPI4	M0, M1, M2	M0: VCCIO1 M1: VCCIO5 M2: VCCIO4

According to the IO level of the SPI peripheral, adjust the power supply of the corresponding power domain, which must be consistent.

SPI2 is assigned to PMIC by default, which is convenient for software, and it is better not to change it.

The pull-down and matching design recommendations of the SPI interface are shown in the table below:

Table 2-51 RK3588 SPI Interface Design

Signal	Connection method	Description (chip end)
SPIx_CLK	direct connection	SPI clock
SPIx_MOSI	direct connection	SPI data output (Master)
SPIx_MISO	direct connection	SPI data input (Master)
SPIx_CS0	direct connection	SPI Chip Select 0
SPIx_CS1	direct connection	SPI Chip Select 1

When the board-to-board connection is achieved through the connector, the TVS device is reserved.

2.3.13 CAN Interface Circuit

The RK3588 chip has 3 CAN controllers and supports the following functions:

- Support CAN 2.0B protocol;
- Support 1Mbps.

Considering the application flexibility of different products, the three CANs are multiplexed in several different power domains, and the suffix _M0/_M1 is used to distinguish different multiplexing positions. _M0/_M1 cannot be used at the same time, and only one of them can be selected when assigning. For example, if CAN_M0 is selected, CAN_M1 cannot be selected.

RK3588 CAN interface distribution:

Table 2-52 RK3588 CAN Interface Distribution

CAN No.	multiplex	Multiplex power domain
CAN0	M0, M1	M0: PMUIO2; M1: VCCIO2
CAN1	M0, M1	M0: VCCIO5; M1: VCCIO6
CAN2	M0, M1	M0: VCCIO5; M1: VCCIO2

According to the IO level of the CAN peripheral, adjust the power supply of the corresponding power domain, which must be consistent.

The pull-down and matching design recommendations of the CAN interface are shown in the table below:

Table 2-53 RK3588 CAN Interface Design

Signal	Connection method	Description (chip end)
CANx_RX	direct connection	CAN data input
CANx_TX	direct connection	CAN data output

When the board-to-board connection is realized through the connector, it is recommended to connect a resistor with a certain resistance value (between 22ohm-100ohm, which can meet the SI test), and reserve TVS devices.

2.3.14 I2C Interface Circuit

The RK3588 chip has 12 I2C controllers and supports the following functions:

- Support I2C bus master mode;
- Support software programmable clock frequency and transmission rate up to 400Kbit/s;
- Supports 7-bit and 10-bit addressing modes.

Considering the application flexibility of different products, these I2Cs are multiplexed in several different power domains, and the suffix _M0/_M1/_M2/_M3/_M4 is used to distinguish different multiplexing positions. _M0/_M1/_M2/_M3/_M4 cannot be used at the same time, only one of them can be selected when assigning, for example: I2C1_M0 cannot be selected, and I2C1_M1 or other M* can be selected.

The distribution of RK3588 I2C interface is as follows:

Table 2-54 RK3588 I2C Interface Distribution

I2C No.	multiplex	Multiplex power domain
I2C0	M0, M1, M2	M0: PMUIO1 M1: VCCIO3 M2: PMUIO2
I2C1	M0, M1, M2, M3, M4	M0: PMUIO2 M1: PMUIO1 M2: PMUIO2 M3: EMMCIO M4: VCCIO1
I2C2	M0, M1, M2, M3, M4	M0: PMUIO2 M1: VCCIO3 M2: EMMCIO M3: VCCIO1 M4: VCCIO4
I2C3	M0, M1, M2, M3, M4	M0: VCCIO1 M1: VCCIO5 M2: VCCIO6 M3: VCCIO3 M4: VCCIO2
I2C4	M0, M1, M2, M3, M4	M0: VCCIO5 M1: VCCIO3 M2: PMUIO2 M3: VCCIO4 M4: VCCIO1
I2C5	M0, M1, M2, M3, M4	M0: VCCIO5 M1: VCCIO6 M2: PMUIO6 M3: VCCIO4 M4: VCCIO3
I2C6	M0, M1, M2, M3, M4	M0: PMUIO2 M1: VCCIO1 M2: PMUIO3 M3: VCCIO6 M4: VCCIO5
I2C7	M0, M1, M2, M3	M0: VCCIO1 M1: VCCIO3 M2: PMUIO5 M3: VCCIO6
I2C8	M0, M1, M2, M3, M4	M0: VCCIO2 M1: VCCIO3 M2: PMUIO4 M3: VCCIO6 M4: VCCIO5
HDMI_TX0_I2C	M0, M1, M2	M0: VCCIO6 M1: PMUIO2 M2: VCCIO5
HDMI_TX1_I2C	M0, M1, M2	M0: VCCIO3 M1: VCCIO5 M2: VCCIO4
HDMI_RX_I2C	M0, M1, M2	M0: PMUIO2 M1: VCCIO5 M2: VCCIO4

HDMI_Txx_SCL/HDMI_Txx_SDA/ HDMI_RX_SCL/HDMI_RX_SDA is the I2C/DDC bus of the HDMI TX controller, which is a dedicated bus.

According to the IO level of the I2C peripheral, adjust the power supply of the corresponding power domain, which must be consistent.

I2C signals SCL and SDA need external pull-up resistors. Depending on the bus load, choose resistors with different resistance values. It is recommended to connect a 2.2kohm pull-up resistor.

The device addresses on the I2C bus should not conflict, and the pull-up power supply must be consistent with the power supply.

The pull-down and matching design recommendations of the I2C interface are shown in the table below:

Table 2-55 RK3588 I2C Interface Design

Signal	Connection methon	Description (chip end)
I2Cx_SCL	direct connection	I2C clock
I2Cx_SDA	direct connection	I2C data output/input

When the board-to-board connection is achieved through the connector, the TVS device is reserved.

2.3.15 PWM Interface Design

The RK3588 chip has integrated 4 independent PWM controllers, each controller has 4 channels, up to 16 PWM channels, and supports the following functions:

- Support capture mode;
- Support continuous mode or one-shot mode;
- Optimized for infrared applications of PWM3, PWM7, PWM11 and PWM15;
- Each channel has two optional clock inputs, one is the fixed frequency input from the crystal oscillator, the other is the frequency division from the PLL bus, and the frequency is configurable.

Considering the application flexibility of different products, these PWMs are multiplexed in several different power domains, and the suffix _M0/_M1 is used to distinguish different multiplexing positions.

The distribution of RK3588 PWM interface is shown in the following table:

Table 2-56 RK3588 PWM Interface Distribution

PWM No.	Multiplex	Multiplex power domain
PWM0	M0, M1, M2	M0: PMUIO2 M1: VCCIO1 M2: VCCIO4
PWM1	M0, M1, M2	M0: PMUIO2 M1: VCCIO1 M2: VCCIO4
PWM2	M0, M1, M2	M0: PMUIO2 M1: VCCIO5 M2: VCCIO3
PWM3_IR	M0, M1, M2, M3	M0: PMUIO2 M1: VCCIO5 M2: VCCIO1 M3: VCCIO4
PWM4	M0, M1	M0: PMUIO2 M1: VCCIO3
PWM5	M0, M1, M2	M0: PMUIO1 M1: PMUIO2 M2: VCCIO3

PWM No.	Multiplex	Multiplex power domain
PWM6	M0, M1, M2	M0: PMUIO2 M1: VCCIO6 M2: VCCIO3
PWM7_IR	M0, M1, M2, M3	M0: PMUIO2 M1: VCCIO2 M2: VCCIO1 M3: VCCIO3
PWM8	M0, M1, M2	M0: VCCIO5 M1: VCCIO2 M2: VCCIO2
PWM9	M0, M1, M2	M0: VCCIO5 M1: VCCIO1 M2: VCCIO5
PWM10	M0, M1, M2	M0: VCCIO5 M1: VCCIO2 M2: VCCIO5
PWM11_IR	M0, M1, M2, M3	M0: VCCIO5 M1: VCCIO6 M2: VCCIO1 M3: VCCIO3
PWM12	M0, M1	M0: VCCIO5 M1: VCCIO6
PWM13	M0, M1, M2	M0: VCCIO5 M1: VCCIO6 M2: VCCIO4
PWM14	M0, M1, M2	M0: VCCIO5 M1: VCCIO6 M2: VCCIO4
PWM15_IR	M0, M1, M2	M0: VCCIO5 M1: VCCIO6 M2: VCCIO1

- According to the IO level of the PWM peripheral, the adjustment of the corresponding power supply domain must be consistent;
- When the board-to-board connection is realized through the connector, it is recommended to connect a resistor with a certain resistance value (between 22ohm-100ohm, which can meet the SI test), and reserve TVS devices;
- When the infrared receiver signal is input, you need to pay attention to the following:
 - In standby, to support the wake-up of the infrared receiver, and considering low power consumption (ie, the VDD_LOGIC power-off scheme), only PWM3/PWM7 can be selected as the input of the infrared receiver;
 - The power of the infrared receiver needs to be powered by VCC3V3_PMU;
 - The power supply of the infrared receiver needs 22-100ohm resistor and more than 10uF capacitor for RC filtering;
 - The infrared receiving head adopts 38KHz by default, if it is changed to other frequency software, it needs to be adjusted accordingly;
 - The level of the output pin of the infrared receiver must match the IO level of the RK3588;
 - It is recommended to connect a 22 ohm resistor and a 1nF capacitor to the output pin of the infrared

receiver, and then connect it to the RK3588 to enhance the anti-static surge capability;

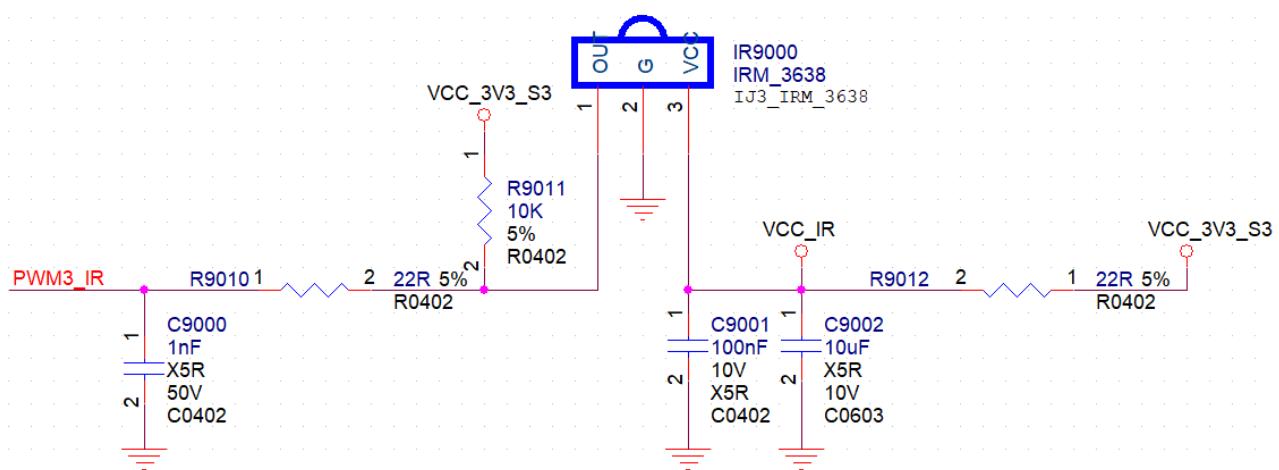


Figure 2-181 Infrared Receiver Circuit

- In the layout of the infrared receiver head, it should be far away from the wireless module antenna, such as the WIFI antenna, so as not to affect the infrared signal reception during wireless data transmission;
- The layout of the infrared receiving head should avoid the direct light of the LED light source on the board, so as to avoid the LED flickering frequency affecting the infrared receiving;
- It is recommended to process the IR signal in the whole process, but it cannot be processed in the whole process. It is recommended that the interval with other signals: ≥ 2 times the line width.

2.3.16 RK3588 Unused Module Pin Processing

Please refer to " RK3588 Methods for Processing Unused Pins_V1.1_20220915" document.

3 PCB Design Recommendations

3.1 PCB Layout Design

In order to reduce the reflection phenomenon in the process of high-speed signal transmission, impedance matching must be maintained on the signal source, the receiving end and the transmission line. The impedance of a single-ended signal line depends on its line width and its relative position to the reference layer. The line width/line spacing between the differential pairs required for a specific impedance depends on the selected PCB stackup. Since the minimum line width and minimum line distance depend on the PCB type and cost requirements, due to this limitation, the selected PCB stackup must be able to achieve all impedance requirements on the board, including inner and outer layers, single-ended and differential lines, etc.

Layer design rules:

- The layers neighboring to the chip is a ground layer, which provides a reference layer for device layer for routing;
- All signal layers are as close as possible to the ground layer
- Try to avoid two signal layers neighboring directly
- The main power supply is as close to the related ground as possible
- A symmetrical structure design should be adopted in principle. The meaning of symmetry includes: the thickness and type of the media layer, the thickness of the copper foil, and the symmetry of the graphic distribution type (large copper foil layer, circuit layer)

PCB multilayer recommended solution: When designing a specific PCB layers, the above rules should be used flexibly, and the layer arrangement should be determined according to actual requirements instead of applying mechanically. The recommended solutions for frequently used layer arrangements are given below for reference only. In layers setting, if there are neighboring layers for routing, the interlayer crosstalk can be reduced by increasing the distance between neighboring layers. For the case of cross-segmentation, ensure that the key signal must have a relatively complete reference ground plane or provide necessary bridging measures.

RK3588 currently uses 10-layer 1-stage, 10-layer 2-stage, 8-layer PTH PCB laminates. The following multilayer structure is an example to help customers in the selection and evaluation of multilayer structure. If you choose another type of multilayer structure, please recalculate the impedance according to the specifications given by PCB manufacturers.

3.1.1 10-Layer 1-Stage HDI PCB Design

In the 10-layer 1-stage PCB design, the reference layer of the top-level signal L1 is L2, and the reference layer of the bottom-level signal L10 is L9. It is recommended to stack as TOP-Signal/Gnd-Gnd/Power-Signal-Gnd/Power-Gnd/Power-Gnd/Power-Signal-Gnd-Bottom, of which 1oZ is recommended for L1, L2, L9, and L10, and HoZ for other inner layers. The following figure shows the reference stack and characteristic impedance line width of 1.6mm board thickness.

Customer Name:					Total Thickness:	1.6+/-0.10mm		
Customer P/N:					Measure from	SM-SM		
Layer No.	sig/pln	Copper thk. before process (oz)	Construction		Finished thikness (um)	Finished thikness (mil)	Tolerance	Dk (1GHz)
S/M								
1	Top	1			25.40	1.00	+/-10	3.5
0					30.48	1.20	+/-10	
1	2	Sig/Gnd	1	PP 1080X1(RC65%)	69.00	2.72	+/-10	4
2					30.48	1.20	+/-10	
3	3	Gnd/Pow	H	PP 1080X1(RC65%)	69.00	2.72	+/-10	4
4				Core	15.24	0.60	+/-10	
5	4	Sig	H		115.00	4.53	+/-10	4.2
6				PP 1080X1(RC65%)	15.24	0.60	+/-10	
7	5	Gnd/Pow	H		69.00	2.72	+/-10	4
8				Core	15.24	0.60	+/-10	
9	6	Gnd/Pow	H		698.50	27.50	+/-10	4.2
0				PP 1080X1(RC65%)	15.24	0.60	+/-10	
1	7	Gnd/Pow	H		69.00	2.72	+/-10	4
2				Core	15.24	0.60	+/-10	
3	8	Sig	H		115.00	4.53	+/-10	4.2
4				PP 1080X1(RC65%)	15.24	0.60	+/-10	
5	9	Gnd	1		69.00	2.72	+/-10	4
6				PP 1080X1(RC65%)	30.48	1.20	+/-10	
7	10	Bottom	1		69.00	2.72	+/-10	4
8	S/M				30.48	1.20	+/-10	
9					25.40	1.00	+/-10	3.5
					总计：	1606.65	63.25	

Figure 3-1 10-Layer 1-Stage HDI PCB Design

Characteristic Impedance								
Impedance control layer	Impedance reference plane		Impedance Value (OHM)		Impedance value control range	Original Impedance		Adjusted Impedance
			Original resistance	Adjusted resistance		mil	mil	
	TOP	BOT				Line width	Line width	
L2	L1	L3	40	40	+/-5ohm	3.50		3.20
L4	L3	L5	40	40	+/-5ohm	3.28		4.00
L8	L7	L9	40	40	+/-5ohm	4.30		4.00
L1		L2	50	50	+/-5ohm	4.00		4.30
L1		L3	50	50	+/-5ohm	20.00		12.00
L4	L3	L5	50	50	+/-5ohm	4.00		2.50
L8	L7	L9	50	50	+/-5ohm	4.00		2.50
L10	L9		50	50	+/-5ohm	4.00		4.30

Differential Impedance								
Impedance control layer	Impedance reference plane		Impedance Value (OHM)		Impedance value control range	Original Impedance		Adjusted Impedance
			Original resistance	Adjusted resistance		mil	mil	
	TOP	BOT				Line width / spacing	Line width / spacing	
L1		L2	100	100	+/-10ohm	3.40 / 4.60		3.30 / 4.70
L4	L3	L5	100	100	+/-10ohm	2.55 / 5.45		2.50 / 5.50
L8	L7	L9	100	100	+/-10ohm	2.70 / 5.30		2.50 / 5.50
L10	L9		100	100	+/-10ohm	3.40 / 4.60		3.30 / 4.70
L1		L2	90	90	+/-10ohm	4.00 / 4.00		4.00 / 4.00
L4	L3	L5	90	90	+/-10ohm	3.15 / 4.85		2.80 / 5.00
L8	L7	L9	90	90	+/-10ohm	3.30 / 4.70		2.80 / 5.00
L10	L9		90	90	+/-10ohm	4.00 / 4.00		4.00 / 4.00
L1		L2	85	85	+/-10ohm	5.00 / 4.00		4.60 / 4.40
L10	L9		85	85	+/-10ohm	5.00 / 4.00		4.60 / 4.40
L2	L1	L3	80	80	+/-10ohm	3.65 / 5.70		3.00 / 6.35
L8	L7	L9	80	80	+/-10ohm	3.80 / 4.00		3.00 / 4.40

Figure 3-2 10-Layer 1-Stage HDI PCB Impedance Line Reference Value

3.1.2 10-Layer 2-Stage HDI PCB Design

In the 10-layer 2-stage PCB design, the reference layer of the top-level signal L1 is L2, and the reference layer of the bottom-level signal L10 is L9. It is recommended to stack as TOP-Gnd-Signal-Gnd-Power-Signal/Pow -Gnd-Signal-Gnd-Bottom, of which 1oZ is recommended for L1, L2, L3, L8, L9 and L10, and HoZ for other inner layers. The following figure shows the reference stack and characteristic impedance line width of 1.6mm board thickness.

Customer Name:			Total Thickness:		1.6+-0.10mm			
Customer P/N:			Measure from		SM~SM			
Layer No.	sig/pln	Copper thk. before process (oz)	Construction		Finished thickness (um)	Finished thickness (mil)	Tolerance	Dk (1GHz)
S/M					25.40	1.00	+/-10	3.5
1	Top	1	PP 1080X1(RC65%)		30.48	1.20	+/-10	
2	Gnd	1	PP 1080X1(RC70%)		66.00	2.60	+/-10	4
3	Sig	1	PP 1080X1(RC70%)		30.48	1.20	+/-10	4
4	Gnd	H	PP 1080X1(RC70%)		82.00	3.23	+/-10	4
5	Pow	H	Core		15.24	0.60	+/-10	
6	Pow/Sig	H	PP 1080X1(RC70%)		400.00	15.75	+/-10	4.2
7	Grd	H	Core		15.24	0.60	+/-10	
8	Sig	1	PP 1080X1(RC70%)		82.00	3.23	+/-10	4
9	Gnd	1	PP 1080X1(RC70%)		30.48	1.20	+/-10	
10	Bottom	1	PP 1080X1(RC65%)		66.00	2.60	+/-10	4
S/M					30.48	1.20	+/-10	3.5
					25.40	1.00	+/-10	3.5
					总计 : 1636.63		64.43	

Figure 3-3 10-Layer 2-Stage HDI PCB Design

Characteristic Impedance								
Impedance control layer	Impedance reference plane		Impedance Value (OHM)		Impedance value control range	Original Impedance		Adjusted Impedance
			Original resistance	Adjusted resistance		mil	mil	
	TOP	BOT				Line width	Line width	
L3	L2	L4	45	45	+/-50ohm	3.00		3.10
L8	L7	L9	45	45	+/-50ohm	3.00		3.10
L1		L3	50	50	+/-50ohm	20.00		12.00
L1		L2	50	50	+/-50ohm	4.0/4.7		4.20
L3	L2	L4	50	50	+/-50ohm	2.4/4.0		2.60
L6	L5	L7	50	50	+/-50ohm	3.90		3.90

Differential Impedance								
Impedance control layer	Impedance reference plane		Impedance Value (OHM)		Impedance value control range	Original Impedance		Adjusted Impedance
			Original resistance	Adjusted resistance		mil	mil	
	TOP	BOT				Line width	/ spacing	Line width
L1		L2	85	85	+/-10ohm	4.40	/ 3.00	4.20 / 3.50
L8	L7	L9	85	85	+/-10ohm	3.30	/ 4.70	3.20 / 4.80
L1		L2	90	90	+/-10ohm	4.00	/ 3.60	3.80 / 3.80
L3	L2	L4	90	90	+/-10ohm	2.70	/ 5.50	2.90 / 5.30
L3	L2	L4	90	90	+/-10ohm	2.40	/ 4.40	2.70 / 4.10
L1		L2	100	100	+/-10ohm	3.50	/ 4.50	3.30 / 4.70
L10	L9		100	100	+/-10ohm	3.50	/ 4.50	3.30 / 4.70
L3	L2	L4	100	100	+/-10ohm	2.20	/ 5.80	2.50 / 5.50
L8	L7	L9	100	100	+/-10ohm	2.20	/ 5.80	2.50 / 5.50

Figure 3-4 10-layer 2-Stage HDI PCB Impedance Line Reference Value

3.1.3 8-Layer PTH PCB Design

In the 8-layer PTH PCB design, the reference layer of the top-level signal L1 is L2, and the reference layer of the bottom-level signal L8 is L7. It is recommended to stack as TOP-Gnd-Power-Power/Signal-Gnd-Signal-Gnd-Bottom, and 1oZ is recommended for all.

The following figure shows the reference stack and characteristic impedance line width of 1.6mm board thickness.

8层通孔1.6+/-0.16mm				
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF
L1	Solder Mask	1.10		
	1/3oz+plating	1.20		
	Prepreg(1080RC65%)	3.15	4.40	0.019
L2	copper	1.20		
L3	Core	5.60	4.2	0.015
	copper	1.20		
	Prepreg (1080+2116)	7.00	4.40	0.019
L4	copper	1.20		
L5	Core	21.60	4.2	0.015
	copper	1.20		
	Prepreg (1080+2116)	7.00	4.40	0.019
L6	copper	1.20		
L7	Core	5.60	4.2	0.015
	copper	1.20		
	Prepreg(1080RC65%)	3.15	4.40	0.019
L8	1/3oz+plating	1.20		
	Solder Mask	1.10		
		64.90		

Figure 3-5 8-Layer PTH PCB Design

Impedance	43 ohm	50 ohm	85 ohm	90 ohm	95 ohm	100 ohm
Reference Layer	Design W(mil)	Design W(mil)				
L1->L2	6.5	4.8	4.4->3.6	4->4	3.6->4.4	3.3->4.7
L3->L2/L4	6.5	4.6	3.9->4.1	3.5->4.5	3.1->4.9	3->5.8
L6->L5/L7	6.5	4.6	3.9->4.1	3.5->4.5	3.1->4.9	3->5.8
L8->L7	6.5	4.8	4.4->3.6	4->4	3.6->4.4	3.3->4.7

Figure 3-6 8-Layer PTH PCB Impedance Line Reference Value

The figure below shows the reference stack and the characteristic impedance line width of the 1.0mm plate thickness:

8层通孔1.0+/-0.1mm				
Layer	Mother Board	Typical layer thickness (mil)	Dielectric Constant	DF
	Solder Mask	1.10		
L1	1/3oz+plating	1.20		
	Prepreg (106)	2.10	4.00	0.019
L2	copper	1.20		
	Core	5.00	4.2	0.015
L3	copper	1.20		
	Prepreg (2116)	3.50	4.00	0.019
L4	copper	1.20		
	Core	8.00	4.2	0.015
L5	copper	1.20		
	Prepreg (2116)	3.50	4.00	0.019
L6	copper	1.20		
	Core	5.00	4.2	0.015
L7	copper	1.20		
	Prepreg (106)	2.10	4.00	0.019
L8	1/3oz+plating	1.20		
	Solder Mask	1.10		
		41.00		
		1.04		

Figure 3-7 8-Layer PTH Board Stackup

Impedance	40 ohm	50 ohm	80 ohm	85 ohm	90 ohm	100 ohm
Reference Layer	Design W(mil)					
L1->L2	5	3.4	4->4	3.7->4.3	3.3->4.7	3->8
L1->L3		13				
L4->L3/L5	5.5	3.8	4.1->3.9	3.7->4.3	3.4->4.6	3.2->7.8
L6->L5/L7	5	3	3.9->4.1	3.5->4.5	3.2->4.8	3->10
L8->L7	5	3.4	4->4	3.7->4.3	3.3->4.7	3->8

Figure 3-8 8-Layer PTH Board Impedance Line Reference Value

3.1.4 RK3588 Fan-Out Design

- Ball fan-out design of the outer two circles

For the outermost balls, you can go out from the TOP layer with a line width of 4mil; the signal of the second circle goes out from the middle of the two balls with a line width of 4mil. It is recommended to set a grid and go out from the middle of the two balls.

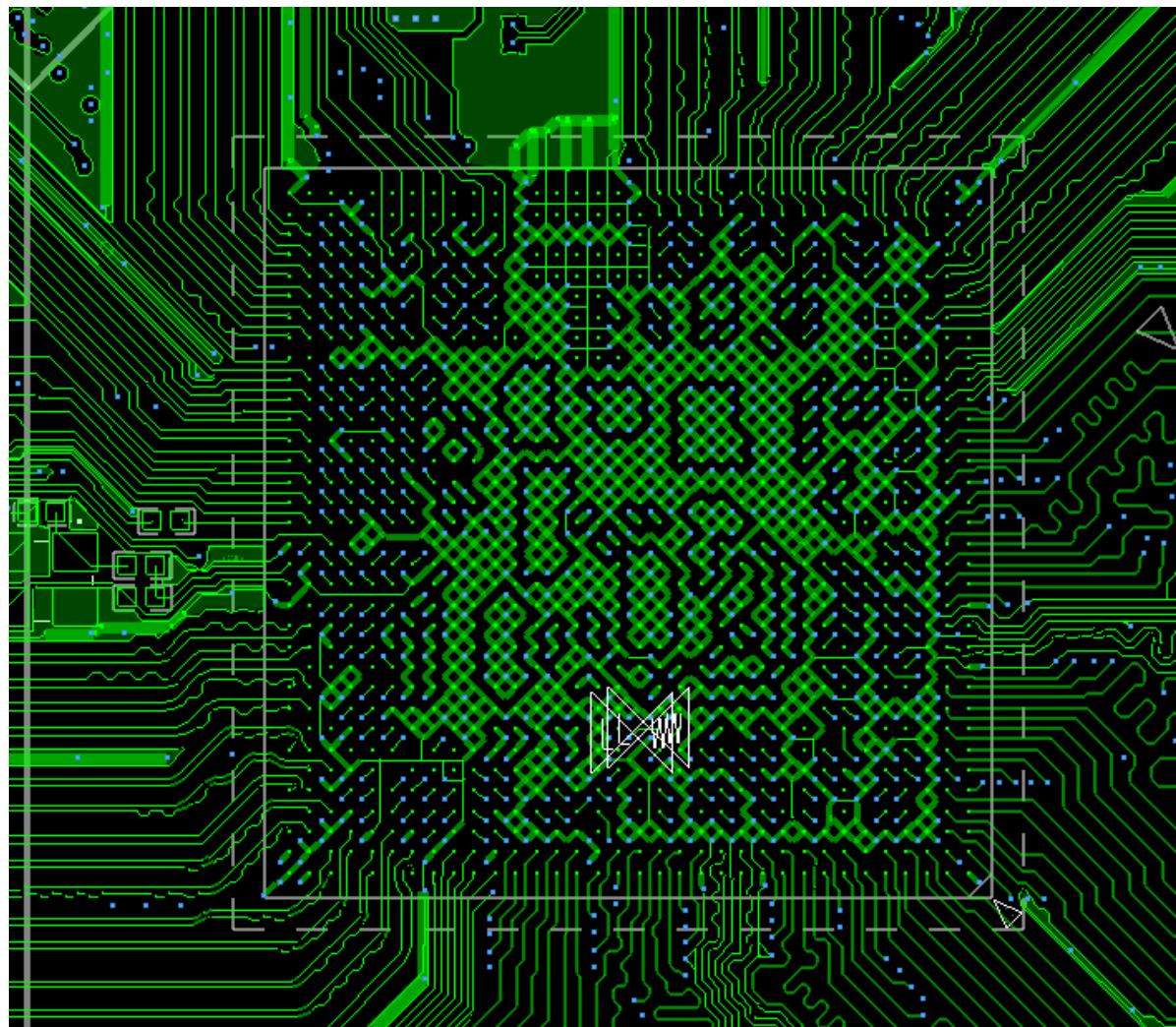


Figure 3-9 RK3588 Fan-Out Diagram 1

- Ball fan-out design in inner circles

If the signals of the first and second circles are useful, then starts from the third circle, it needs to change to inner layers. Please make sure to follow the rules of layer changing vias, and it is recommended to place layer changing via at intervals of 2-4 rows, and leave an empty row not placing layer changing vias to keep as large a channel as possible for the ground layer and the power layer.

The ground layer copper covering situation shown in the figure below, there are multiple channels connected with the outside ground, which is good for SI/PI and heat dissipation

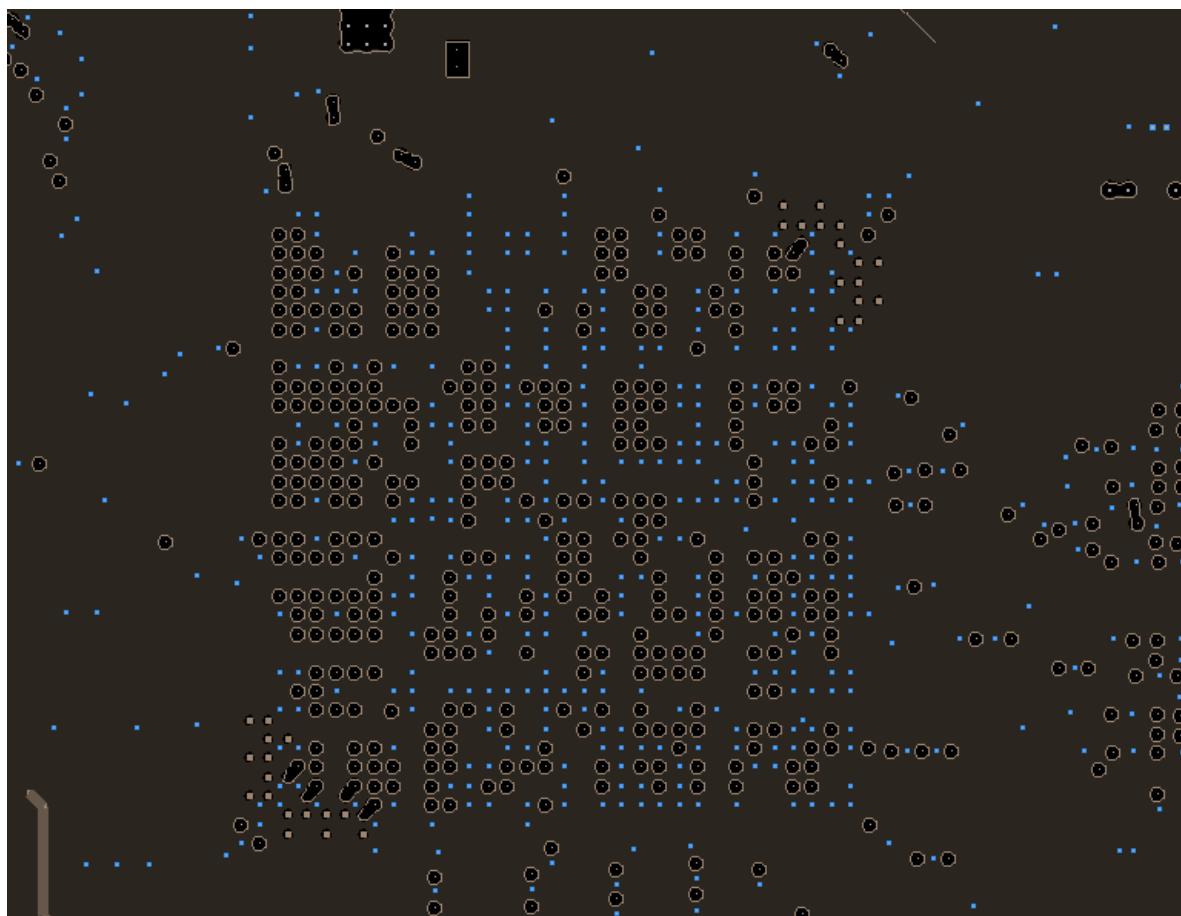


Figure 3-10 RK3588 Fan-Out Diagram 2

As shown in the figure below, the power layer plane copper pour situation, the regular placement of vias can make various power sources have as much copper pour channels as possible, and effectively improve the quality of power supply.

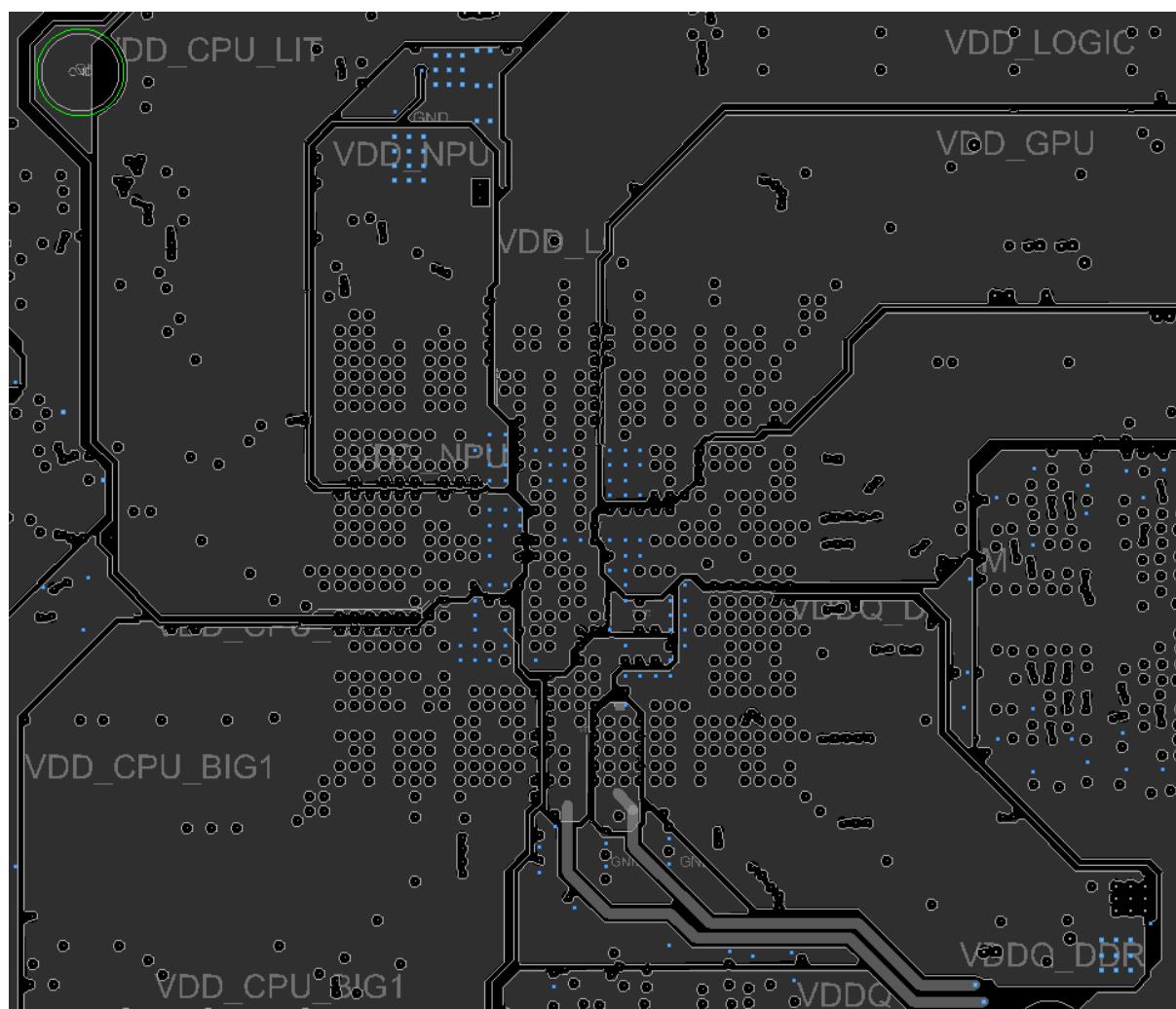


Figure 3-11 RK3588 Fan-Out Diagram 3

The trace of bottom layer (the trace of inner layer is similar) is shown in the figure below, the layer-changing vias are set according to the grid and placed in the middle of balls, and 3.5mil line width fanned out between two vias.

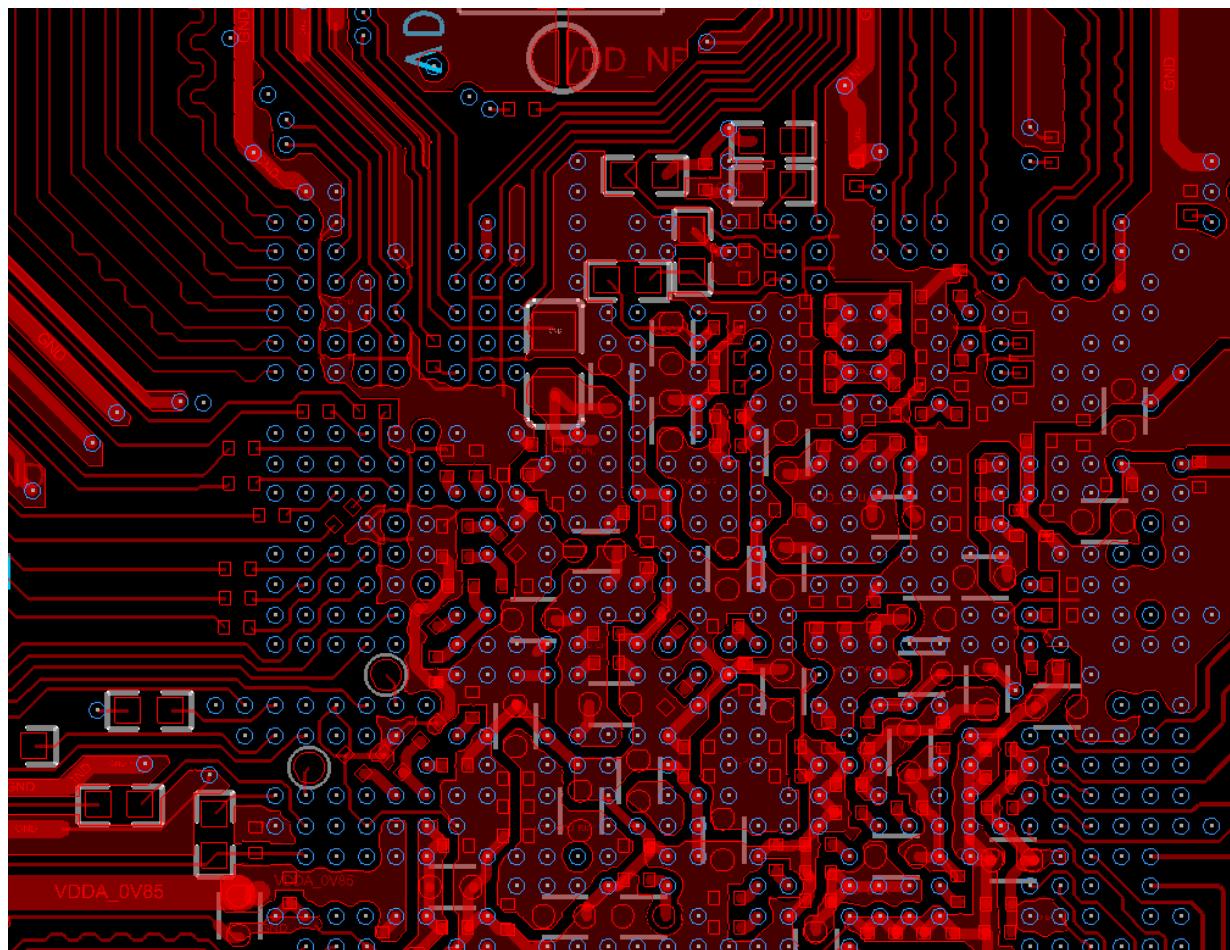


Figure 3-12 RK3588 Fan-Out Diagram 4

3.2 General Design Recommendation

- (1) Trace length should include package and via.
- (2) Intra-pair skew is the term used to define the difference length between + and - in a differential pair. Inter-pair skew is used to define the difference length between a differential pair and another differential pair. The space between signals is defined as air-gap distance.

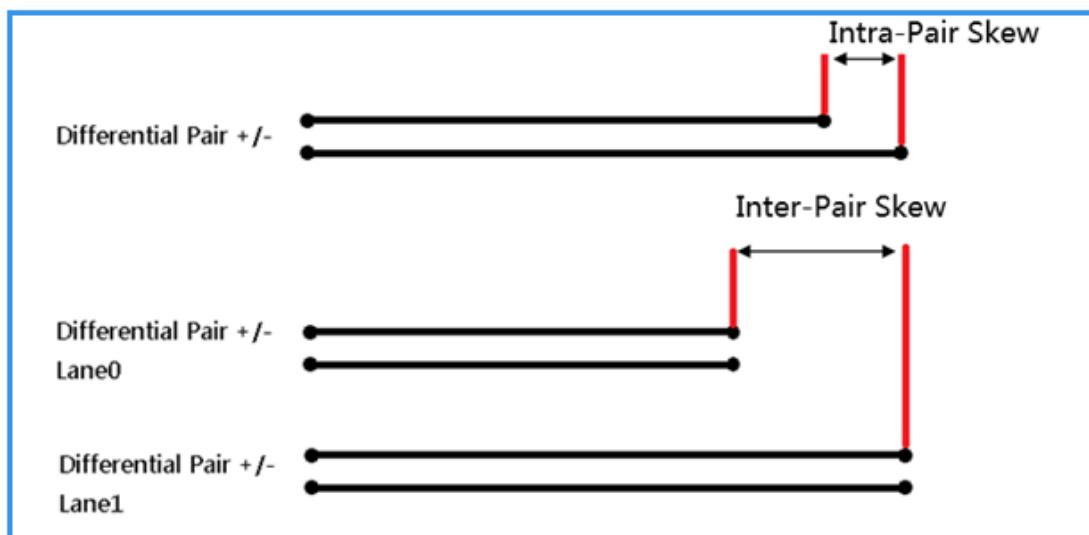


Figure 3-13 Differential Pair Skew

- (3) Route trace over continuous GND plane without interruption. Any discontinuity or split on the reference plane will degrade signal integrity significantly.

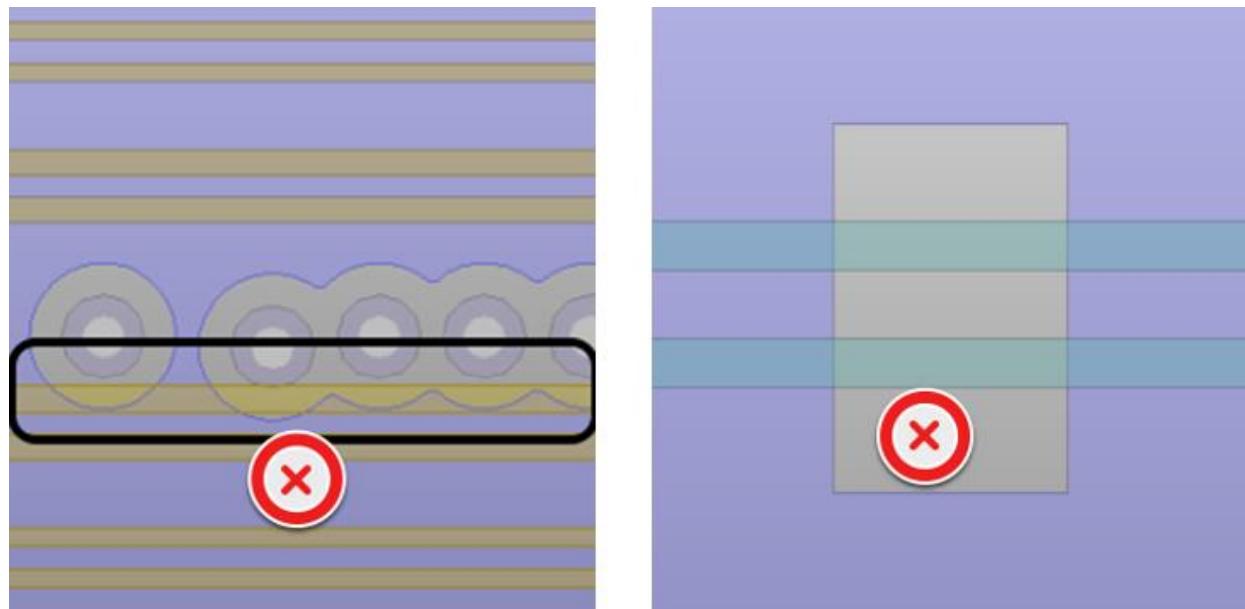


Figure 3-14 Discontinuous Reference Plane

(4) Voiding the ground plane underneath the SMT signal pad is necessary to minimize the impedance mismatch. SMT component include AC capacitor, ESD, CMC(common mode choke), connector, etc. If no specific requirement provided, keep the voiding size as same as the pad or slightly bigger.

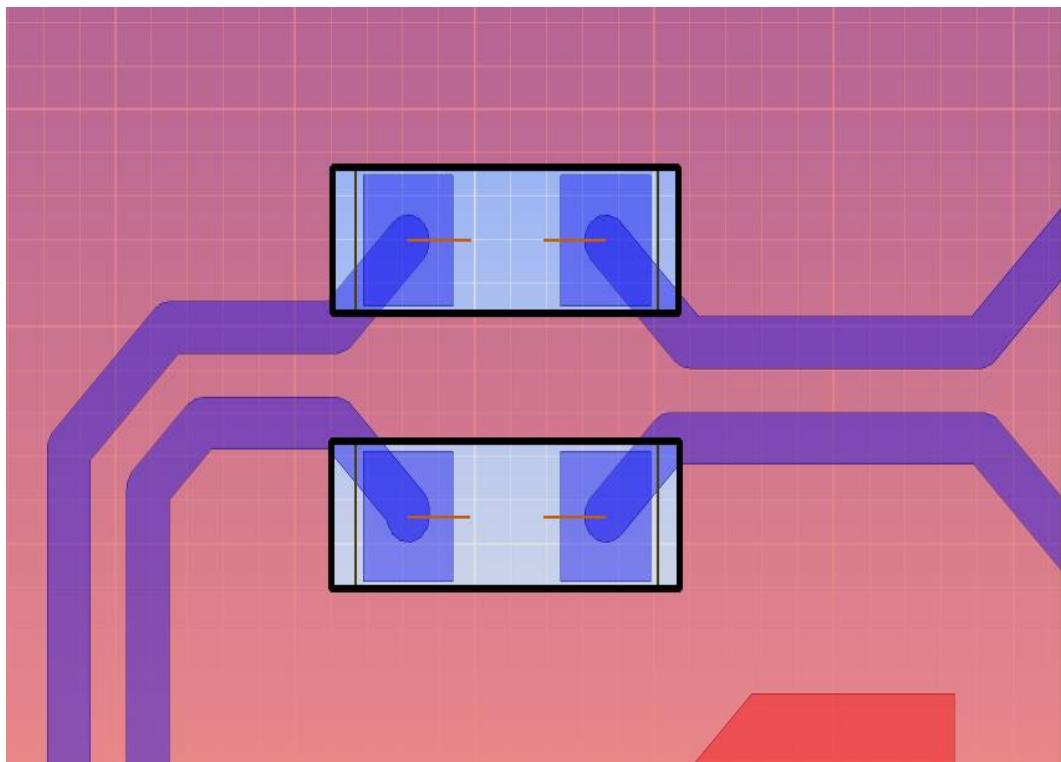


Figure 3-15 Reference Plane Voiding

(5) Recommend keeping traces ≥ 4 times the width of trace from GND plane on same layer.

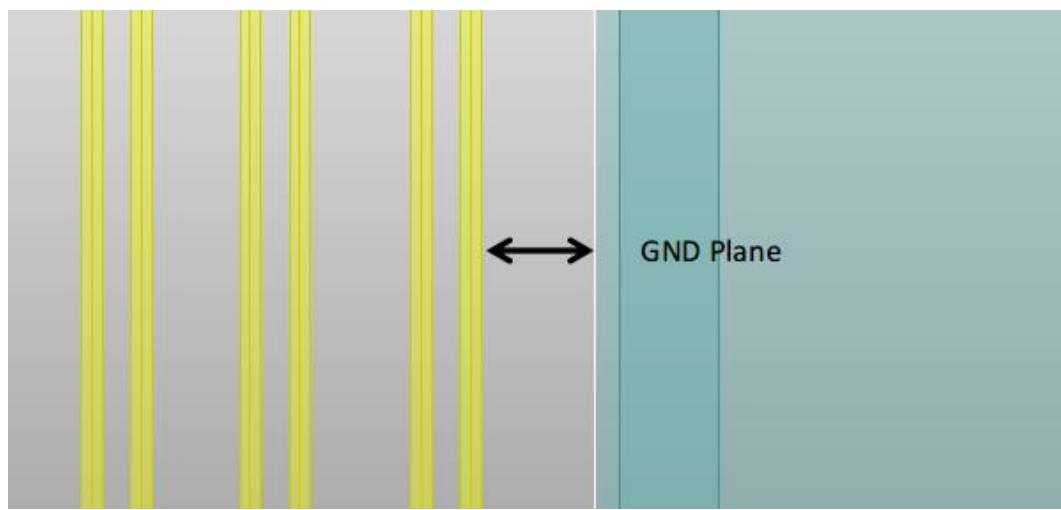


Figure 3-16 Airgap Between Trace and Plane

(6) Avoid via stub. If the length of the via stub is more than 12mil, we recommend to simulate the impact of via stub.

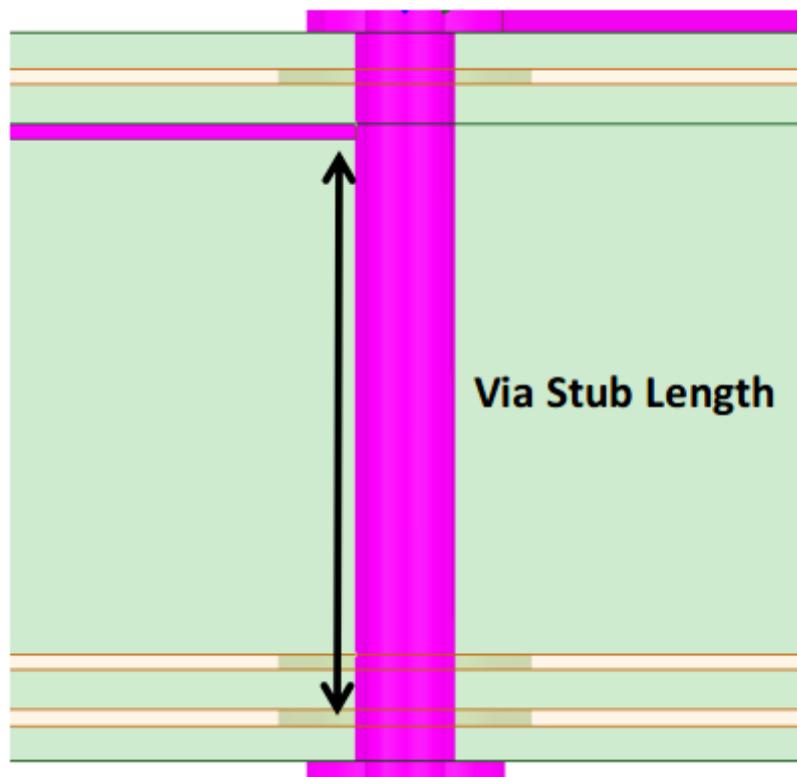


Figure 3-17 Via Stub

(7) Avoid routing across different reference planes. Recommend that high-speed differential signals are routed ≥ 40 mils from the edge on the reference plane.

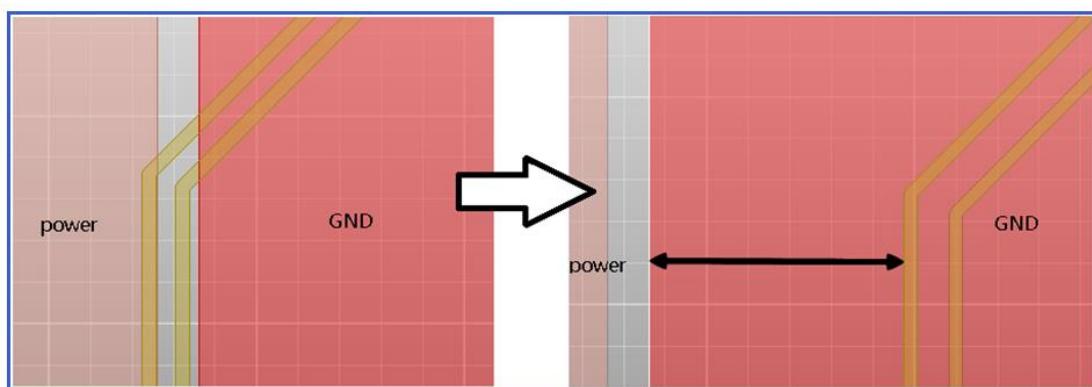


Figure 3-18 Reference Plane Edge

(8) It's not recommend to place test point on any high-speed signals.

(9) Bend should be minimized. If bends are needed, use 135 °bends instead of 90 °.

(10) AC coupling capacitor is recommended to be placed near connector.

(11) Serial resistor recommend to be placed near transmitter. For example, EMMC_CLK serial resistor placed near RK3588 within 400mil.

(12) Each GND PAD at IC(such as emmc device、 flash) recommend place a GND PTH Via.

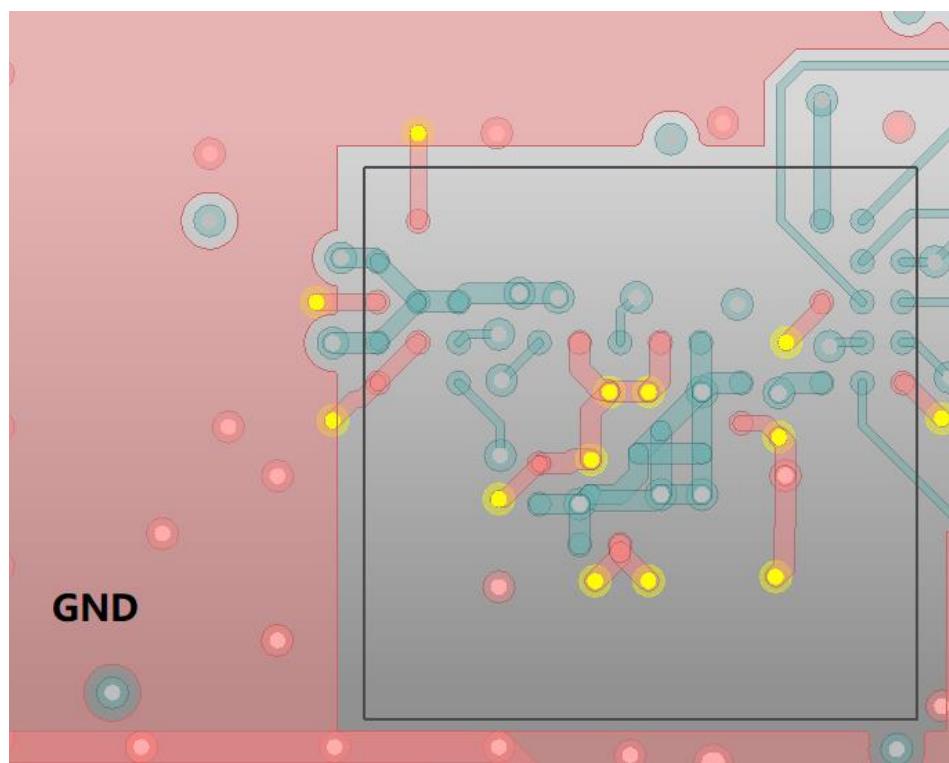


Figure 3-19 GND Via Placement

(13) Avoid routing under or near crystals, oscillators, clock signal generators, switching regulators,mounting holes, magnetic devices or IC's that used for duplicate clock signals.

(14) Remove all non-functional via pads.

(15) Recommend each ESD GND pad has a GND PTH via,and keep the length from pad to via as short as possible.

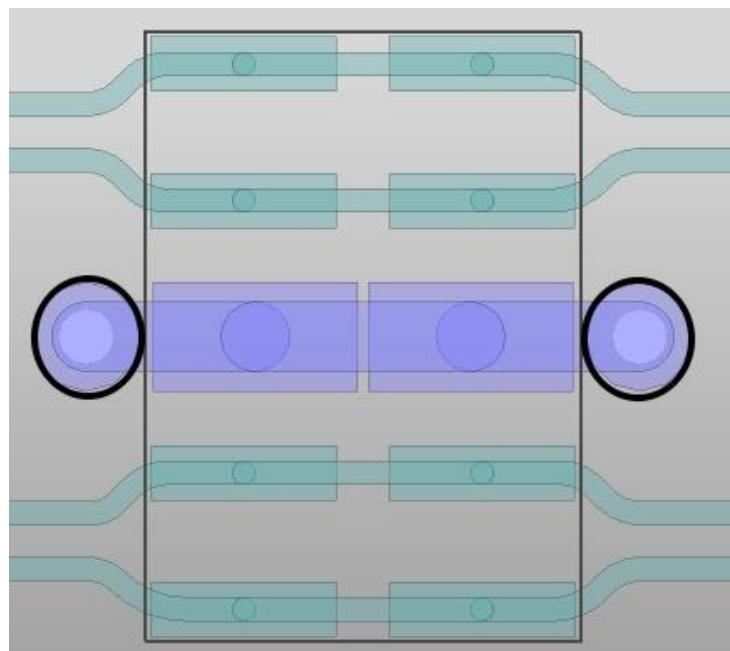


Figure 3-20 GND Via Placement for ESD Component

(16) Differential signals require equal lengths within pairs, that is, the time delay difference between P and N should be as small as possible. Therefore, when the time delay difference occurs between the differential lines P and N, the nearby winding is compensated. Special attention should be paid to the size of the winding, which should meet the requirements shown in the figure below to reduce the impact of sudden changes in impedance.

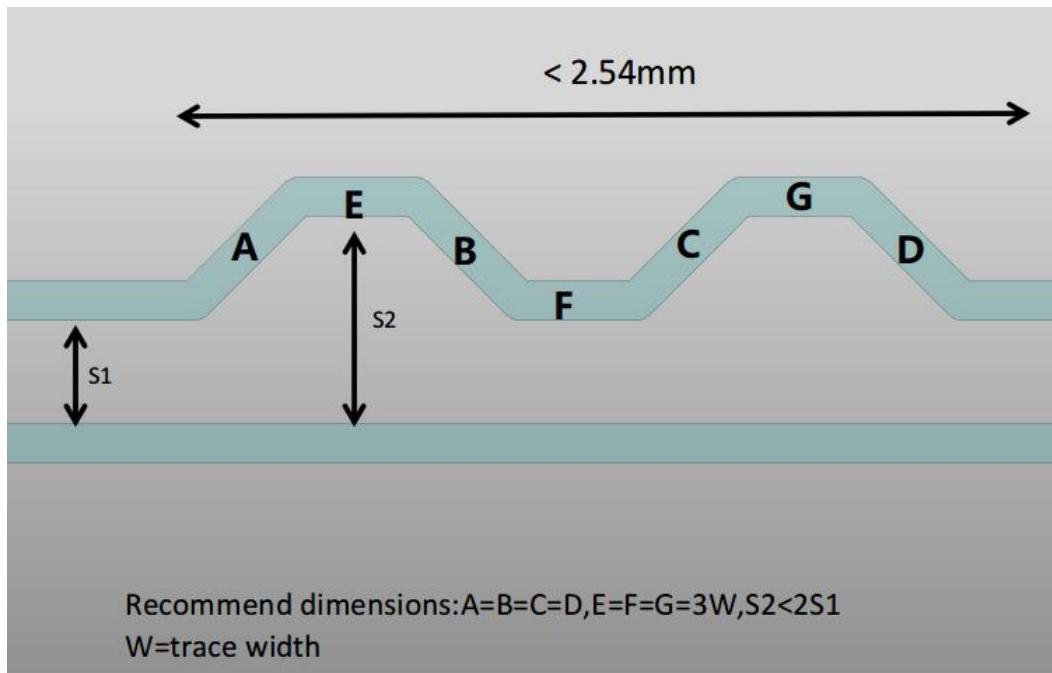


Figure 3-21 Winding Dimension

(17) If there is an unequal length (within 300mil) in the differential pair, make the compensation as soon as possible.

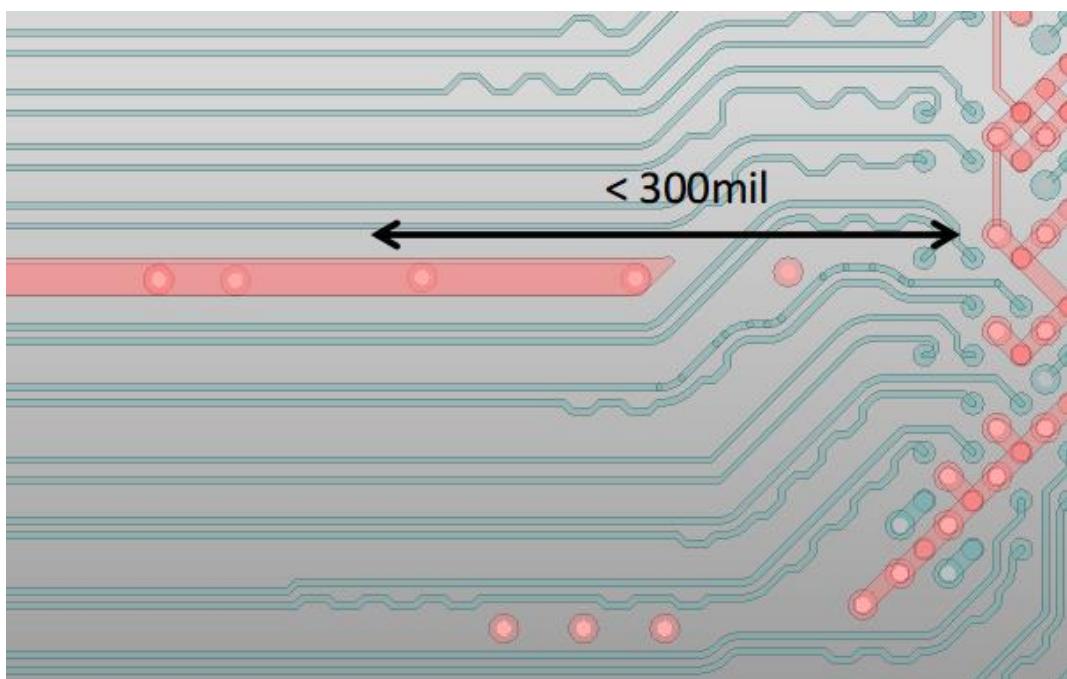


Figure 3-22 Skew Compensation

(18) Place ground stitching vias near the signal transition vias. For differential signals, both signal vias and stitching vias should be placed symmetrically.

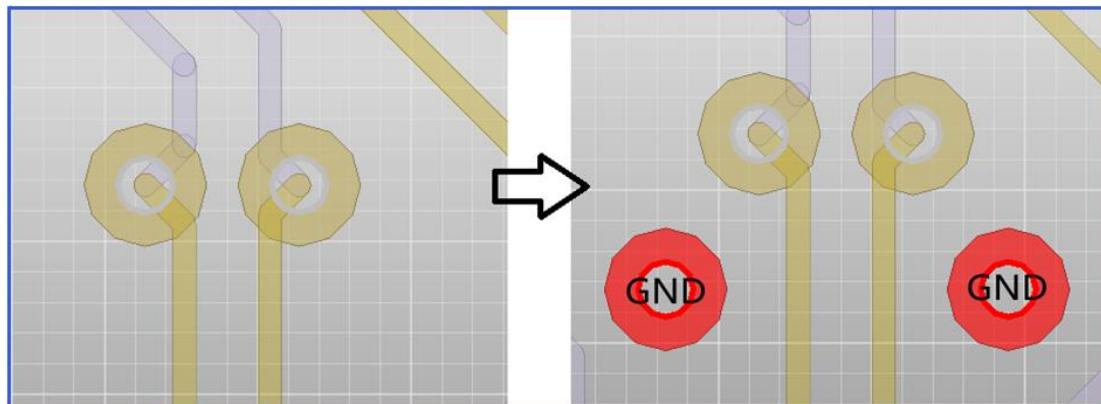


Figure 3-23 Gnd Via for Differential Via

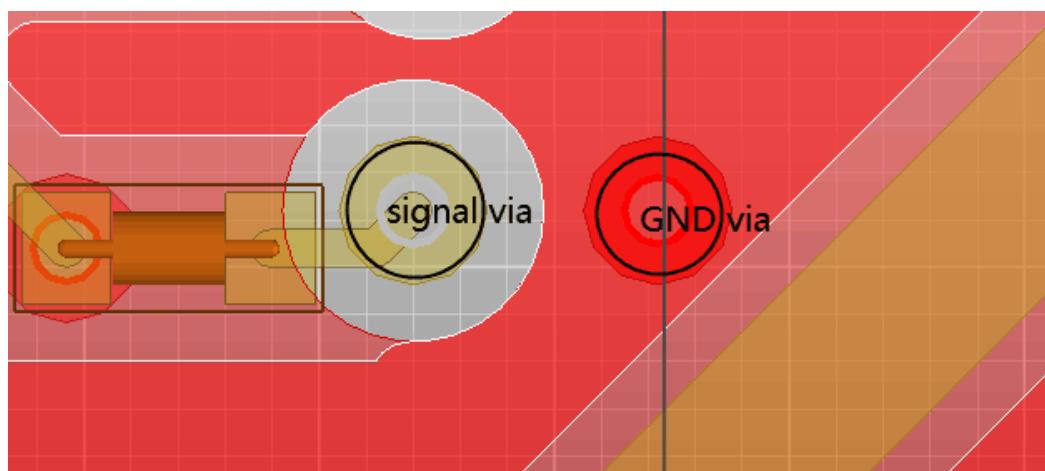


Figure 3-24 Gnd Via for Single-ended Via

(19) Route differential pairs on symmetry.

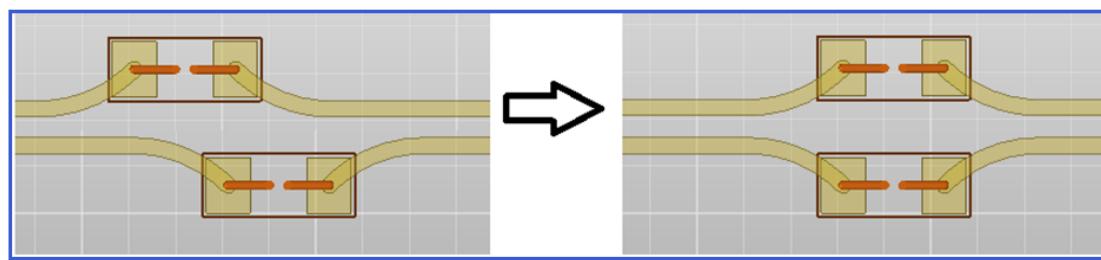


Figure 3-25 symmetry layout

(20) It is recommended to place at least one ground through via in each ground pad of the high-speed connector, and the through via should be as close as possible to the pad.

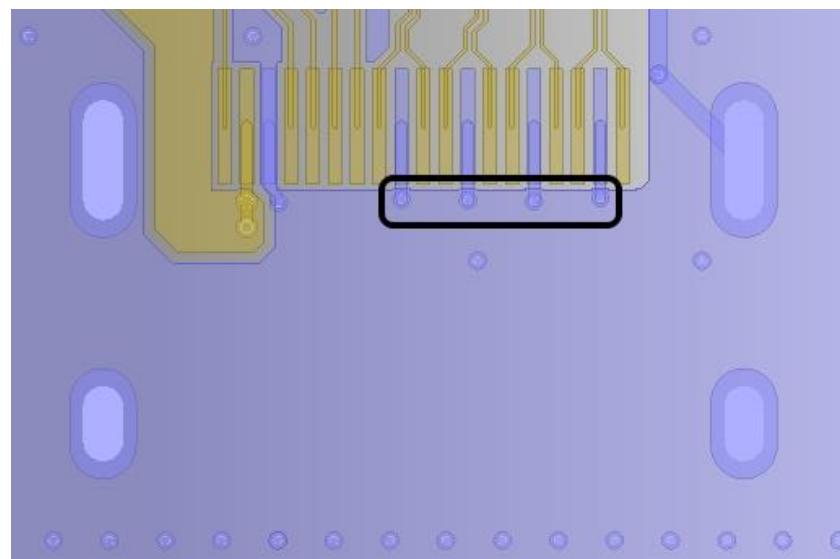


Figure 3-26 Gnd Via Placement

(21) Ground shape at connector near GND PAD recommend \leq PAD size.

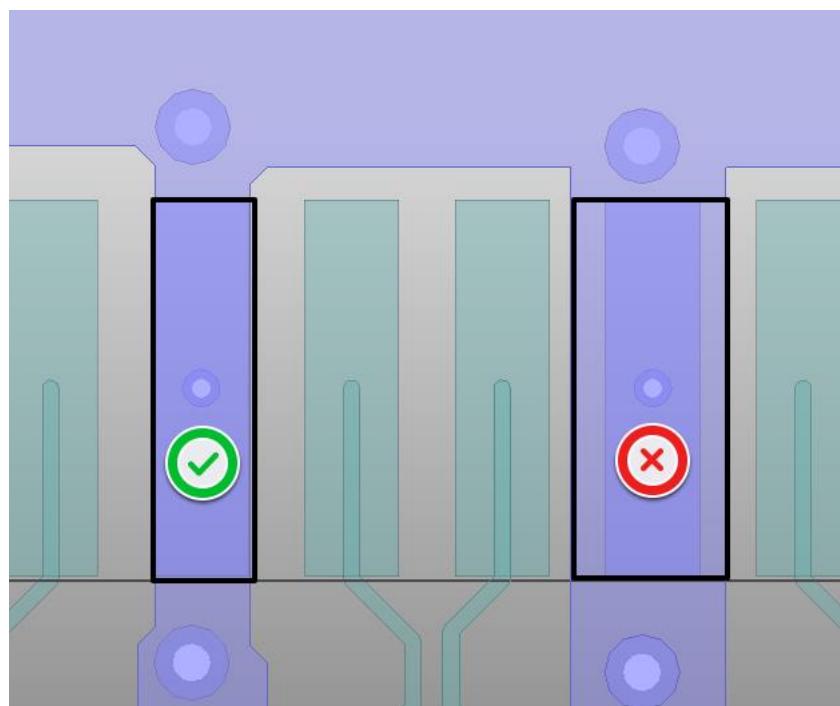


Figure 3-27 Ground Shape Near Connector Pad

(22) Recommend distance between ground plane and pad ≥ 3 times the width of trace at connector.

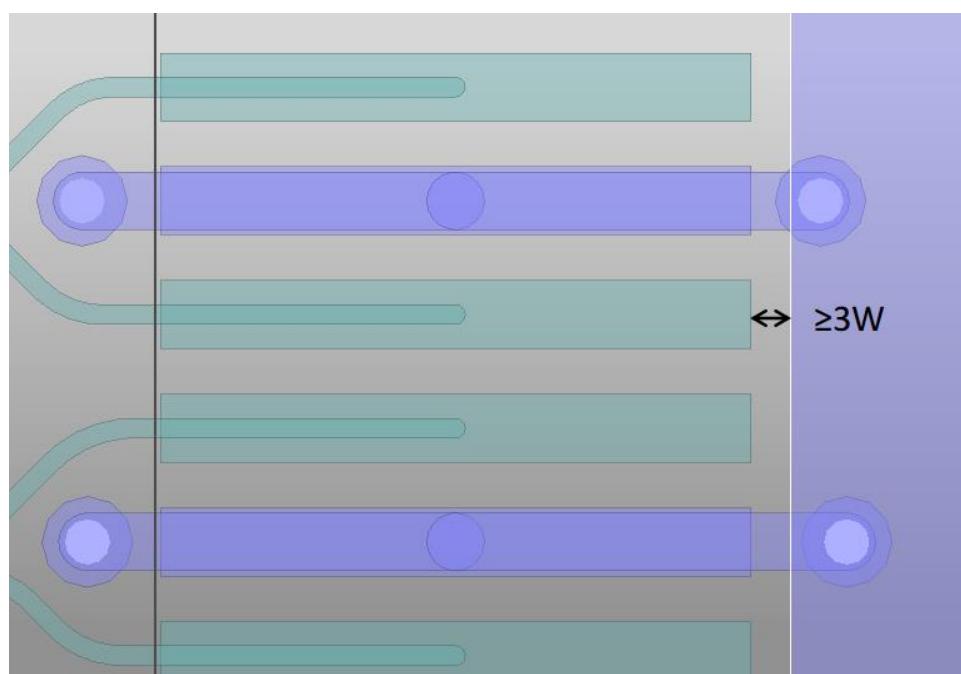


Figure 3-28 Airgap Between Pad to Plane

(23) Connect the fragmentary ground plane by wire in BGA zone.

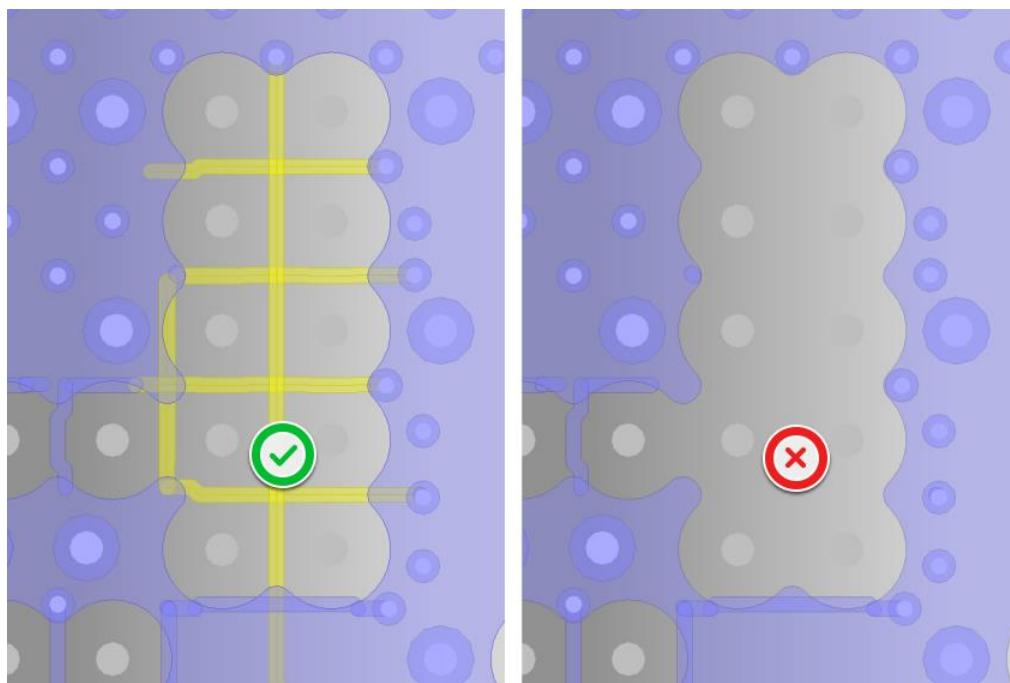


Figure 3-29 Ground Plane in BGA Zone

(24) Proposed ground shielding.

L: GND via interval length.

D: Distance from shielding to trace $\geq 4*W$.

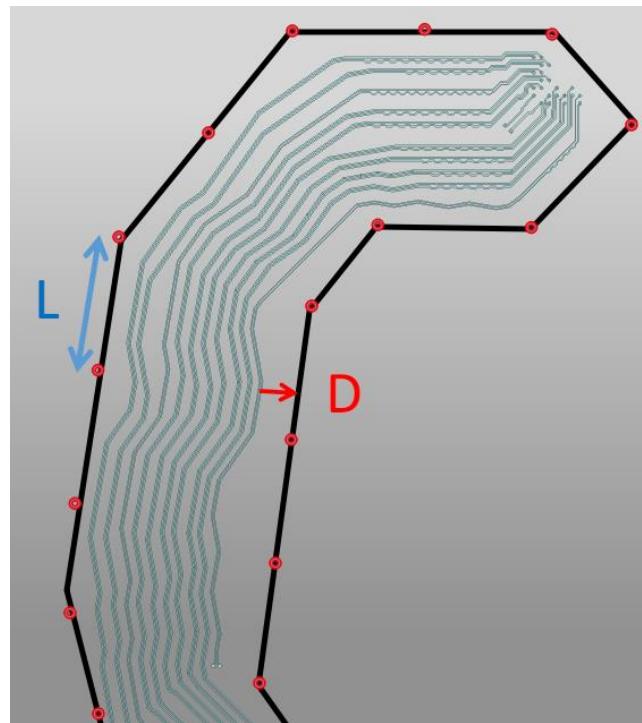


Figure 3-30 Ground Shielding

(25) Route important single-ended trace(such as emmc_clk、emmc_datastrobe、RGMII_CLK, etc) with ground shielding. Add a GND via on shielding trace every 500mil.

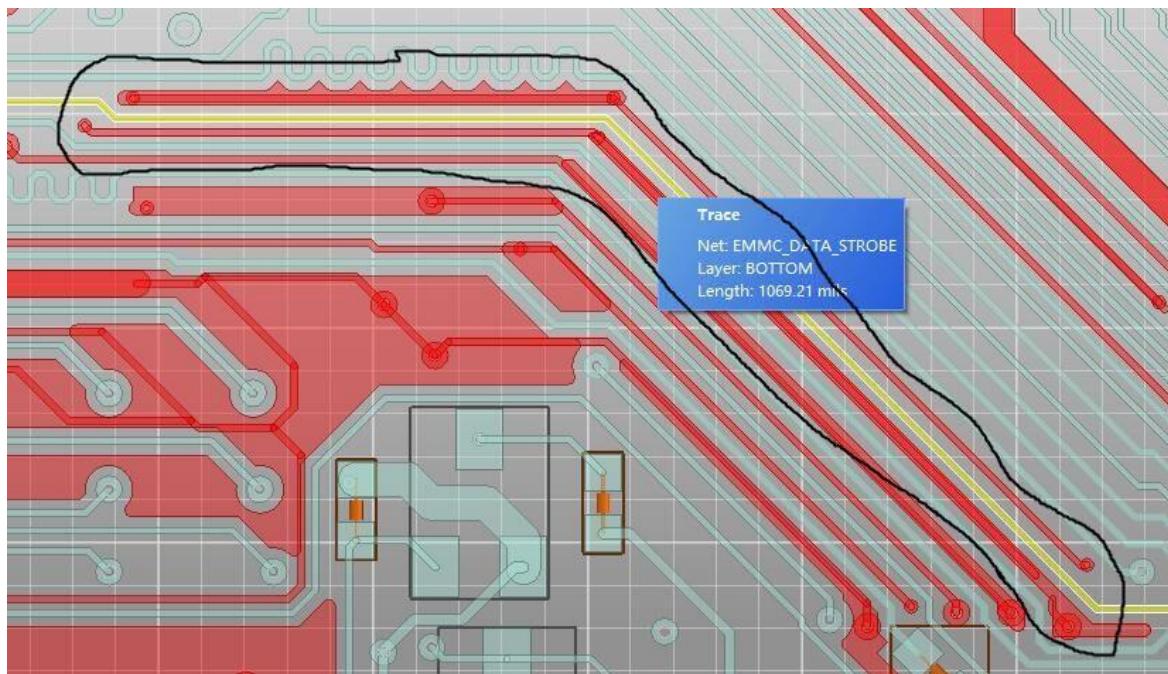


Figure 3-31 Ground Shielding for Single-End Signals

(26) Serpentine traces (also called meander) are often needed when a certain trace length needs to be achieved. Keep a minimum distance of four times the trace width between adjacent copper in a single trace.

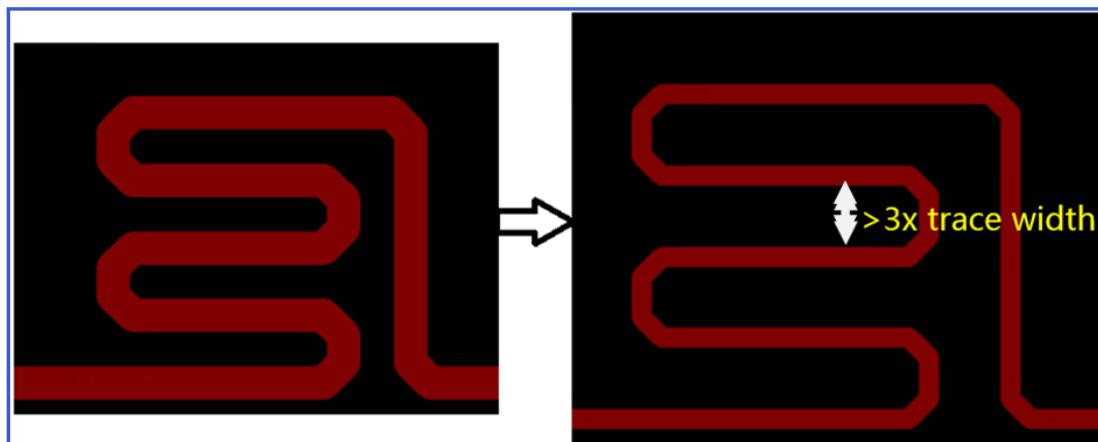


Figure 3-32 Serpentine Trace Recommendation

(27) Minimize the stub length as much as possible, it is recommended to keep the stub length as zero.

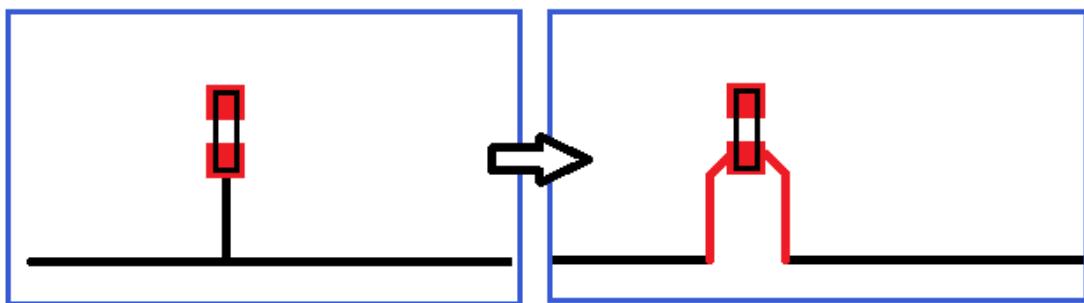


Figure 3-33 Trace Stub

(28) If a signal needs to be routed over two different reference planes, each reference plane should place a capacitor to ground to provide continuous return path.

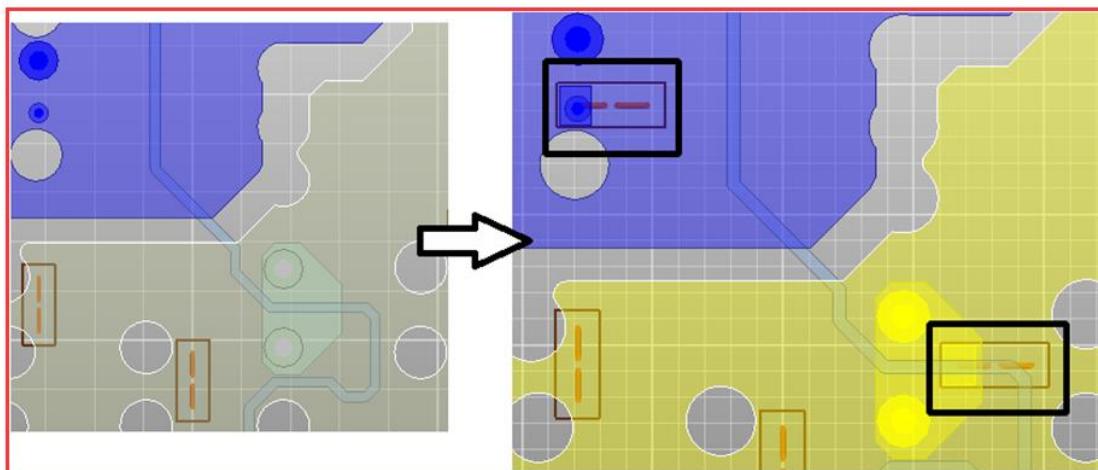


Figure 3-34 Route Across Different Reference Plane

(29) It is recommended that in the RK3588 BGA area, there should be one ground via for every 1.3 ground pads, and the ground via should connect the ground pad to all ground planes.

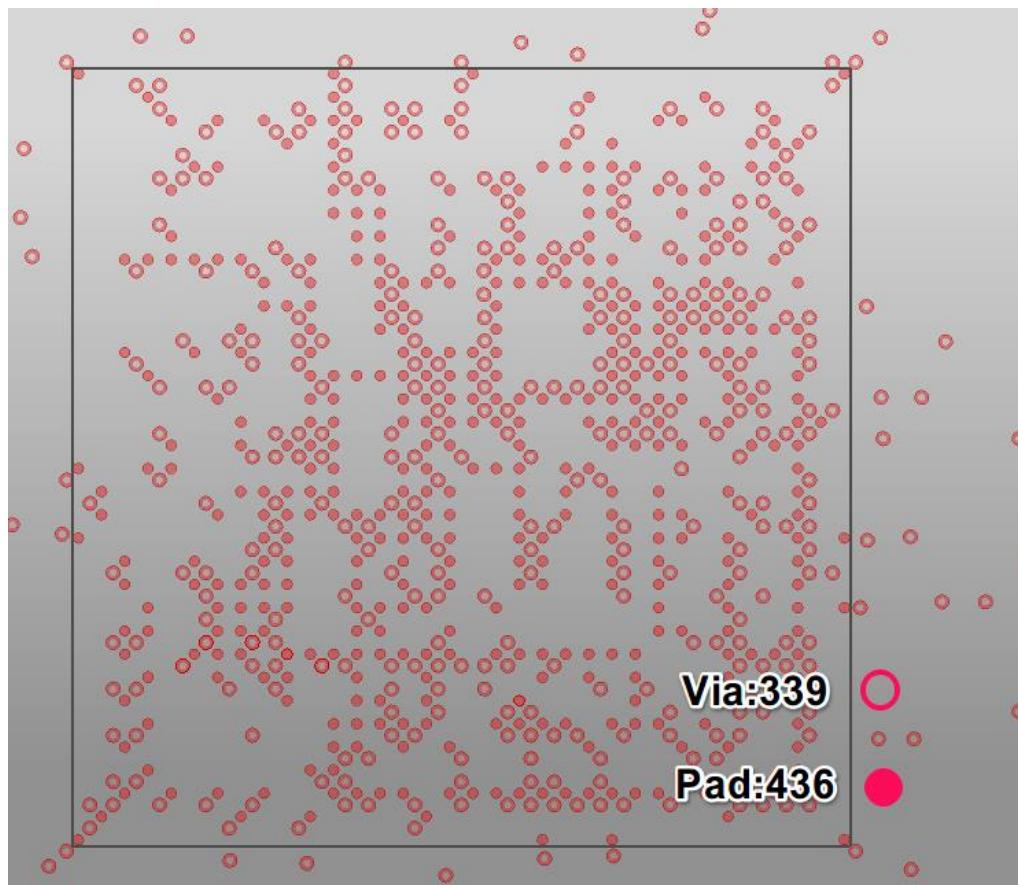


Figure 3-35 Ground Via and Pad Distribution

3.3 Routing Requirements for Signal Running \geq 8GT/s

The signals of the interfaces below can work up to 8GT/s. Due to the high rate, the PCB design requirements will be more strict. In addition to the chapter "3.2 General Design Recommendations", there are some requirements for these signals in this chapter.

Table 3-1 RK3588 Differential Signal \geq 8GT/s

Interface	Signal
DP1.4@8.1Gbps	TYPEC0_SSRX1P/DP0_TX0P; TYPEC0_SSRX1N/DP0_TX0N TYPEC0_SSTX1P/DP0_TX1P; TYPEC0_SSTX1N/DP0_TX1N TYPEC0_SSRX2P/DP0_TX2P; TYPEC0_SSRX2N/DP0_TX2N TYPEC0_SSTX2P/DP0_TX3P; TYPEC0_SSTX2N/DP0_TX3N TYPEC1_SSRX1P/DP1_TX0P; TYPEC1_SSRX1N/DP1_TX0N TYPEC1_SSTX1P/DP1_TX1P; TYPEC1_SSTX1N/DP1_TX1N TYPEC1_SSRX2P/DP1_TX2P; TYPEC1_SSRX2N/DP1_TX2N TYPEC1_SSTX2P/DP1_TX3P; TYPEC1_SSTX2N/DP1_TX3N
HDMI2.1@12Gbps	HDMI_TX0_D0P/EDP_TX0_D0P; HDMI_TX0_D0N/EDP_TX0_D0N HDMI_TX0_D1P/EDP_TX0_D1P; HDMI_TX0_D1N/EDP_TX0_D1N HDMI_TX0_D2P/EDP_TX0_D2P; HDMI_TX0_D2N/EDP_TX0_D2N HDMI_TX0_D3P/EDP_TX0_D3P; HDMI_TX0_D3N/EDP_TX0_D3N HDMI_TX1_D0P/EDP_TX1_D0P; HDMI_TX1_D0N/EDP_TX1_D0N HDMI_TX1_D1P/EDP_TX1_D1P; HDMI_TX1_D1N/EDP_TX1_D1N HDMI_TX1_D2P/EDP_TX1_D2P; HDMI_TX1_D2N/EDP_TX1_D2N HDMI_TX1_D3P/EDP_TX1_D3P; HDMI_TX1_D3N/EDP_TX1_D3N
PCI-E3.0@8Gbps	PCI-E30_PORT0_RX0P; PCI-E30_PORT0_RX0N PCI-E30_PORT0_RX1P; PCI-E30_PORT0_RX1N PCI-E30_PORT1_RX0P; PCI-E30_PORT1_RX0N PCI-E30_PORT1_RX1P; PCI-E30_PORT1_RX1N

3.3.1 Void the Ground Plane Under the BGA Pads BGA

If these interface operating $\geq 8\text{GT/s}$, we strongly recommend to void the GND reference plane (on Layer 2) under the BGA pad of signal in Table 2-1 to reduce capacitance. The voiding size is 10mil in radius.

If these interface operating below 8GT/s ,for example, DP only running at 5.4GT/s or lower,then there is no need to void.

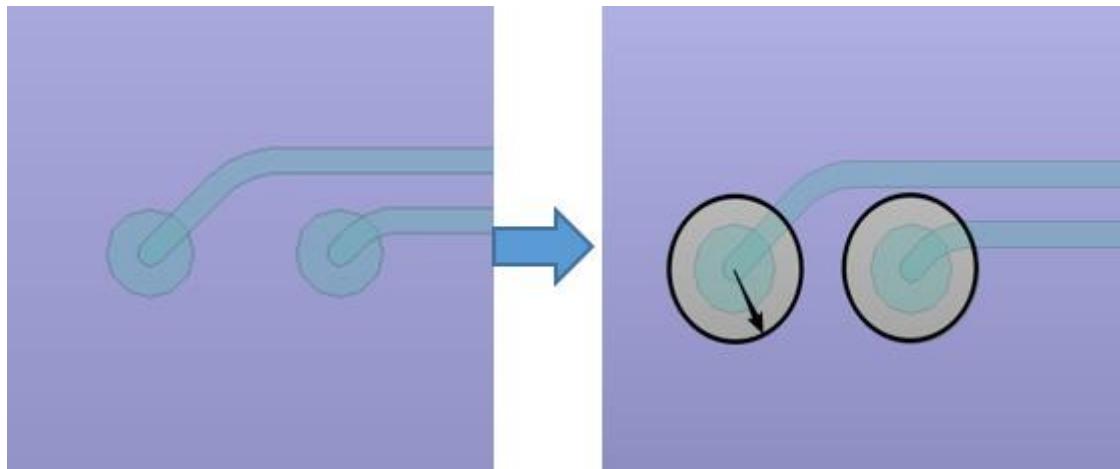


Figure 3-36 Reference Plane Voiding

3.3.2 Fiber Weave Effect Mitigation

Trace of differential pair will experience different dielectric constants of the fiberglass weave and epoxy that comprise a PCB. As signals travel faster when ϵ_r is lower, an intra-pair skew can develop. The skew between the differential signals can significantly degrade the eye diagram.

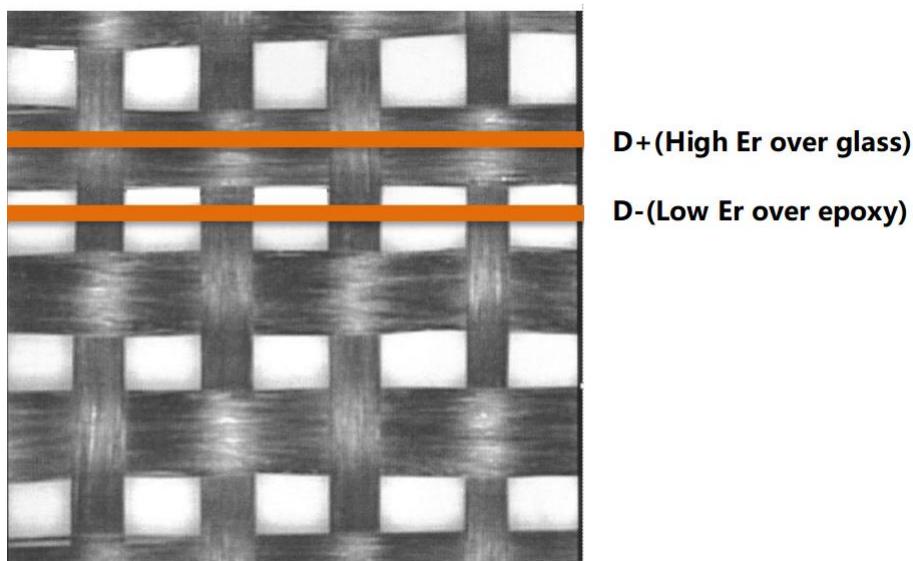


Figure 3-37 Fiber Weave Effect

When high speed interface in Table 3-1 operating $\geq 8\text{GT/s}$ and PCB trace length above 1.5inch, we strongly recommend to adopt at least one method to minimize the impact of PCB fiber weave effect.

Method A:Route at 10 ° to 35 ° or rotate PCB at 10 °

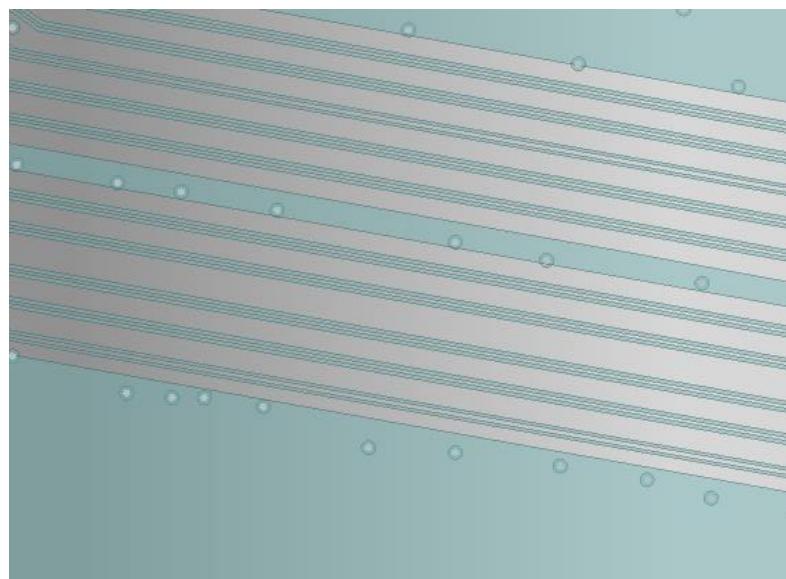


Figure 3-38 Route at 10 °

Method B:Route in zig-zag across PCB and keep $W \geq 3 \times$ glass pitch(eg: W=60mil,θ=10°,L=340mil)

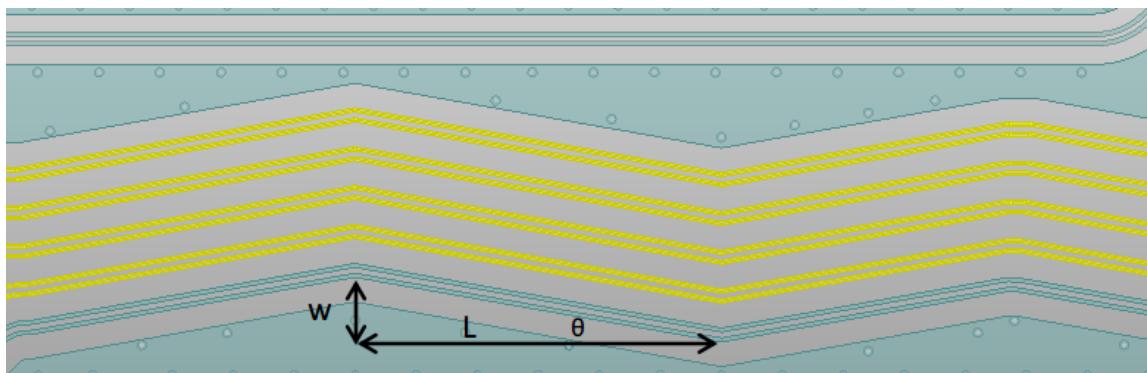


Figure 3-39 Zig-zag Trace

3.3.3 Differential Via Layout Requirement

If these interface in Table 3-1 operating $\geq 8\text{GT/s}$, then differential via's dimension recommend to be optimized by simulation according to customer's PCB layer stack. Also, there are some dimensions for reference according to EVB's HDI PCB(1+N+1) stack.

R_Drill=0.1mm (Via drill hole radius)

R_Pad=0.2mm (Via pad radius).

D1:Differential via-to-via pitch.

D2:anti-pad from top to bottom layer.

D3:Distance between GND return path Via and signal via

Table 3-2 Differential Via Dimension Recommendation

option	D1(mil)	D2(mil)	D3(mil)	Via Zdiff
1	26	18	22~26	100 ohm
2	24	18	22~26	95 ohm
3	22	18	22~26	90 ohm
4	22	15	22~26	85 ohm

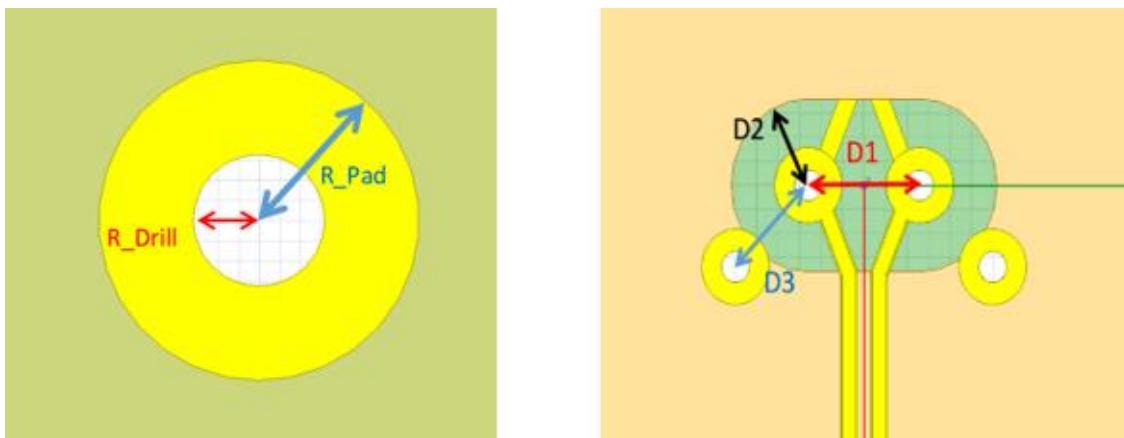


Figure 3-40 Differential Via Dimension

3.3.4 AC Capacitor Layout Requirement

If the operating rate of the interfaces in Table 3-1 is $\geq 8\text{GT/s}$, it is recommended to optimize the differential DC capacitance of these interfaces as follows.

Cutout on layer2(and layer3) under capacitor's pads, and set layer 3(or layer 4 if layer3 voided) under capacitor as ground plane. Cutout size recommend to be decided by simulation according customer's PCB layer stack. Also, there are some dimensions for reference according to EVB's HDI PCB(1+N+1) stack.

In addition, place 4pcs GND PTH Vias around ESD to connect the ground reference layers of the L2~L4 layers.

Table 3-3 Voiding Size at AC Capacitor Recommendation

Interface	Cutout Layer	D1	H	L
DP1.4	Layer2&Layer3	25mil	20mil	Pad Length
HDMI2.1	Layer2&Layer3	25mil	20mil	Pad Length
PCI-E3.0	Layer2	25mil	20mil	Pad Length

D1: center to center distance; L:voiding length; H:voiding weight.

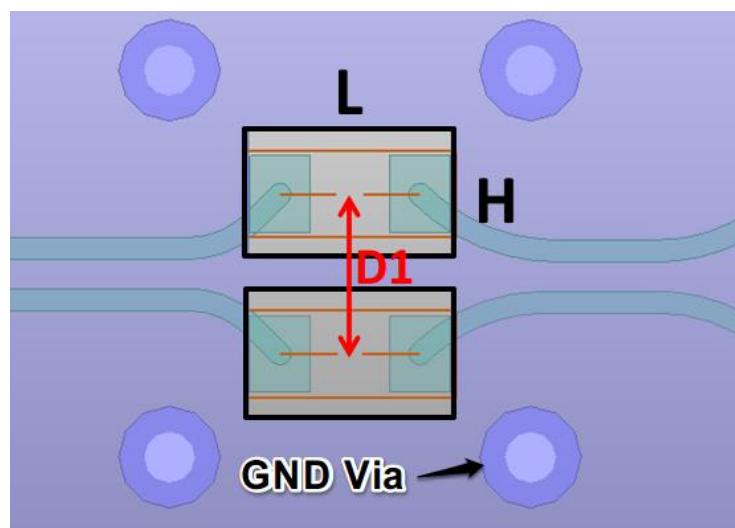


Figure 3-41 Void Size for AC Cap

3.3.5 ESD Layout Requirement

If the operating rate of the interfaces in Table 3-1 is $\geq 8\text{GT/s}$, the differential pair ESD devices for these interfaces are recommended to be optimized as follows.

Cutout on layer2(and layer3) under connector pads, and set layer 3(or layer 4 if layer3 voided) under ESD device as ground plane. Cutout size recommend to be decided by simulation according customer's PCB layer stack. Also, there are some dimensions for reference according to EVB's HDI PCB(1+N+1) stack.(ESD PN: ESD73034D).

In addition, place 4pcs GND PTH Vias around ESD to connect the ground reference layers of the L2~L4 layers.

Table 3-4 Voiding Size at ESD Recommendation

Interface	Cutout Layer	H	W
DP1.4	Layer2&Layer3	22mil	Pad Length
HDMI2.1	Layer2&Layer3	22mil	Pad Length

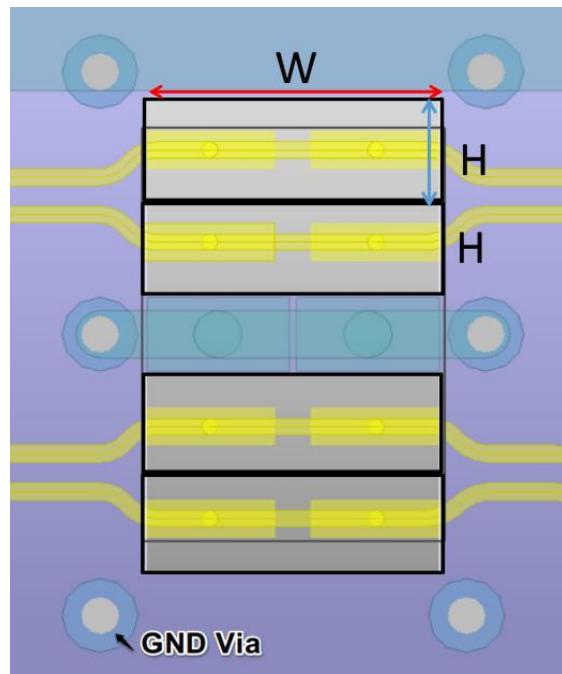


Figure 3-42 Voiding size for ESD

3.3.6 Recommend PCB Layout Guideline at Connector

If these interface in Table 3-1 operating $\geq 8\text{GT/s}$, connectors must meet HDMI2.1/DP1.4/PCI-E3.0 specification, we recommend to use connectors from Molex, HRS, Amphenol, etc.

Cutout on layer2(and layer3) under capacitor's pads, and set layer 3(or layer 4 if layer3 voided) under connector as ground plane. Cutout size recommend to be decided by simulation according customer's PCB layer stack. Also, there are some dimensions for reference according to EVB's HDI PCB(1+N+1) stack.

In addition, recommend each GND Pad has 2pcs GND PTH-Via for DP、HDMI2.1、PCI-E3.0 connector, and keep via located closely enough to pad.

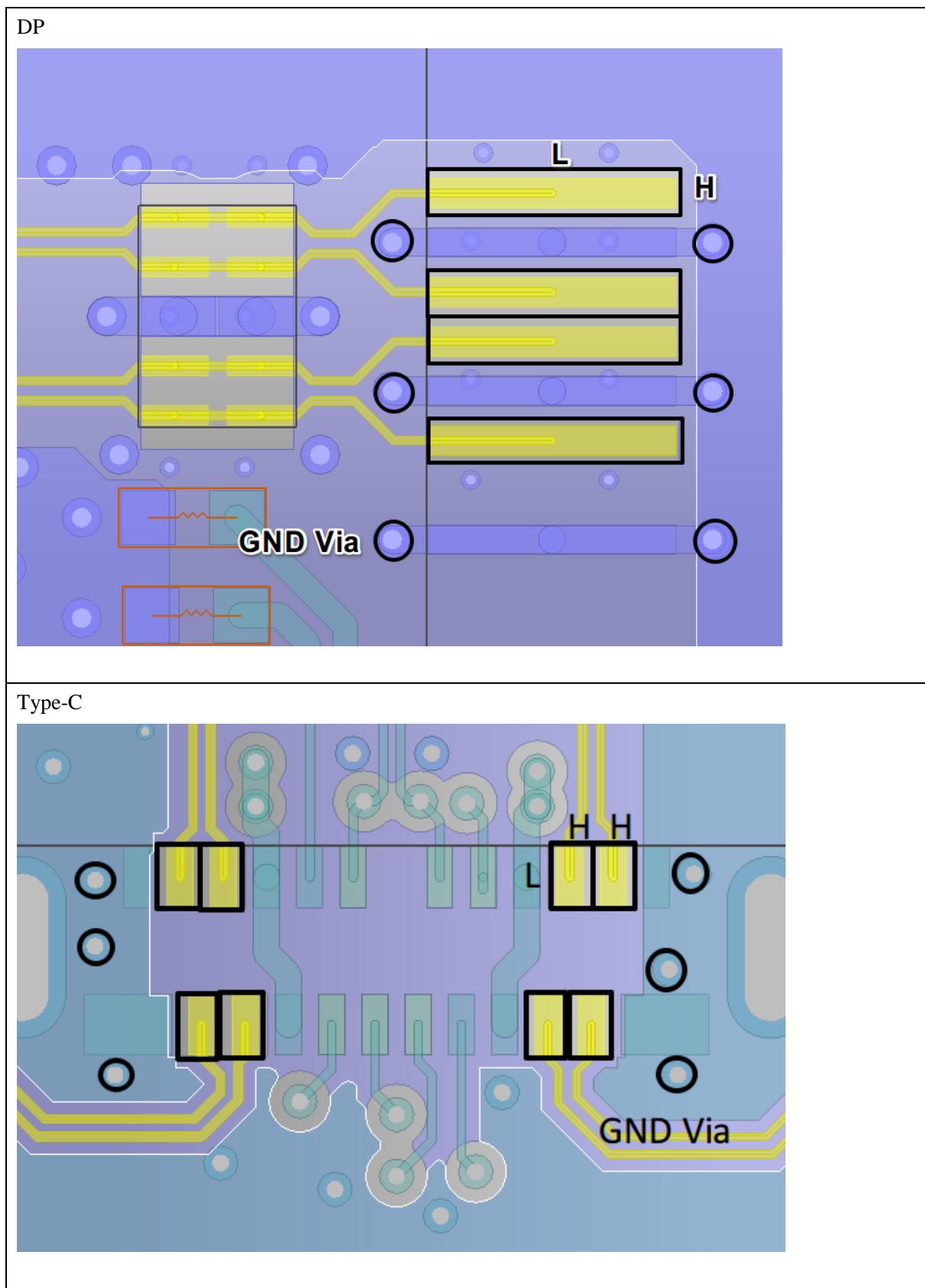
There are some dimensions for reference according to EVB's HDI PCB(1+N+1) stack.

Table 3-5 Voiding Size at Recommendation

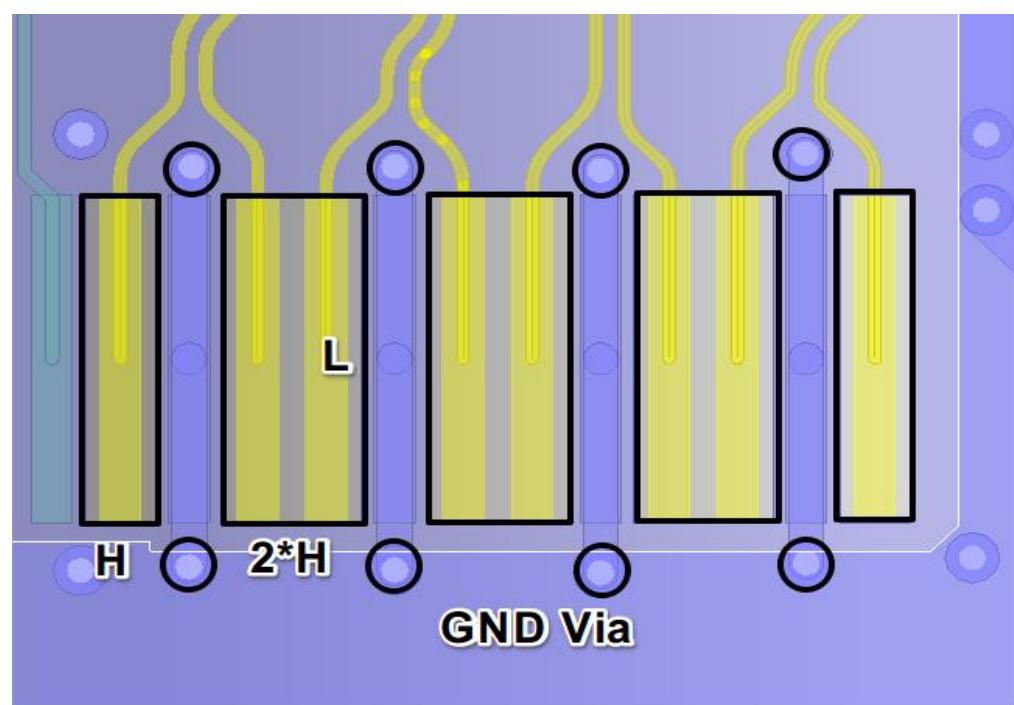
Connector	Part Number	Cutout Layer	H	L
DP	Molex 472720029	Layer2&Layer3	18mil	Pad Length
Type-C	Molex 1054500101	Layer2&Layer3	20mil	Pad Length
HDMI2.1	Molex 2086581051	Layer2&Layer3	20mil	Pad Length
PCI-E3.0	Amphenol 10076266-101TLF	Layer2	91mil	89mil

Recommend connector layout example:

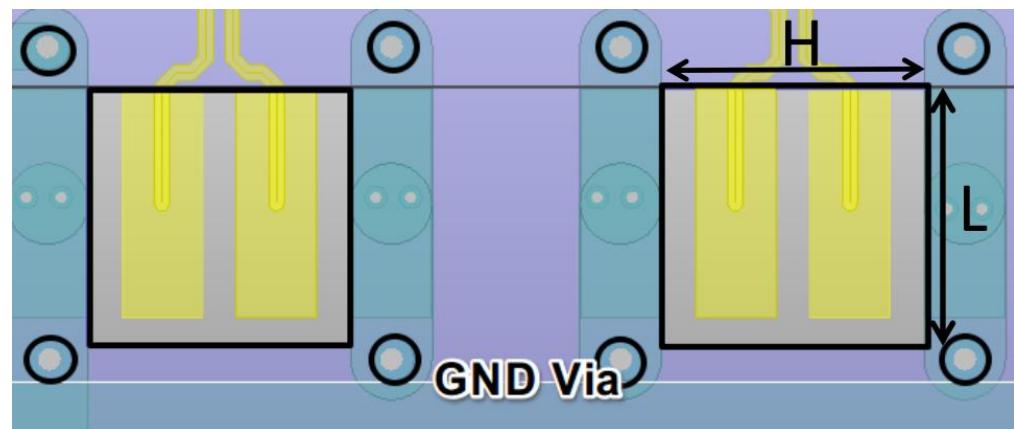
Table 3-6 Recommend Layout at Connector



HDMI2.1



PCI-E3.0



3.4 Interfaces Design Guide

3.4.1 Clock/Reset Circuit PCB Design

Pay attention to the following items in the PCB design of the clock circuit:

- Give priority to the layout of the crystal circuit, which should be placed on the same layer as the chip and as close as possible to avoid drilling vias. The crystal trace should be as short as possible, away from interference sources, and as far as possible from the edge of the board;
- The crystal and clock signal traces should be surrounded by ground throughout the whole process, and at least one GND via is added every 200-300mil for the surrounded ground line, and it is necessary to ensure the integrity of the ground reference plane of the neighboring layer;
- If the crystal circuit layout is placed on a different layer from the chip, the crystal traces must be surrounded by ground throughout the whole process, to avoid interference;
- Clock traces Xin, Xout and the projection area under the crystal are prohibited from any traces to avoid noise coupling into the clock circuit;
- A ground loop can be placed around the top layer under the crystal. The ground loop is connected to the neighboring ground layer through vias to isolate noise;
- The second layer under the crystal maintains a complete ground reference plane to avoid any trace division, which helps to isolate noise and maintain the crystal output

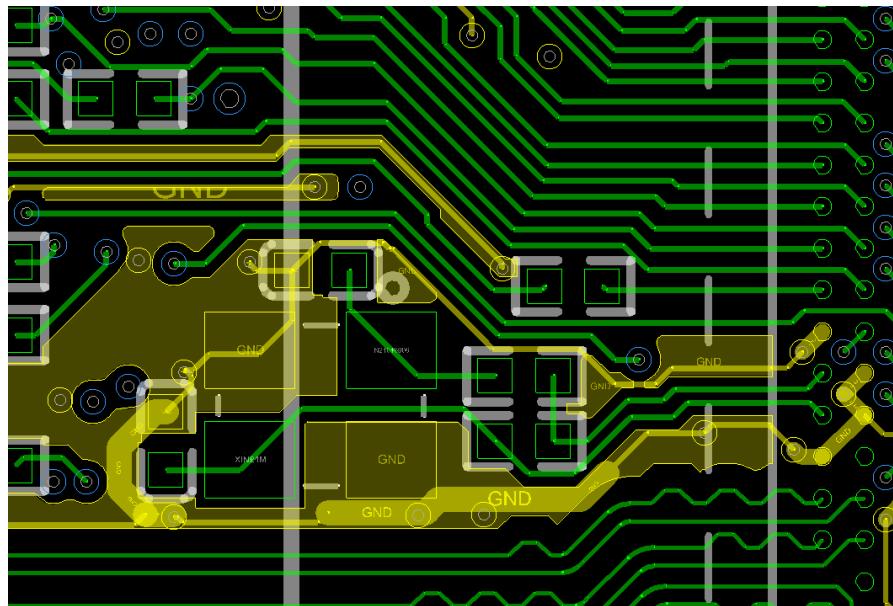


Figure 3-43 RK3588 Crystal Layout and Routing

- The decoupling capacitors for PLL_DVDD0V75, PLL_AVDD1V8, OSC_1V8, PMU_0V75 power supply must be placed on the back of the chip pins. When routing, try to form it through the capacitor pads and then to the chip pins.

Pay attention to the following items in the PCB design of the reset circuit:

- During layout, the RESETn reset signal should be kept away from the edge of the board and metal connectors to prevent the reset module from crashing due to abnormalities caused by ESD;

- The RESETn filter capacitor should be placed as close as possible to the chip pin layout. The signal must pass through the capacitor before entering the chip. Note that the ground pad of the filter capacitor must have a 0402 ground via. It is recommended to make more than two ground holes if space permits;
- The RESETn signal should be far away from strong interference signals such as DCDC and RF to prevent interference. If the trace is long, it is recommended to cover the ground, and add at least one GND via every 400mil;
- The TVS protection diode of the RESETn button should be placed as close as possible to the button. The signal topology is: button--->TVS--->100 ohm--->capacitance (near CPU&PMIC)--->CPU&PMIC; when ESD occurs, The ESD current must be attenuated by the TVS device first.

3.4.2 PMIC/Power Circuit PCB Design

3.4.2.1 RK806 Power Supply PCB Design Solution

In the overall layout, from the perspective of power quality, RK806 should be placed as close as possible to RK3588 (when considering heat dissipation design, it needs to be placed properly, not too close or too far away). When placing the direction, try to give priority to the wiring (copper) from RK3588 to RK806's BUCK1, BUCK2, BUCK3, BUCK4 is smooth, which have relatively large output current.

Note:

- Takes 0.5*0.3mm vias as an example. A single via for high-voltage power supply is recommended to go 0.8A, and low-voltage power supply (below 1V) is calculated at 0.5A;
- The negative pole of the high-current buck input and output capacitors must have the same number of vias as the positive pole, so as to have a better wave filtering effect (many customers tend to ignore the power supply vias of the negative pole of the capacitor);
- It is not recommended that the pads and vias of some parts of the power supply components be treated with thermal pads and cross connections, and should be covered with copper.

The EPAD grounding pad of RK806 should firstly ensure that there are enough vias. It is recommended to ensure that 6*6 vias of 0.5*0.3mm or 8*8 vias of 0.4*0.2mm or more are used to reduce grounding impedance and enhance heat conduction. Blind and buried holes are added to the board to help reduce impedance.

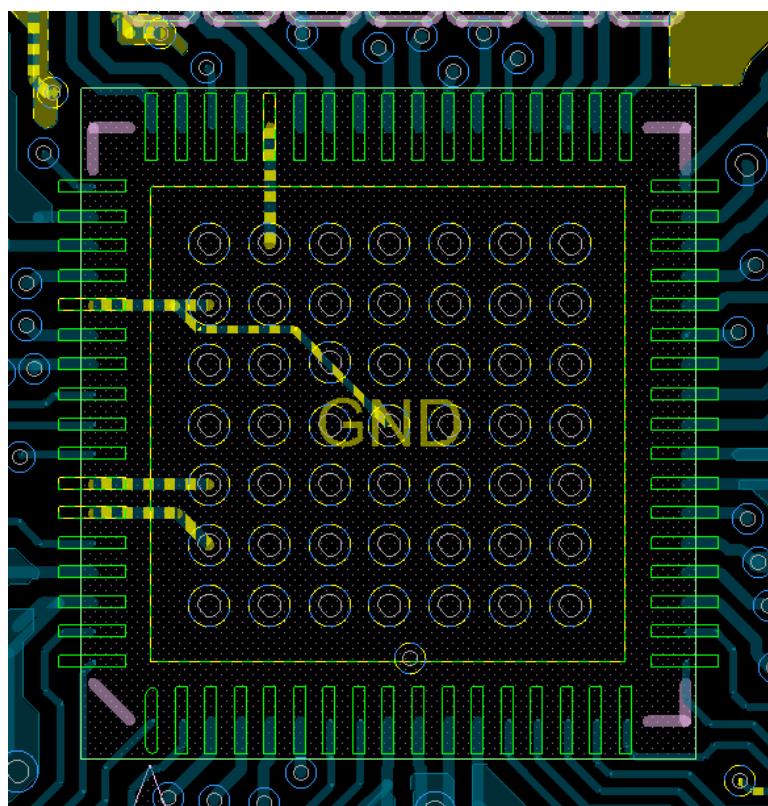


Figure 3-44 RK806 EPAD Via Distribution

- BUCK1\3 design requirements of RK806:

The input capacitor must be as close as possible to the chip (if the input capacitor is placed on the back of the chip, make sure that the GND terminal of the capacitor is close to the ePad of the RK806), and the connection loop between the input capacitor and VCC and GND should be as small as possible. It should be ensured that the SW traces are as short and thick as possible (make the area larger as soon as possible after the chip pins are routed out) to improve the over-current capability and power efficiency; for places where vias need to be drilled, VCC1/3 should be at least required if the power supply is combined. 5 vias of 0.5*0.3mm, if they need 3 or more vias of 0.5*0.3mm, the GND terminals of the output capacitors of BUKC1 and BUCK3 can be shared together, but at least 15 or more 0.5 *0.3mm vias, if there are positions, small vias or blind vias can be added; if there is a layer change in the BUCK1 output, at least 15 or more 0.5*0.3mm vias are guaranteed, and the same BUCK3 must ensure 12 or more 0.5 *0.3mm via hole;

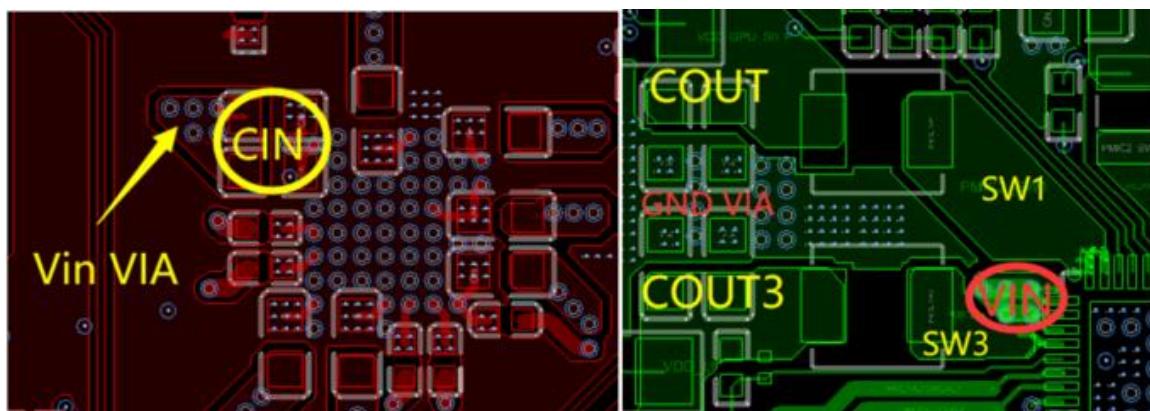


Figure 3-45 RK806 BUCK1/BUCK3 Layout and Routing

- BUCK2 PCB design requirements of RK806:

The input capacitor must be as close as possible to the chip (if the input capacitor is placed on the back of the chip, make sure that the GND terminal of the capacitor is close to the ePad of the RK806), and the connection loop between the input capacitor and VCC and GND should be as small as possible. It should be ensured that the SW traces are as short and thick as possible (make the area larger as soon as possible after the chip pins are routed out) to improve the over-current capability and power efficiency; for places where vias need to be drilled, at least three 0.5* VCC2 power supplies are required 0.3mm vias, at least 12 0.5*0.3mm vias are required on the GND end of the output capacitor. If there are positions, small vias or blind holes can be added; if there is a layer change in the output, at least 12 or more 0.5* 0.3mm layer-changing vias.

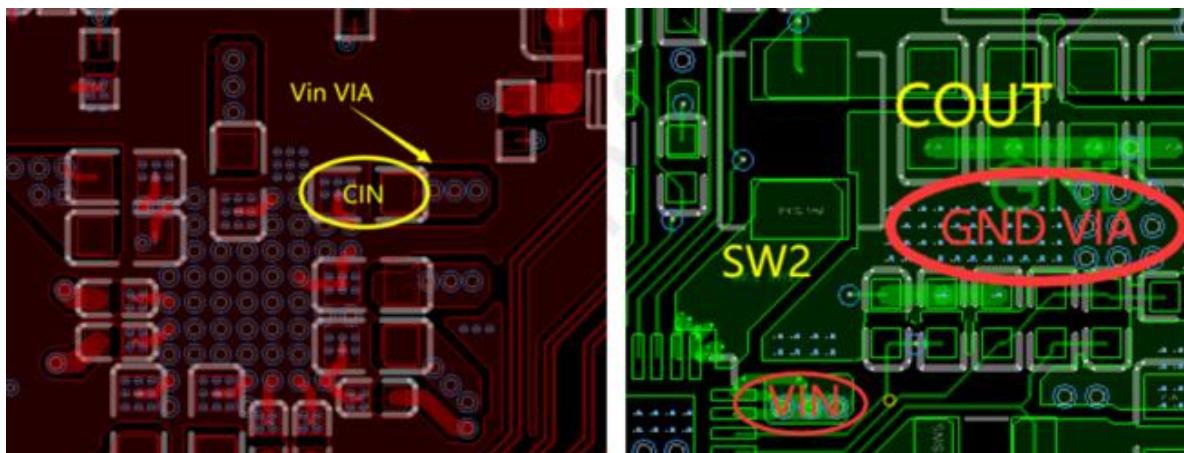


Figure 3-46 RK806 BUCK2 Layout and Routing

- BUCK4 PCB design requirements of RK806:

The input capacitor must be as close as possible to the chip (if the input capacitor is placed on the back of the chip, make sure that the GND terminal of the capacitor is close to the ePad of the RK806), and the connection loop between the input capacitor and VCC and GND should be as small as possible. It should be ensured that the SW traces are as short and thick as possible (make the area larger as soon as possible after the chip pins are routed out) to improve the overcurrent capability and power efficiency; for places where vias need to be drilled, at least three 0.5* VCC4 power supplies are required 0.3mm vias, at least 12 or more 0.5*0.3mm vias at the GND end of the output capacitor, if not enough, blind holes can be made to supplement; if there is a layer change in the output, at least 12 or more 0.5*0.3mm vias should be changed. vias.

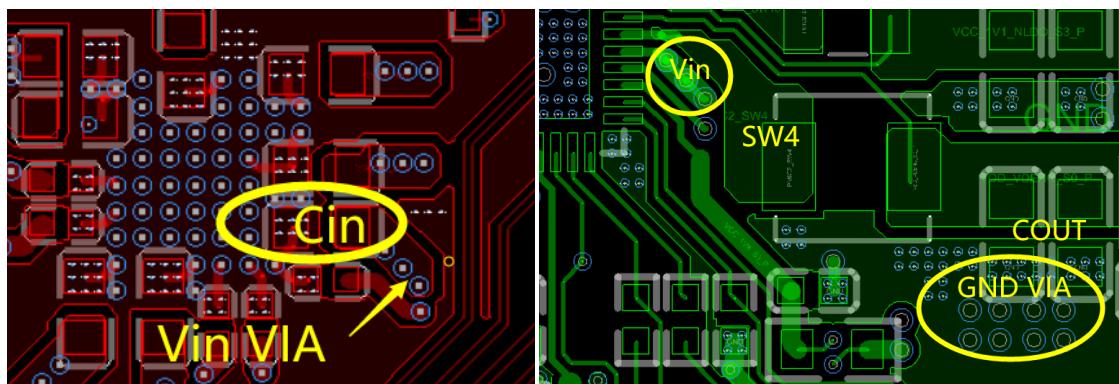


Figure 3-47 RK806 BUCK4 Layout and Routing

- RK806 2.5A BUCK PCB Design Requirements:

The input capacitor must be as close as possible to the chip (if the input capacitor is placed on the back of the chip, make sure that the GND terminal of the capacitor is close to the ePad of the RK806), and the connection loop between the input capacitor and VCC and GND should be as small as possible. It should be ensured that the SW traces are as short and thick as possible (make the area larger as soon as possible after the chip pins are routed out) to improve the power supply overcurrent capability and efficiency; 9/10 power supply requires at least 2 vias of 0.5*0.3mm (3 vias of 0.5*0.3mm are required if the pins are close to VCC5 and VCC7, VCC6 and VCC10), and the GND terminal of the output capacitor must be at least 5 If there are more than 0.5*0.3mm vias, blind holes can be made to supplement them; if there is a layer change in the output, at least 5 or more 0.5*0.3mm layer-changed vias are guaranteed.

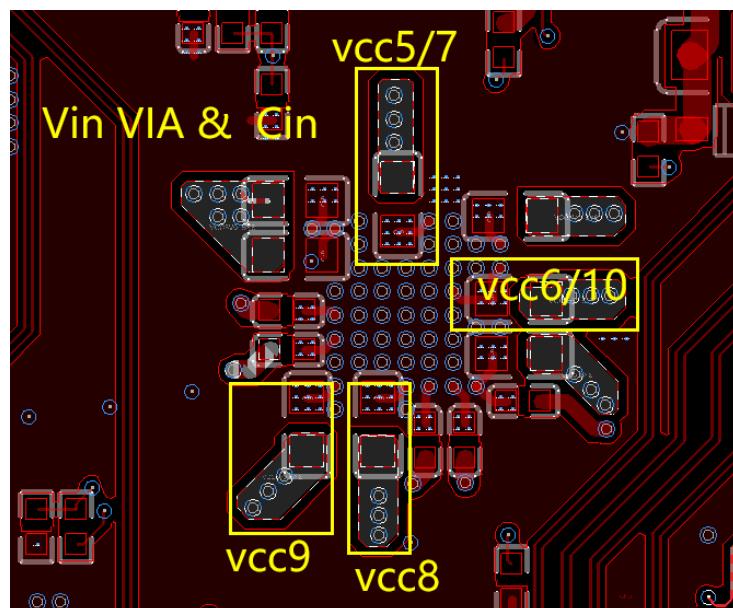


Figure 3-48 RK806 2.5A BUCK VCC Input Capacitor Layout and Routing

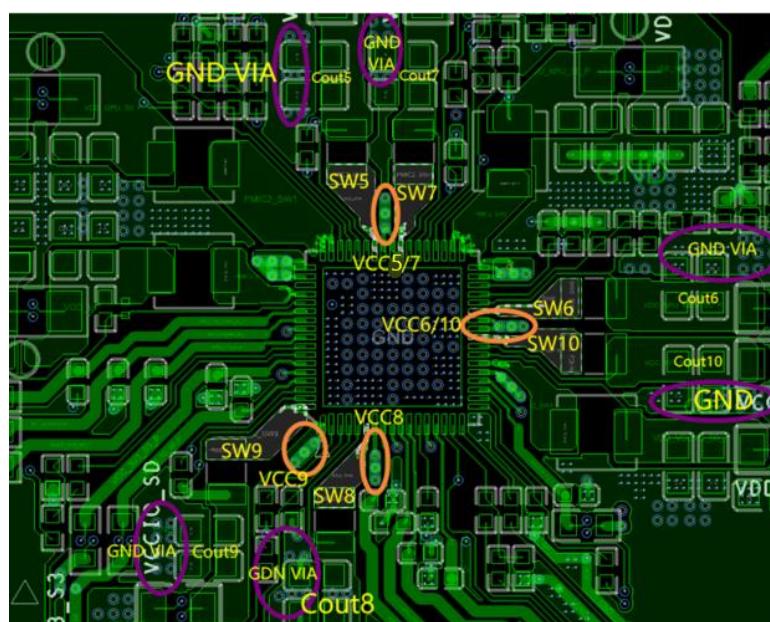


Figure 3-49 RK806 2.5A BUCK Layout and Routing

- LDO PCB design requirements of RK806:

- The input capacitor must be as close as possible to the chip, and the connection loop between the input capacitor and VCC11/12/13/14 and GND should be as small as possible;
- The output capacitor must be as close as possible to the chip, and the connection loop between the output capacitor and PLDO1/2/3/4/5/6 and NLDO1/2/3/4/5 and GND should be as small as possible;
- If voltage rail $\geq 1.8v$ from LDO, power trace width should be above 1mm per Amper; If voltage rail $< 1.8v$ from LDO and supply trace length above 10cm, power trace width should be above 2mm per Amper. After being drawn out, it should be thickened to the required size as soon as possible, and special attention should be paid to the trace length and loss of the low-voltage and high-current NLDO to meet the power supply voltage and ripple requirements of the target chip.

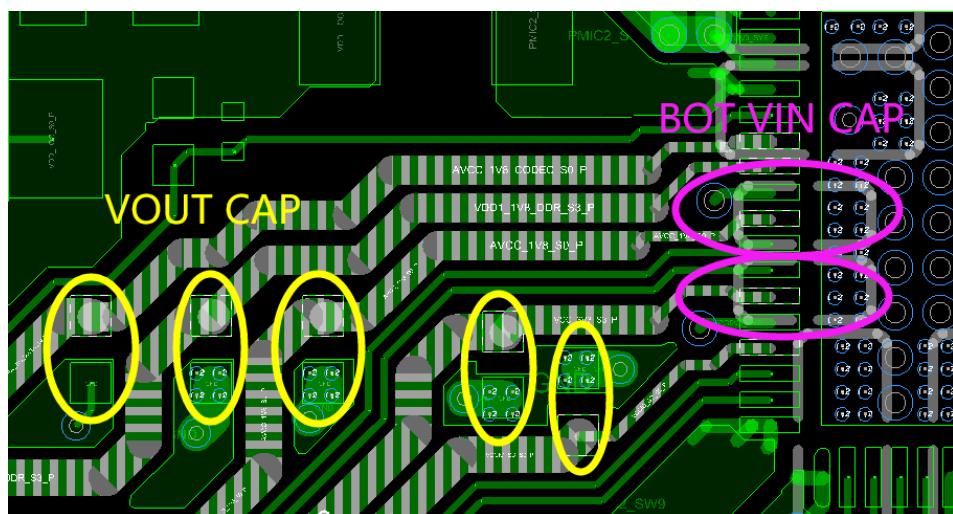


Figure 3-50 RK806 LDO Layout and Routing

- The VCCA capacitor of RK806 must be placed close to the pins and away from other interference sources. The ground pad of the capacitor must be well grounded, that is, the path between the ground pad of the VCCA capacitor and the RK806 ePad must be the shortest, and must not be divided by other signals;
- The 100nF capacitor of Pin 67 (RESETB) of RK806 must be close to the pin of RK806 to improve the anti-interference ability of the chip;
- It is recommended that the pins of RK806 should not be covered with copper. All pins are connected to the outside through wiring. The width of the wiring should not exceed the width of the pins, so as to prevent the patch from being easily connected to tin after the pad becomes larger.

3.4.2.2 DC-DC PCB Design of Discrete Power Supply

The input capacitor C_{in} and the output capacitor C_{out} are placed between Vin pin, Vout pin and the GND of the DC/DC to minimize the loop area between Vin, Vout and the GND of the DC/DC, which can reduce the power supply EMI amplitude, greatly improving the stability of the DCDC, as shown below:

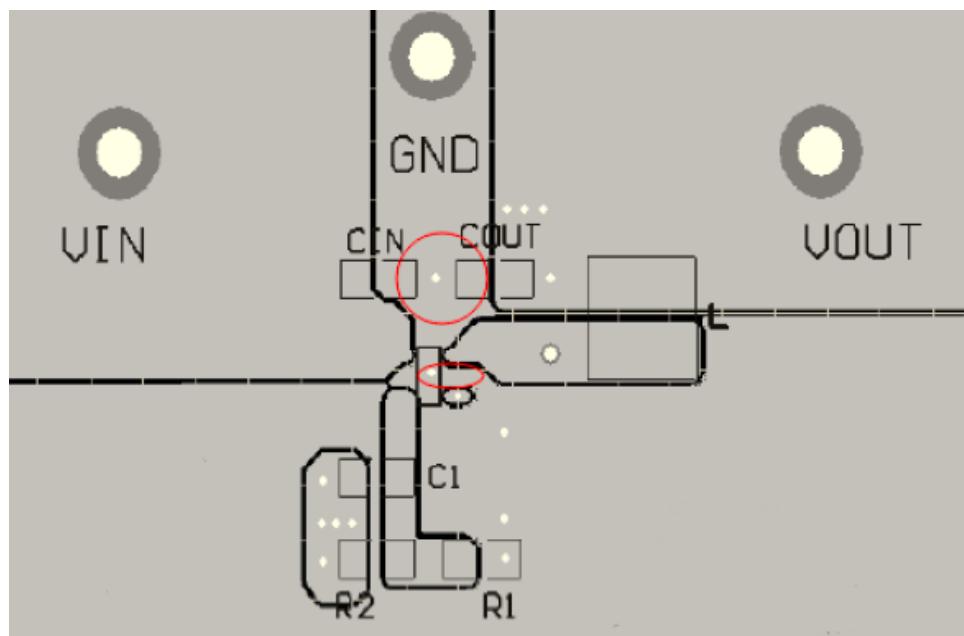


Figure 3-51 Discrete Power DC/DC Layout and Routing

Input capacitor C_{in} , output capacitor C_{out} and DC/DC GND should make as many vias as possible. It is recommended to make more than 4 vias of 0503. If the V_{IN} and V_{OUT} power supply layers are changed, it is recommended to make more vias, and more than 4 0503 vias (related to the current, which will be described below). The inductor should be as close to the DC/DC as possible, the trace should be as thick and short as possible, and the resistance ground of the FB terminal should be kept away from the interference source as far as possible.

3.4.2.3 RK860 Power Supply PCB Design

RK860-x is used as an auxiliary supplementary power supply for a single RK806-1, generally supplying high current power such as CPU, GPU or NPU. The overall layout should be as close as possible to the RK3588 (preferably within 10mm).

The RK860 PCB layout is recommended to refer to the following diagram: the input and output capacitors are placed at both ends of the chip and as close to the chip as possible. The capacitors, inductors and the chip are layout on the same layer, the GND pad of the capacitor and the GND of the chip are in the same direction of the pads direction to form a minimum closed loop; the inductor is placed on the output capacitor and both ends of the chip to ensure that the SW trace is as short as possible to prevent interference with other modules; the V_{OUT} feedback signal of the chip must be taken from the output capacitor (avoid from the inductor pad Take the signal), and try to avoid too close to the SW; for the place where vias need to be punched, V_{IN} can punch 5 vias of $0.5*0.3mm$, and the buck output needs at least 12 vias of $0.5*0.3mm$. In particular, the GND vias are as close as possible to the chip GND and capacitor pads. If the board is blind and buried, some blind holes should be filled in the GND pads of the chip and capacitors.

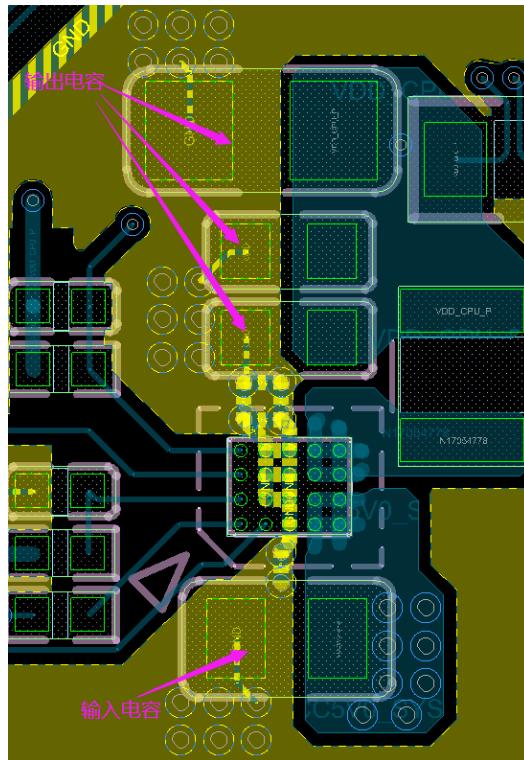


Figure 3-52 VDD_CPU Power Supply DC/DC Layout and Routing

3.4.2.4 DC-DC Remote Feedback Design of VDD_LOGIC, VDD_GPU, VDD_NPU, VDD_CPU power supply

The 100ohm feedback resistor needs to be placed close to the output capacitor. One end of the resistor is connected to the DC-DC output capacitor, the other end is connected to the VOUT feedback pin of the PMIC, and at the same time is connected to the farthest load of the same power network as the RK3588 power pin. The width of the feedback line is 4 mil, and it must be traced with the power supply copper to avoid interference; the feedback line and other signals are separated by more than 6 mils, such as the schematic diagram of the VDD_GPU power supply copper coating and the feedback line, and other power supplies are handled similarly.

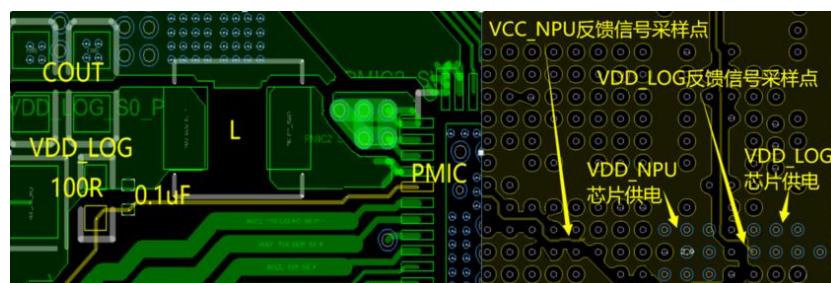


Figure 3-53 Schematic Diagram of DC/DC Remote Feedback Design

3.4.2.5 RK3588 VDD_CPU_BIG0/1 Power Supply PCB Design

The copper cladding width of VDD_CPU_BIG0/1 should meet the current requirements of the chip. The copper cladding connected to the power pins of the chip should be wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm that it is connected to each power supply pin of the CPU. paths are sufficient.

When the power supply of VDD_CPU_BIG is changed in the peripheral layer, it is necessary to make as many power supply vias as possible (12 or more vias of 0.5*0.3mm) to reduce the voltage drop caused by the changed layer vias; GND vias of decoupling capacitors It should be consistent with the number of power supply vias, otherwise the capacitance effect will be greatly reduced.

For the power pins of VDD_CPU_BIG0/1 of the RK3588, it is recommended that each Ball has a corresponding power supply via., and it is necessary to ensure that each power supply ≥ 10 power supply vias in the worst case. The top layer is in a "#" shape and cross-connected, and the recommended trace width is 10mil.

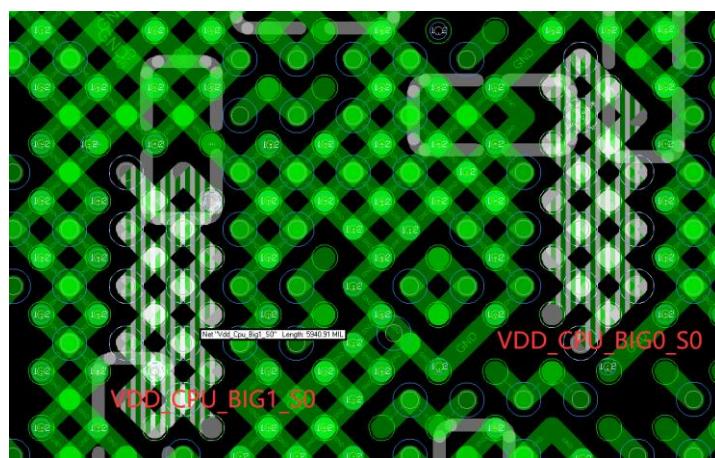


Figure 3-54 Power Pin Traces and Vias of RK3588 Chip VDD_CPU_BIG0/1

The decoupling capacitors close to the VDD_CPU_BIG power pins of RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close to the GND Ball in the center of the chip as possible, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.



Figure 3-55 Placement of Decoupling Capacitors on the Back of Power Pins of RK3588 Chip VDD_CPU0/1

Since the VDD_CPU_BIG current is relatively large, the copper width of the CPU area is recommended to be greater than 300mil, and the effective overcurrent width needs to be $\geq 110\text{mil}$. The width of the peripheral area is recommended to be greater than 600mil. It is recommended to have two layers of power planes and two layers of adjacent GND return planes, and there should be at least one layer of power planes and one layer of adjacent GND return planes in the worst case. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-57 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5\text{mil}$.

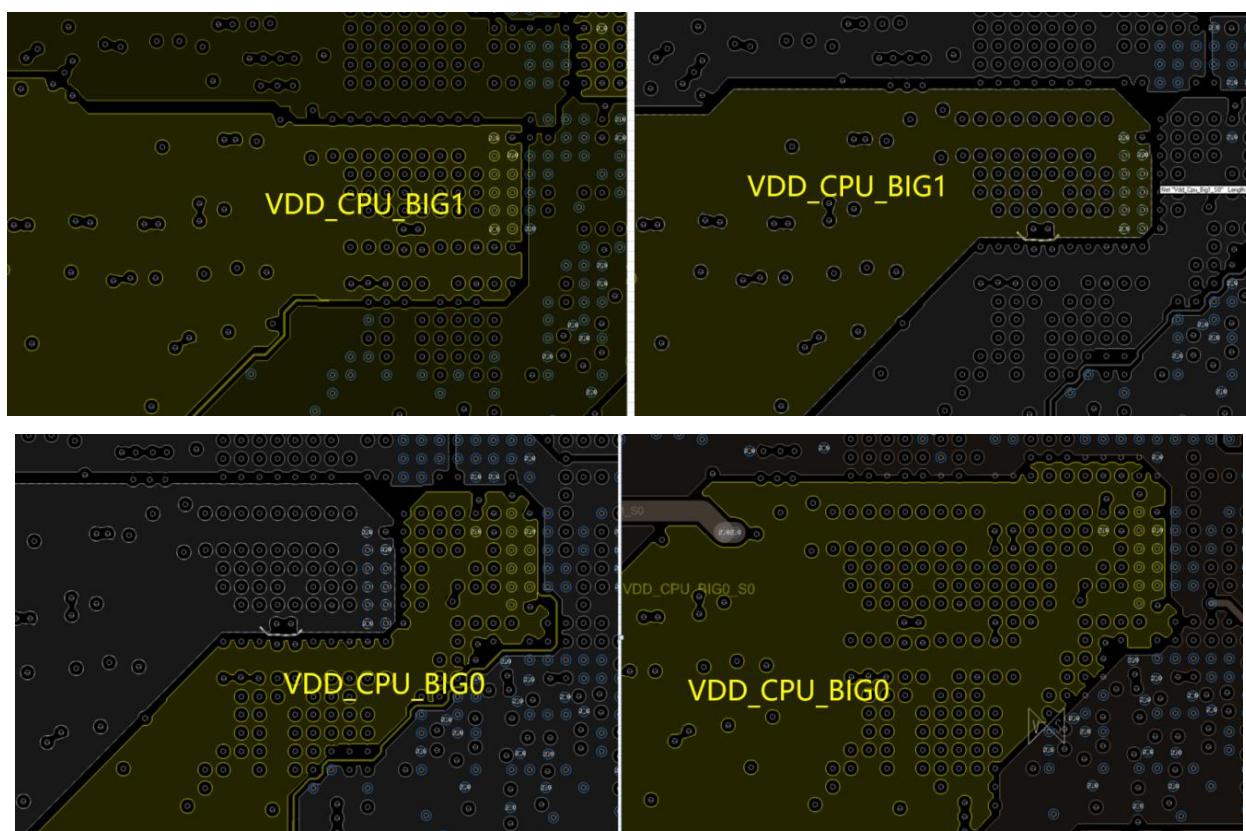


Figure 3-56 RK3588 Chip VDD_CPU_BIG0/1 Power Layer Copper Cladding

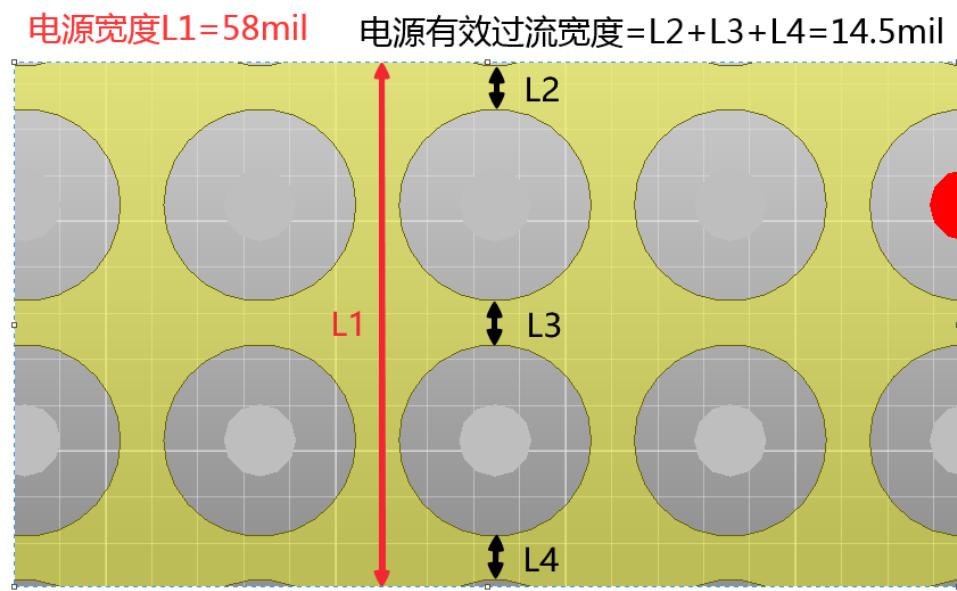


Figure 3-57 Schematic of the Effective Overcurrent Width of the Power Supply

In the CPU area, the number of GND vias within the 40 mil range of BIG0 power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 12 .

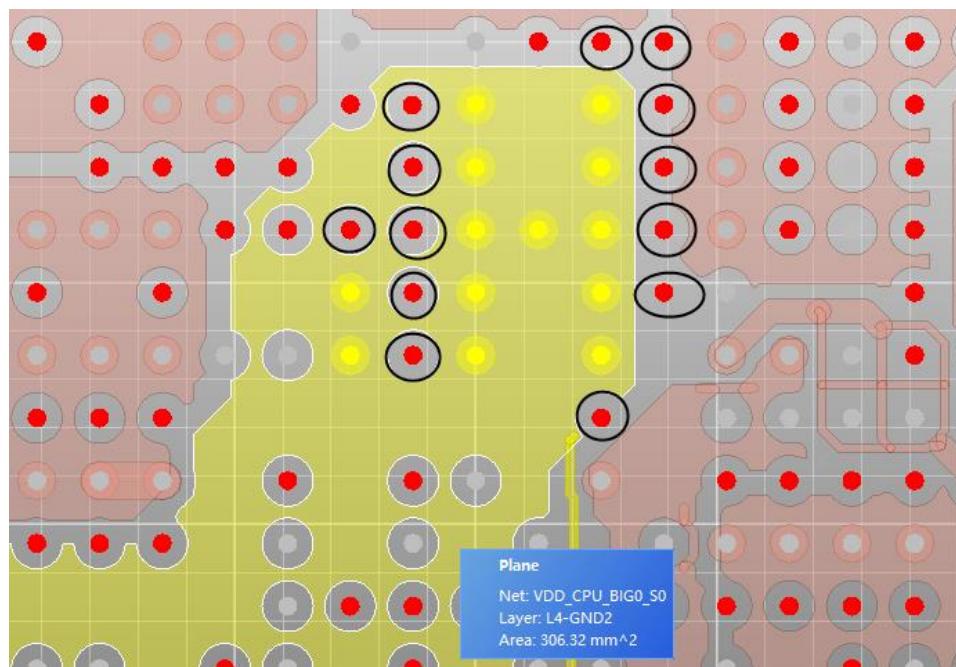


Figure 3-58 BIG0 Power Ground Via Placement Diagram

In the CPU area, the number of GND vias within the 40mil range of BIG1 power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 12 .

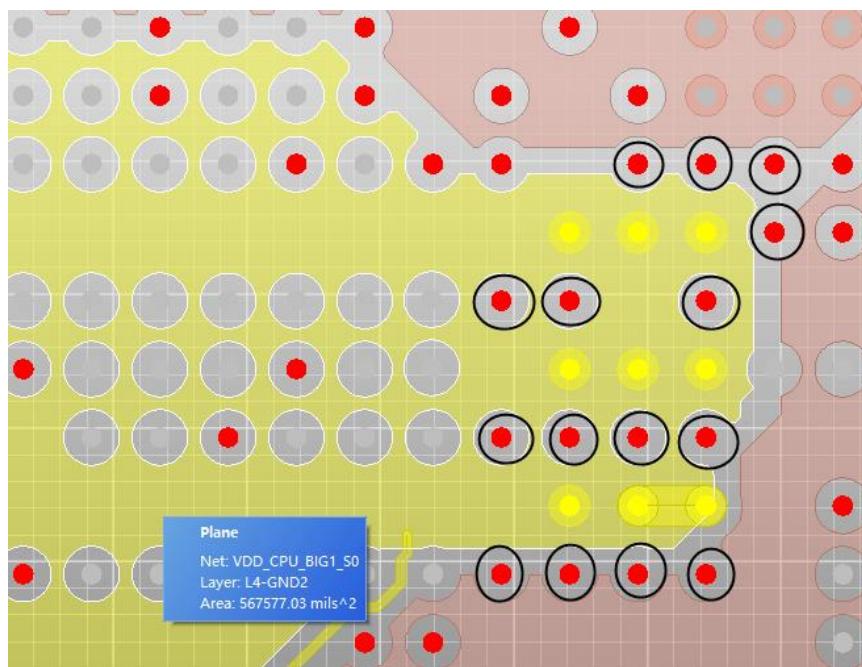


Figure 3-59 BIG1 Power Ground Via Placement Diagram

The recommended target impedance value of the power rail PDN is as follows:

Table 3-7 Recommended value of the target impedance of the power rails PDN

Frequency	Impedance value (ohm)
100Khz~1Mhz	≤ 0.02
1Mhz ~30Mhz	≤ 0.03
30Mhz~100Mhz	≤ 0.1

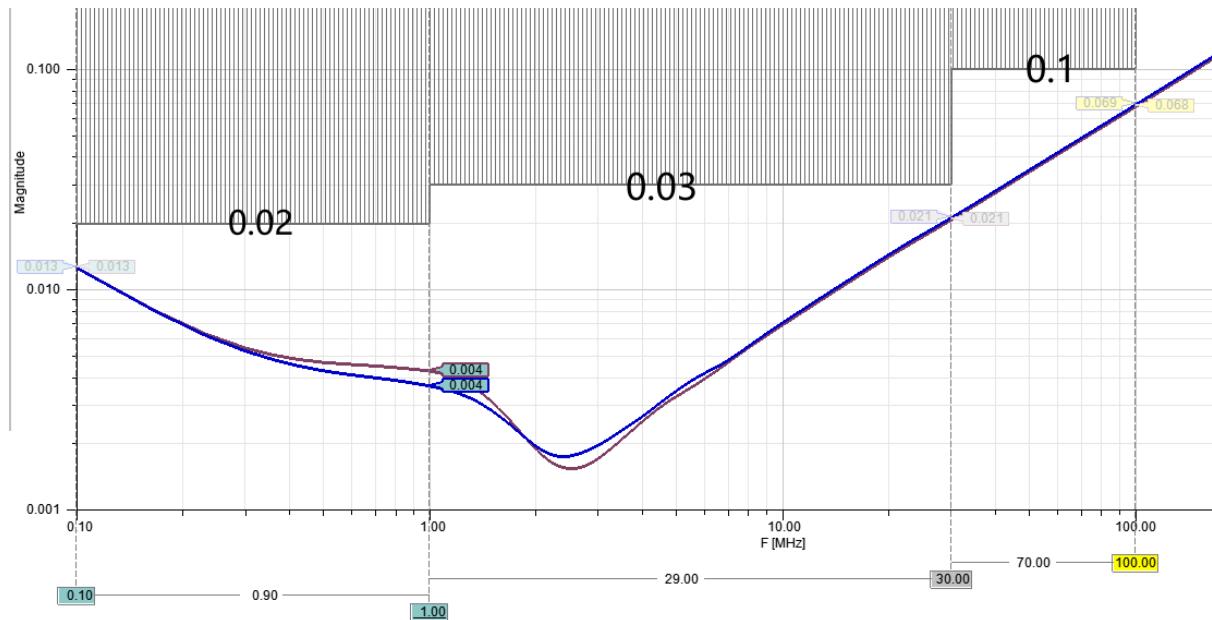


Figure 3-60 Suggested PDN requirements for BIG Power rails

3.4.2.6 RK3588 VDD_LOGIC Power Supply PCB Design

The copper cladding width of VDD_LOGIC needs to meet the current requirements of the chip. The copper cladding connected to the power pins of the chip should be wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm the path connected to each power pin of the CPU.

When the power supply of VDD_LOGIC changes layers at the periphery, it is necessary to make as many power supply vias (more than 8 vias of 0.5*0.3mm) as possible to reduce the voltage drop caused by the changed layer vias; the GND vias of the decoupling capacitors should be Keep the same number as its power supply vias, otherwise the capacitance effect will be greatly reduced.

For the power pins of VDD_LOGIC of the RK3588 chip, each Ball needs to correspond to a via hole, and the top layer is in a "well" shape and cross-connected. The recommended line width is 10mil.

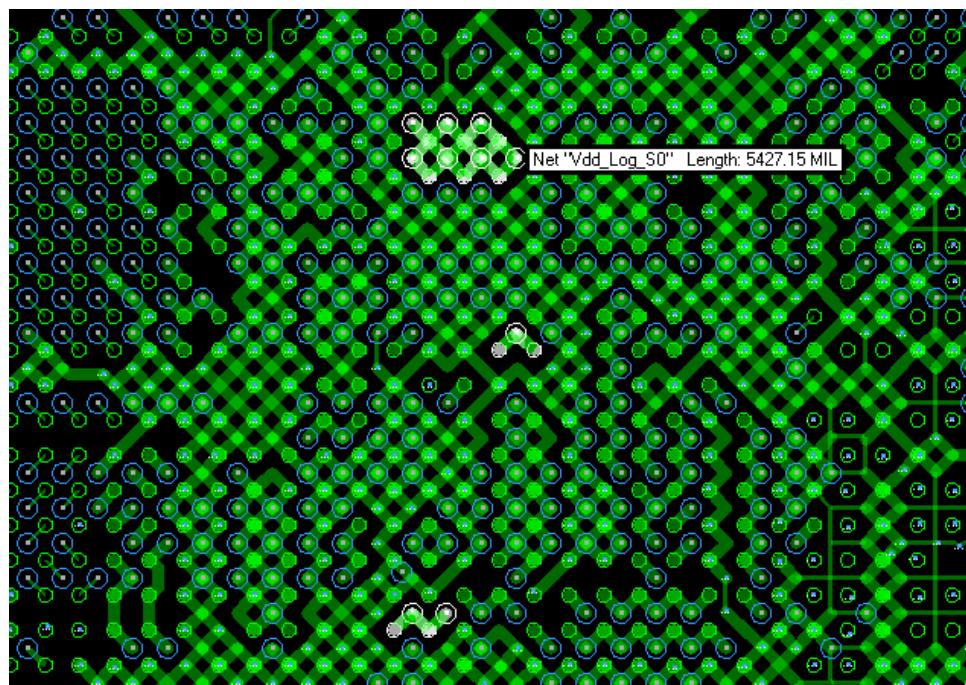


Figure 3-61 RK3588 VDD_LOGIC Power Pin Traces and Vias

The decoupling capacitors close to the VDD_LOGIC power pins of RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.

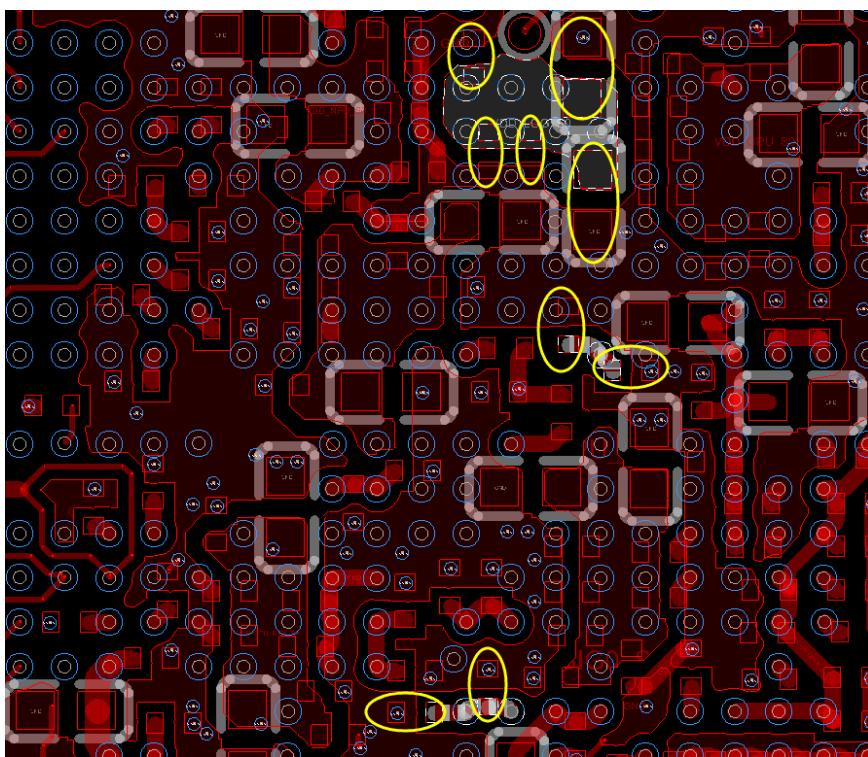


Figure 3-62 Placement of Decoupling Capacitors on the Back of Power Pins of RK3588 Chip VDD_LOGIC

Since the VDD_LOGIC current is relatively large, the copper width of the CPU area is recommended to be greater than 300mil, and the effective overcurrent width needs to be $\geq 110\text{mil}$. The width of the peripheral area is recommended to be greater than 500mil. It is recommended to have two layers of power planes and two layers of adjacent GND return planes, and there should be at least one layer of power planes and one layer of adjacent GND return planes in the worst case. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-64 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5\text{mil}$.

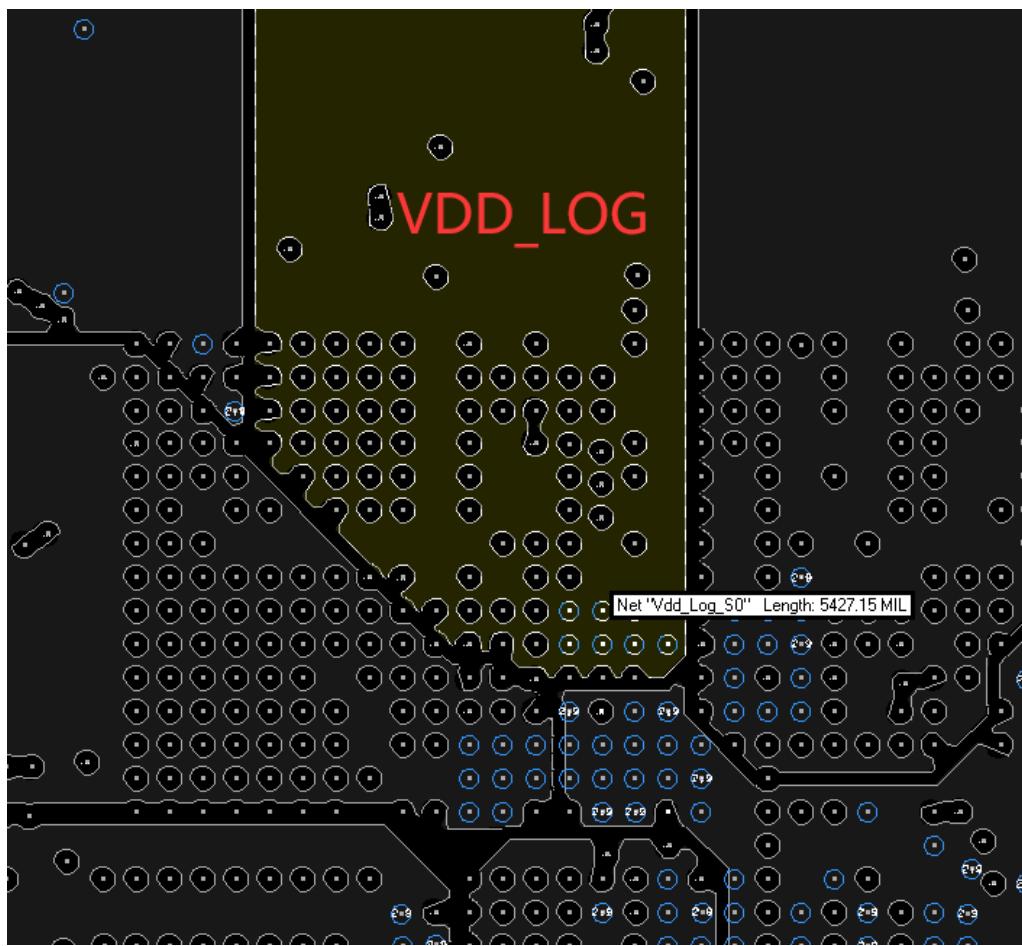


Figure 3-63 RK3588 VDD_LOGIC Power Layer Copper Cladding

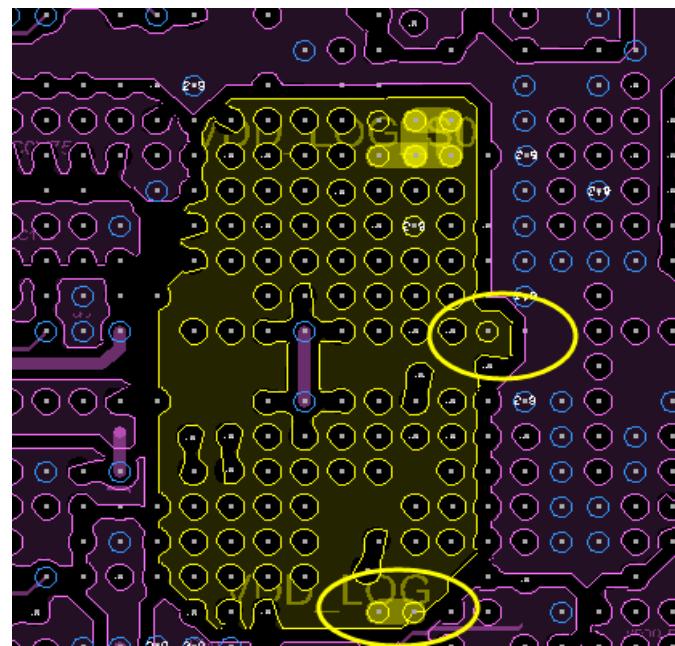


Figure 3-64 RK3588 VDD_LOGIC Chip Low Power Supply Layer Copper Cladding

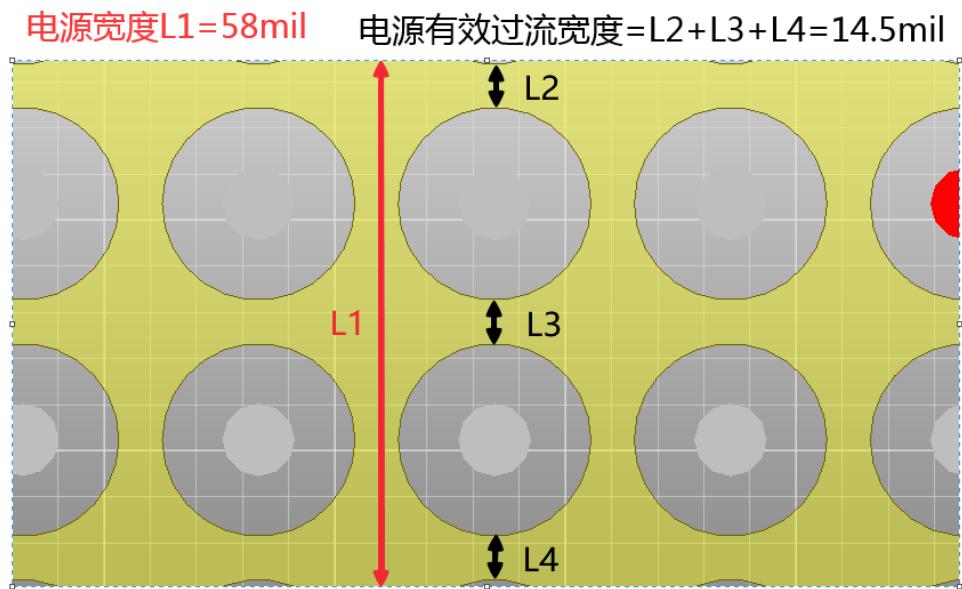


Figure 3-65 Schematic of the Effective Overcurrent Width of the Power Supply

In the CPU area, the number of GND vias within the 40mil range of power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 11 .

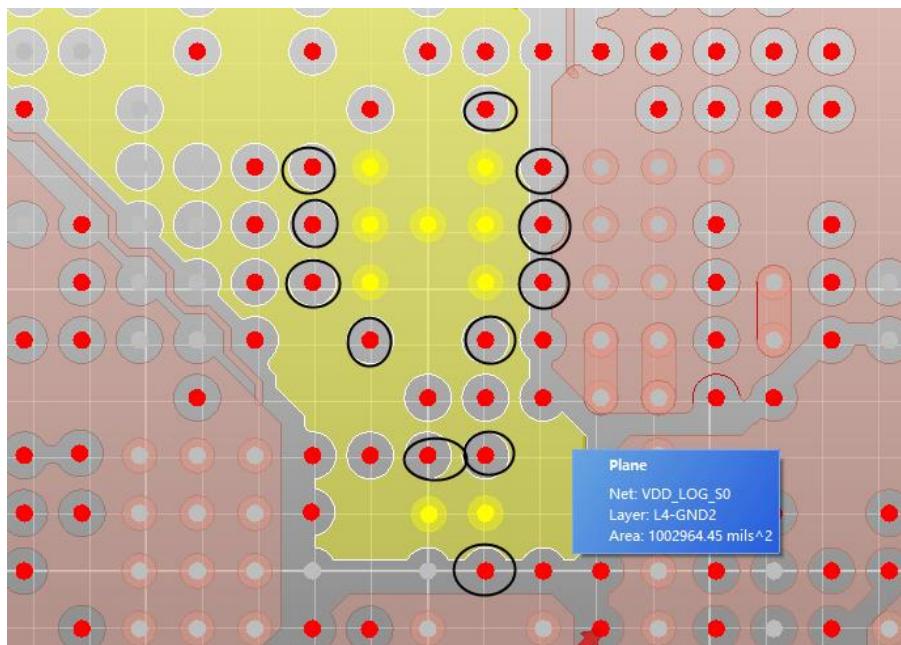


Figure 3-66 LOGIC Power Ground Via Placement Diagram

The recommended target impedance value of the power rails PDN is as follow:

Table 3-8 The suggested target impedance value of the power supply PDN

Frequency	Impedance value (ohm)
100Khz~1Mhz	≤ 0.02
1Mhz ~30Mhz	≤ 0.03
30Mhz~100Mhz	≤ 0.095

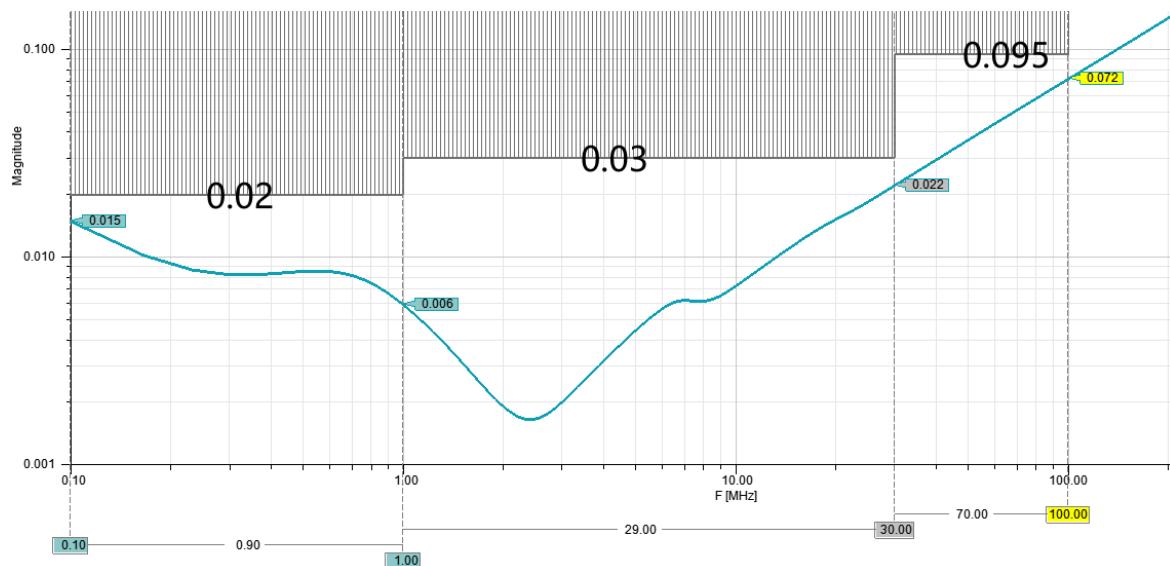


Figure 3-67 Suggested PDN requirements for LOGIC Power rails

3.4.2.7 RK3588 VDD_GPU Power Supply PCB Design

The copper cladding width of VDD_GPU needs to meet the current requirements of the chip. The copper cladding connected to the power pins of the chip is wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm the path connected to each power pin of the CPU. are enough.

When the power supply of VDD_GPU is changed on the periphery, it is necessary to make as many power supply vias (more than 12 vias of 0.5*0.3mm) as possible to reduce the voltage drop caused by the changed layer vias; the GND vias of the decoupling capacitors should be Keep the same number as its power supply vias, otherwise the capacitance effect will be greatly reduced.

For the power pins of the RK3588 chip VDD_GPU needs ≥ 11 power vias, and the top layer is in a "#" shape and cross-connected. The recommended line width is 10mil.

The power pins of the RK3588 chip VDD_GPU need ≥ 11 power supply vias, and the top layer is in a "well" shape and cross-connected. The recommended line width is 10mil.

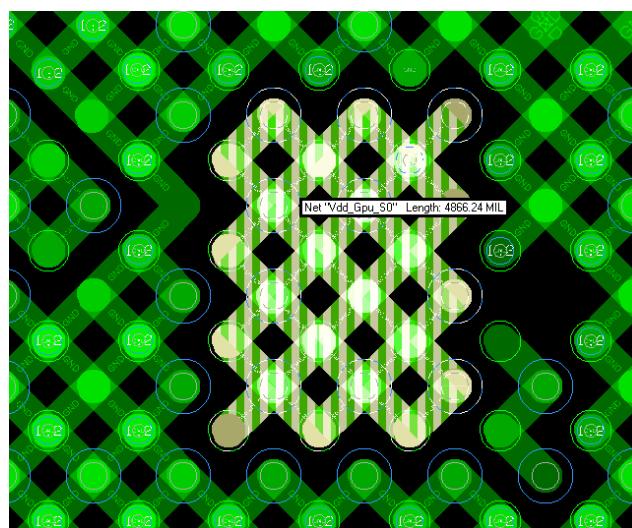


Figure 3-68 RK3588 VDD_GPU Power Pin Traces and Vias

The decoupling capacitors close to the VDD_GPU power pins of RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.

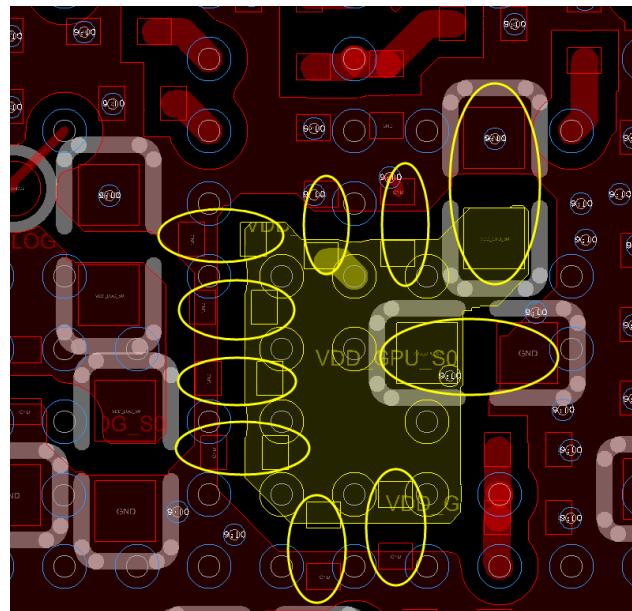


Figure 3-69 RK3588 chip VDD_GPU Power Pins Decoupling Capacitors on the Back

Since the VDD_GPU current is relatively large, the copper width of the CPU area is recommended to be greater than 400mil, and the effective overcurrent width needs to be $\geq 160\text{mil}$. The width of the peripheral area is recommended to be greater than 700mil. It is recommended to have two layers of power planes and two layers of adjacent GND return planes, and there should be at least one layer of power planes and one layer of adjacent GND return planes in the worst case. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the

positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-69 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5\text{mil}$.

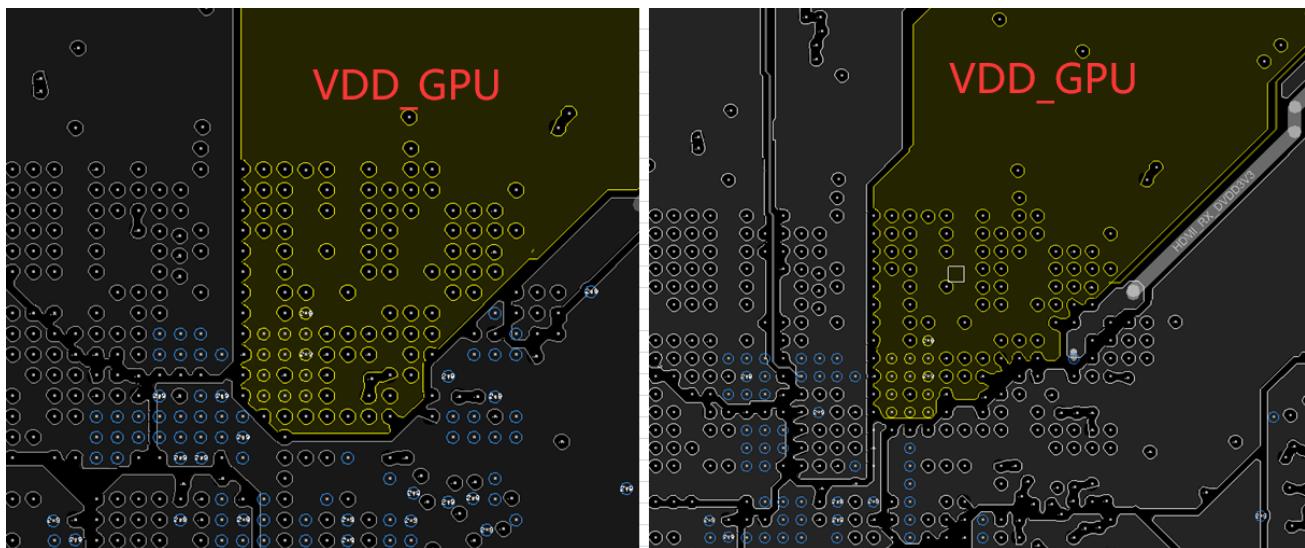


Figure 3-70 RK3588 VDD_GPU Power Layer Copper Cladding

电源宽度 $L1=58\text{mil}$ 电源有效过流宽度= $L2+L3+L4=14.5\text{mil}$

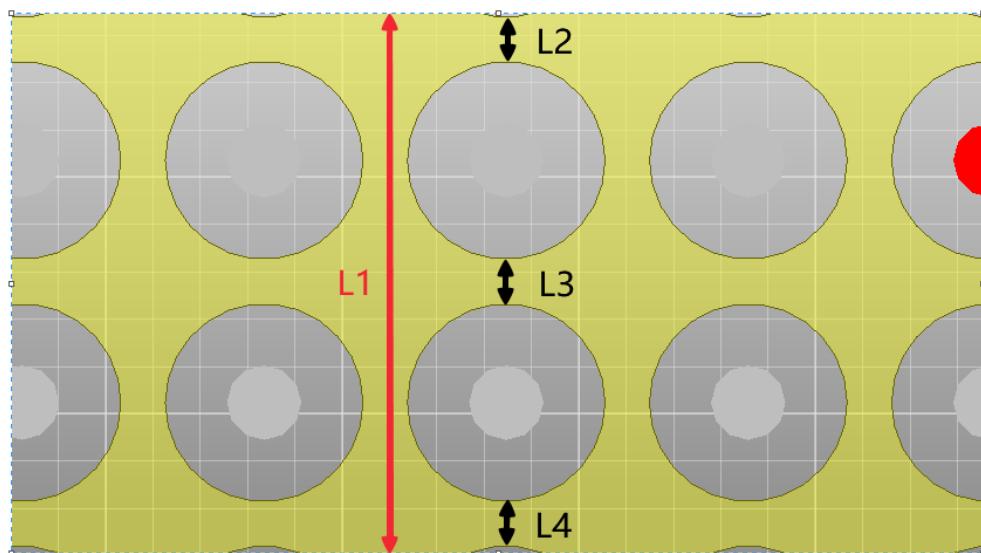


Figure 3-71 Schematic of the effective overcurrent width of the power supply

The number of GND vias within the 40mil range of power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 14 .

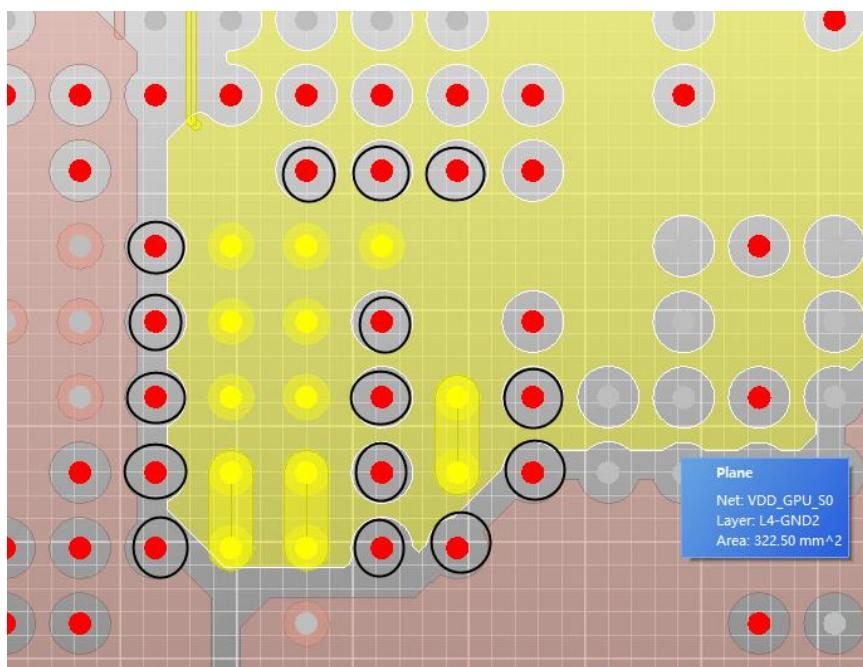


Figure 3-72 GPU Power Ground Via Placement Diagram

The recommended target impedance value of the power rails PDN is as follow:

Table 3-9 The suggested target impedance value of the power rails PDN

Frequency	impedance value (ohm)
100Khz~1Mhz	≤ 0.02
1Mhz ~30Mhz	≤ 0.03
30Mhz~100Mhz	≤ 0.09

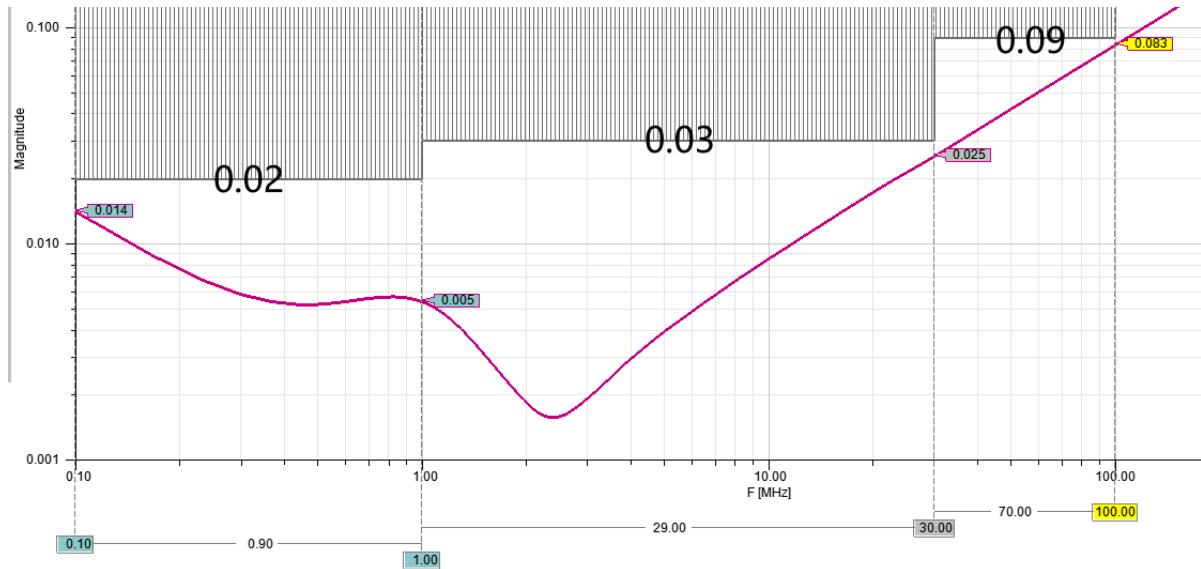


Figure 3-73 Suggested PDN requirements for GPU Power rails

3.4.2.8 RK3588 VDD_NPU Power PCB Design

The copper cladding width of VDD_NPU needs to meet the current requirements of the chip. The copper cladding connected to the power pins of the chip is wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm the path connected to each power pin of the CPU are enough.

When the power supply of VDD_NPU is changed in the peripheral layer, it is necessary to make as many power supply vias as possible (more than 7 vias of 0.5*0.3mm) to reduce the voltage drop caused by the changed layer vias; the GND vias of the decoupling capacitors should be Keep the same number as its power supply vias, otherwise the capacitance effect will be greatly reduced.

For the power pins of the VDD_NPU of the RK3588 chip, there is a corresponding via near each Ball, and the top layer is in a "#" shape and cross-connected. The recommended line width is 10mil.

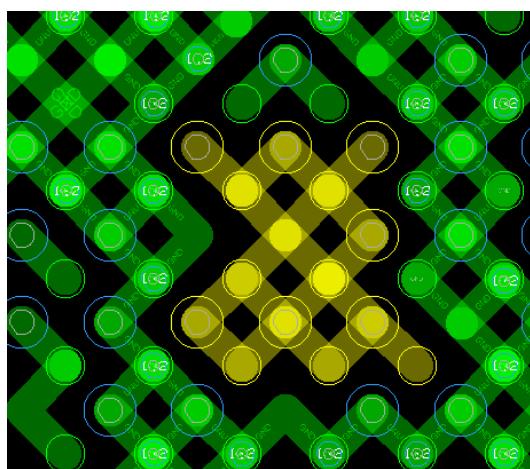


Figure 3-74 Power Pin Traces and Vias of RK3588 Chip VDD_NPU

The decoupling capacitors close to the VDD_NPU power pins of RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.



Figure 3-75 Decoupling Capacitors on the Back of the Power Pins of the RK3588 Chip VDD_NPU

For VDD_NPU power, the copper width of the CPU area should be greater than 300mil, and the effective overcurrent width needs to be ≥ 100 mil. The width of the peripheral area is recommended to be greater than 500mil. There should be at least one layer of power planes and one layer of adjacent GND return planes. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-74 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5$ mil.



Figure 3-76 RK3588 Chip VDD_NPU Power Layer Copper Cladding

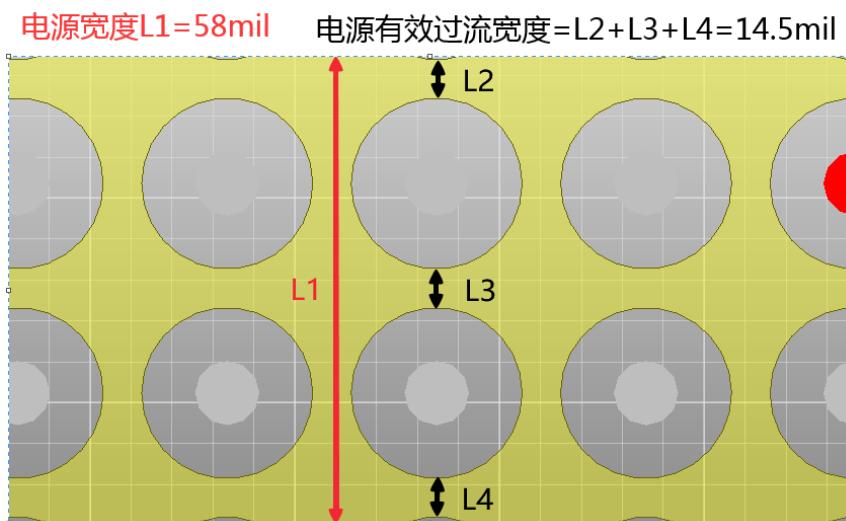


Figure 3-77 Schematic of the effective overcurrent width of the power supply

In the CPU area, the number of GND vias within the 40mil range of power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 9 .

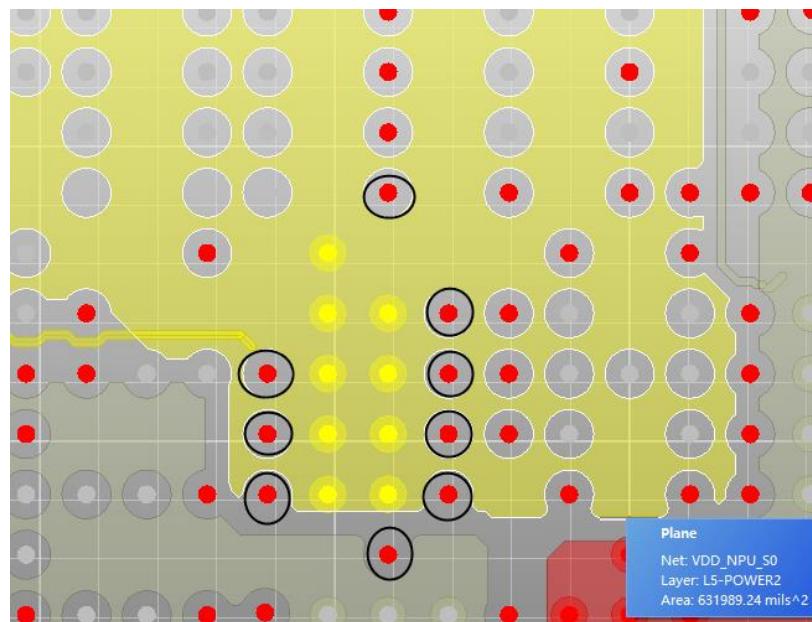


Figure 3-78 NPU Power Ground Via Placement Diagram

The recommended target impedance value of the NPU power rails PDN is as follow:

Table 3-10 The suggested target impedance value of the NPU power rails PDN

Frequency	impedance value (ohm)
100Khz~1Mhz	≤ 0.02
1Mhz ~30Mhz	≤ 0.04
30Mhz~100Mhz	≤ 0.13

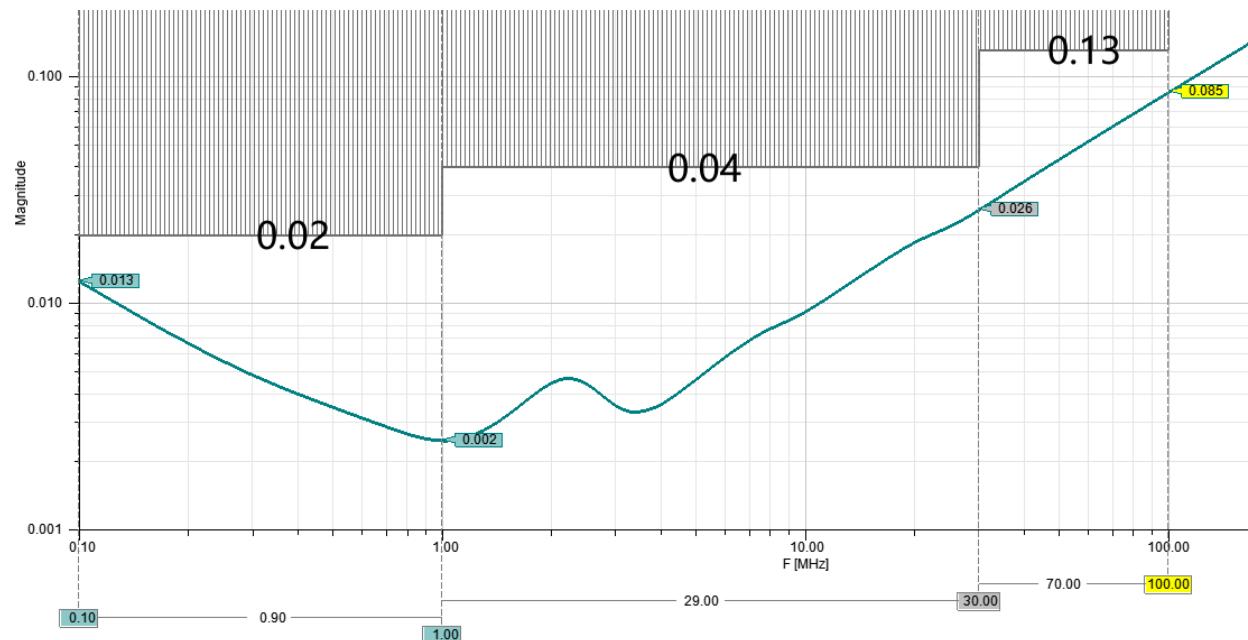


Figure 3-79 Suggested PDN requirements for NPU power rails

3.4.2.9 RK3588 VDD_CPU_LIT Power PCB Design

The copper cladding width of VDD_CPU_LIT must meet the current requirements of the chip. The copper cladding connected to the power pins of the chip is wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm the path connected to each power PIN pin of the CPU. are enough.

When the power supply of VDD_CPU_LIT is changed on the periphery, it is necessary to make as many power supply vias (9 or more 0.5*0.3mm vias) as possible to reduce the voltage drop caused by the changed layer vias; the GND vias of the decoupling capacitors should be Keep the same number as its power supply vias, otherwise the capacitance effect will be greatly reduced.

For the power pins of the RK3588 chip VDD_CPU_LIT, there is a corresponding via hole near each Ball, and the top layer is in a "well" shape and cross-connected. The recommended line width is 10mil.

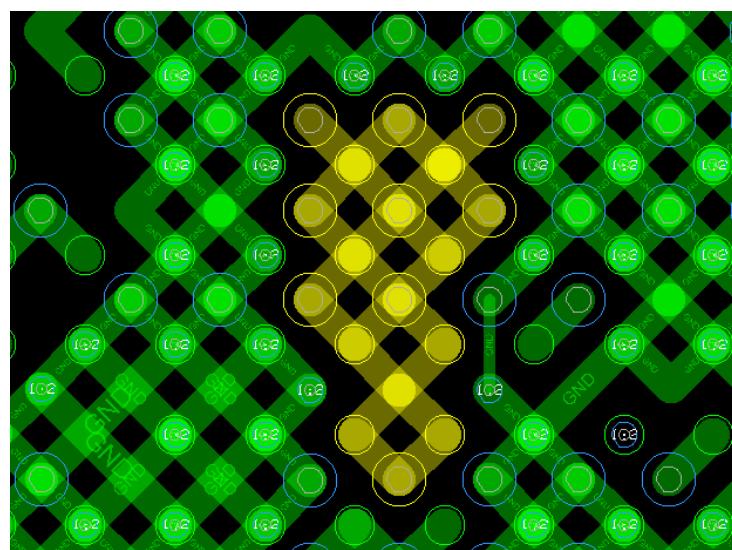


Figure 3-80 RK3588 VDD_CPU_LIT Power Pin Traces and Vias

The decoupling capacitors close to the VDD_CPU_LIT power pins of RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.

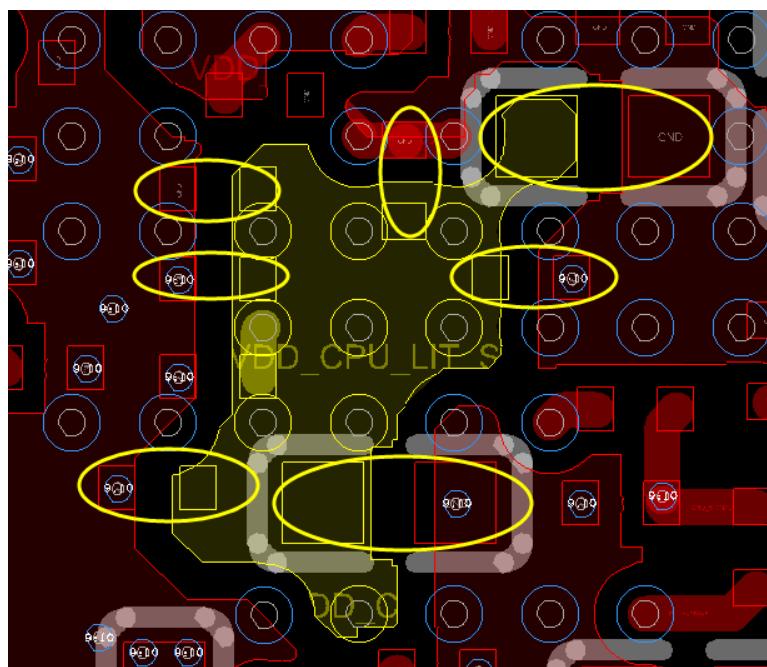


Figure 3-81 Distribution of Decoupling Capacitors on the Back of Power Pins of RK3588 VDD_CPU_LIT

For VDD_CPU_LIT power, the copper width of the CPU area should be greater than 180mil, and the effective overcurrent width needs to be $\geq 80\text{mil}$. The width of the peripheral area is recommended to be greater than 500mil. There should be at least one layer of power planes and one layer of adjacent GND return planes. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-79 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5\text{mil}$.

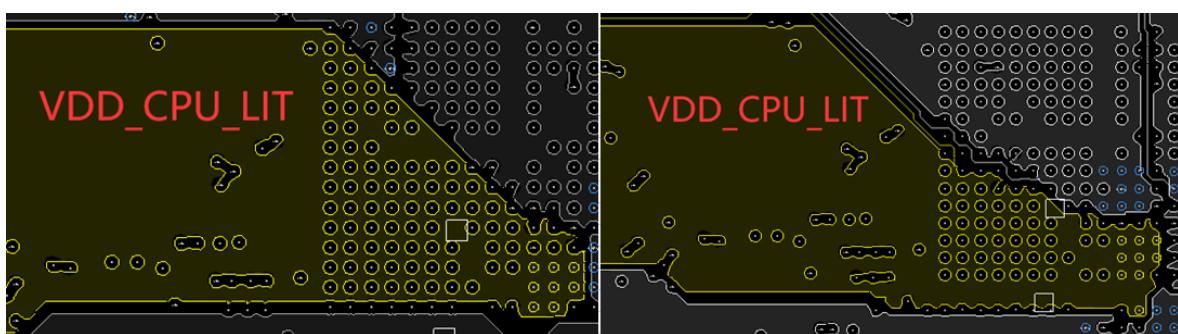


Figure 3-82 RK3588 VDD_CPU_LIT Power Layer Copper Cladding

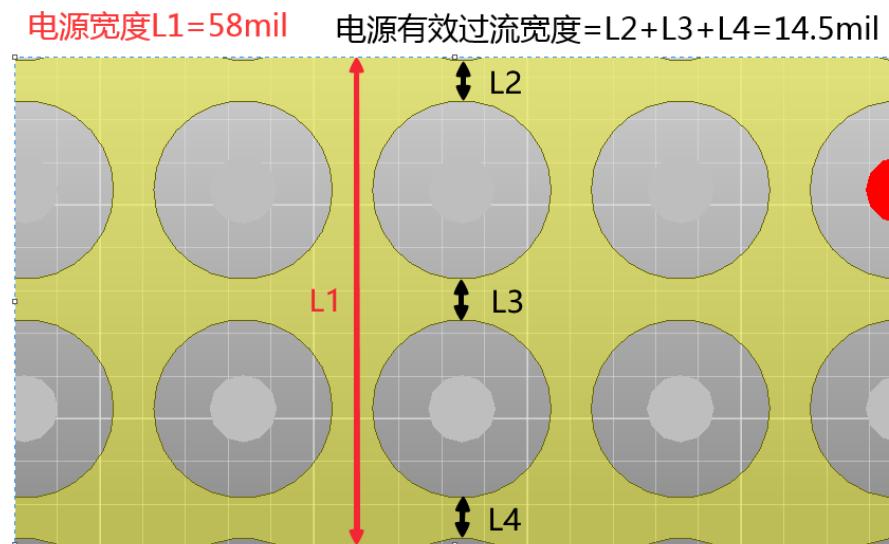


Figure 3-83 Schematic of the effective overcurrent width of the power supply

In the CPU area, the number of GND vias within the 40mil range of power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 9 .

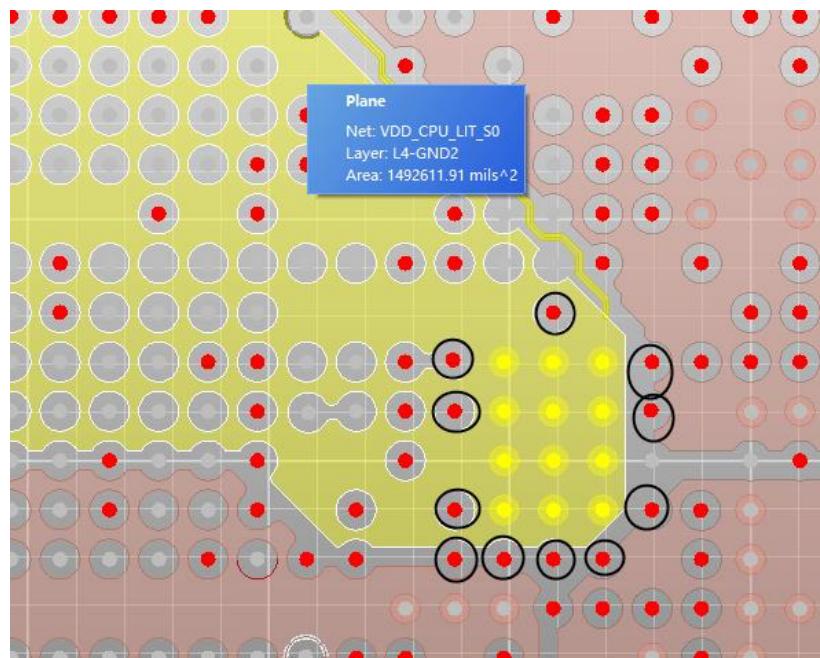


Figure 3-84 LIT Power Ground Via Placement Diagram

The suggested PND target impedance value of LIT power rails is as follow:

Table 3-11 The suggested PND target impedance value of LIT power rails

Frequency	impedance value (ohm)
100Khz~1Mhz	≤ 0.025
1Mhz ~30Mhz	≤ 0.035
30Mhz~100Mhz	≤ 0.11

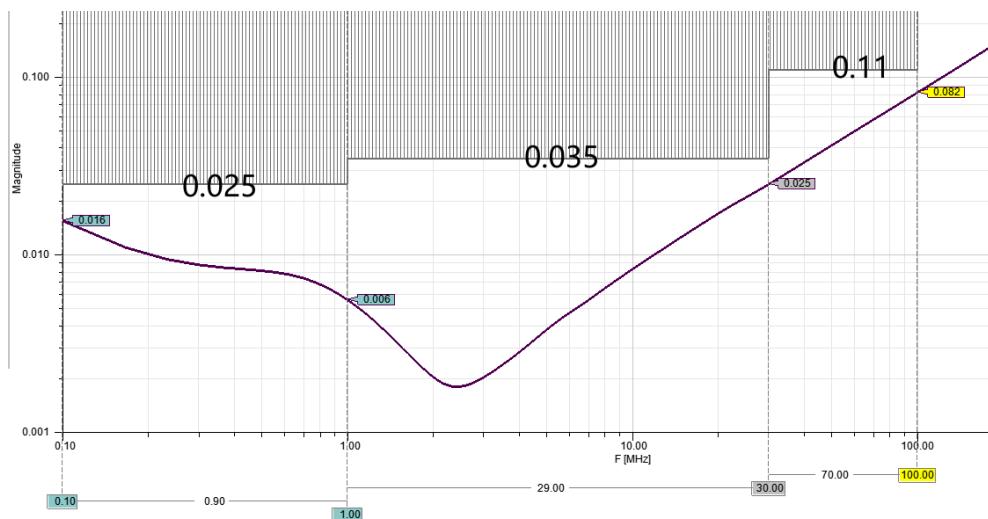


Figure 3-85 suggested PDN requirements for LIT power rails

3.4.2.10 RK3588 VDD_VDENC Power PCB Design

The copper cladding width of VDD_VDENC needs to meet the current requirements of the chip. The copper cladding connected to the power pins of the chip is wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm the path connected to each power PIN pin of the CPU. are enough.

When the power supply of VDD_VDENC is changed on the periphery, it is necessary to make as many power supply vias (9 or more 0.5*0.3mm vias) as possible to reduce the voltage drop caused by the changed layer vias; the GND vias of the decoupling capacitors should be Keep the same number as its power supply vias, otherwise the capacitance effect will be greatly reduced.

For the power pins of the VDD_VDENC chip of RK3588, there is a corresponding via hole near each Ball, and the top layer is in a "#" shape and cross-connected. The recommended line width is 10mil.

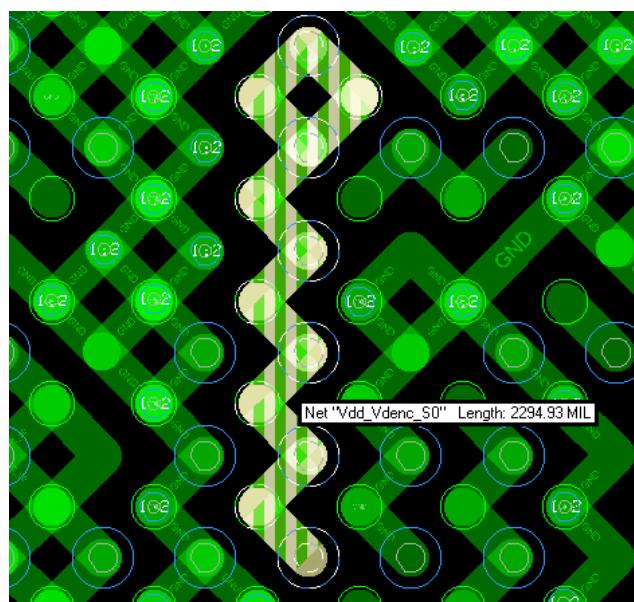


Figure 3-86 RK3588 VDD_VDENC Power Pin Traces and Vias

The decoupling capacitors close to the VDD_VDENC power pins of the RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.

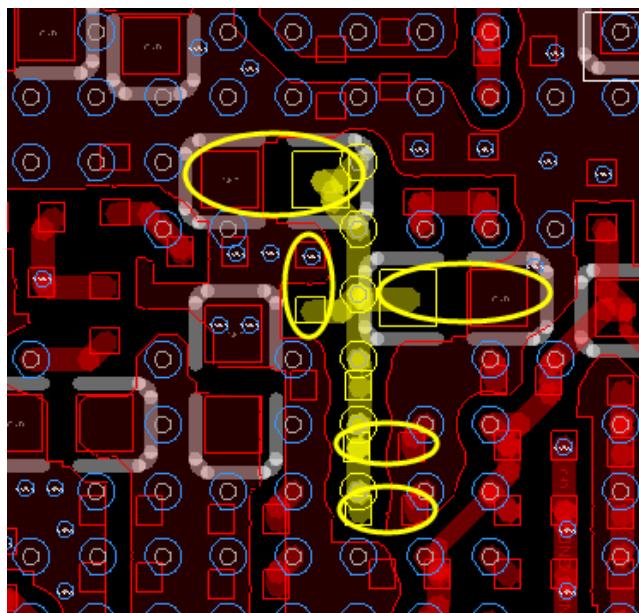


Figure 3-87 Distribution of Decoupling Capacitors on the Back of Power Pins of RK3588 VDD_VDENC

For VDD_VDENC power, the copper width of the CPU area should be greater than 120mil, and the effective overcurrent width needs to be $\geq 65\text{mil}$. The width of the peripheral area is recommended to be greater than 300mil. There should be at least one layer of power planes and one layer of adjacent GND return planes. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-84 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5\text{mil}$.

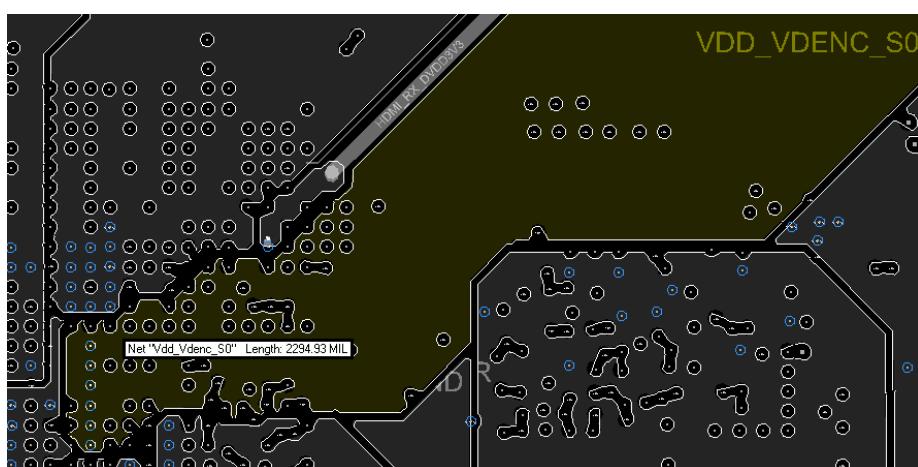


Figure 3-88 RK3588 VDD_VDENC Power Layer Copper Cladding

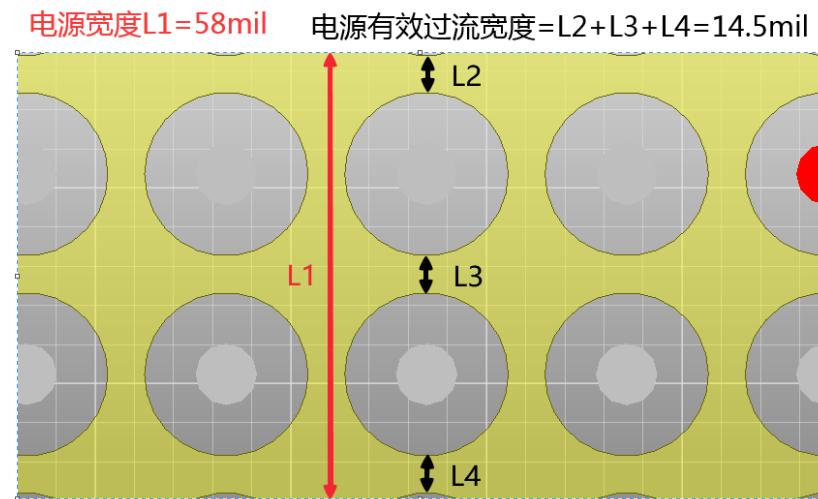


Figure 3-89 Schematic of the Effective Overcurrent Width of the Power Supply

In the CPU area, the number of GND vias within the 30mil range of power vias (the distance from the center of the via to the center of the via) is recommended to be ≥ 8 .

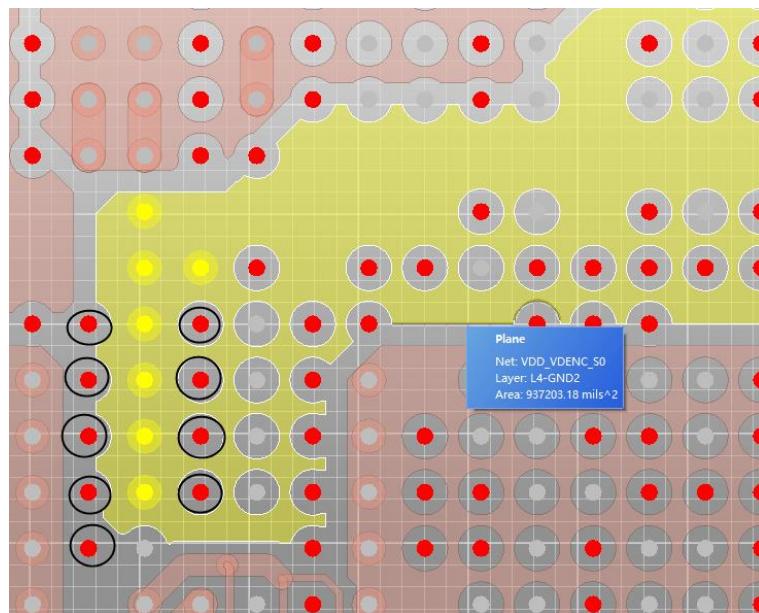


Figure 3-90 VDENC power ground via placement diagram

The suggested PND target impedance value of VDENC power rail is as follow:

Table 3-12 The suggested PND target impedance value of VDENC power rail

Frequency	impedance value (ohm)
100Khz~1Mhz	≤ 0.03
1Mhz ~30Mhz	≤ 0.04
30Mhz~100Mhz	≤ 0.14

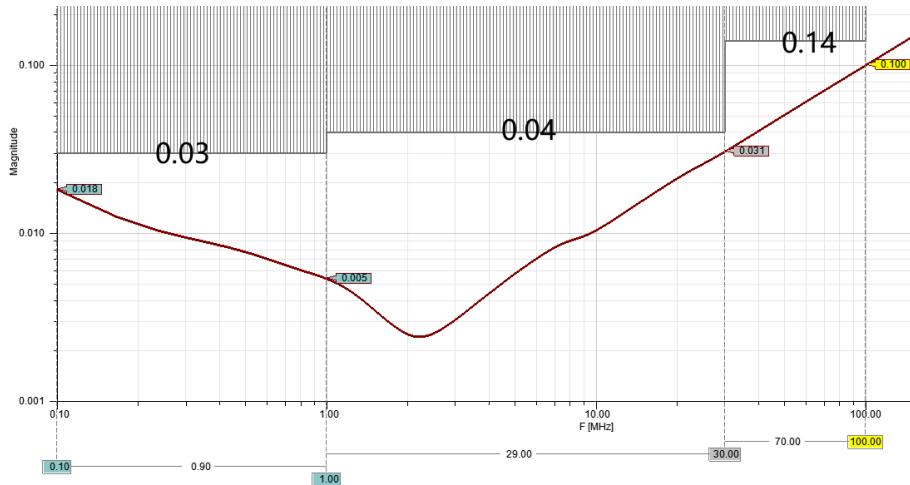


Figure 3-91 Suggested PDN requirements for VDENC Power rails

3.4.2.11 RK3588 VCC_DDR Power PCB Design

The copper cladding width of VCC_DDR needs to meet the current requirements of the chip. The copper cladding connected to the power pins of the chip is wide enough, and the path cannot be divided too seriously by vias. The effective line width must be calculated to confirm the path connected to each power pin of the CPU. are enough.

When the power supply of VCC_DDR is changed on the periphery, it is necessary to make as many power supply vias (9 or more 0.5*0.3mm vias) as possible to reduce the voltage drop caused by the changed layer vias; the GND vias of the decoupling capacitors should be Keep the same number as its power supply vias, otherwise the capacitance effect will be greatly reduced.

RK3588 chip VCC_DDR (VCC_DDR/VDDQ_DDR) power supply pins, each power supply needs ≥ 10 power supply vias, and the top layer is in a "#" shape and cross-connected. The recommended line width is 10mil.



Figure 3-92 Power pin traces and vias of RK3588 chip VCC_DDR&VDDQ_DDR

When LPDDR4x mode:

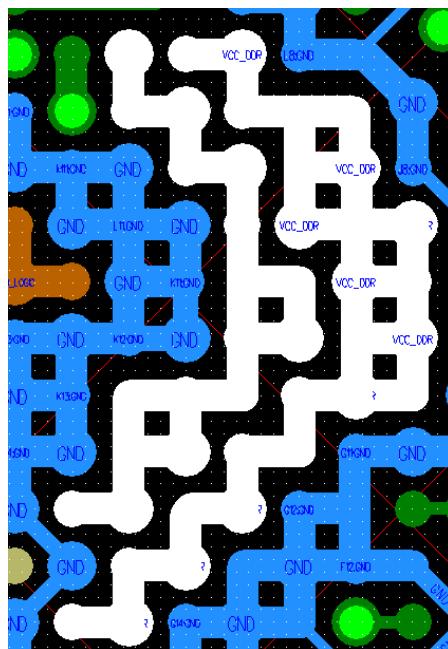


Figure 3-93 Power Pin Traces and Vias of VCC_DDR/VCC0V6_DDR in K3588 LPDDR4x Mode

The decoupling capacitors close to the VCC_DDR power pins of the RK3588 must be placed on the back of the corresponding power pins, the GND pad of the capacitors should be placed as close as possible to the GND Ball in the center of the chip, and the rest of the decoupling capacitors should be placed as close to the RK3588 as possible.

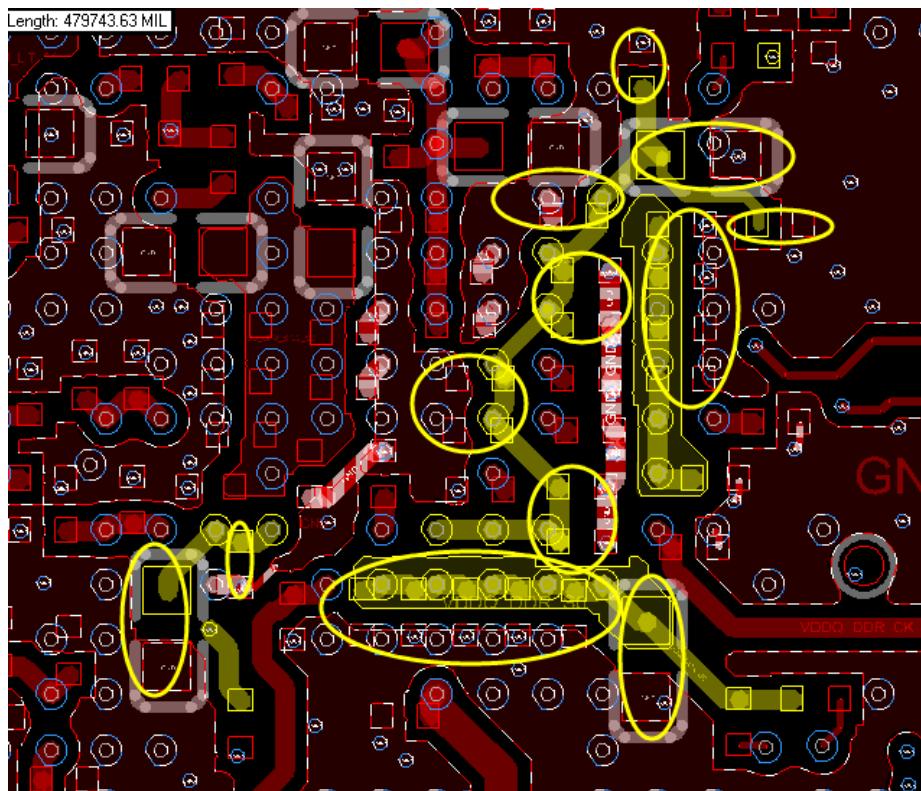


Figure 3-94 Distribution of Decoupling Capacitors on the Back of Power Pins of RK3588 VCC_DDR&VDDQ_DDR

The line width of VCC_DDR and VDDQ_DDR power supply in the CPU area is recommended to be greater than 120mil, and the effective overcurrent width of the power supply needs to be $\geq 55\text{mil}$; the width of the

peripheral area is recommended to be greater than 200mil. A power plane and an adjacent GND return plane are required. On the one hand, the function of the plane can reduce the voltage drop, and on the other hand, the plane capacitance between the power plane and the GND plane of the adjacent layer can effectively reduce the high-frequency PDN. It is recommended to use one ounce of copper for the power supply, which helps to reduce the current density.

The power plane will be destroyed by the via anti-pad. When designing the PCB, pay attention to adjusting the positions of other signal vias so that the effective width of the power supply meets the requirements. L1 in the Figure3-90 shows the power copper skin width is 58 mil. Since the anti-pad of the via hole will destroy the copper skin, the actual effective overcurrent width is only $L2+L3+L4=14.5\text{mil}$.

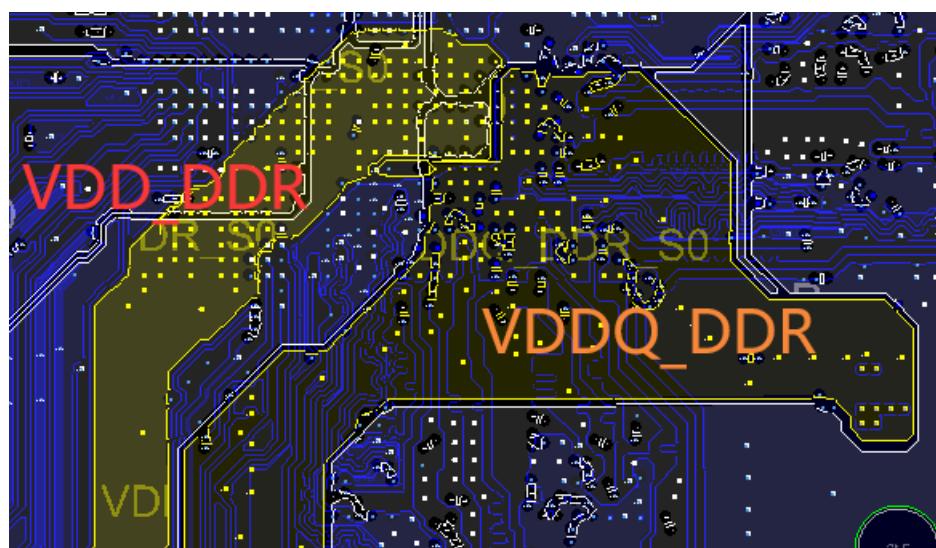


Figure 3-95 RK3588 VCC_DDR&VDDQ_DDR Power Layer Copper Cladding

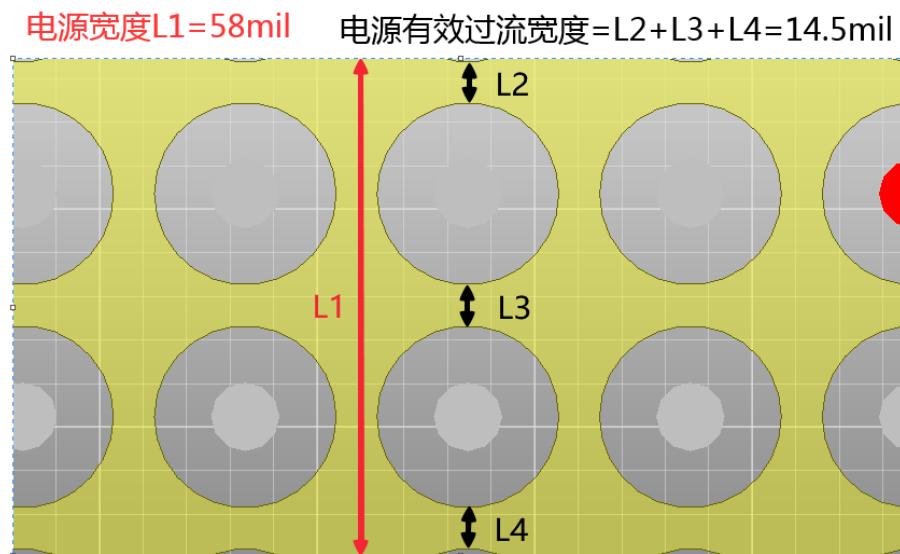


Figure 3-96 Schematic of the Effective Overcurrent Width of the Power Supply

3.4.2.12 RK3588 GND Pin PCB Design

For the GND pin of the RK3588 chip, at least ensure that every 1.5 balls needs to correspond to one via hole, and try to correspond to one via hole for each ball to provide better SI and PI conditions, and also help with heat dissipation.

The adjacent layer of the RK3588 chip must be a complete GND plane to ensure that the main reference ground is close to the Ball of the CPU, which is used to ensure power integrity and strengthen the heat dissipation of the PCB.

The GND Ball of the same network under the RK3588 chip is in a "井" shape on the top layer and cross-connected. The recommended line width is 10mil.

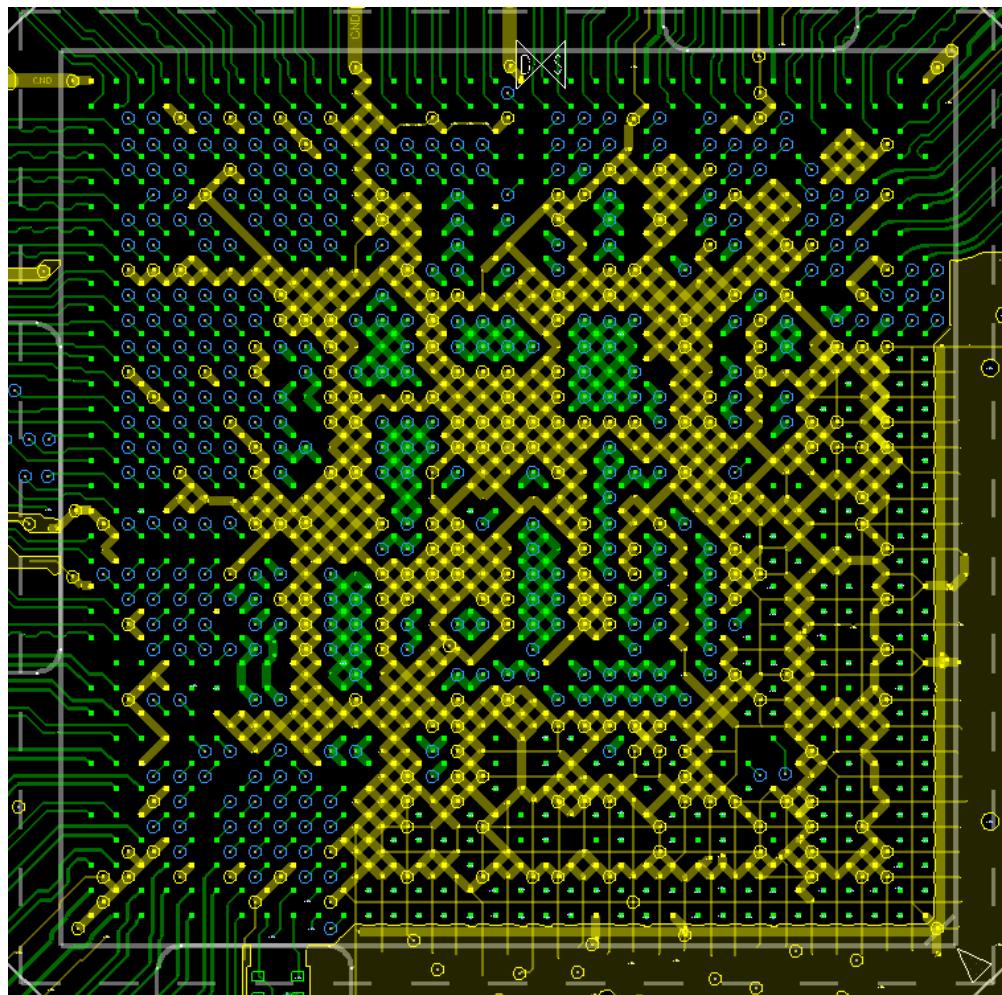


Figure 3-97 Pin Traces and Vias of RK3588 VSS

During Layout, when each signal of RK3588 is placed in layer-changing vias, it is required to be placed in the middle of the Ball interval, and it must be placed regularly, as shown in the figure, the copper cladding of the GND layer, the ground in the middle of the RK3588 chip has a large area of copper. The connection between the skin and the outer copper skin is beneficial to the power supply and signal integrity on the one hand, and it is beneficial to the heat dissipation of the chip on the other hand.

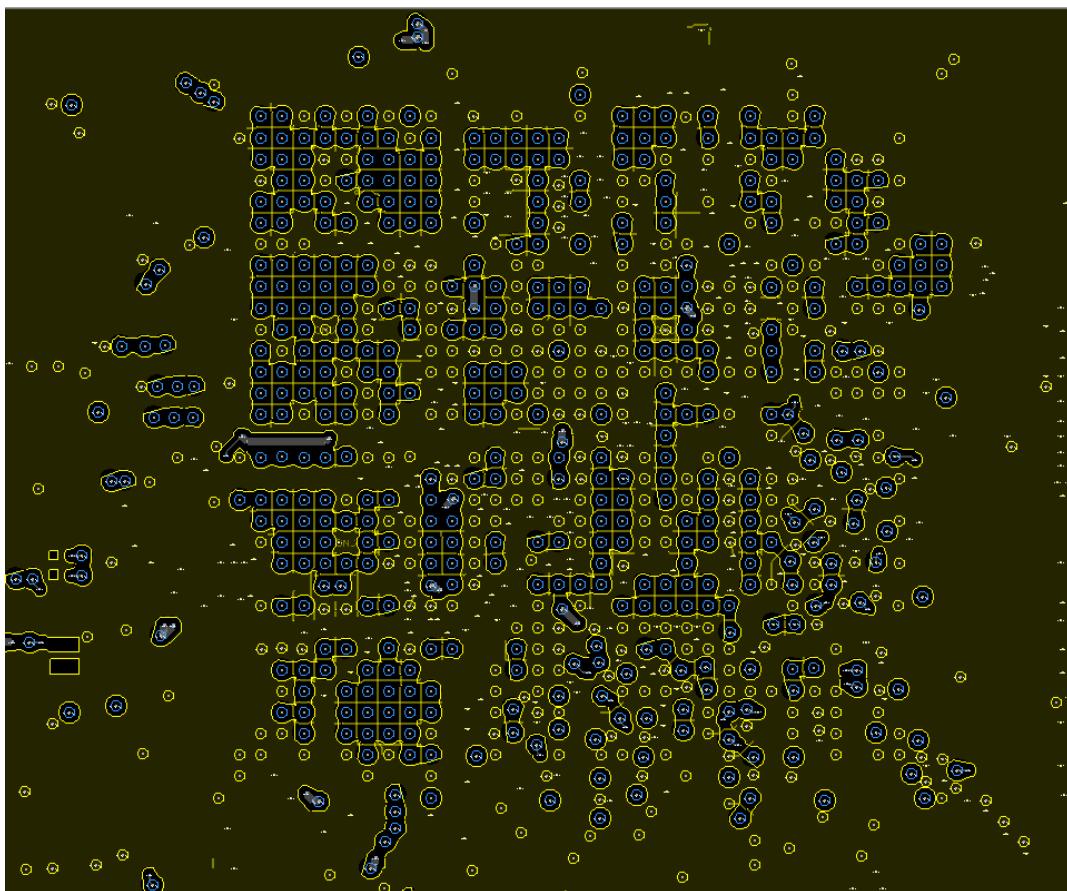


Figure 3-98 RK3588 Ground Layer Copper Cladding

3.4.2.13 PCB Design of Other Power Supplies for RK3588

The decoupling capacitors of other power supplies of RK3588 must be placed on the back of the chip pins. When routing, try to form the capacitor pads first and then to the chip pins. One GND pad of the capacitor is recommended to correspond to one GND via hole. In the worst case, at least two GND pads should have one GND via hole. Worst-case designs should be used as little as possible.

3.4.3 DRAM Circuit PCB Design

The performance of 10-layer HDI PCB board with LPDDR4 and LPDDR4X interfaces is better than 8-layer PTH PCB board. It is recommended to choose 10-layer HDI PCB board first. The LPDDR5 interface template is a 10-layer HDI PCB board.

3.4.3.1 DRAM Circuit PCB Design (10-Layer HDI PCB)

As RK3588 DDR interface operates up to 4266Mbps, the PCB design is difficult, so it is strongly recommended to use the DDR template and corresponding DDR firmware provided by RK. DDR templates are released after rigorous simulation and verification. If you do not use DDR templates and design PCB by yourself, please refer to the following PCB design suggestions, then perform simulation.

(1) The CPU GND pads should have enough vias, it is recommended to strictly refer to the template design. The GND vias cannot be deleted. For example, a 10-layer HDI first-order PCB template design is as shown in the figure below.

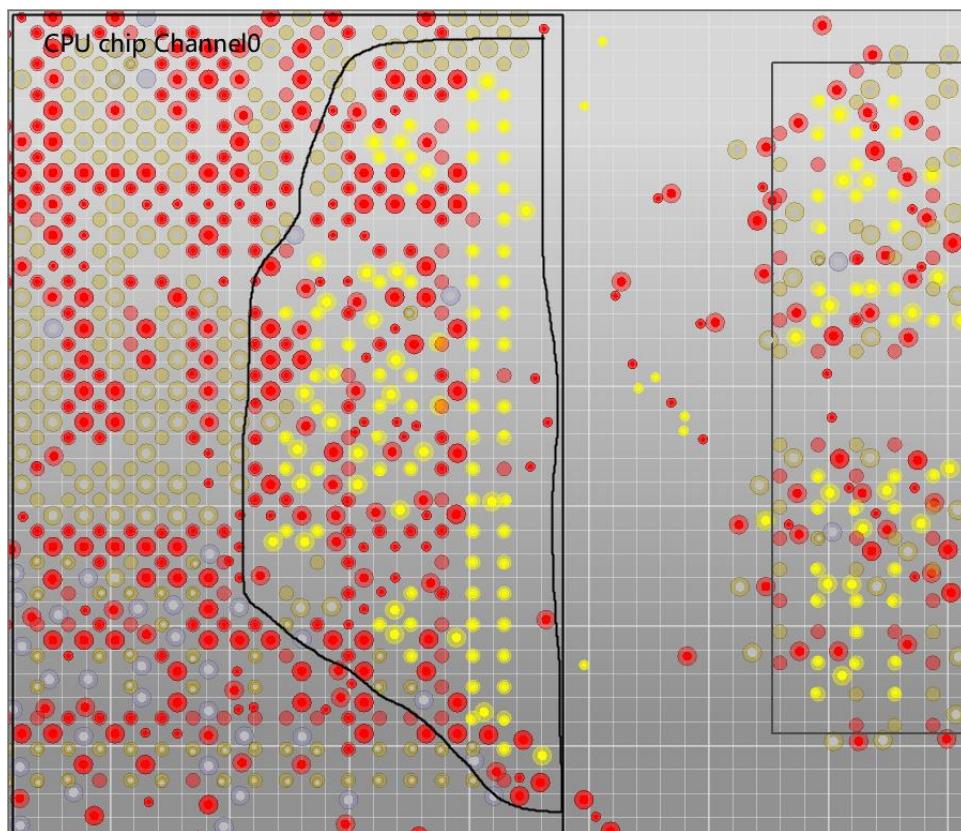


Figure 3-99 vias design of 10-layer HDI first-order PCB template SOC channel 0 area

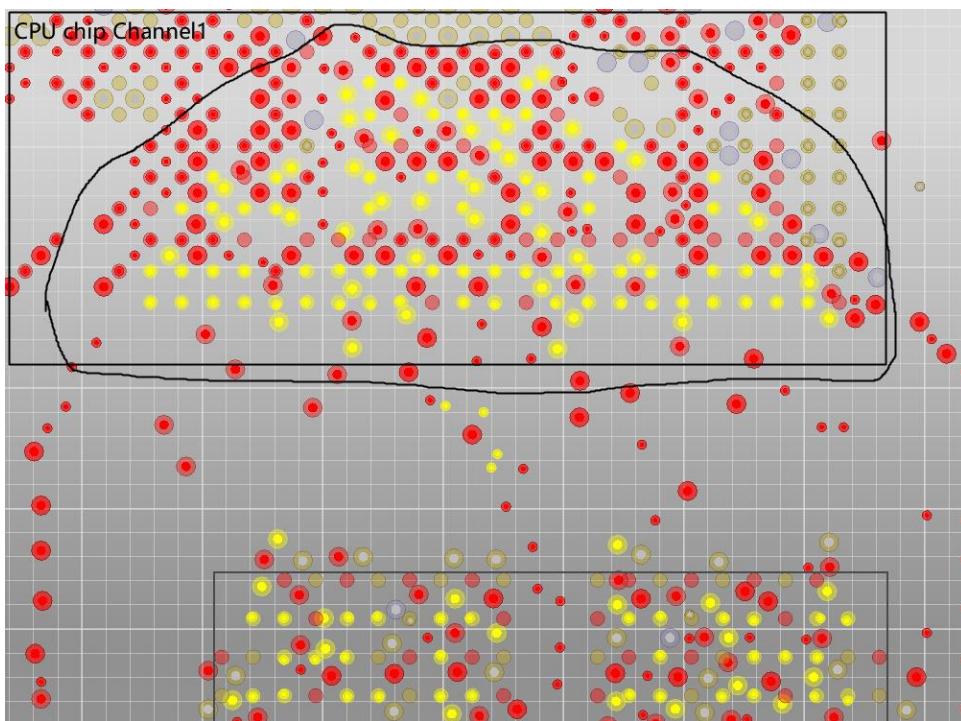


Figure 3-100 vias design of 10-layer HDI first-order PCB template SOC channel 1 area

(2) If a signal trace changes layer and the reference plane is GND, stitching GND vias should be added close to the layer change vias within 25 mils. One Signal via should have \geq one GND via. Increase GND via as much as you can.

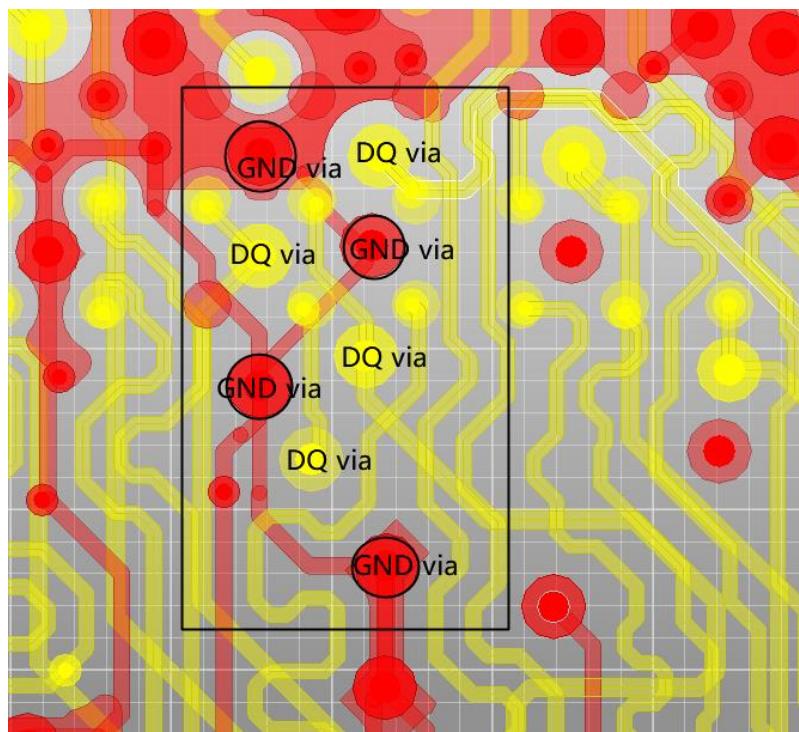


Figure 3-101 Schematic of the GND via corresponding to the signal via

(3) GND vias recommend to be placed between signal vias. Four signal vias together is not recommended. Use GND vias to separate signal vias as shown in the figure below, will improve performance.

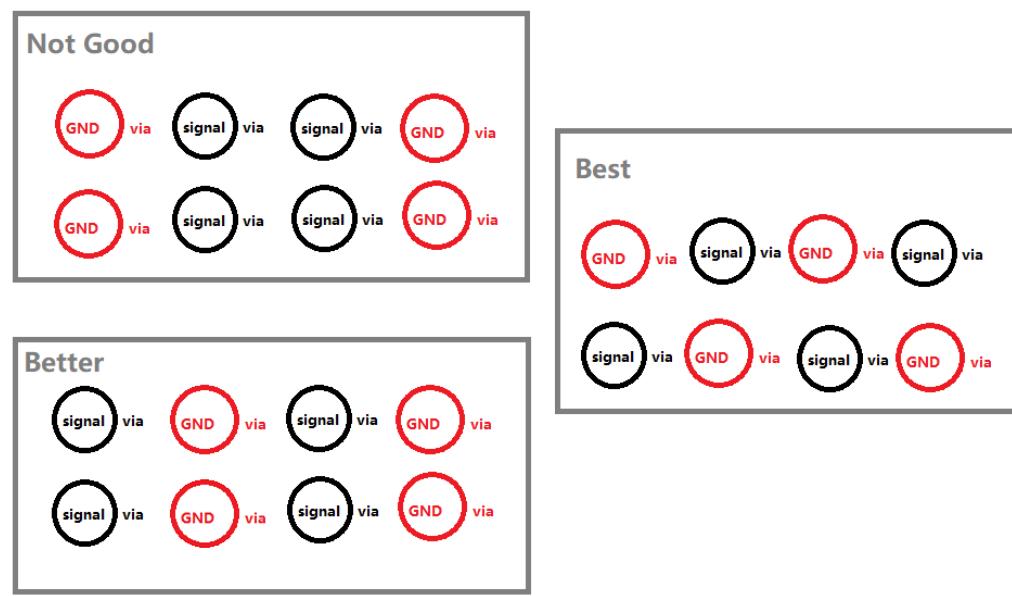


Figure 3-102 Schematic of different via design

(4) DQ and DQS signals should route all traces over continuous GND planes, with no interruptions. Any discontinuity or split in the ground plane can cause signal reflections and should be avoided. Command and control signals are recommended to preferably refer to a solid GND plane. when the command and control signals routed

to the inner layer with one GND continuous reference plane and one power reference plane, 100nF stitching capacitor recommended to be added.

(5) Avoid return path discontinuities such as a slit, you can optimize the reference layer with GND traces.

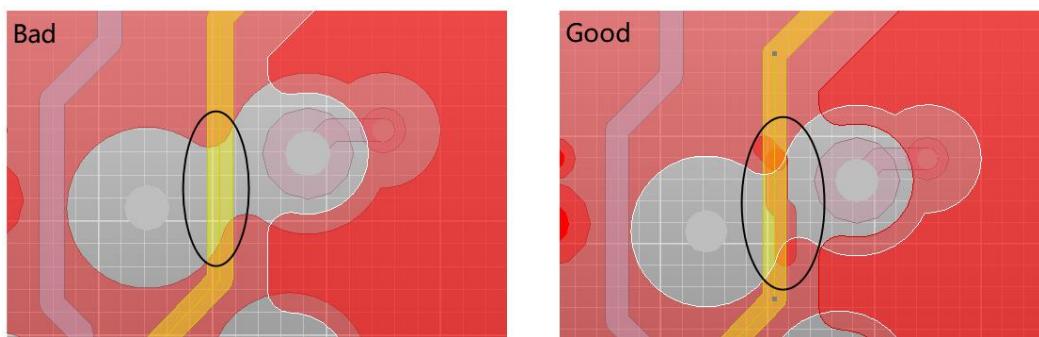


Figure 3-103 GND traces optimization the reference layer

(6) The recommended distance between the trace and the edge of the reference layer is ≥ 12 mil.



Figure 3-104 the distance between the trace and the edge of the reference layer

(7) Micro-strip line and strip-line propagation delay is difference. Differential micro-strip signals have a shorter flight time than single-ended micro-strip signals. Thus DQ, DQS, CLK, and WCLK signals recommended to be routed to the inner layer. The CKE signal is recommended to go on the surface layer to better meet the target impedance of 50 ohms, and other Command lines and control lines recommended to be routed to the inner layer.

(8) An adequate spacing should be maintained between the inside traces of a bend. Recommend 3times the trace width or greater($S \geq 3W$).

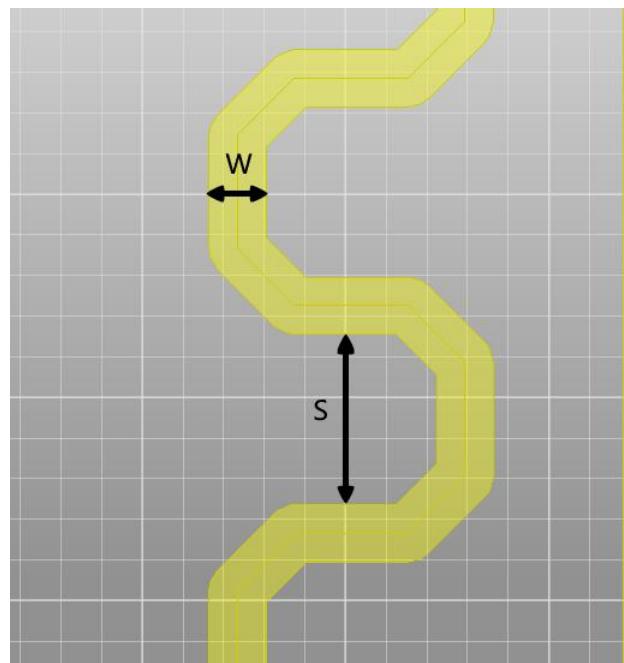


Figure 3-105 adequate spacing

(9) The propagation delay associated with vias should be accounted for in the trace length.

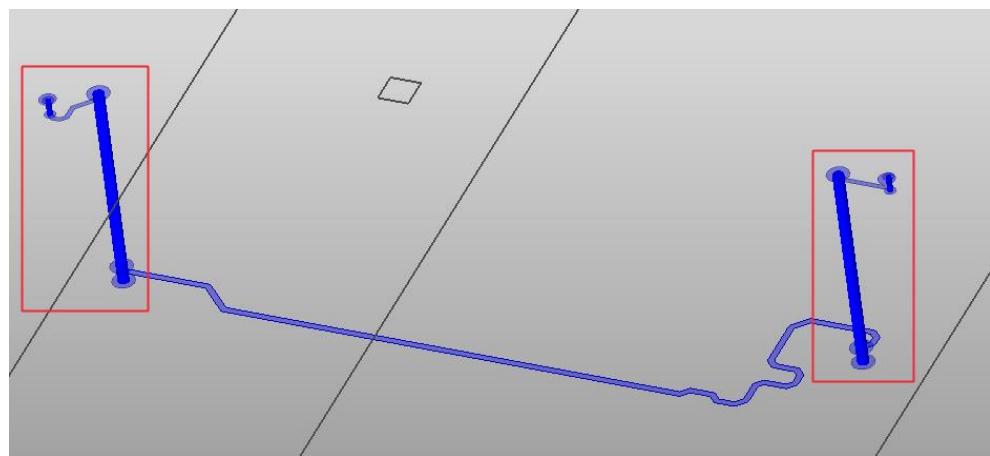


Figure 3-106 Schematic of vias length

(10) One via per GND pad of Dram chip. Add GND vias as much as you can.

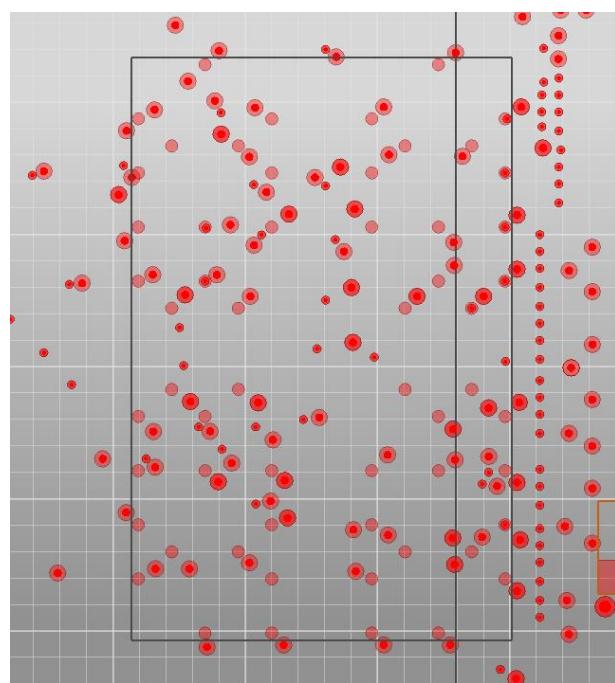


Figure 3-107 Schematic of the number of GND vias

(11) Remove unused via pads, because they cause unwanted capacitance and destroy plane.

(12) The closer the trace is to the via, the worse the reference plane is. Recommend route trace far away ($\geq 8\text{mil}$) from the via pad.

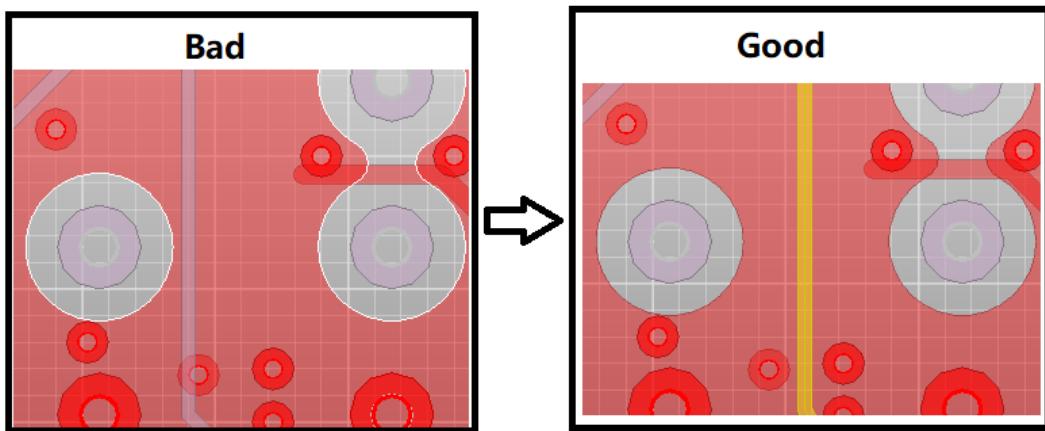


Figure 3-108 Recommended spacing for traces and via pads

(13) Avoid making slits of plane due to the via clearance as possible.

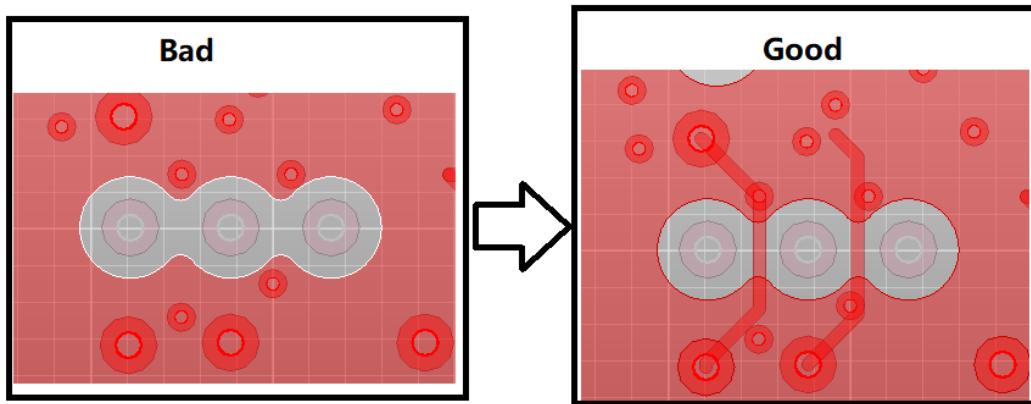


Figure 3-109 Schematic of route optimization plane slits

(14) DQS,CLK,WCLK signal should use ground shielding for the entire trace including vias. Recommend ground shielding line $\geq 400\text{mil}$, add one GND via.

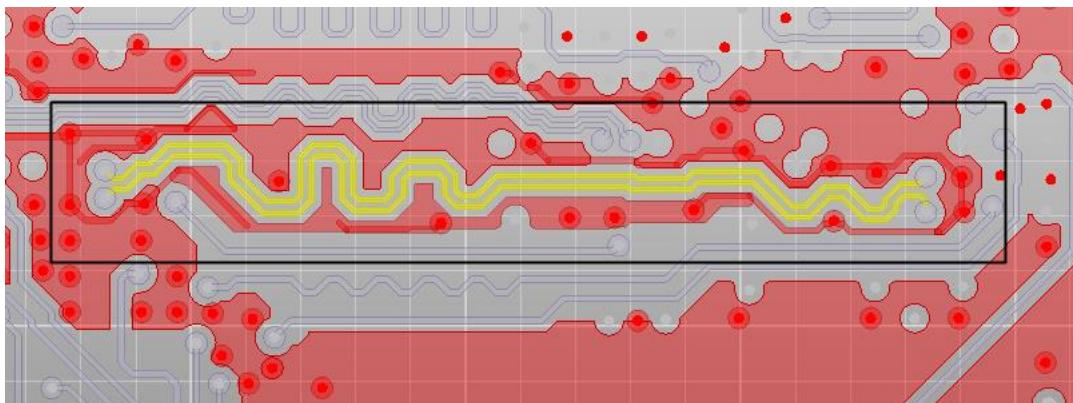


Figure 3-110 Schematic of ground shielding design

(15) For VCC_DDR_S0 power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.



Figure 3-111 the vias requirement when power layer changed

(16) For VDDQ_DDR_S0 power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.

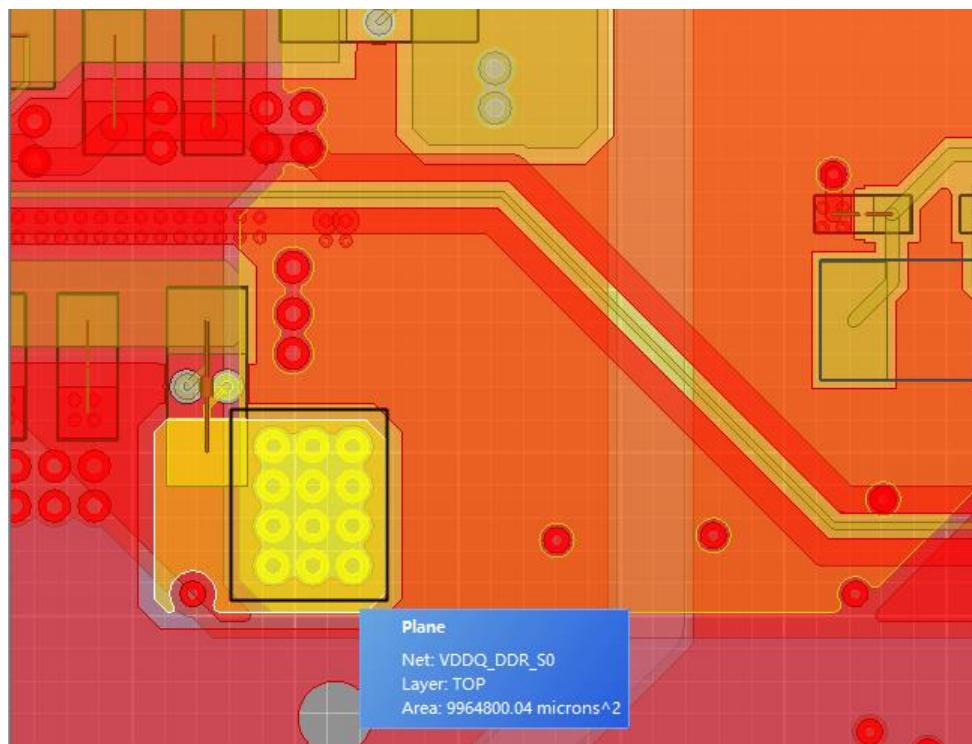


Figure 3-112 the vias requirement when power layer changed

(17) For VDD2_DDR_S3 and VDD2H_DDR_S3 power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.

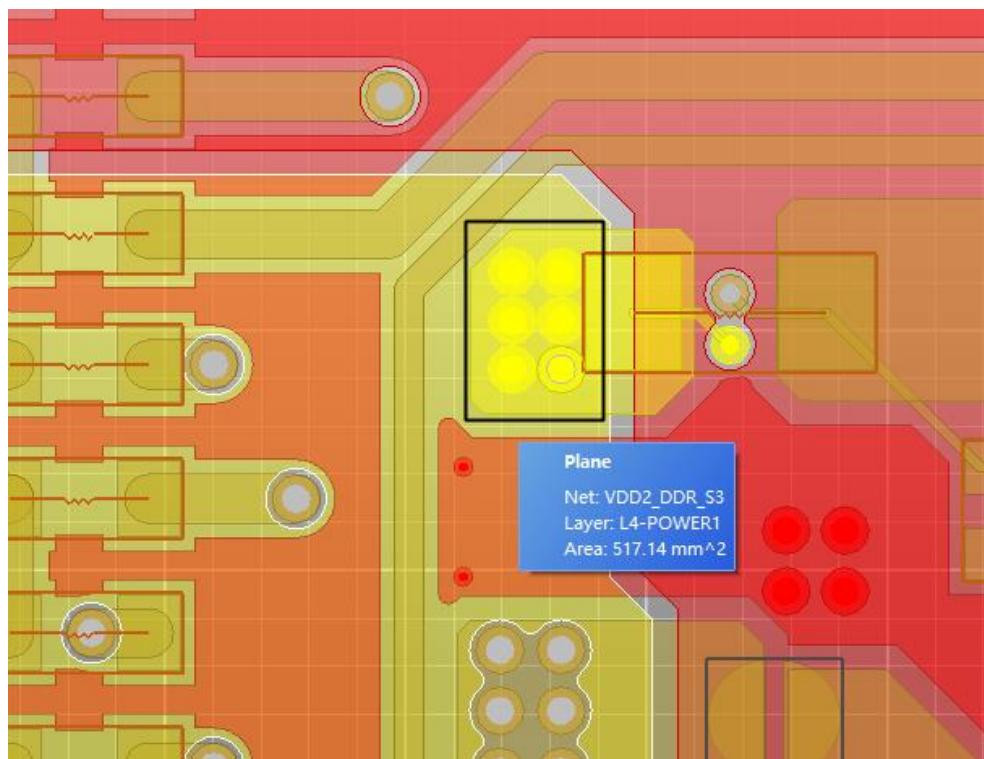


Figure 3-113 the vias requirement when power layer changed

(18) For VDD1_1V8_DDR power supply, it is recommended ≥ 2 vias(0402 via) when the power plane is changed.

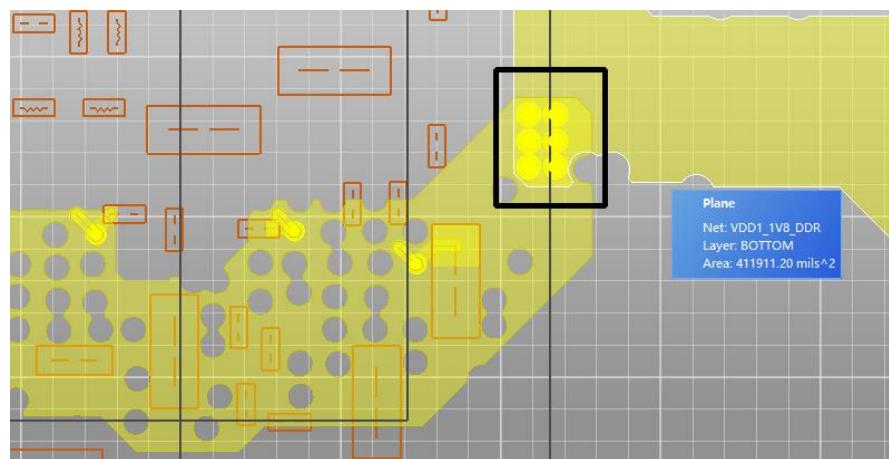


Figure 3-114 the vias requirement when power layer changed

(19) At least one via per pad of Capacitor. For 0603 or 0805 capacitors, it is recommended that one pad corresponds to two vias.

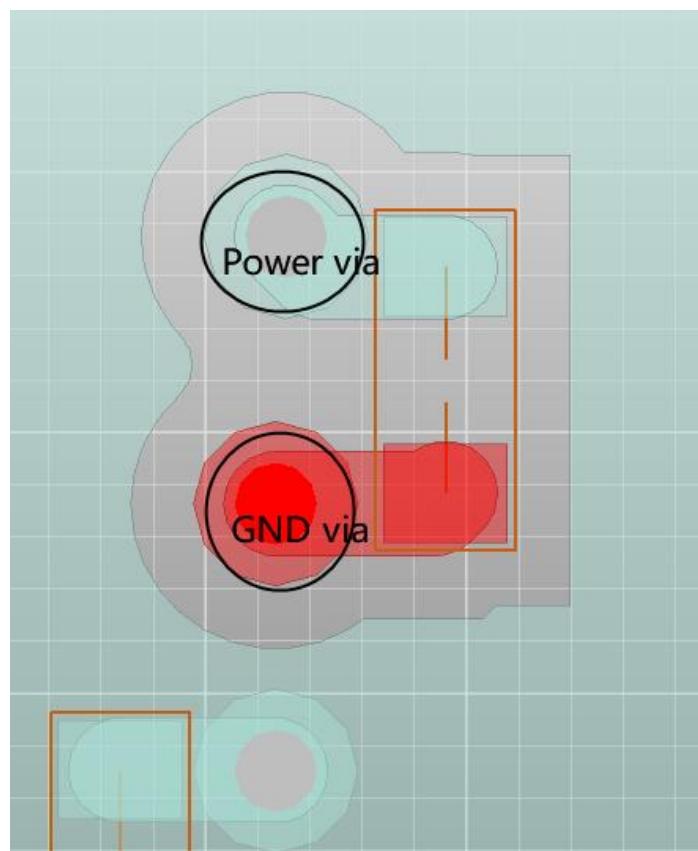


Figure 3-115 Number of vias corresponding to capacitor pads

(20) Place via closer to the pin to reduce the loop inductance.

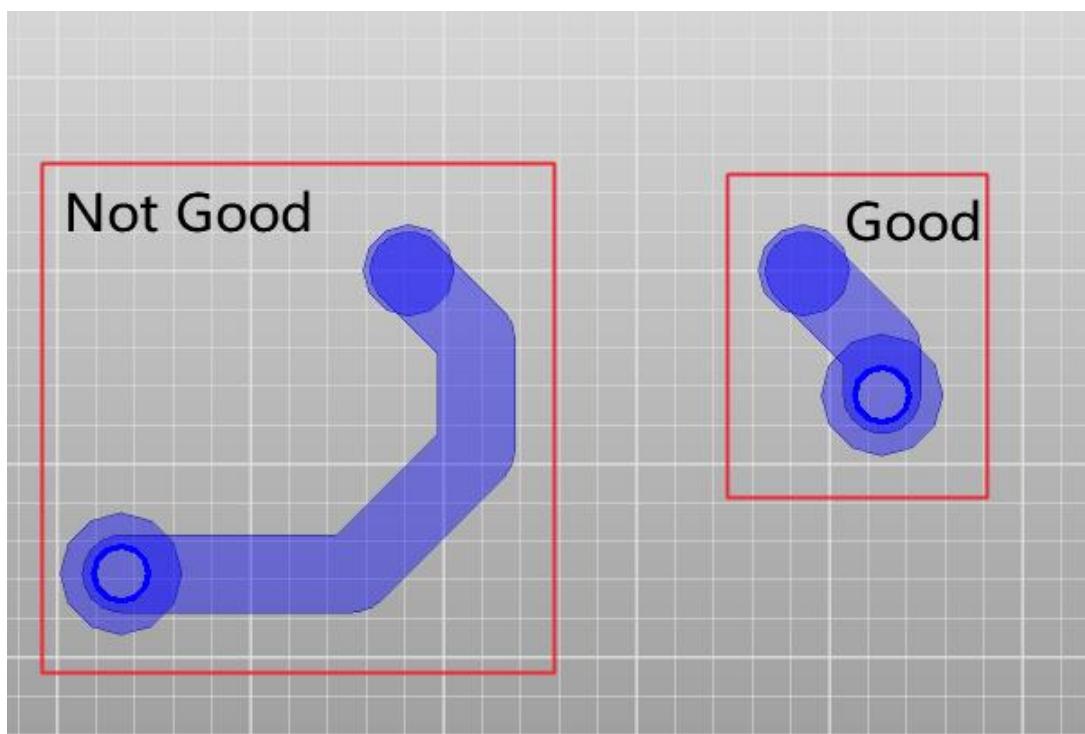


Figure 3-116 Schematic of placement of vias close to pins

(21) The number of power vias corresponding to the VDDQ_DDR_S0 and VDD_DDR_S0 pins of the CPU refer to the DDR template. It is not recommended to delete the power vias.

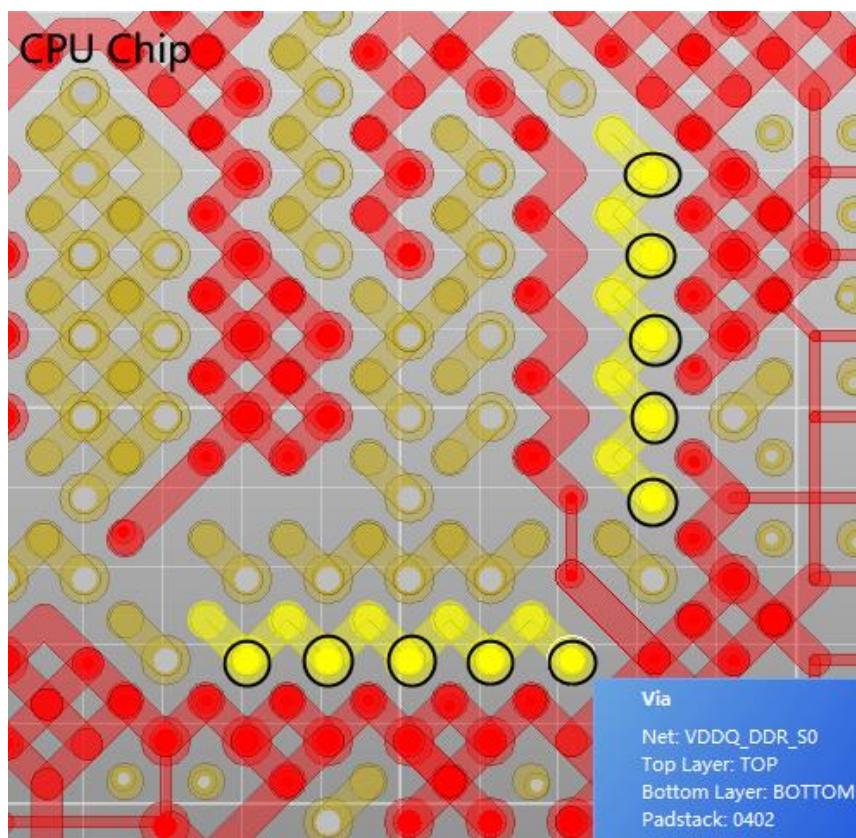


Figure 3-117 Requirements for the number of vias corresponding to the power pins

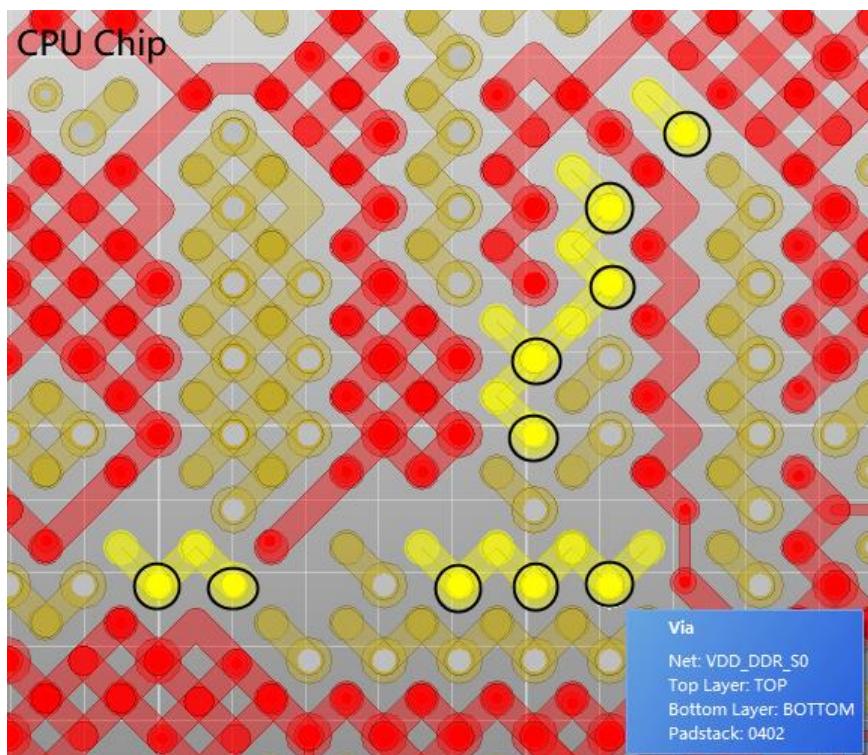


Figure 3-118 Requirements for the number of vias corresponding to the power pins

(22) VDDQ_DDR, VDD2_DDR_S3, VDD1_1V8_DDR power supply of DDR chip, it is recommended that one pin corresponds to one power via, for example as follows.

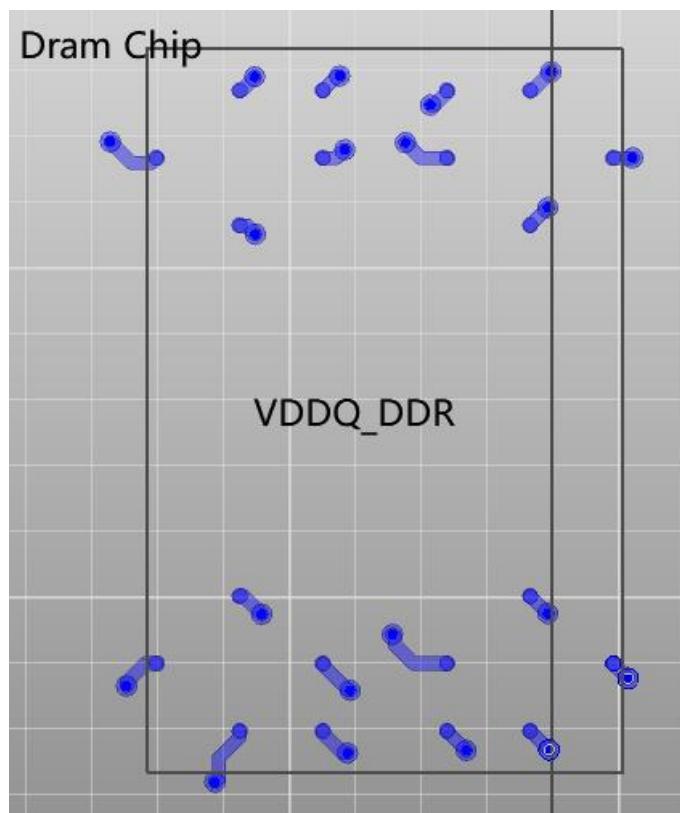


Figure 3-119 Requirements for the number of vias corresponding to the power pins

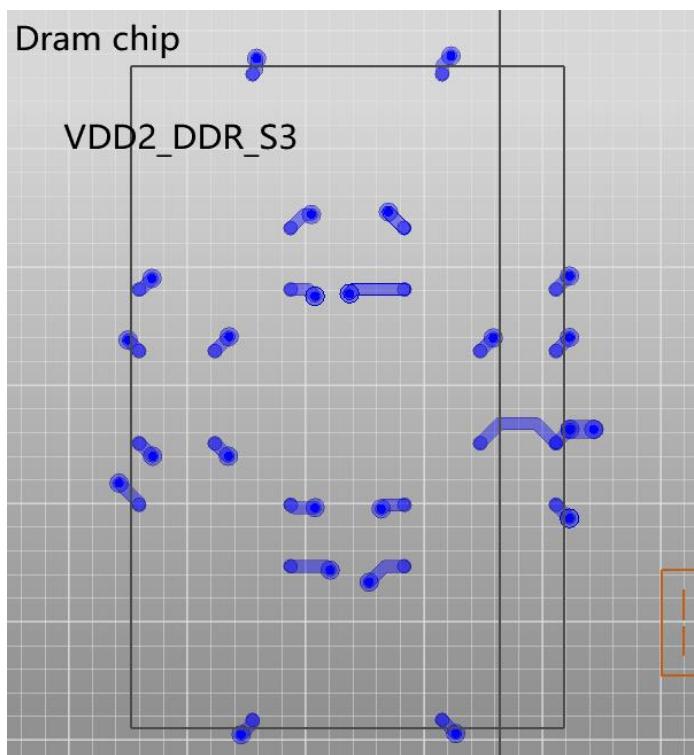


Figure 3-120 Requirements for the number of vias corresponding to the power pins

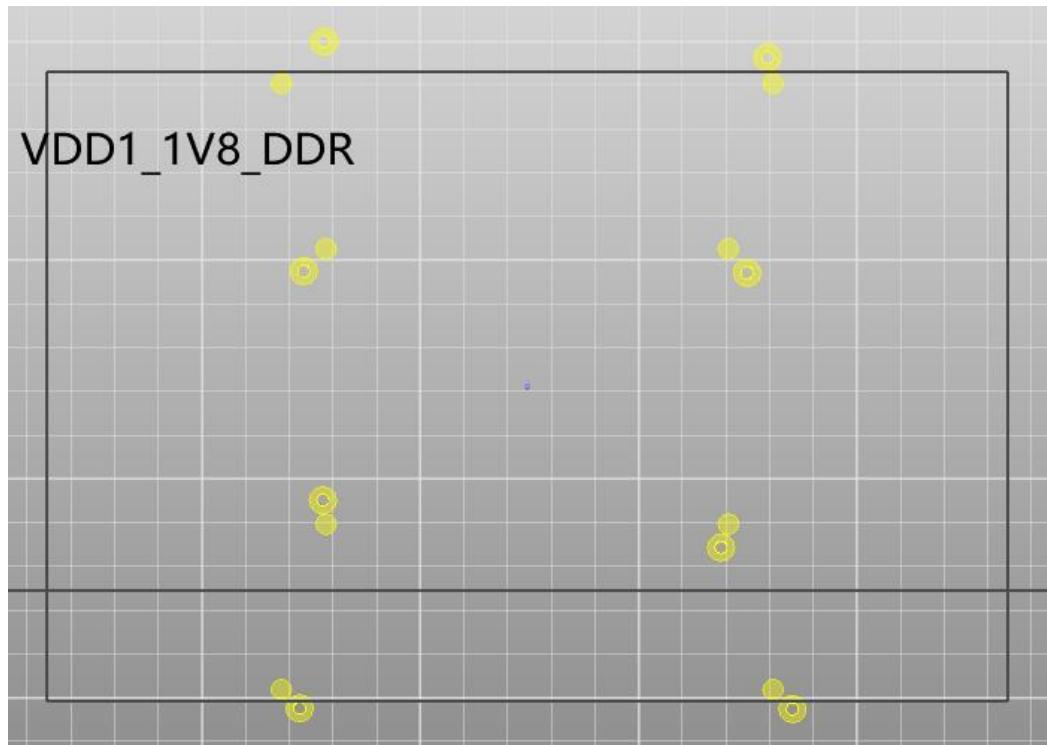


Figure 3-121 Requirements for the number of vias corresponding to the power pins

(23) For VDD2H_DDR_S3 power supply of DDR chip, it is recommended that each power supply pin has ≥ 0.7 power vias.

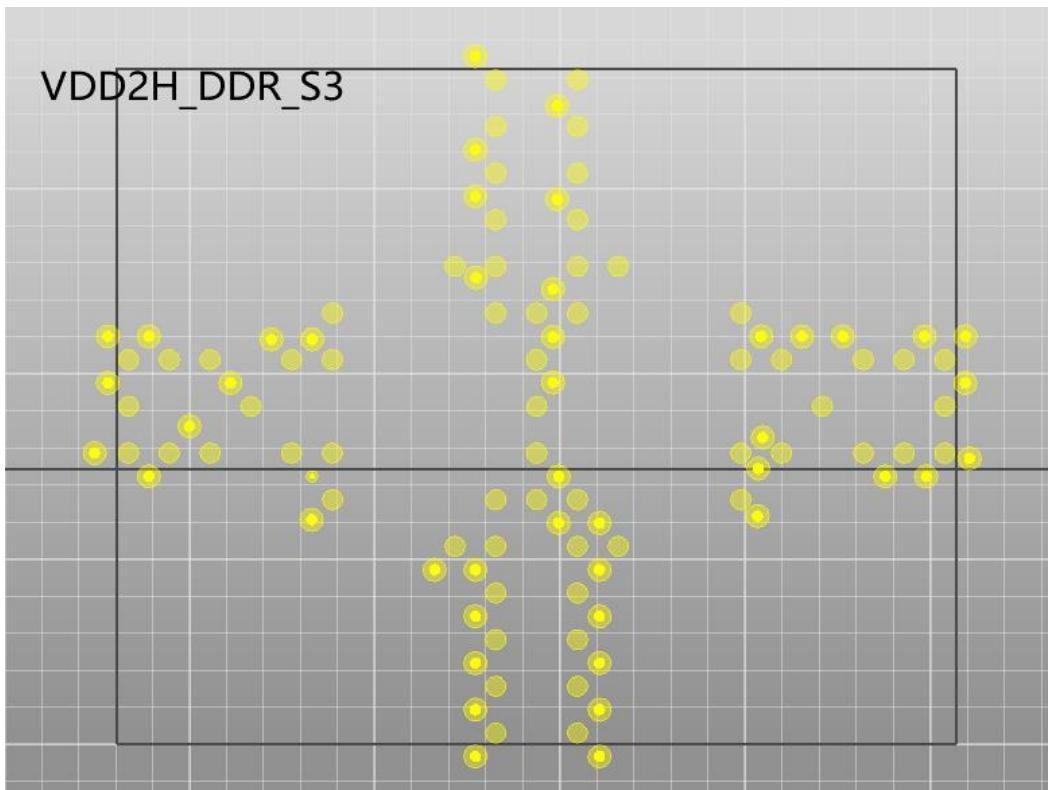


Figure 3-122 Requirements for the number of vias corresponding to the power pins

(24) The layer change of power should be minimized. When changing layers of DDR power supply (VDDQ_DDR, VDD2_DDR_S3, VDD_DDR, VDD2H_DDR_S3), enough power vias (≥ 8 0402 vias or 6 0503 vias) should be drilled, for example as follows.

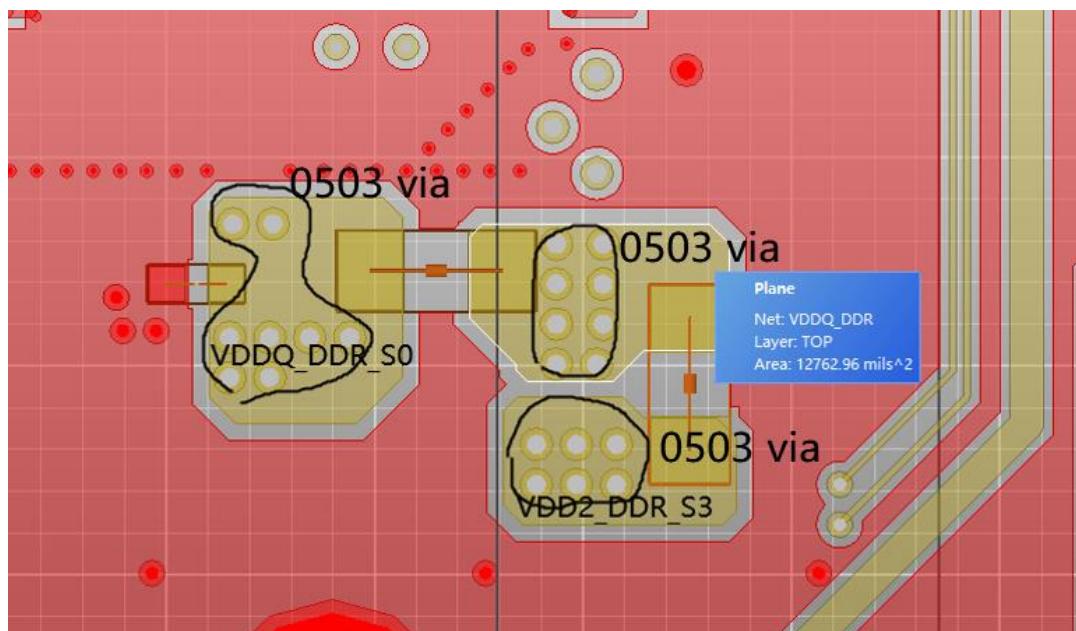


Figure 3-123 the vias requirement when power layer changed

(25) Avoid discontinuity in power plane by inserting other signal nets or matrix of vias with their associated anti-pads.

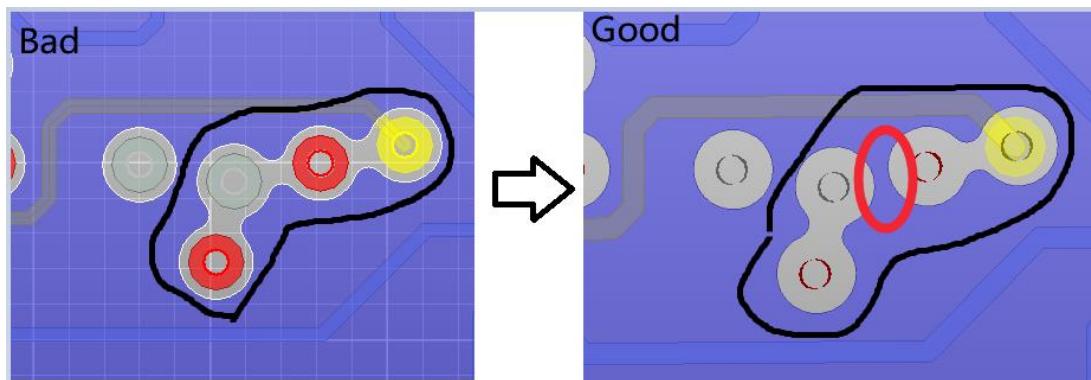


Figure 3-124 Schematic of preventing the power layer from being damaged by the row of vias

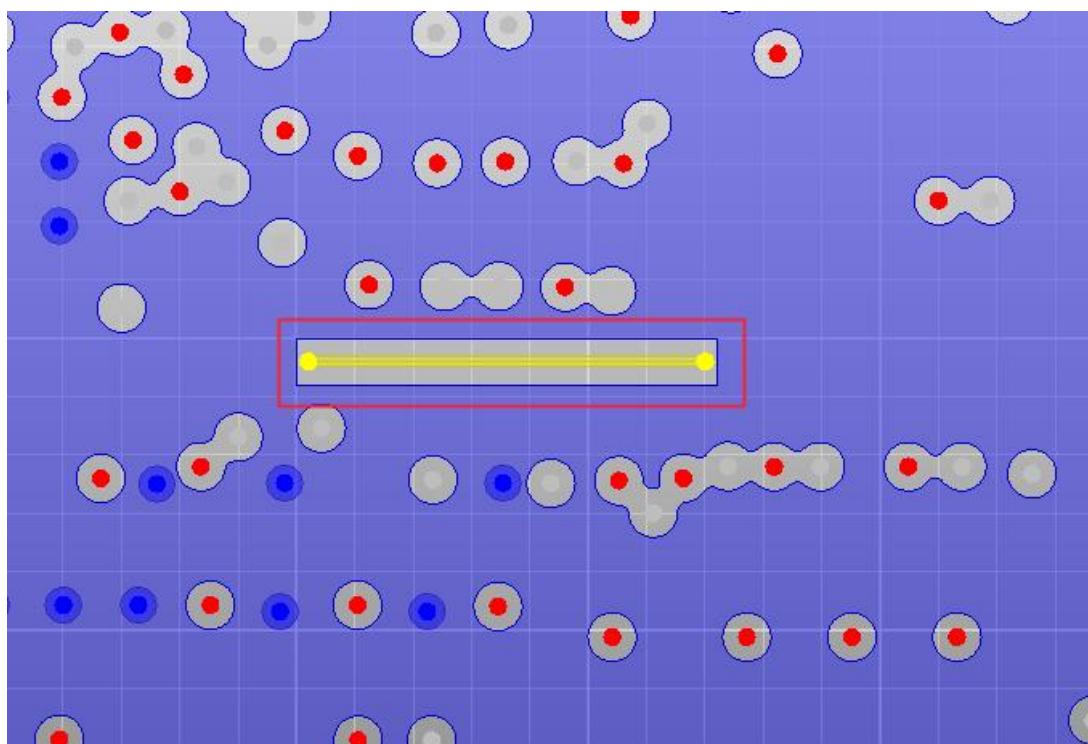


Figure 3-125 Schematic of the power plane being damaged by traces

(26) The decoupling capacitor should be placed close to the DDR chip pin, in order to reduce the loop inductance of the capacitors. The number of capacitors is recommended to refer to the DDR template design, and it is not recommended to delete the capacitors. Capacitors should be evenly placed.

(27) The recommended PDN requirement for the VDD_DDR_S0 power at the CPU area is as shown below.

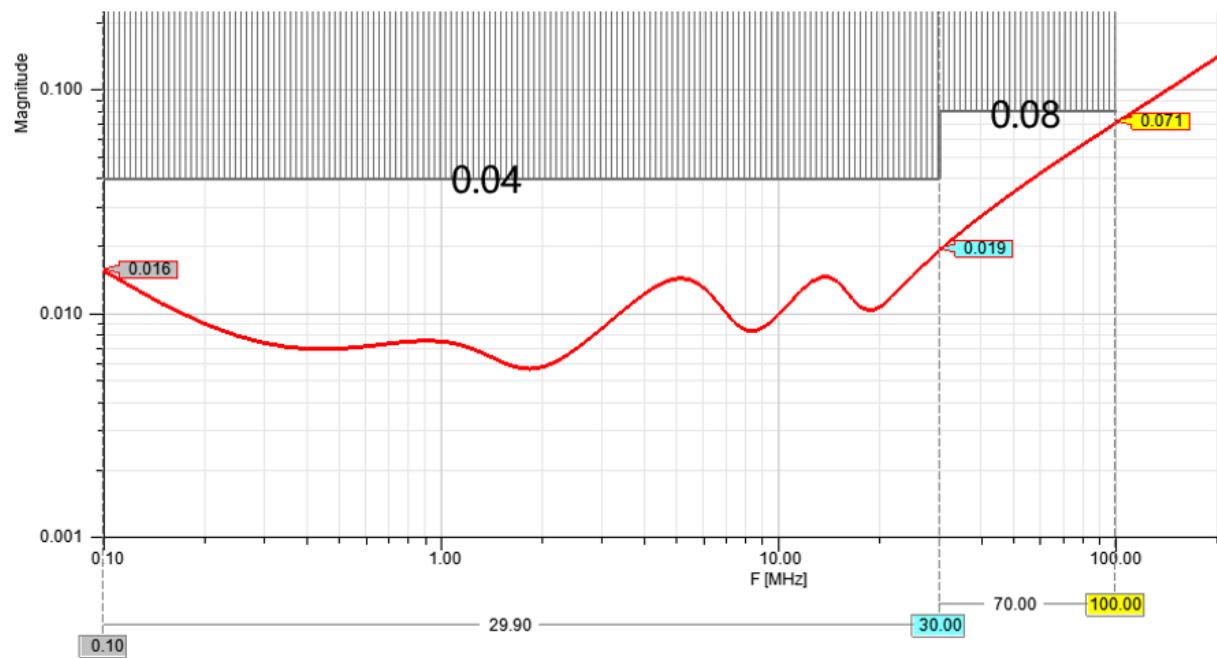


Figure 3-126 the recommended PDN requirements of VDD_DDR_S0 power supply

(28) The recommended PDN requirement for the VDDQ_DDR_S0 power at the CPU area is as shown below.

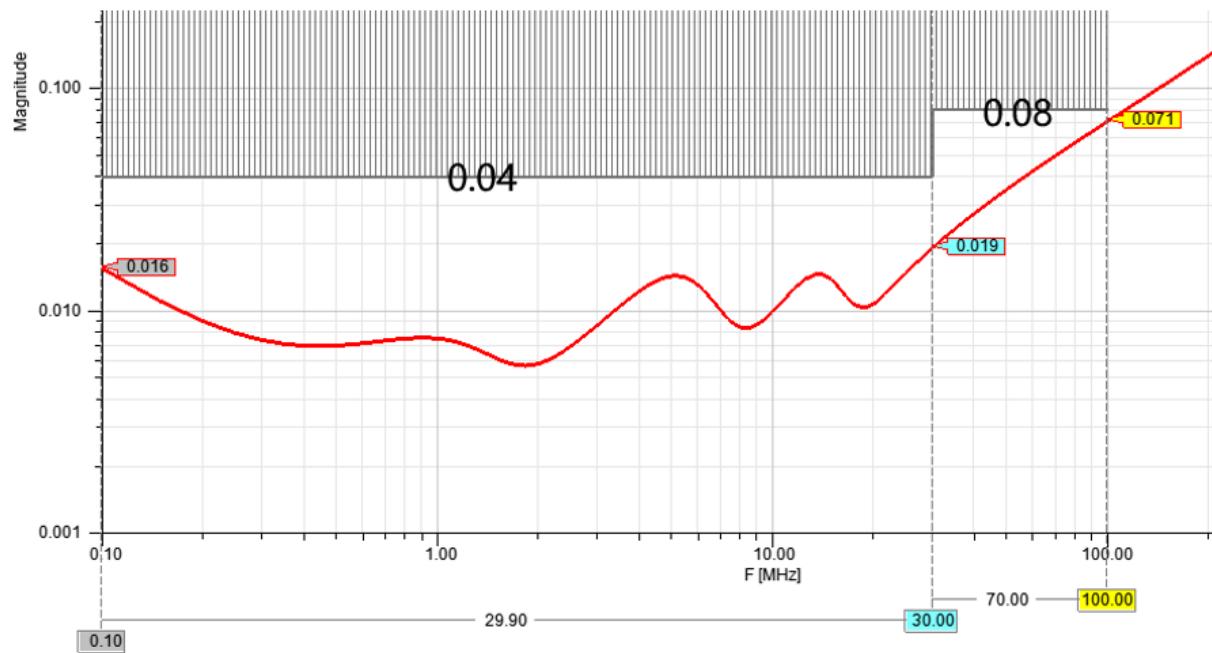


Figure 3-127 the recommended PDN requirements of VDDQ_DDR_S0 power supply

(29) The recommended PDN requirements for the VDDQ_DDR power at the DDR chip area are as follows.

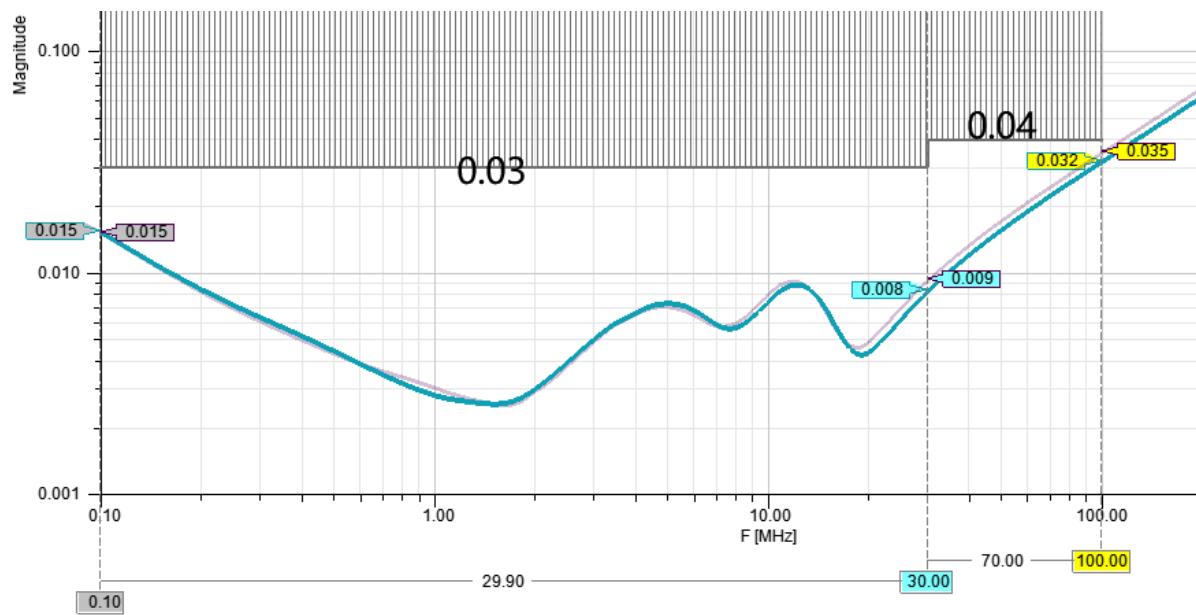


Figure 3-128 the recommended PDN requirements of VDDQ_DDR power supply

(30) The recommended PDN requirements for the VDD2_DDR_S3 power at the DDR chip area are as follows.

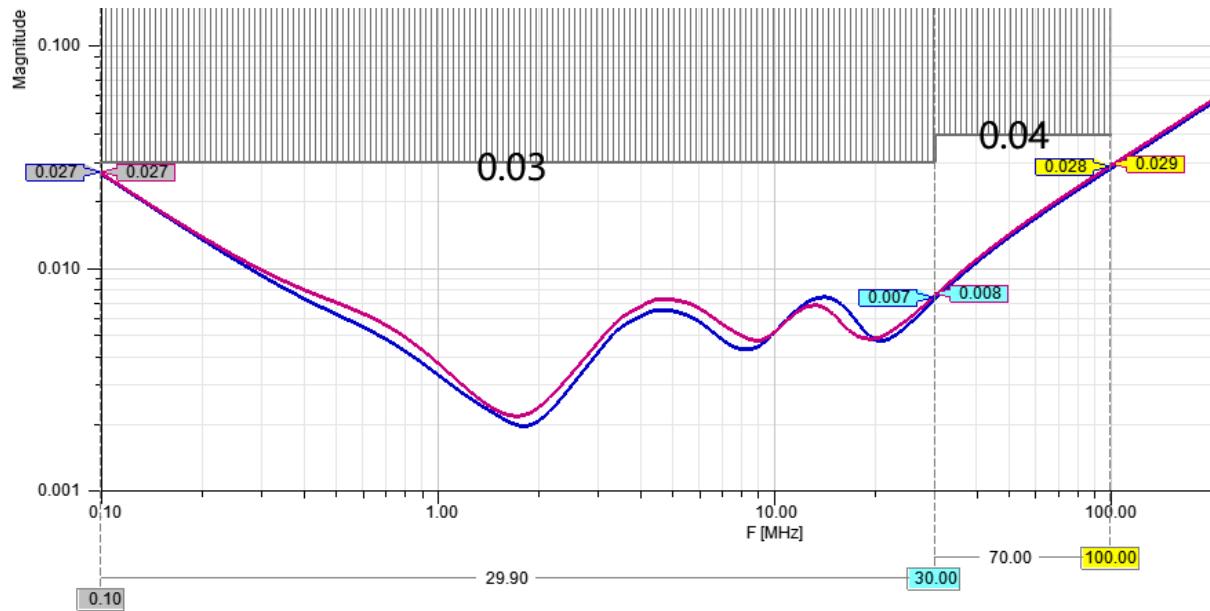


Figure 3-129 the recommended PDN requirements of VDD2_DDR_S3 power supply

(31) The recommended PDN requirements for the VDD2H_DDR_S3 power at DDR chip area are as follows.

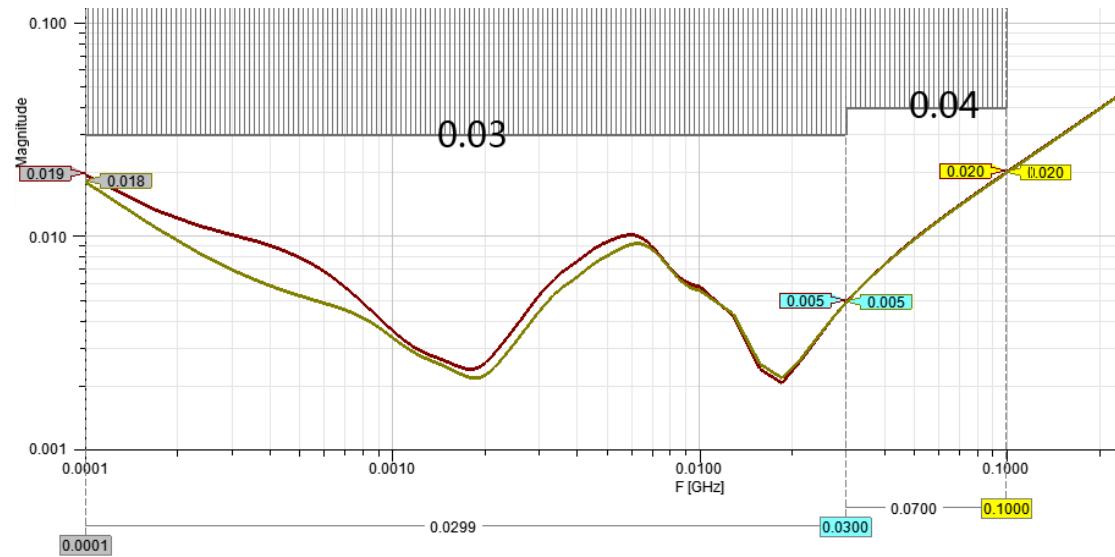


Figure 3-130 the recommended PDN requirements of VDD2H_DDR_S3 power supply

3.4.3.1.1 LPDDR5

Due to the 10-layer HDI board, the DQ, DM, DQS, WCLK, address, and CLK signals go to the inner layer, and the rate difference between the differential signal and the single-ended signal is small, so the design rules are required by line length, thus the PCB software setting is simple.

Table 3-13 LPDDR5 Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	40 Ohm $\pm 10\%$
Address, control line single-ended signal impedance	(40~50)Ohm $\pm 10\%$
Differential Signal Impedance	80Ohm $\pm 10\%$ (80Ohm target impedance is preferred ,if stackup limits, 80Ohm can not meet,at least meet 90Ohm $\pm 10\%$)
Equal length between DQ and DQS, WCLK (the same Byte)	$\leq 25\text{mil}$
Equal length between DM and DQS, WCLK (the same Byte)	$\leq 25\text{mil}$
Equal length between address, control lines and CLK	$\leq 40\text{mil}$
Equal length between DQS_P and DQS_N (the same Byte)	$\leq 5\text{mil}$
Equal length between WCLK_P and WCLK_N (the same Byte)	$\leq 5\text{mil}$
Equal length between CLK_P and CLK_N	$\leq 5\text{mil}$
Equal length between DQS, WCLK and CLK	$\leq 200\text{mil}$
The space between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
The distance between DQ and WCLK in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.1.2 LPDDR4X

Due to the 10-layer HDI board, DQ, DM, DQS, WCLK, address, and CLK signals go to the inner layer, and the rate difference between the differential signal and the single-ended signal is small, so the design rules are required by line length, thus the PCB software setting is simple.

Table 3-14 LPDDR4X Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	40 Ohm $\pm 10\%$
Address control lines (except CKE signals) single-ended signal impedance	40 Ohm $\pm 10\%$
CKE single-ended signal impedance	50 Ohm $\pm 10\%$
Differential Signal Impedance	80Ohm $\pm 10\%$ (80Ohm target impedance is preferred ,if stackup limits, 80Ohm can not meet,at least meet 90 Ohm $\pm 10\%$)
Equal length between DQ and DQS (within the same Byte)	$\leq 25\text{mil}$
Equal length between DM and DQS (within the same Byte)	$\leq 25\text{mil}$
Equal length between address, control lines and CLK	$\leq 40\text{mil}$
Equal length between DQS_P and DQS_N (within the same Byte)	$\leq 5\text{mil}$
Equal length between CLK_P and CLK_N	$\leq 5\text{mil}$
Equal length between DQS and CLK	$\leq 250\text{mil}$
The space between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.1.3 LPDDR4

Due to the 10-layer HDI board, DQ, DM, DQS, WCLK, address, and CLK signals go to the inner layer, and the rate difference between the differential signal and the single-ended signal is small, so the design rules are required by line length, thus the PCB software setting is simple.

Table 3-15 LPDDR4 Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	40 Ohm $\pm 10\%$
Address control lines (except CKE signals) single-ended signal impedance	40 Ohm $\pm 10\%$
CKE single-ended signal impedance	50 Ohm $\pm 10\%$
Differential Signal Impedance	80Ohm $\pm 10\%$ (80Ohm target impedance is preferred ,if stackup limits, 80 Ohm can not meet,at least meet 90Ohm $\pm 10\%$)
Equal length between DQ and DQS (within the same Byte)	$\leq 25\text{mil}$
Equal length between DM and DQS (within the same Byte)	$\leq 25\text{mil}$

Parameter	Requirements
Equal length between address, control lines and CLK	$\leq 40\text{mil}$
Equal length between DQS_P and DQS_N (within the same Byte)	$\leq 5\text{mil}$
Equal length between CLK_P and CLK_N	$\leq 5\text{mil}$
Equal length between DQS and CLK	$\leq 250\text{mil}$
The space between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.2 DRAM Circuit PCB Design (8-Layer PTH PCB)

As RK3588 DDR interface operates up to 4266Mbps, the PCB design is difficult, so it is strongly recommended to use the DDR template and corresponding DDR firmware provided by RK. DDR templates are released after rigorous simulation and verification. If you do not use DDR templates and design PCB by yourself, please refer to the following PCB design suggestions, then perform simulation. Compared with the 10-layer first-order HDI design, the signal margin of the 8-layer PTH will be reduced. It is recommended to choose the 10-layer HDI DDR template first.

(1) The CPU GND pads should have enough vias, it is recommended to strictly refer to the template design. The GND vias cannot be deleted. For example, the 8-layer PTH PCB template design is as shown in the figure below.

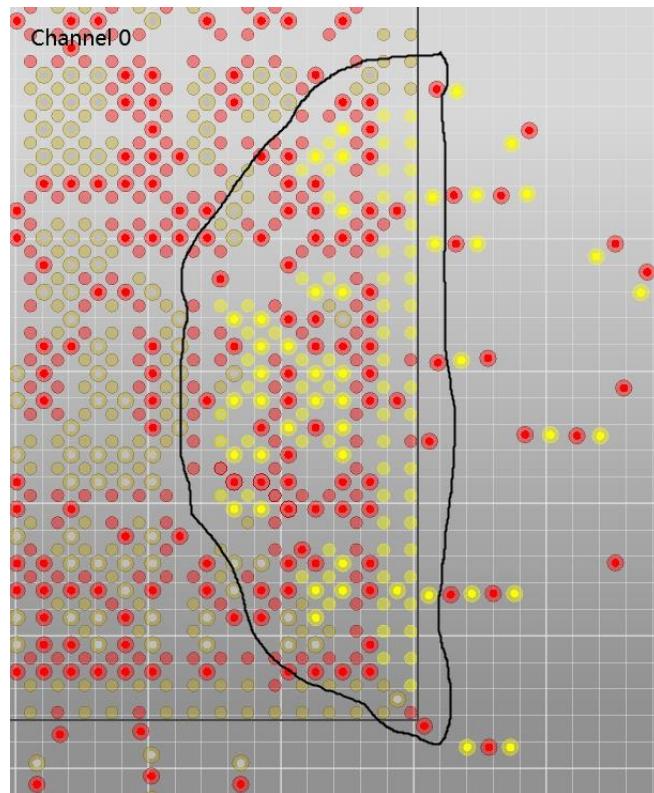


Figure 3-131 vias design of 8-layer HDI first-order PCB template SOC channel 0 area

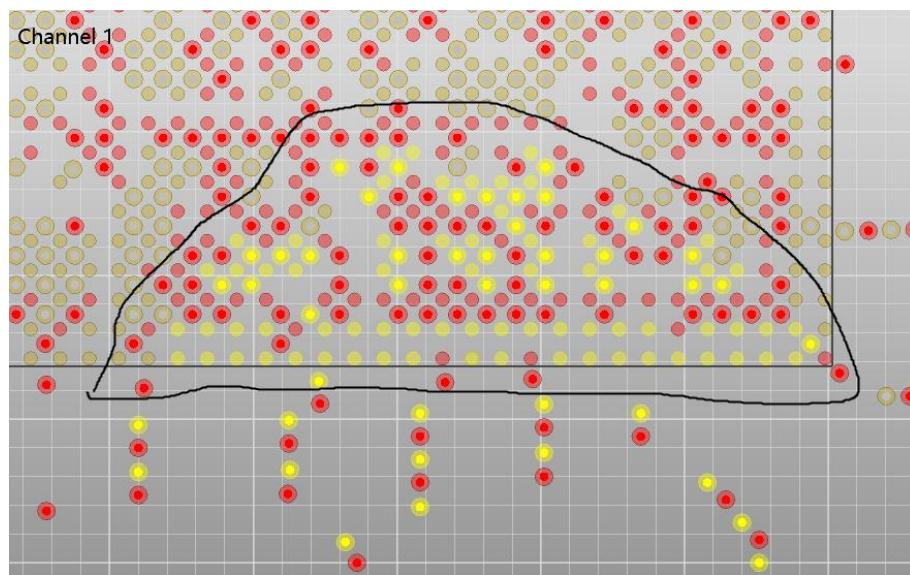


Figure 3-132 vias design of 8-layer HDI first-order PCB template SOC channel 1 area

(2) If a signal trace changes layer and the reference plane is GND, stitching GND vias should be added close to the layer change vias within 25 mils. One Signal via should have \geq one GND via. Increase GND via as much as you can.

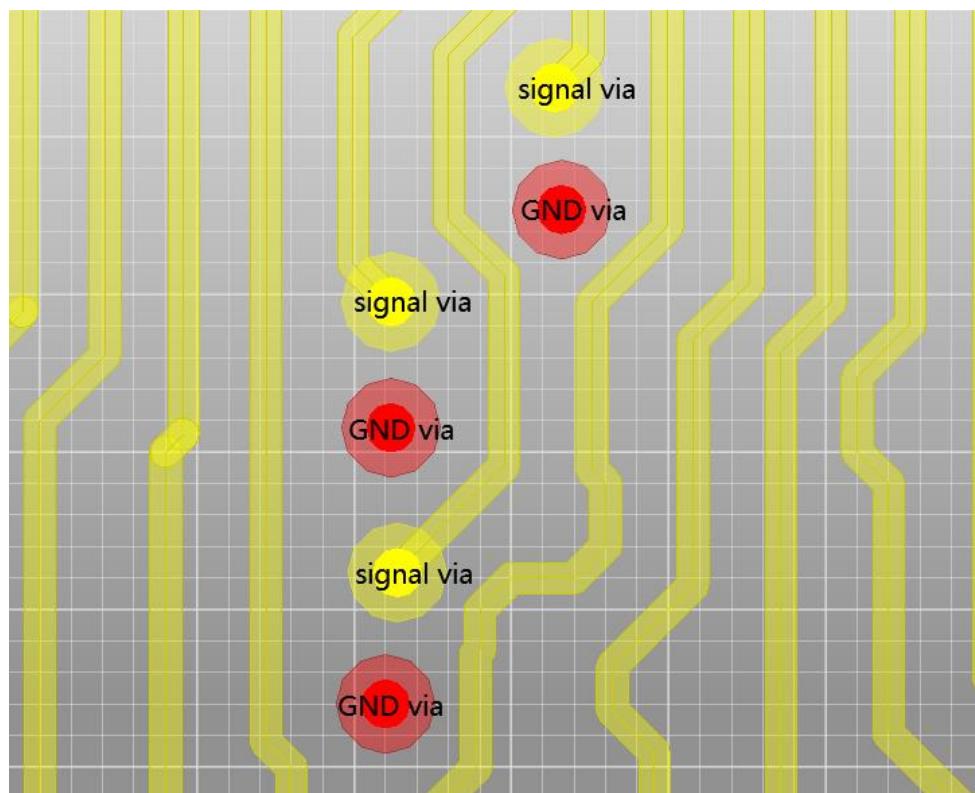


Figure 3-133 Schematic of the GND via corresponding to the signal via

(3) GND vias recommend to be placed between signal vias. Four signal vias together is not recommended. Use GND vias to separate signal vias as shown in the figure below, will improve performance.

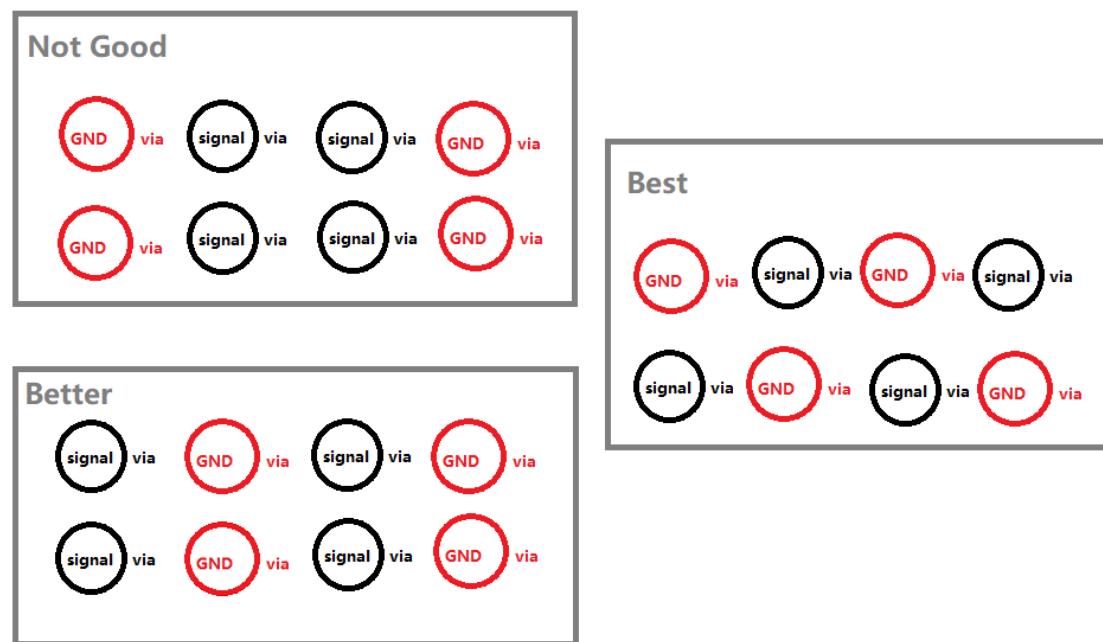


Figure 3-134 Schematic of different via design

(4) For an 8-layer board, it is recommended that the DDR signal routed to the first, sixth, and eighth layers. route all traces over continuous GND planes, with no interruptions.

(5) Avoid return path discontinuities such as a slit, you can optimize the reference layer with GND traces.

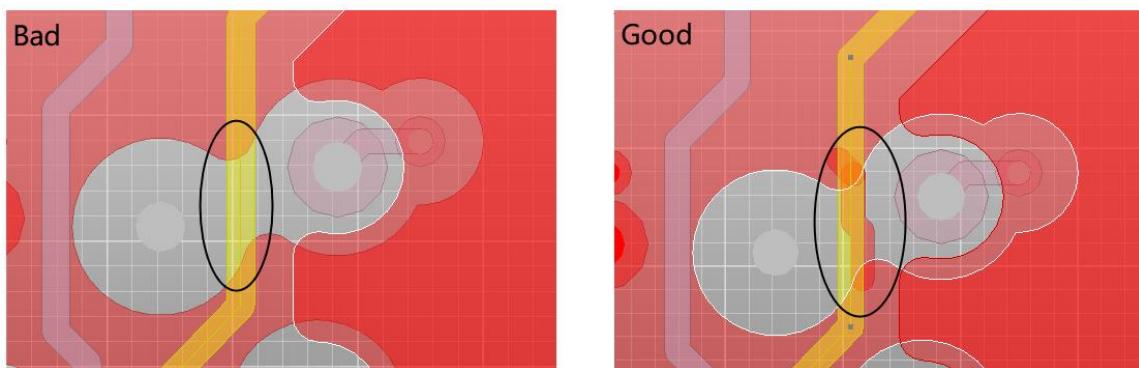


Figure 3-135 GND traces optimization the reference layer

(6) The recommended distance between the trace and the edge of the reference layer is ≥ 12 mil.

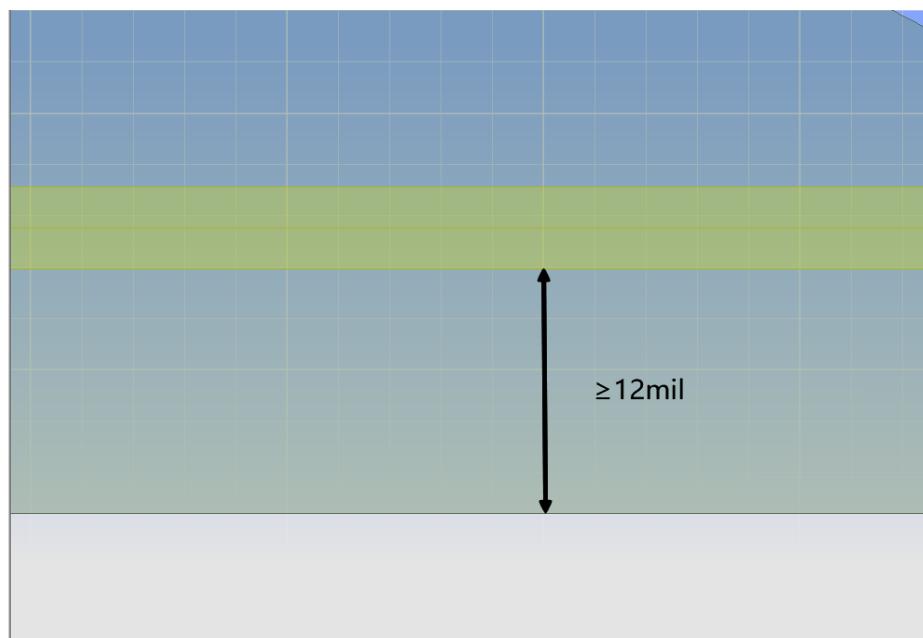


Figure 3-136 the distance between the trace and the edge of the reference layer

(7) An adequate spacing should be maintained between the inside traces of a bend. Recommend 3times the trace width or greater($S \geq 3W$).

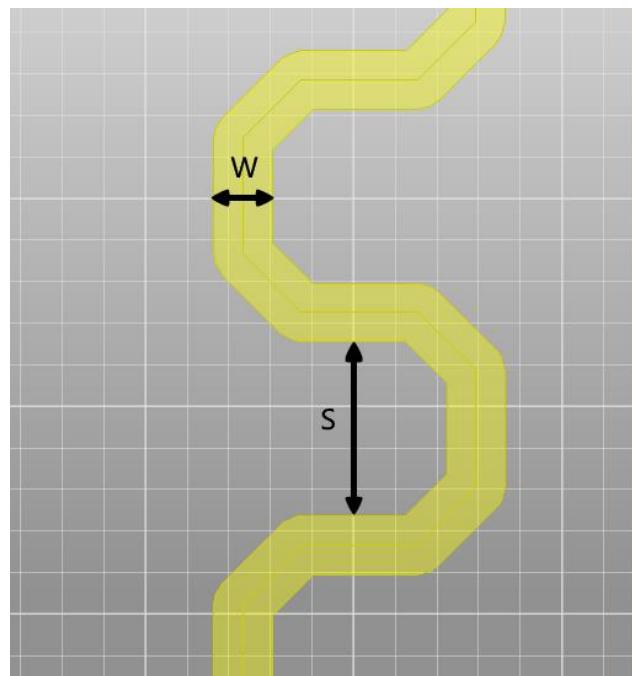


Figure 3-137 adequate spacing

(8) The propagation delay associated with vias should be accounted for in the trace length.

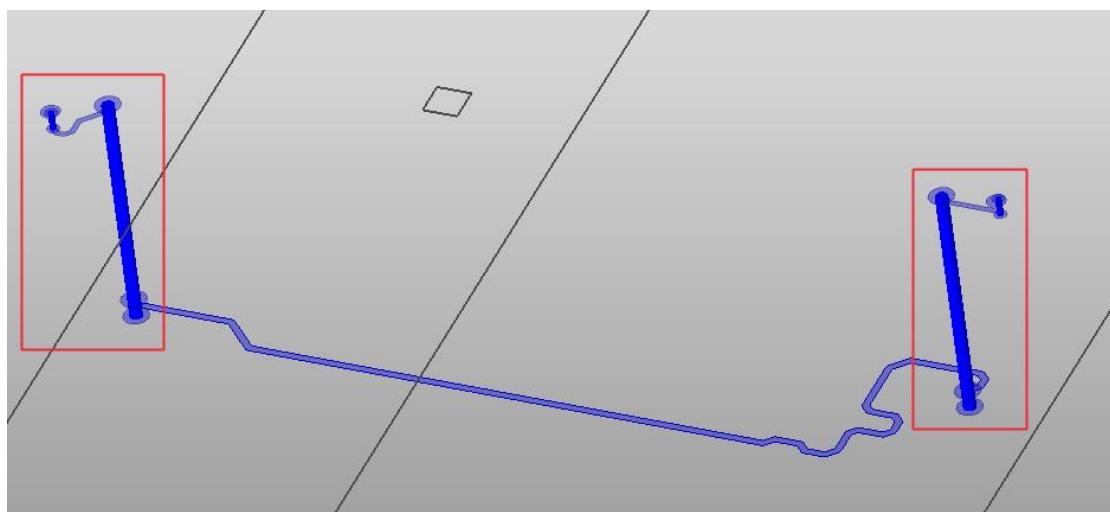


Figure 3-138 Schematic of vias length

(9) One via per GND pad of Dram chip. Add GND vias as much as you can.

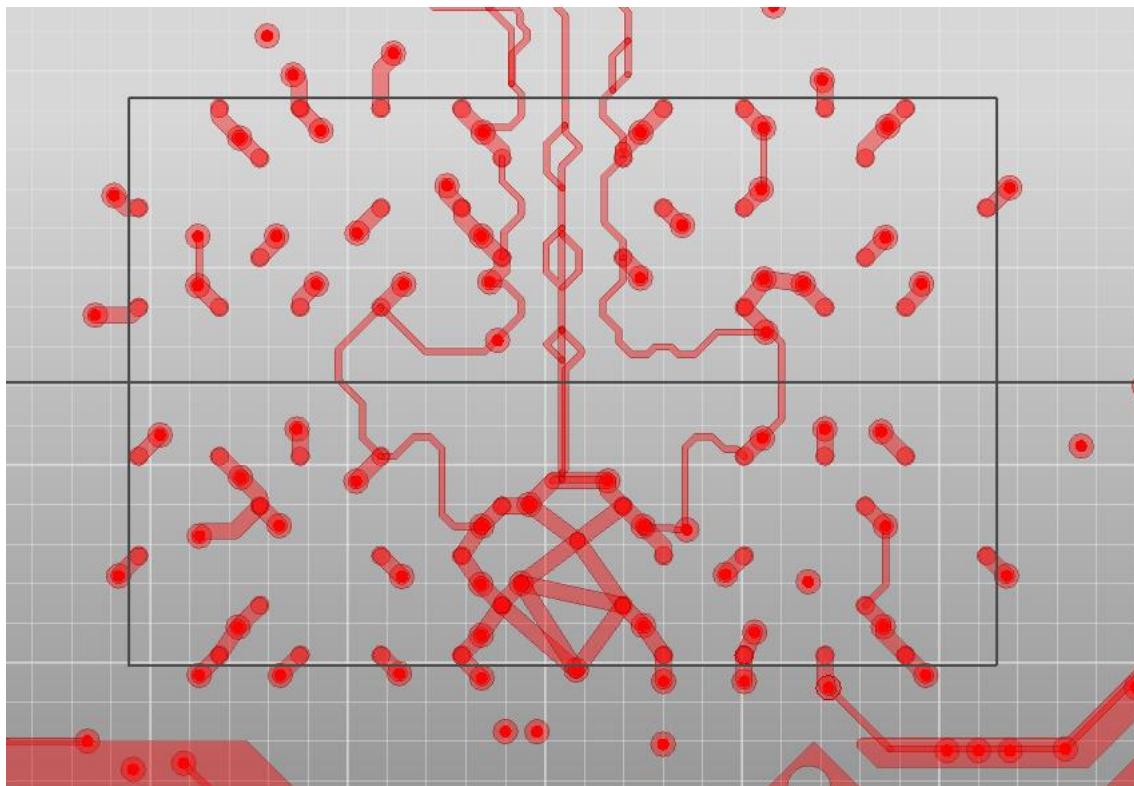


Figure 3-139 Requirements for the number of GND vias in the DDR area

(10) Remove unused via pads, because they cause unwanted capacitance and destroy plane.

(11) The closer the trace is to the via, the worse the reference plane is. Recommend route trace far away ($\geq 8\text{mil}$) from the via pad.

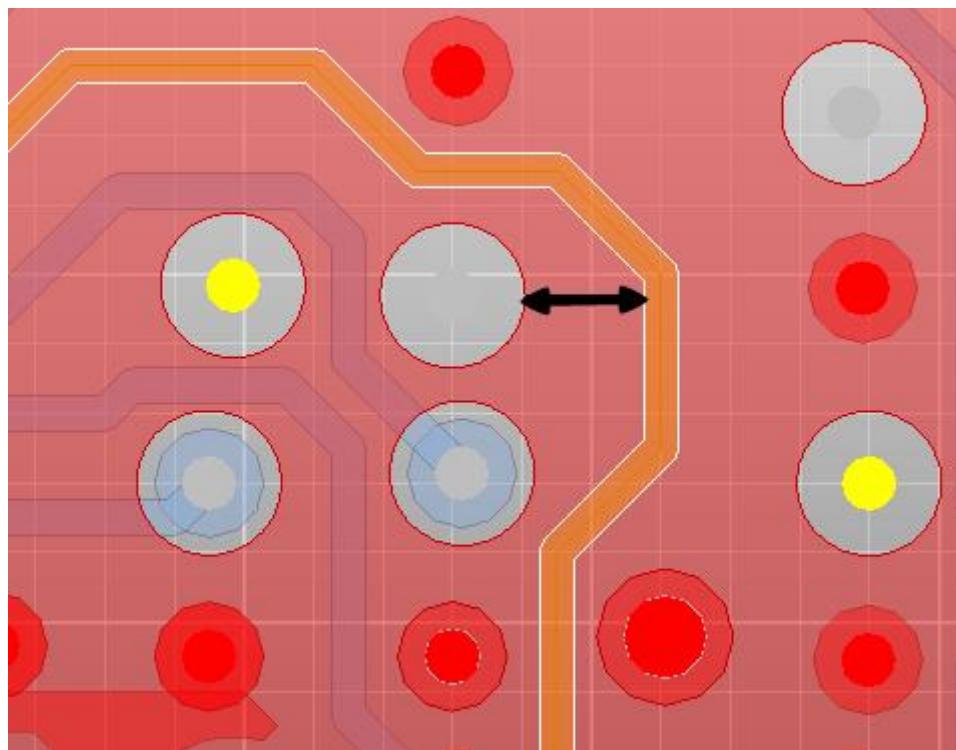


Figure 3-140 Increase trace and via pad spacing

(12) Avoid making slits of plane due to the via clearance as possible.

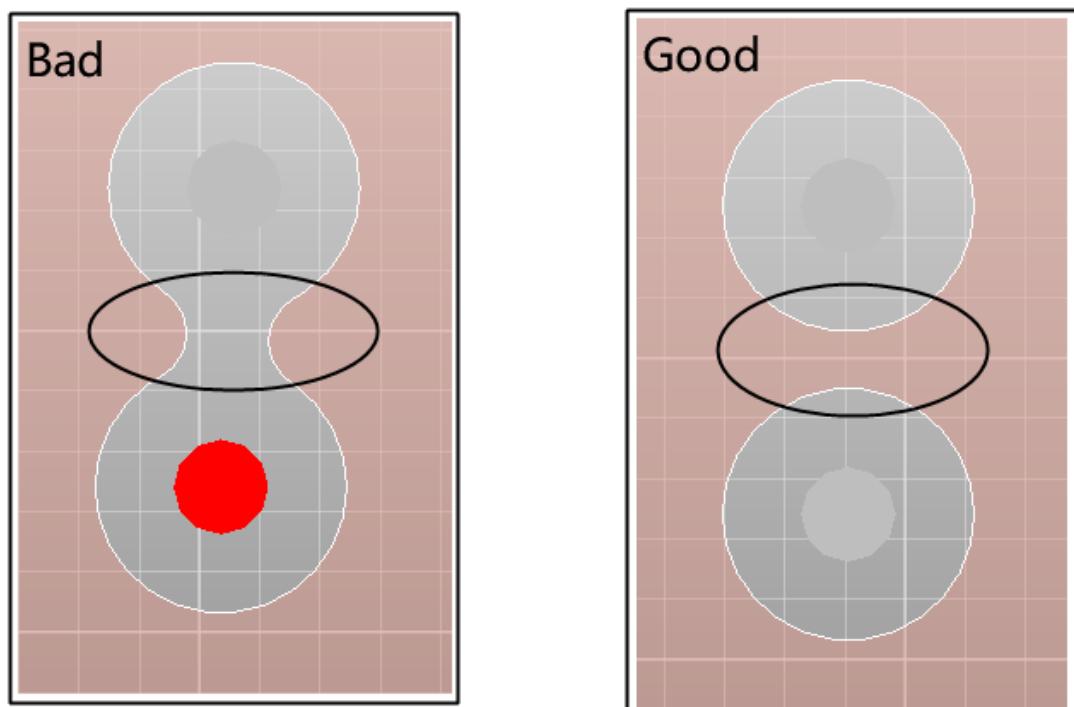


Figure 3-141 Schematic of route optimization plane slits

(13) DQS,CLK,WCLK signal should use ground shielding for the entire trace including vias. Recommend ground shielding line $\geq 400\text{mil}$,add one GND via.

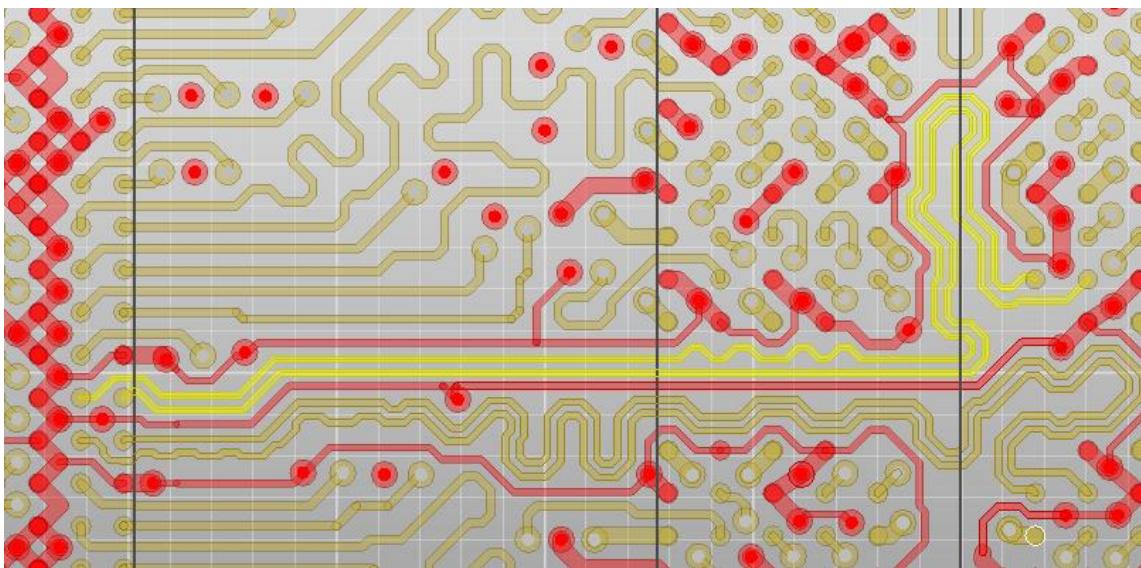


Figure 3-142 Schematic of ground shielding design

(14) For VCC_DDR_S0 power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.



Figure 3-143 the vias requirement when power layer changed

(15) For VDDQ_DDR_S0 power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.

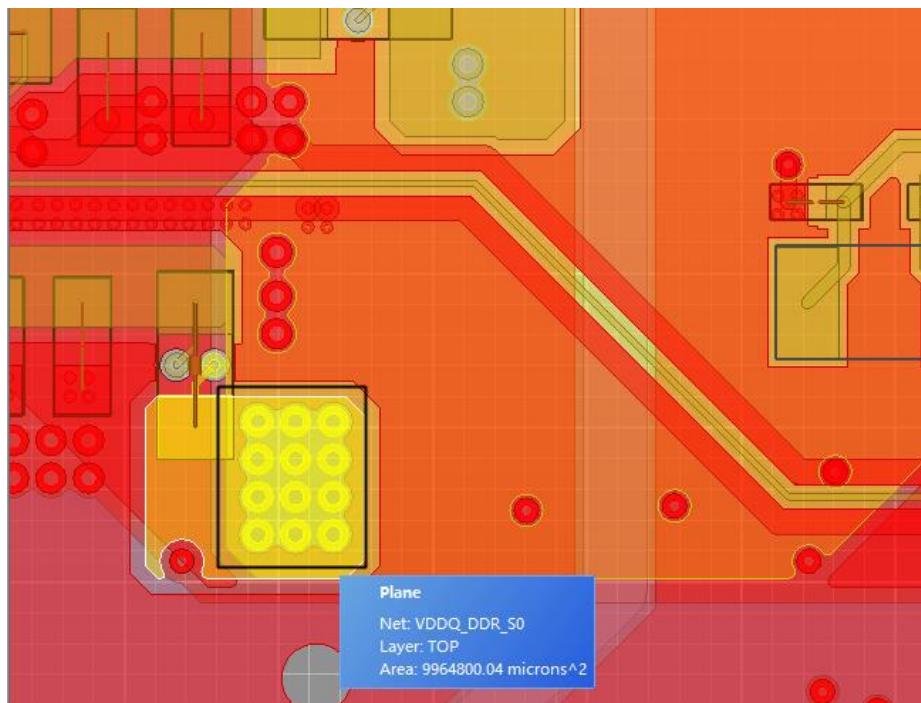


Figure 3-144 the vias requirement when power layer changed

(16) For VDD2_DDR_S3 power, recommend ≥ 6 vias (0503 via) when power layer is changed at DCDC output.

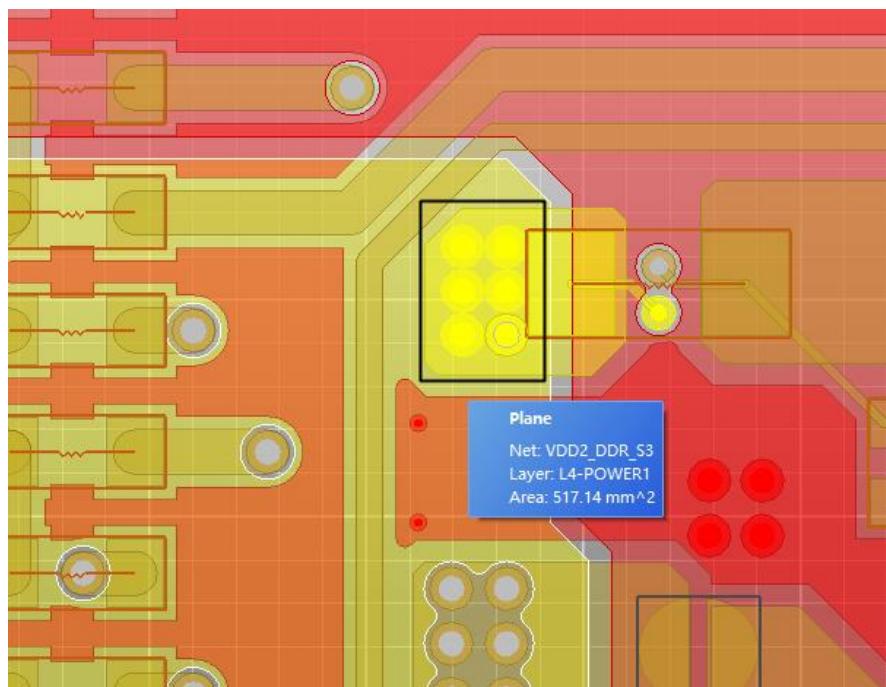


Figure 3-145 the vias requirement when power layer changed

(17) For VDD1_1V8_DDR power supply, it is recommended ≥ 2 vias(0402 via) when the power plane is changed.

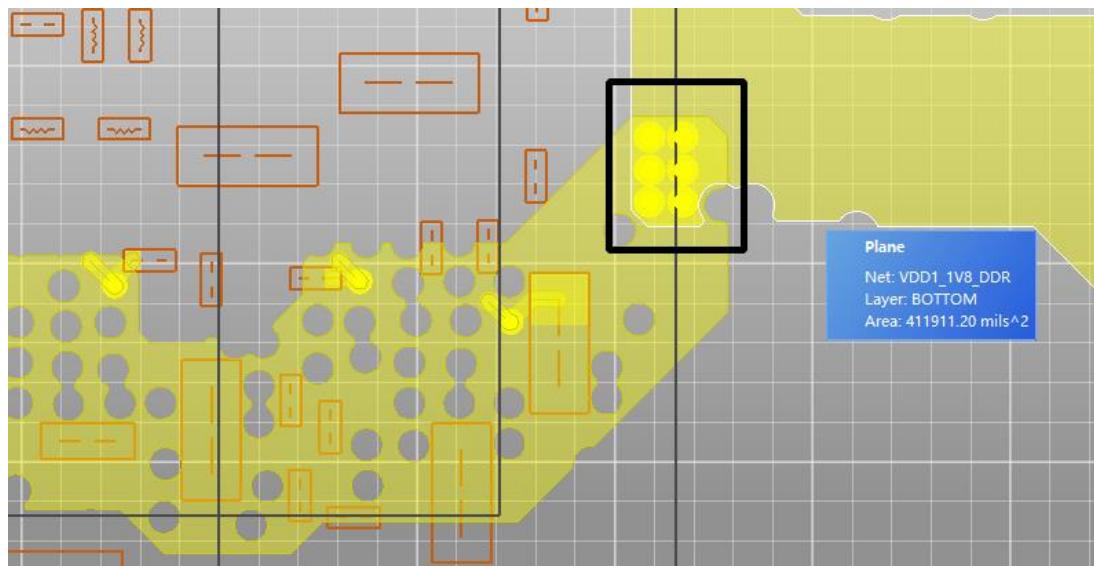


Figure 3-146 the vias requirement when power layer changed

(18) At least one via per pad of Capacitor. For 0603 or 0805 capacitors, it is recommended that one pad corresponds to two vias.

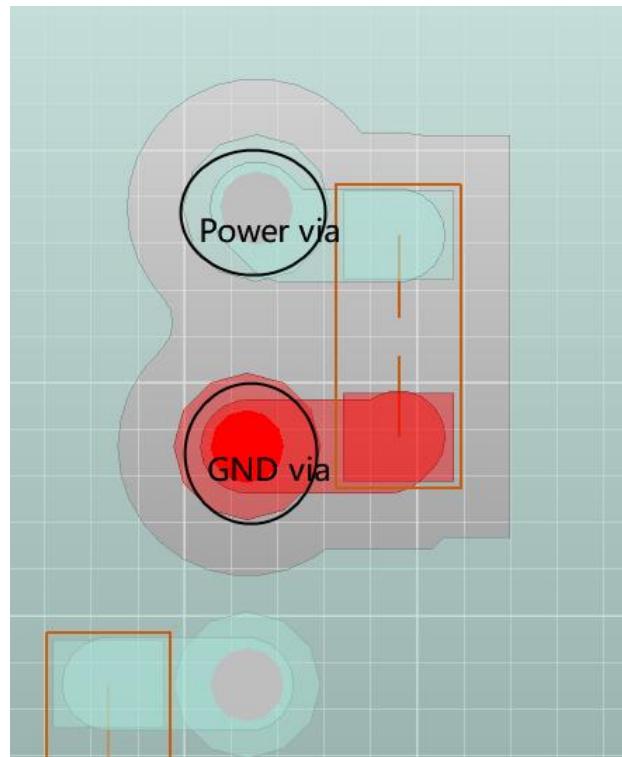


Figure 3-147 Number of vias corresponding to capacitor pads

(19) Place via closer to the pin to reduce the loop inductance.

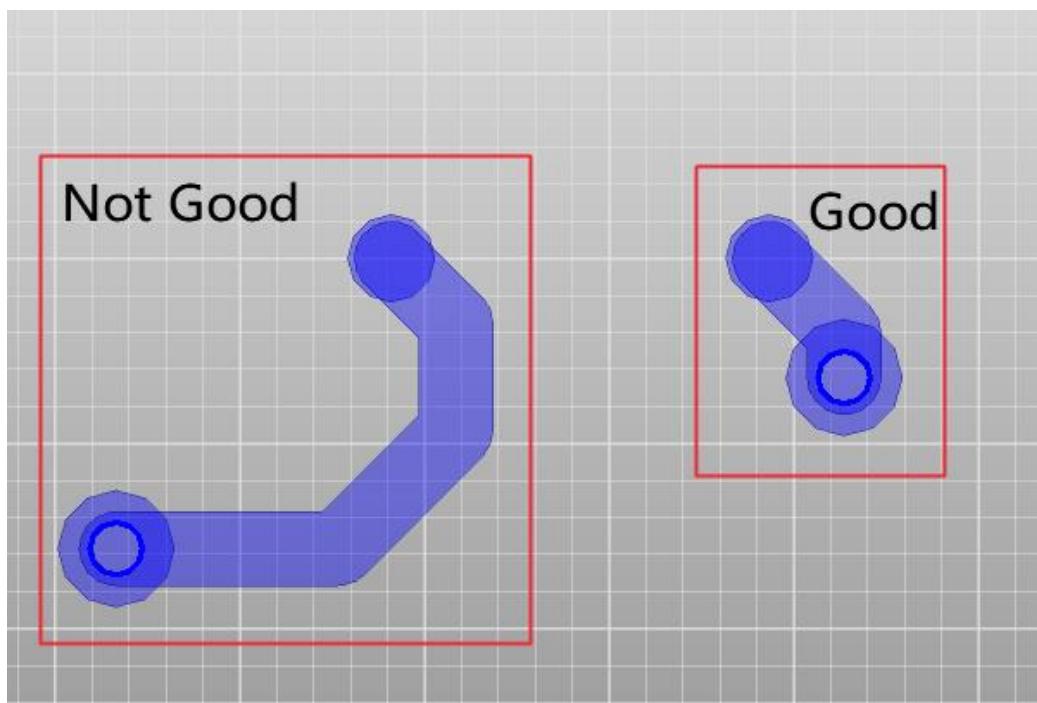


Figure 3-148 Schematic of placement of vias close to pins

(20) For the number of power vias corresponding to the VDDQ_DDR and VDD_DDR pins of the CPU, refer to the DDR template. It is not recommended to delete the power vias.

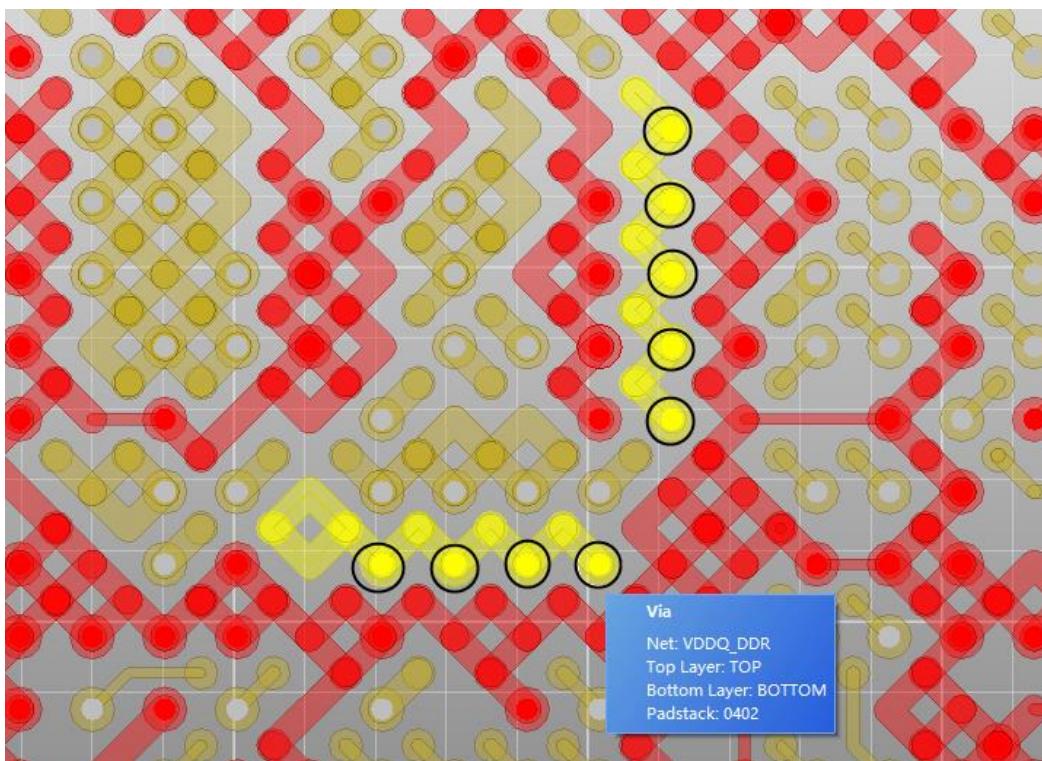


Figure 3-149 Requirements for the number of vias corresponding to the power pins

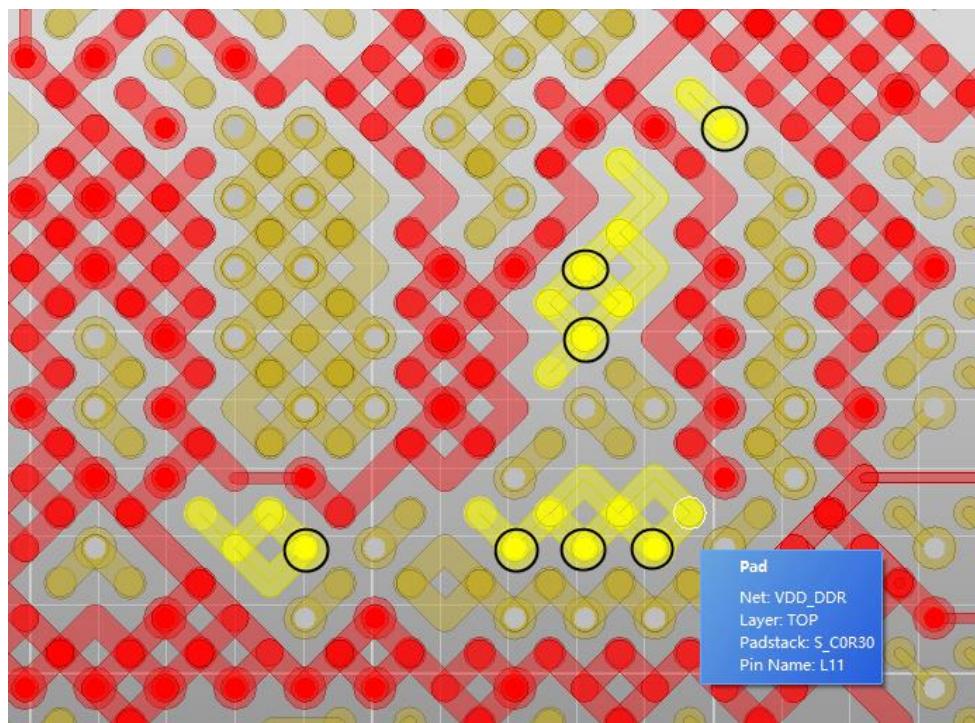


Figure 3-150 Requirements for the number of vias corresponding to the power pins

(21) VDDQ_DRAM, VDD2_DDR, VDD1_1V8_DDR power supply of DDR chip, it is recommended that one pin corresponds to one power via, for example as follows.

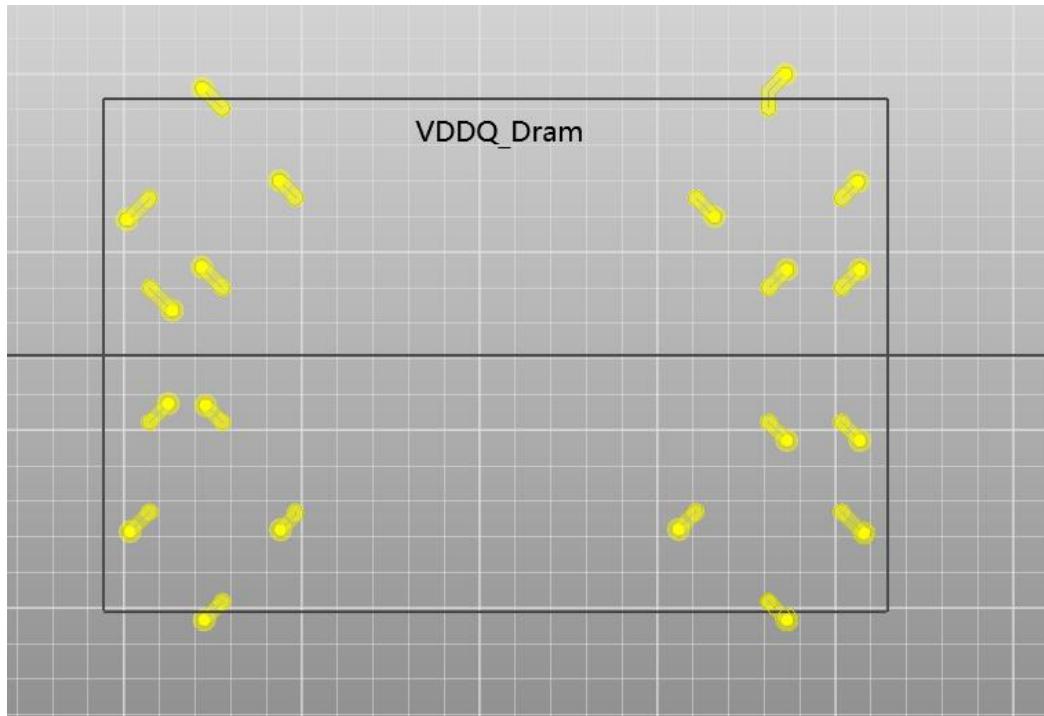


Figure 3-151 Requirements for the number of vias corresponding to the power pins

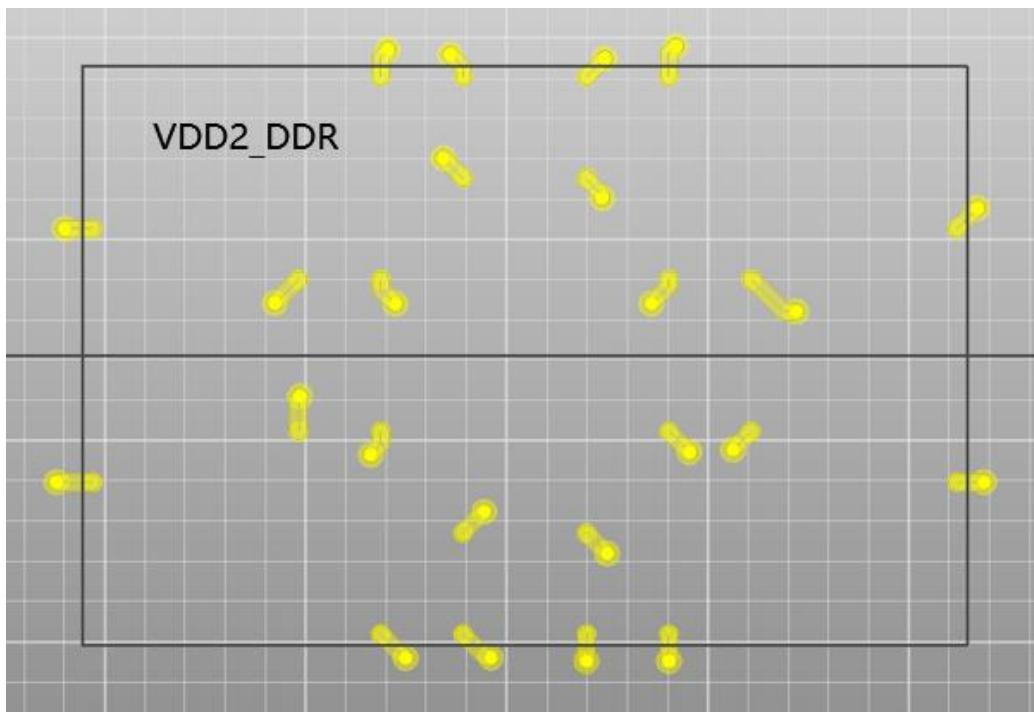


Figure 3-152 Requirements for the number of vias corresponding to the power pins

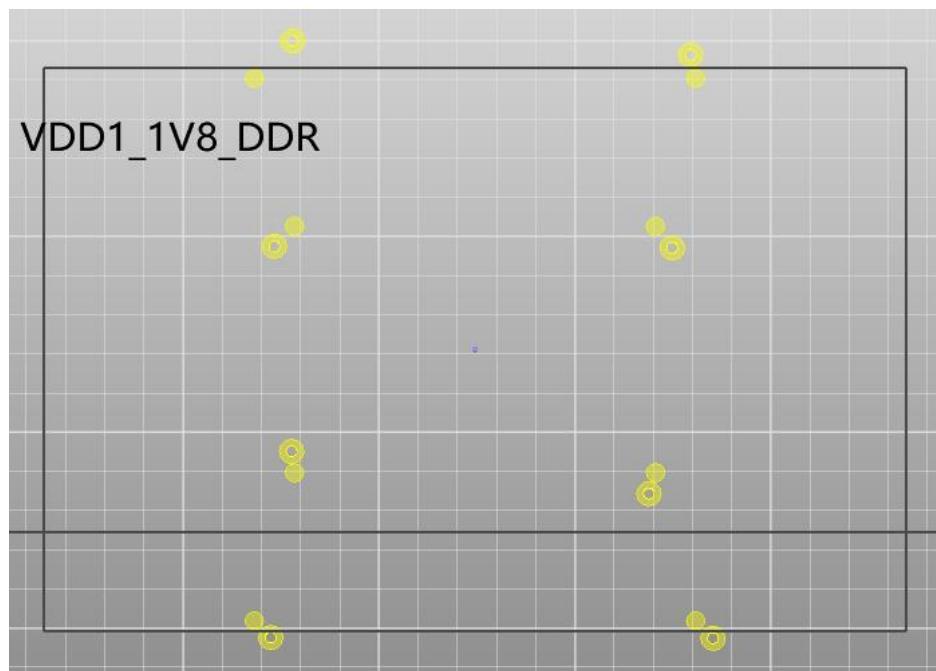


Figure 3-153 Requirements for the number of vias corresponding to the power pins

(22) The layer change of power should be minimized. When changing layers of DDR power supply (VDD_DDR, VDDQ_DDR, VDD2_DDR, VDDQ_DRAM), enough power vias (≥ 8 0402 vias or 6 0503 vias) should be drilled, for example as follows.

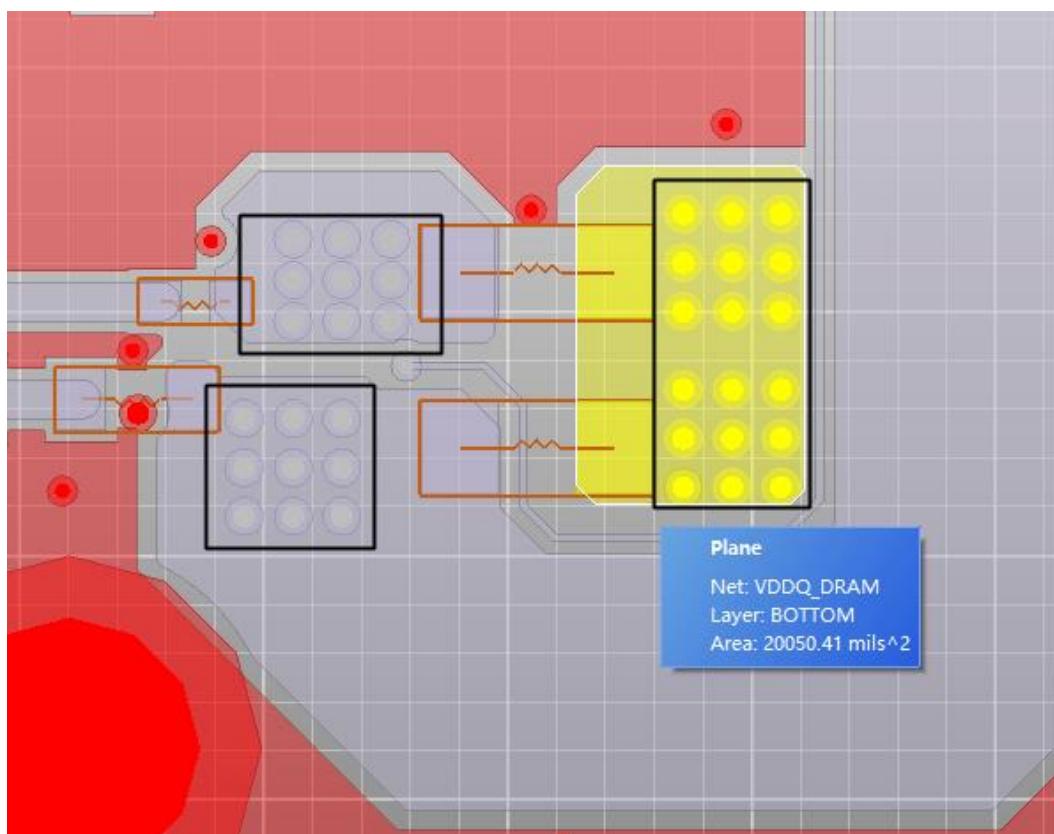


Figure 3-154 the vias requirement when power layer changed

(23) Avoid damage to the power layer by traces or vias.

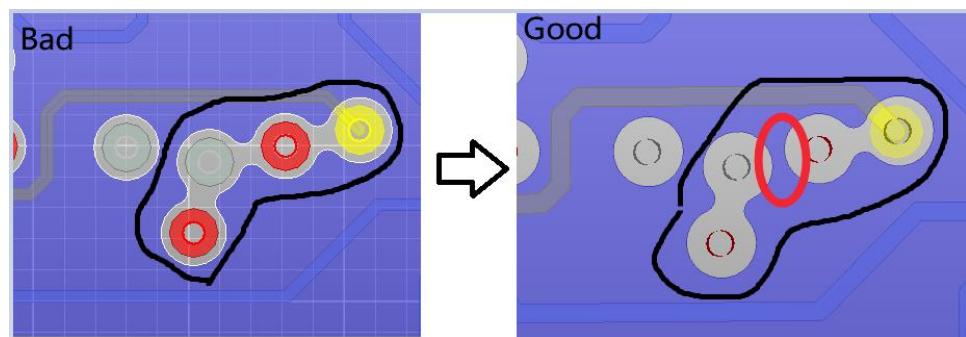


Figure 3-155 Schematic of preventing the power layer from being damaged by the row of vias

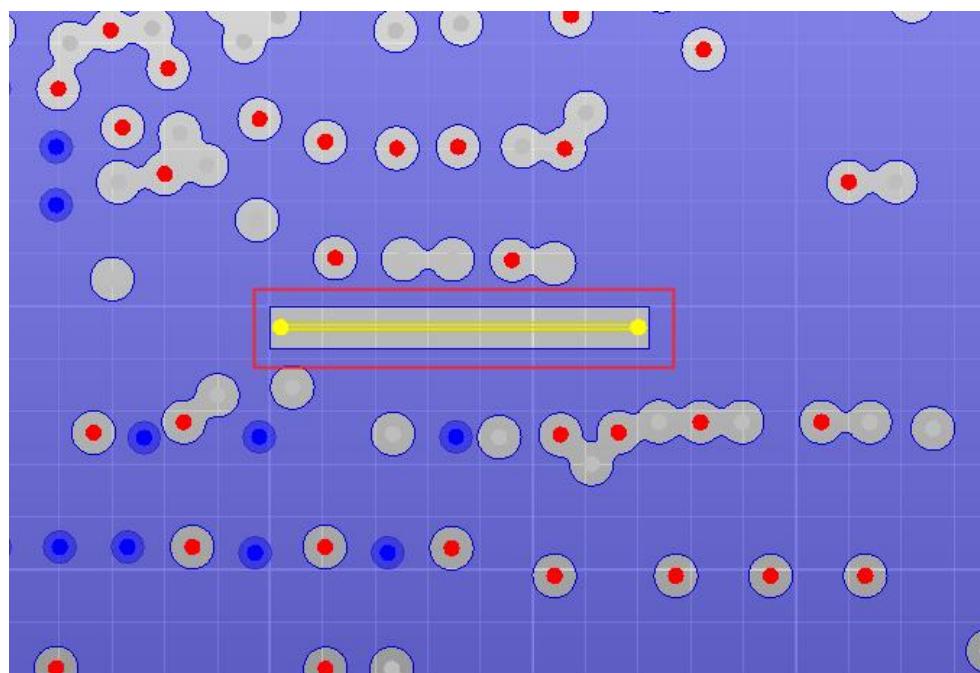


Figure 3-156 Schematic of the power plane being damaged by traces

(24) The decoupling capacitor should be placed close to the DDR chip pin, in order to reduce the loop inductance of the capacitors. The number of capacitors is recommended to refer to the DDR template design, and it is not recommended to delete the capacitors. Capacitors should be evenly placed.

(25) The recommended PDN requirement for the VDD_DDR power at the CPU area is as shown below.

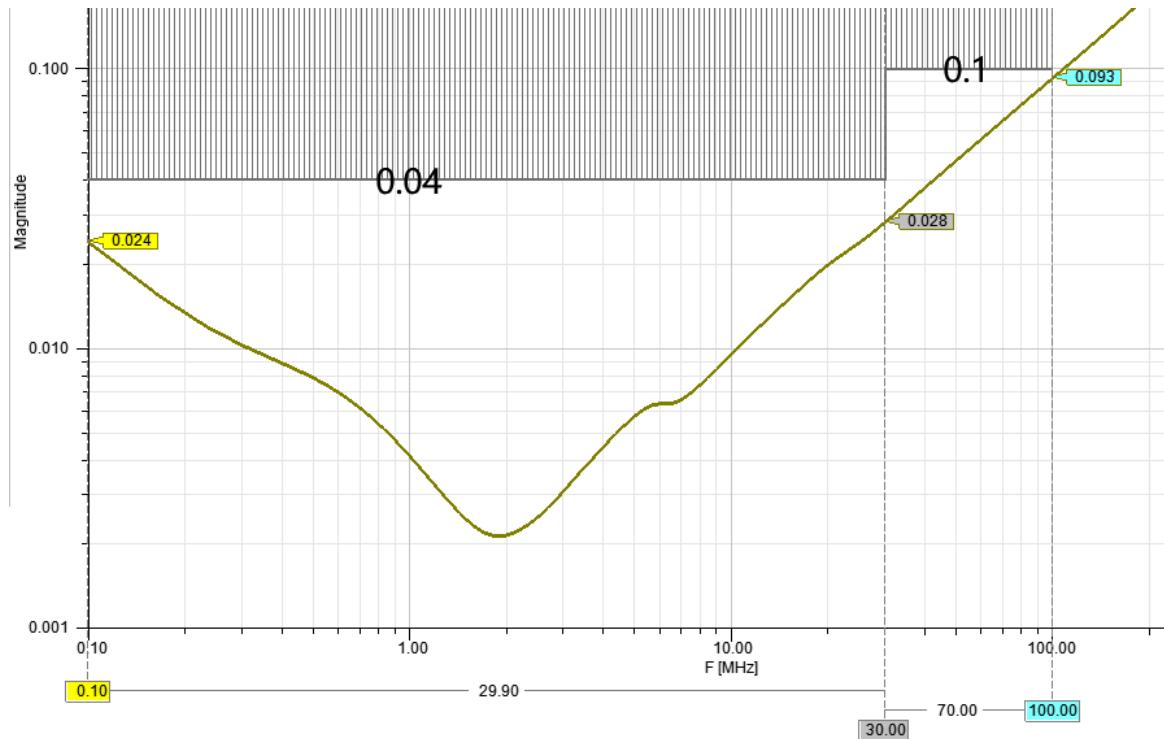


Figure 3-157 the recommended PDN requirements of VDD_DDR power supply

(26) The recommended PDN requirement for the VDDQ_DDR power at the CPU area is as shown below.

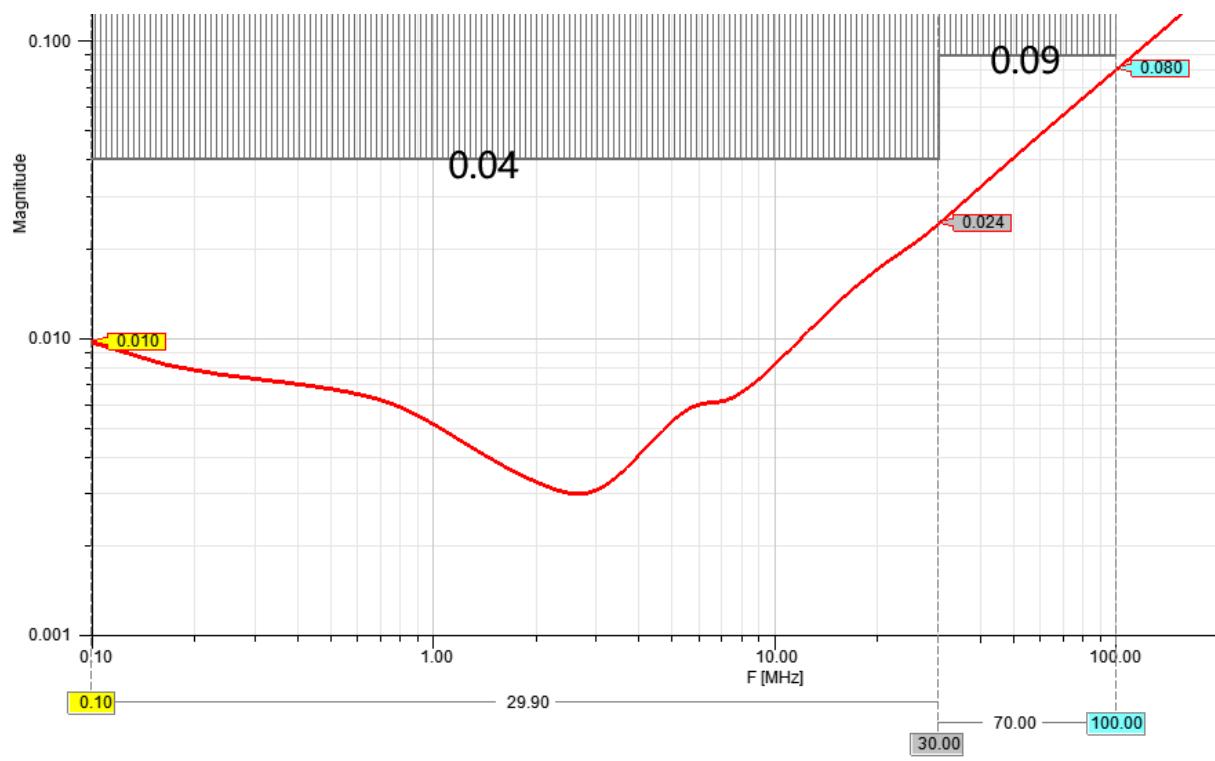


Figure 3-158 the recommended PDN requirements of VDDQ_DDR power supply

(27) The PDN requirements for the VDDQ_DRAM power supply at the DDR chip area are as shown in the figure below.

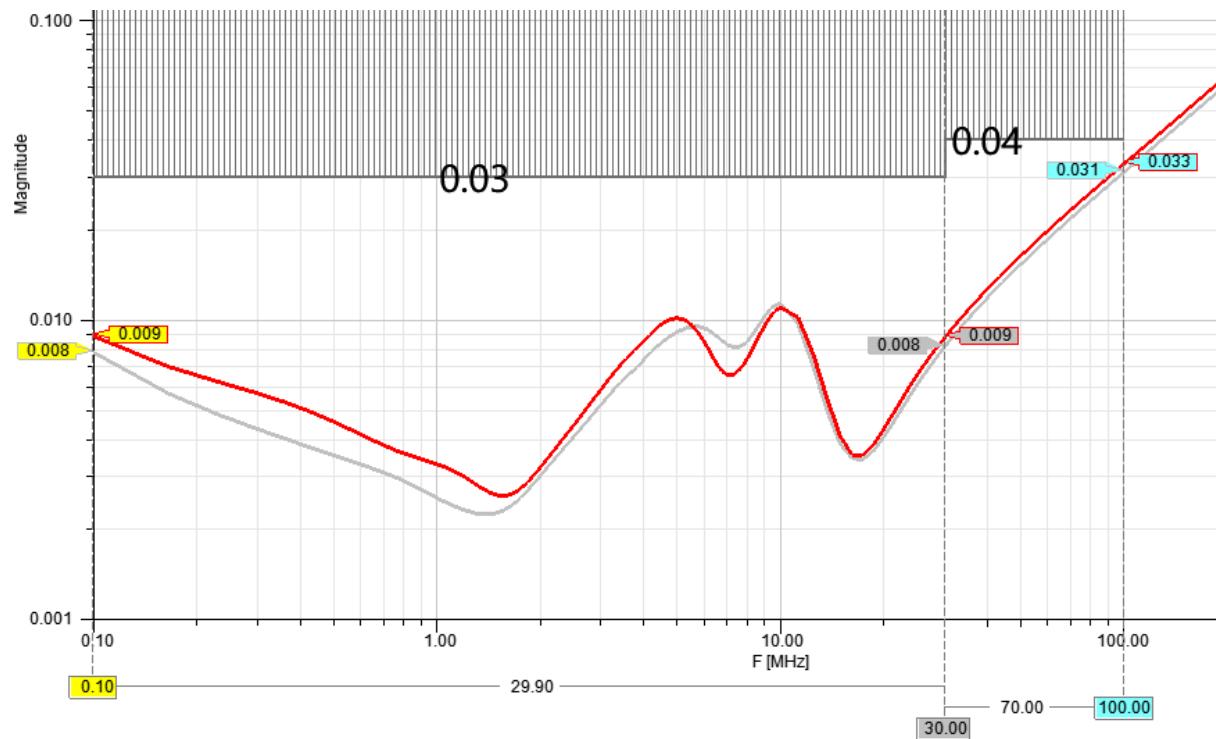


Figure 3-159 the recommended PDN requirements of VDDQ_DRAM power supply

(28) The PDN requirements for the VDD2_DDR power supply at the DDR chip area are as shown below.

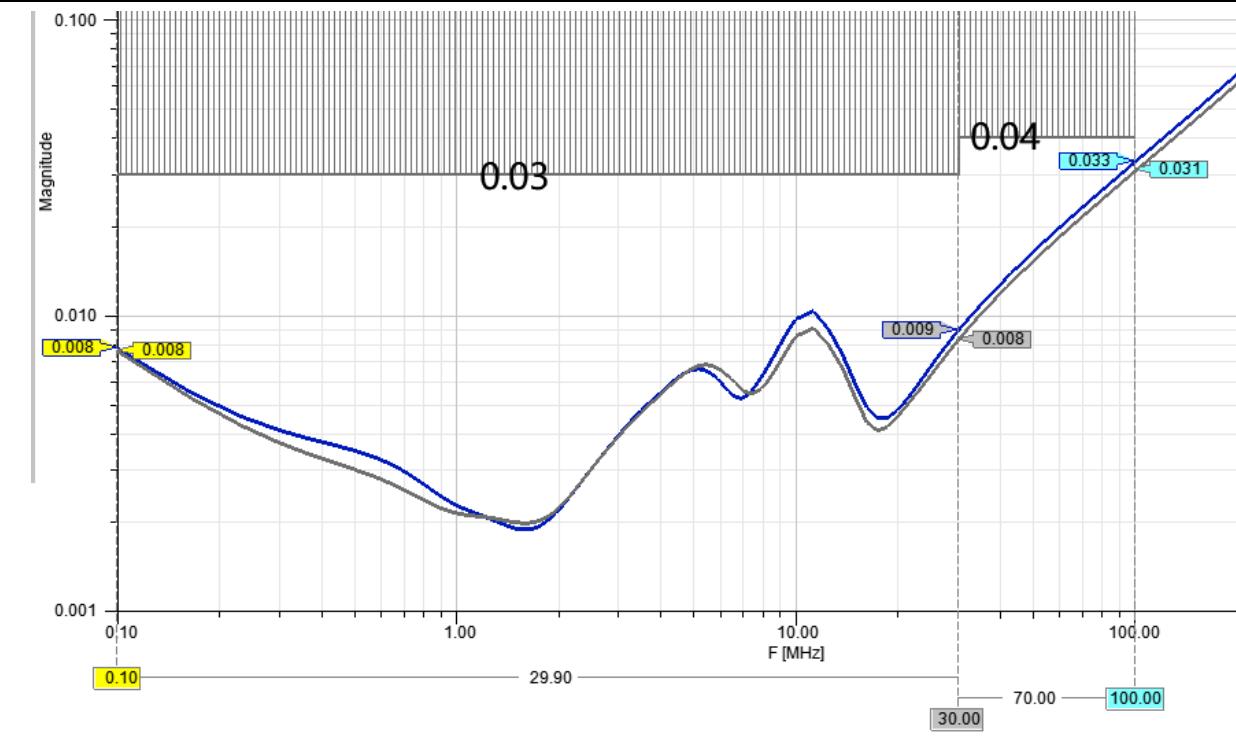


Figure 3-160 the recommended PDN requirements of VDD2_DDR power supply

3.4.3.2.1 LPDDR4X

Since it is an 8-layer board, there are traces on the surface and inner layers. Whether single-ended signal or differential signal, the speed of the surface trace and the inner trace is different. Single-ended signals and differential signals have different speed when routed as surface trace. The speed between single-ended signals and differential signals is small when routed as inner layer traces. The via speed and the trace speed is different. In order to reduce the impact of the skew difference on the signal margin, the design rules need to be based on delay. When designing the PCB, it is necessary to set the stack-up parameters according to the stack-up of the actual board, and consider the package delay and the via delay. For details, refer to the document "Delay Setting Guide".

Table 3-16 LPDDR4X Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	40 Ohm $\pm 10\%$ (if stackup limits, 40 Ohm can not meet, at least meet 45 Ohm $\pm 10\%$. 40 Ohm is preferred, since signal quality is better than 45 Ohm)
Address control lines (except CKE signals) single-ended signal impedance	40 Ohm $\pm 10\%$ (if stackup limits, 40 Ohm can not meet, at least meet 45 Ohm $\pm 10\%$. 40 Ohm is preferred, since signal quality is better than 45 Ohm)
CKE single-ended signal impedance	50 Ohm $\pm 10\%$
Differential Signal Impedance	80Ohm $\pm 10\%$ (80 Ohm target impedance is preferred ,if stackup limits, 80 Ohm can not meet, at least meet 90 Ohm $\pm 10\%$)
Equal length between DQ and DQS (within the same Byte)	$\leq 16\text{ps}$
Equal length between DM and DQS (within the same Byte)	$\leq 16\text{ps}$

Parameter	Requirements
Equal length between address, control lines and CLK	$\leq 16\text{ps}$
Equal length between DQS_P and DQS_N (within the same Byte)	$\leq 1\text{ps}$
Equal length between CLK_P and CLK_N	$\leq 1\text{ps}$
Equal length between DQS and CLK	$\leq 40\text{ps}$
Spacing between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.3.2.2 LPDDR4

Since it is an 8-layer board, there are traces on the surface and inner layers. Whether single-ended signal or differential signal, the speed of the surface trace and the inner trace is different. Single-ended signals and differential signals have different speed when routed as surface trace. The speed between single-ended signals and differential signals is small when routed as inner layer traces. The via speed and the trace speed is different. In order to reduce the impact of the skew difference on the signal margin, the design rules need to be based on delay. When designing the PCB, it is necessary to set the stack-up parameters according to the stack-up of the actual board, and consider the package delay and the via delay. For details, refer to the document "Delay Setting Guide".

Table 3-17 LPDDR4 Routing Requirements

Parameter	Requirements
DQ, DM single-ended signal impedance	40 Ohm $\pm 10\%$ (if stackup limits, 40 Ohm can not meet, at least meet 45 Ohm $\pm 10\%$. 40 Ohm is preferred, since signal quality is better than 45 Ohm)
Address control lines (except CKE signals) single-ended signal impedance	40 Ohm $\pm 10\%$ (if stackup limits, 40 Ohm can not meet, at least meet 45 Ohm $\pm 10\%$. 40 Ohm is preferred, since signal quality is better than 45 Ohm)
CKE single-ended signal impedance	50 Ohm $\pm 10\%$
Differential Signal Impedance	80Ohm $\pm 10\%$ (80 Ohm target impedance is preferred ,if stackup limits, 80 Ohm can not meet, at least meet 90 Ohm $\pm 10\%$)
Equal length between DQ and DQS (within the same Byte)	$\leq 16\text{ps}$
Equal length between DM and DQS (within the same Byte)	$\leq 16\text{ps}$
Equal length between address, control lines and CLK	$\leq 16\text{ps}$
Equal length between DQS_P and DQS_N (within the same Byte)	$\leq 1\text{ps}$
Equal length between CLK_P and CLK_N	$\leq 1\text{ps}$
Equal length between DQS and CLK	$\leq 40\text{ps}$
Spacing between different Bytes (airgap)	≥ 2 times the trace width
The distance between DQ and DQ in the same Byte (airgap)	≥ 2 times the trace width
The distance between DQ and DQS in the same Byte (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

Parameter	Requirements
Spacing between address control lines (airgap)	≥ 2 times the trace width
Spacing between CLK and other signal lines (airgap)	Recommended ≥ 3 times the trace width At least 2 times the trace width

3.4.4 DP1.4

Table 3-18 Layout Requirements for DP1.4

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential (DP only) $95\Omega \pm 10\%$ differential (USB3.0 / DP1.4 Alt)
Max intra-pair skew	<6mil
Max mismatch between data pairs	<1000mil
Max trace length on carrier board	<6 inches
Minimum airgap between pair to pair	Recommend ≥ 6 times the width of DP trace.
Minimum airgap between DP and other signal	Recommend ≥ 6 times the width of DP trace.
Maximum allowed via	Recommend ≤ 2 vias
AC Capacitor	Recommend 100nF (75nF to 200nF including tolerance)
ESD	Typical I/O-to-GND Capacitance $\leq 0.2\text{pF}$

Place GND through via in BGA zone as showed below and recommend to follow ground shielding guideline in Section 3.2, item (24), GND via interval length should less than 300mil.

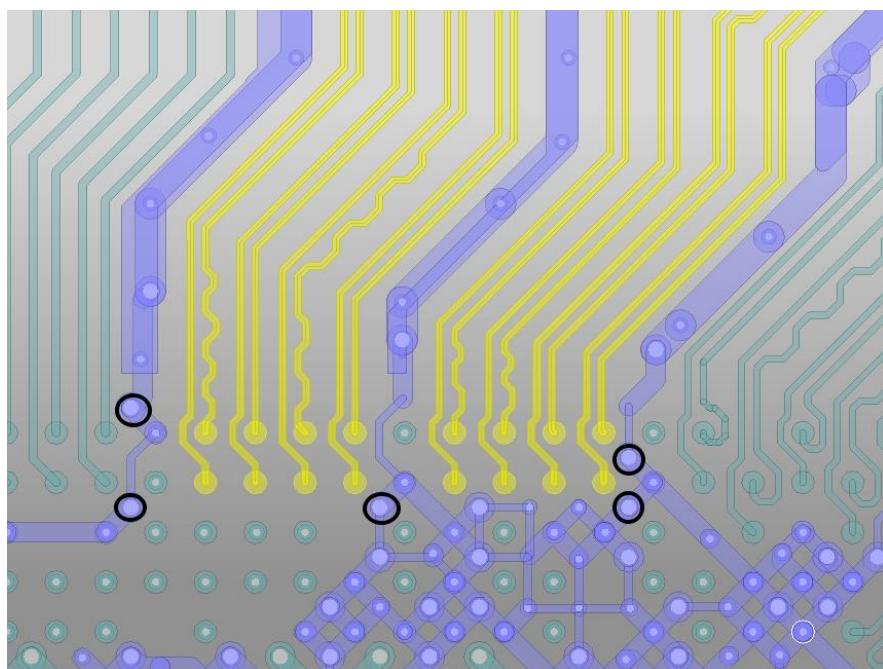


Figure 3-161 GND through via placement in BGA zone

3.4.5 PCIE2.0 (Combo PHY)

Table 3-19 Layout Requirements for PCI-E2.0

Parameter	Requirement
Trace Impedance	$85\Omega \pm 10\%$ differential
Max intra-pair skew	<6mil
Max inter-pair skew	<6inches
Max trace length on carrier board	<6 inches
AC coupling capacitors	100nF $\pm 20\%$, discrete 0201 package preferable
Minimum airgap between pair to pair	≥ 4 times the width of the trace.
Max intra-pair skew of REFCLK	<12mil
Trace Impedance of REFCLK	$100\Omega \pm 10\%$ differential
Minimum airgap between PCI-E and other Signals	Recommend ≥ 5 times the width of PCI-E trace. At least 4 times the width of PCI-E trace.
Maximum allowed via	Recommend ≤ 2 vias

3.4.6 PCIE3.0

Table 3-20 Layout Requirements for PCI-E 3.0

Parameter	Requirement
Trace Impedance	$85\Omega \pm 10\%$ differential
Max intra-pair skew	<6mil
Max inter-pair skew	<6inches
Max length (coupled traces) TX and RX	<6 inches (When PCIE3.0 operates only in PCIE 2.0 mode, the allowable trace length <8 inches, and it is necessary to ensure that the impedance of the pathway meets requirements, especially at the locations of connector pads, capacitors, etc.)
AC coupling capacitors	220nF $\pm 20\%$, discrete 0201 package preferable
Minimum airgap between pair to pair	Recommend ≥ 5 times the width of the trace
Max intra-pair skew of REFCLK	<12mil
Trace Impedance of REFCLK	$100\Omega \pm 10\%$ differential
Minimum airgap between PCI-E and other Signals	Recommend ≥ 5 times the width of PCI-E trace.
Maximum allowed via	Recommend ≤ 2 vias

Place GND through via in BGA zone as showed below and recommend to follow ground shielding guideline in Section 3.2, item (24), GND via interval length should less than 300mil.

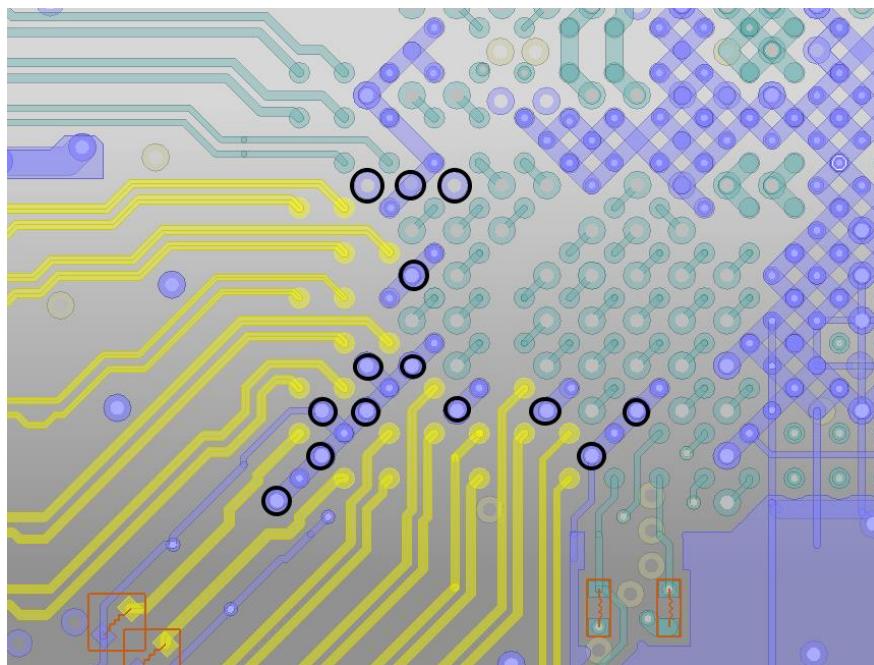


Figure 3-162 GND through via placement in BGA zone

3.4.7 HDMI 2.0 RX

Table 3-21 Layout Requirements for HDMI2.0 RX

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential
Max intra-pair skew	<6mil
Max mismatch between clock and data pairs	<480mil
Max length on carrier board	<6 inches
Minimum airgap between pair to pair	Recommend ≥ 5 times the width of HDMI trace. At least 4 times the width of HDMI trace.
Minimum airgap between HDMI and other Signals	Recommend ≥ 5 times the width of HDMI trace. At least 4 times the width of HDMI trace.
Maximum allowed via	Recommend ≤ 2 vias

3.4.8 HDMI 2.1

Table 3-22 Layout Requirements for HDMI2.1

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential
Max intra-pair skew	<6mil
Max mismatch between pairs	<480mil
Max trace length on carrier board	<4 inches
AC coupling capacitors	220nF $\pm 20\%$, discrete 0201 package preferable

Parameter	Requirement
Minimum airgap between pair to pair	Recommend ≥ 7 times the width of HDMI trace
Minimum airgap between HDMI and other Signals	Recommend ≥ 7 times the width of HDMI trace
Maximum allowed via	Recommend novias
ESD	Typical I/O-to-GND Capacitance $\leq 0.2\text{pF}$

(1) Place GND through via in BGA zone as showed below and recommend to follow ground shielding guideline in Section 3.2, item (24), GND via interval length should less than 150mil.

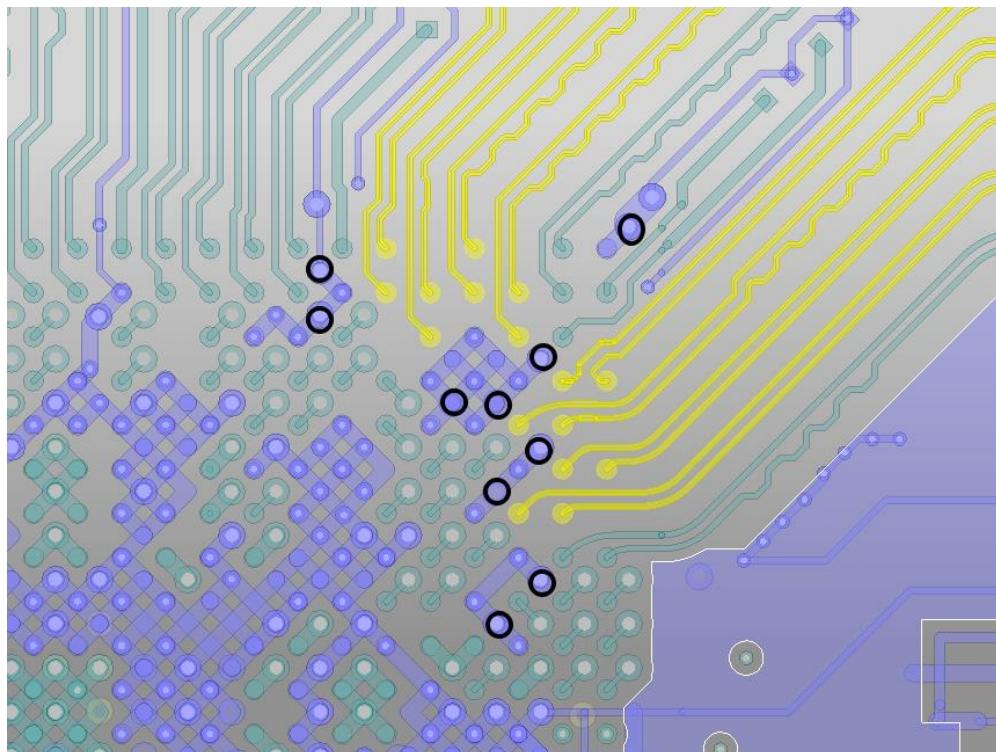


Figure 3-163 GND through via placement in BGA zone

(2) Trace between DC blocking capacitor and resistor should be routed as differential pair.

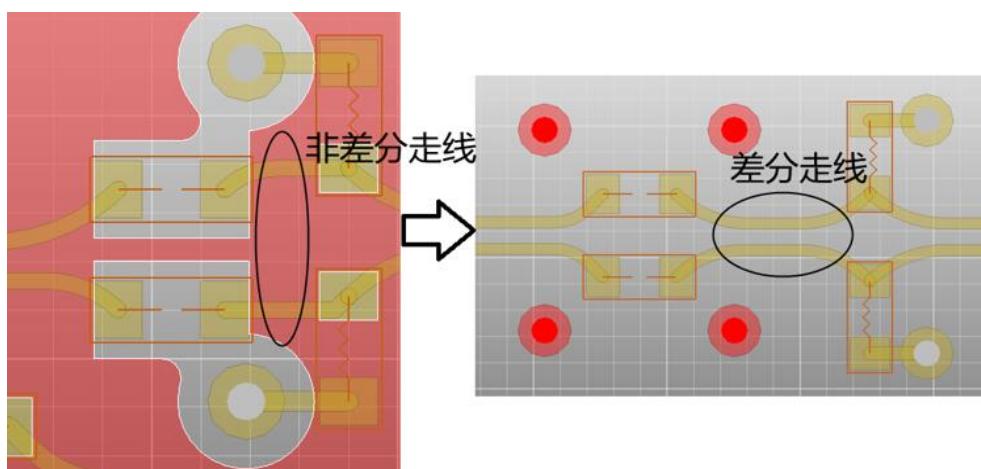


Figure 3-164 Route as differential pair

(3) Void reference plane under 590ohm resistor's pad. Keep no stub between trace and resistor pads.

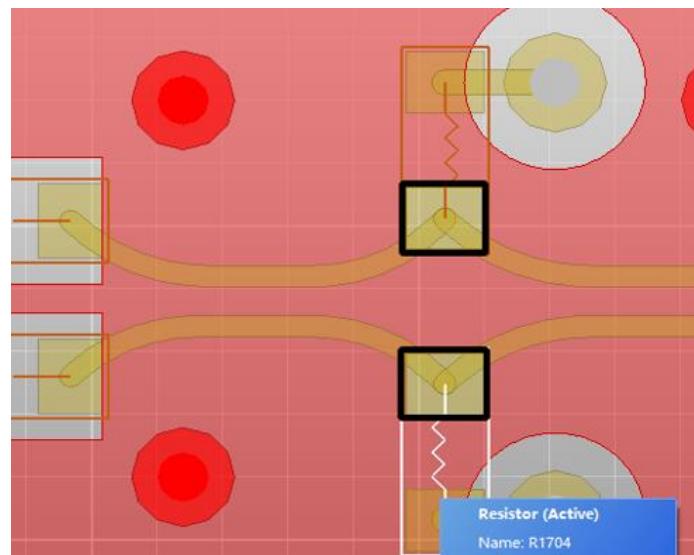


Figure 3-165 590ohm resistor layout diagram

3.4.9 SATA 3.0

Table 3-23 Layout Requirements for SATA3.0

Parameter	Requirement
Trace Impedance	100Ω ±10% differential (100 Ohm target impedance is preferred ,if stackup limits, 100 Ohm can not meet,at least meet 90 Ohm ±10%)
Max intra-pair skew	<6mil
Max trace length on carrier board	<6 inches
AC coupling capacitors	10nF ±20%, discrete 0201 package preferable
Minimum airgap between pair to pair	≥4 times the width of SATA trace.
Minimum airgap space between SATA and other Signals	≥4 times the width of SATA trace.
Maximum allowed via	Recommend≤ 2 vias

3.4.10 USB 2.0

Table 3-24 Layout Requirements for USB2.0

Parameter	Requirement
Trace Impedance	90Ω ±10% differential
Max intra-pair skew	<20mil
Max trace length on carrier board	<6 inches
Maximum allowed via	Recommend less than 4 vias Cannot exceed 6 vias

3.4.11 USB 3.0

Table 3-25 Layout Requirements for USB3.0

Parameter	Requirement
Trace Impedance	$90\Omega \pm 10\%$ differential
Max intra-pair skew	<6mil
Max trace length on carrier board	<6 inches
AC coupling capacitors	100nF $\pm 20\%$, discrete 0201 package preferable
Minimum airgap between pair to pair	≥ 4 times the width of USB trace.
Minimum airgap between USB and other Signals	≥ 4 times the width of USB trace.
Maximum allowed via	Recommend less ≤ 2 vias

3.4.12 MIPI-D/C PHY

Table 3-26 Layout Requirements for MIPI-DPHY

Parameter	Requirement
Trace Impedance	$100\Omega \pm 10\%$ differential (if stackup limits, 100 Ohm can not meet, at least meet $95\Omega \pm 10\%$. 100 Ohm is preferred first)
Max intra-pair skew	<6mil
Data to clock matching	<12mil
Max trace length	<6 inches
Maximum allowed via	4
Minimum airgap between pair to pair	Recommend ≥ 4 times the width of MIPI trace. At least 3 times the width of MIPI trace.
Minimum airgap between MIPI and other Signals	Recommend ≥ 4 times the width of MIPI trace. At least 3 times the width of MIPI trace.

Table 3-27 Layout Requirements for MIPI-CPHY

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Max intra-pair skew(TRIO_A\TRIO_B\TRIO_C)	< 6 mil
Inter-pair skew(TRIO0\TRIO1\TRIO2)	<100mil
Max trace length	<5 inches
Maximum allowed via	2
Airgap between Signals	Recommend ≥ 4 times the width of MIPI trace.
Minimum airgap between MIPI and other Signals	Recommend ≥ 4 times the width of MIPI trace.

Place GND through via in BGA zone as showed below.

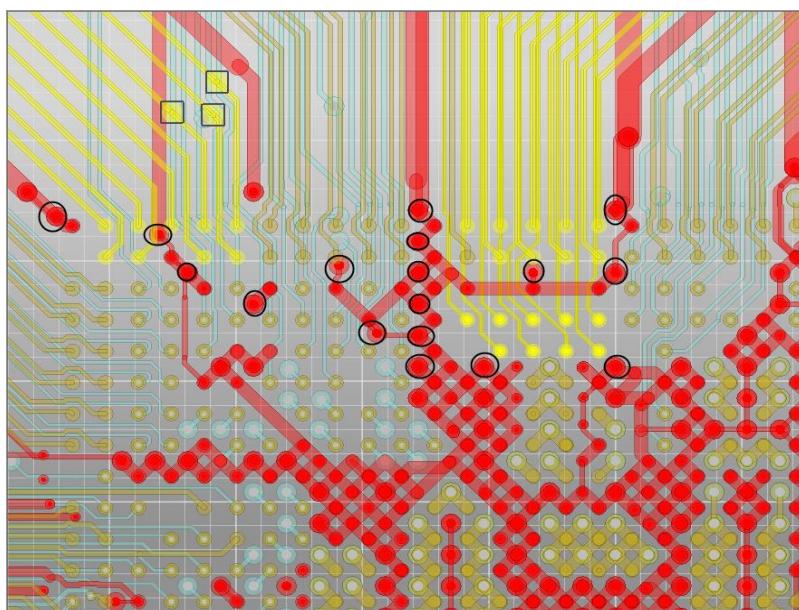


Figure 3-166 GND through via placement in BGA zone

3.4.13 eDP

Table 3-28 Layout Requirements for EDP

Parameter	Requirement
Trace Impedance	$90\Omega \pm 10\%$ differential (make sure EDP cable impedance is same as PCB)
Max intra-pair skew	<6mil
Max trace length on carrier board	<6 inches
Minimum airgap between pair to pair	≥ 4 times the width of EDP trace.
AC coupling capacitors	$220nF \pm 20\%$, discrete 0201 package preferable
Minimum airgap between EDP and other Signals	≥ 4 times the width of EDP trace.
Maximum allowed via	Recommend ≤ 2 vias

3.4.14 eMMC

Table 3-29 Layout Requirements for eMMC

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock matching	<120mil
Max trace length	<3.5 inches
Minimum airgap of eMMC Signals	At least 2 times the width of eMMC trace.
Minimum airgap between eMMC and other Signals	Recommend 3 times the width of eMMC trace. At least 2 times the width of eMMC trace.
Maximum allowed via	Recommend ≤ 4 vias

EMMC signal should route with reference to ground plane, and place stitching via within 30mil (center-to-center) of the signal transition vias. Via-stitch should able to connect both reference plane to ensure continuous grounding.

3.4.15 SDMMC

Table 3-30 Layout Requirements for SDMMC

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<120mil
Max trace length	<4 inches
Minimum airgap of SDMMC Signals	At least 2 times the width of SDMMC trace.

3.4.16 SDIO

Table 3-31 Layout Requirements for SDIO

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<120mil
Max trace length	<4 inches
Minimum airgap of SDIO Signals	At least 2 times the width of SDIO trace.

3.4.17 FSPI

Table 3-32 Layout Requirements for FSPI

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<200mil
Max trace length	<4 inches
Minimum airgap of FSPI Signals	At least 2 times the width of FSPI trace.

3.4.18 BT1120

Table 3-33 Layout Requirements for BT1120

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
Data to clock mismatch	<180mil
Max trace length	<5 inches
Minimum airgap of BT1120 Signals	Recommend 2 times the width of BT1120 trace.

3.4.19 RGMII

Table 3-34 Layout Requirements for RGMII

Parameter	Requirement
Trace Impedance	$50\Omega \pm 10\%$ single ended
(TXD{0-3},TXEN) to TXCLK mismatch	<120mil
(RXD{0-3},RXDV) to RXCLK mismatch	<120mil
Max trace length	<5 inches
Minimum airgap of RGMII Signals	At least 2 times the width of RGMII trace.
Minimum airgap between RGMII and other Signals	Recommend 3 times the width of RGMII trace. At least 2 times the width of RGMII trace.

3.4.20 Audio Interface Circuit PCB Design

For the digital audio interface of the RK3588 platform, the wiring requirements are as follows:

- All CLK signals are recommended to be connected in series with a 22ohm resistor and placed close to the RK3588 to improve signal quality;
- All CLK signal traces can not be next to each other to avoid crosstalk; independent grounding is required, and the grounded traces must have ground vias within 300mil intervals;
- The decoupling capacitors of each IO power domain of the chip must be placed on the back of the corresponding power pins; for single-sided stickers, they should be placed near the chip;
- For the case where one I2S interface is connected to multiple devices, the related CLks should be connected according to the daisy chain wiring topology;
- For the case where one PDM interface is connected to multiple devices, the related CLks should be connected according to the daisy-chain routing topology; if GPIOs are abundant, both CLks in a group of PDM interfaces can be used to optimize the routing branching;
- It is recommended that the SPDIF signal be grounded throughout the process, and the grounded traces must have ground vias within 300 mils.

For the relevant audio signal routing requirements of peripherals, the design guidelines of the corresponding device shall prevail. If there is no emphasis, please refer to the following instructions:

- The SPKP/SPKN signal of the speaker is coupled and routed, and the whole group is grounded. The line width is calculated according to the output peak current, and the line is shortened as much as possible to control the line resistance;
- If the power amplifier output of the speaker is placed with magnetic beads, LC filters and other devices, it is recommended to place it close to the power amplifier output to optimize EMI;
- The left and right channel outputs of the Headphone should be independently grounded to avoid crosstalk and optimize isolation. It is recommended that the trace width be greater than 10mil;
- When the microphone is single-ended connected, the MIC signal is routed separately and wrapped separately;

- When the microphone is connected differentially, especially in most cases of pseudo-differential, it should also be routed according to the differential, and the whole group should be grounded;
- The recommended line width of the microphone signal is more than 8mil;
- All audio signals should be based on high-speed signal lines such as LCD and DRAM. It is forbidden to route the adjacent layers of high-speed signal lines, the adjacent layer of audio signals must be the ground plane, and it is forbidden to punch holes and change layers near the high-speed signal lines;
- All audio signal traces should be kept away from inductive areas, away from RF signals and devices;
- For the TVS protection diodes of the headphone holder and microphone, place them as close as possible to the connection base, and the signal topology is: headphone holder/microphone→TVS→IC; in this way, when an ESD phenomenon occurs, the ESD current is attenuated by the TVS device first; There should be no residual piles. It is recommended to increase the ground vias as much as possible for the ground pins of TVS, and ensure at least two vias of 0.4mm*0.2mm to enhance the electrostatic discharge capability.

3.4.21 WIFI/BT PCB Design

- In the overall layout, the WIFI module should be properly placed, and the module should be far away from DDR, HDMI, USB, LCD circuits, speakers and other easily interfered modules or connectors;
- No trace is allowed on the TOP layer below the module. Make sure that the reference plane is a complete ground plane. It is recommended that SDIO/PCIe/UART/PCM signal trace bypass the projection area of the module and connect to the module pins;
- Give priority to the crystal circuit layout which should be on the same layer as the chip and placed as close as possible to avoid vias. The crystal traces should be as short as possible, away from interference sources and antenna area as far as possible;
- The crystal and clock signals need to be surrounded by ground throughout the whole process. At least one GND via is added to the ground trace every 100 mils, and the ground reference plane of the neighboring layer must be complete;
- If the crystal circuit layout is placed on a different layer from the chip, the crystal traces must be surrounded by ground all the way to avoid interference;
- 32.768k is routed separately and surrounded by ground, and at least one GND via is added every 400 mil for the ground trace;
- For SDIO WIFI, please refer to chapter 3.4.16 requirements for PCB design requirements of SDIO signal;
- For PCIe WIFI, please refer to chapter 3.4.5 or 3.4.6 for PCIe signal PCB design requirements;
- When layout the inductance of the module, please note that after the trace comes out through the inductance, it passes through the capacitor first, and then enters the module power pin;

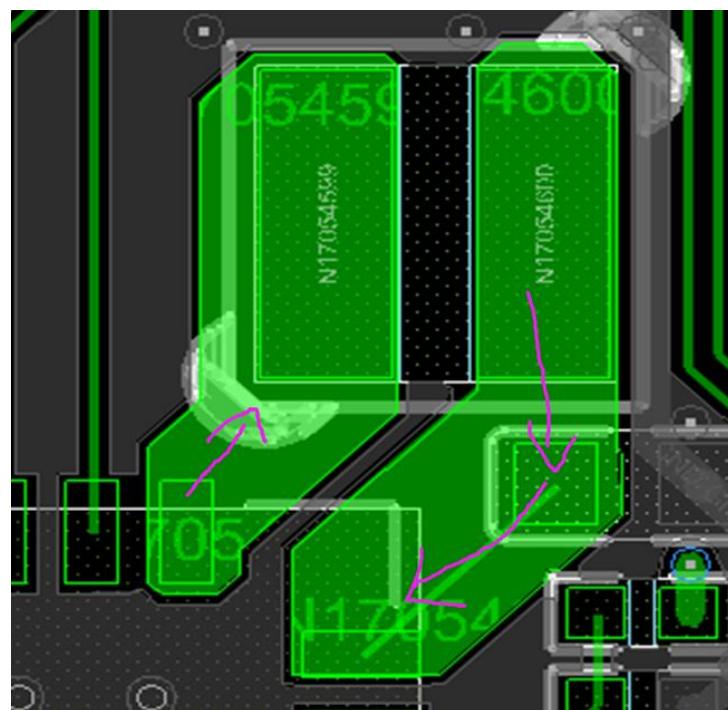


Figure 3-167 Schematic Diagram of the Inductor and Capacitor Wiring of the WIFI Module

- The power decoupling capacitor of the module must be close to the power pin of the module;
- The width of the VBAT pin trace of the module must be greater than 40mil;
- The longer the antenna trace, the greater the energy loss. Therefore, in the design, the antenna path should be as short as possible. There should be no branches, and try not to change layers;
- The antenna matching circuit must be close to the antenna connector, and the antenna trace must be 50 ohms to ensure that the reference ground is complete, the impedance does not change suddenly, and no other signal traces or power sources are allowed below; the accompanying ground of the trace needs to be connected to the main ground reference plane by ground wall;

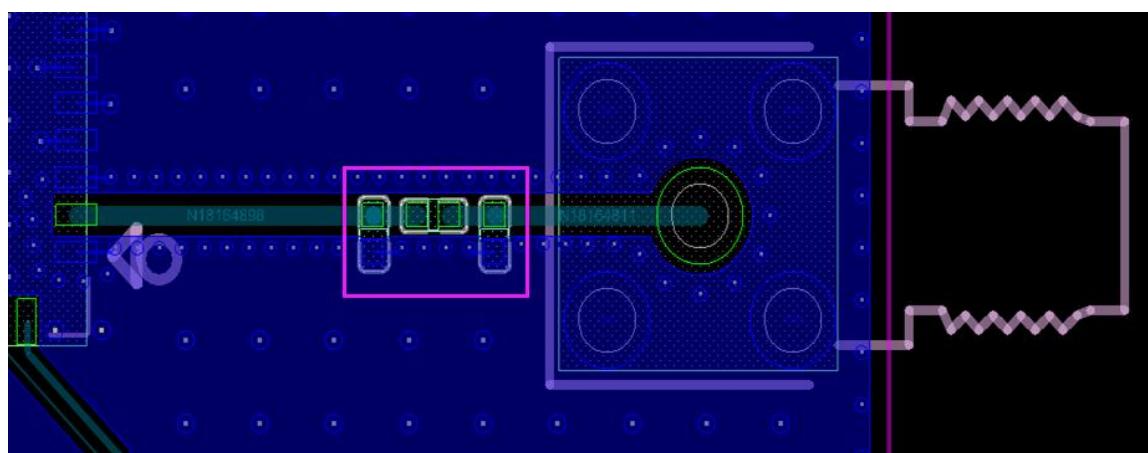


Figure 3-168 Schematic Diagram of WIFI Module Antenna Wiring

- The antenna of the module and all layers below the antenna routing area are not allowed to other signal traces or power sources;
- If it is a 2X2 MIMO antenna interface, the exit direction between the two antenna ports has to consider

the location of the two antennas where should be as far away as possible to avoid interference, and vertical placement is recommended to avoid mutual interference.

3.4.22 VGA OUT PCB Design

- In the overall layout, the VGA connector should be placed as close to the conversion chip as possible, and the VGA analog signal trace should be shortened as much as possible.
- The decoupling capacitors for the power supply of the conversion chip should be placed as close as possible to the power supply pins of the conversion chip.
- The VGA_R/G/B trace width should be as thick as possible, and it is recommended to be more than 12mil.
- The length difference between VGA_R/G/B must not exceed 200mil
- VGA_R/G/B 75ohm resistor must be placed close to the chip
- The VGA_R/G/B filter circuit must be placed close to the VGA connector
- VGA_R/G/B signals are required to be surrounded by ground separately in the whole process, and there must be ground vias within 300 mils of the ground traces.
- The neighboring layer of VGA_R/G/B signal must be ground plane instead of power plane
- Keep VGA_R/G/B signals away from high-speed signal lines such as LCD, DRAM, etc. It is forbidden to route on the neighboring layers of high-speed signal trace; it is forbidden to drill vias to change layers near high-speed signal traces; do not route through inductance areas; keep away from RF signals and devices.
- The RC filter of VGA_HSYNC/VSYNC must be placed close to VGA connector, and the trace must not exceed 6 inches
- All signal TVS diode of VGA connector should be placed as close as possible to the connector. The signal topology is: VGA socket → TVS → chip pins; when an ESD phenomenon occurs, the ESD current must be attenuated by the TVS device first; There should not be stubs on the TVS device trace.
- It is recommended to increase the ground vias as much as possible for the ground pins of TVS, at least two 0.4*0.2mm vias should be guaranteed to strengthen the electrostatic discharge capability

3.4.23 LCD Screen and Touch Screen PCB Design

- Please place the current limiting resistor on the FB side of the LED backlight IC close to the screen connector instead of DC-DC.
- For backlight boost circuit, please pay attention to capacitor placement and power supply trace to ensure that the power supply's charging and discharging loop is minimized.
- If there are reserved test points for the screen and touch screen connectors, they should be close to the connector and the stub on the trace should be as short as possible.

3.4.24 Camere PCB Design

- When the camera is with a connector: when the MIPI differential signal passes through the connector, the GND pin must be used for isolation between neighboring differential signal pairs;
- For CIF/MIPI and other signals, if there is a board-to-board connection is realized through the connector,

it is recommended that all signals be connected in series with a certain resistance (between 2.2ohm-10ohm as long as it can meet the SI test), and reserved TVS device;

- If the camera connector has reserved test points, it should be close to the connector and the stub on the trace should be as short as possible;
- The decoupling capacitors of the AVDD/DOVDD/DVDD power supply of the connector should be placed as close to the camera connector as possible;
- The camera layout needs to be far away from high-power radiating devices, such as GSM antennas;
- Please refer to section 3.4.12 for MIPI CSI RX signal PCB design requirements.

4 Thermal Design Suggestion

Good thermal design is especially important for the improvement of RK3588 product performance, system stability, and product safety

4.1 Thermal Simulation Result

For the RK3588 FCBGA1088_23x23mm_Pitch 0.65mm package, the EVB-based 10-layer PCB adopts Finite Element Modeling (FEM), and the simulation report of thermal resistance can be obtained. This report is based on the JEDEC JESD51-2 standard. The system design and environment of the application may be different from the JEDEC JESD51-2 standard, and it needs to be analyzed according to the application conditions.



Note!

Thermal resistance is the reference value when there is no radiator on PCB. The detailed temperature is related to the board's size, thickness, material and other physical factors.

4.1.1 Result Overview

Thermal resistance simulation results are as follows:

Table 4-1 RK3588 Thermal Resistance Simulation Report Results

Package (EHS-FCBGA)	θ_{JA} (°C/W)	θ_{JB} (°C/W)	θ_{JC} (°C/W)
JEDEC PCB	8.7	3.5	0.12

Note: The simulated data is only used for reference only.

4.1.2 PCB description

The PCB structure used for thermal resistance simulation is as follows:

Table 4-2 RK3588 PCB Structure used for Thermal Resistance Simulation

JEDEC PCB	PCB Dimension(L x W)	101 x 114mm
	PCB Thickness	1.6mm
	Number of Cu Layer	10-layers

4.1.3 Terms Interpretation

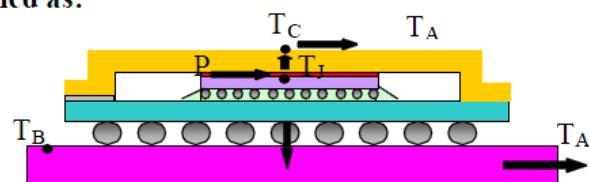
Terms in this chapter are explained below:

- T_j : The maximum junction temperature;
- T_a : The ambient or environment temperature;
- T_c : The maximum compound surface temperature;
- T_b : The maximum surface temperature of PCB bottom;
- P : Total input power.

The thermal parameter can be define as following

1. Junction to ambient thermal resistance, θ_{JA} , defined as:

$$\theta_{JA} = \frac{T_J - T_A}{P}; \quad (1)$$



Thermal Dissipation of EHS-FCBGA

Figure 4-1 θ_{JA} Definition

2. Junction to case thermal resistance, θ_{JC} , defined as:

$$\theta_{JC} = \frac{T_J - T_C}{P}; \quad (2)$$

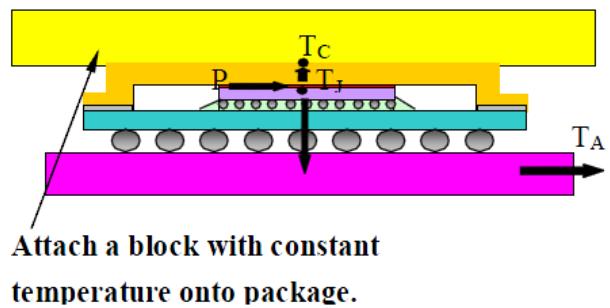


Figure 4-2 θ_{JC} Definition

3. Junction to board thermal resistance, θ_{JB} , defined as:

$$\theta_{JB} = \frac{T_J - T_B}{P}; \quad (3)$$

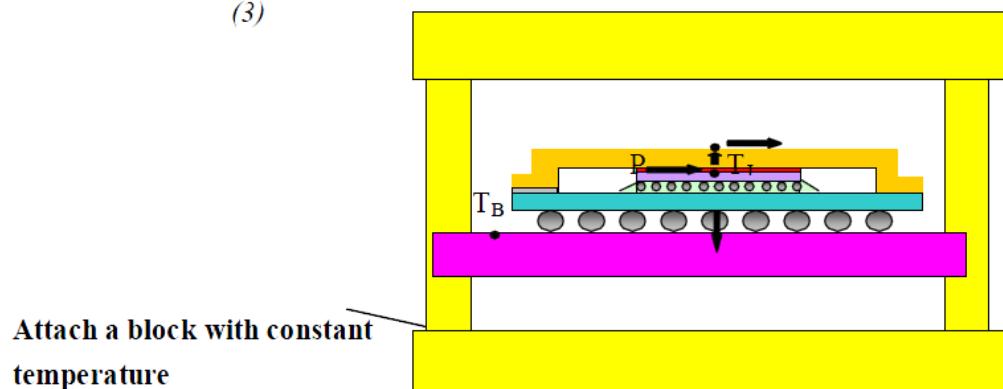


Figure 4-3 θ_{JB} Definition

4.2 Thermal Control Method Inside the Chip

4.2.1 Thermal Control Strategy

In Linux kernel, it defines one thermal control frame called Linux Generic Thermal System Drivers, which can control system temperature through different strategies. Currently below 3 strategies are commonly used:

- Power_allocator: Introduce PID (percentage-integral-differential) control to dynamically allocate power for cooling device according to current temperature, when the temperature is low, the power that can be allocated is larger, that is, the frequency that can be operated is higher. As the temperature rises, the power that can be allocated is gradually reduced, and the frequency that can be operated is gradually reduced, so as to achieve the effect of limiting frequency according to temperature.
- Step_wise: Limit frequency step by step according to current temperature.
- Fair share: The cooling devices with more frequency gears will give priority to frequency reduction
- Userspace: Do not limit frequency.

There is a T-sensor inside the RK3588 to detect the on-chip temperature, and the Power_allocator strategy is used by default

4.2.2 Temperature Control Configuration

The RK3588 SDK can provide temperature control strategies for CPU and GPU respectively. For specific configuration, please refer to "Rockchip_Developer_Guide_Thermal_CN.pdf".

<https://redmine.rock-chips.com/projects/fae/documents>

4.3 Thermal Design Reference

4.3.1 Circuit Schematic Thermal Design Reference

- Under the condition of stability, provide overall power efficiency, such as using as less as high-voltage LDOs, and reduce the heat generated by the power supply itself during the power conversion process;
- According to actual products, try not to supply power to the modules that are not used by the chip or do power down processing by software;
- Choose a material with a large thermal conductivity, and re-estimate the size of the radiator to be used according to the product definition, usage environment and other conditions. It is recommended to use a larger radiator as much as possible.

4.3.2 PCB Thermal Design Reference

For RK3588 products, RK3588 chip is the device that generates the most heat, so all heat dissipation treatments should be based on the chip.

Except RK3588, other main heating devices include: PMIC, charging IC and related inductors, backlight IC and related inductors.

- Reasonable structural design can ensure that there is a heat exchange path between the internal machine and air;

- In the overall layout, the components with high power consumption or heat generation should be uniformly distributed to avoid local overheating. It is recommended RK3588 and RK806 should be placed appropriately, not too close or too far away. It is recommended that the distance between the two is 20mm-50mm. Avoid to place them on the edge of the board, for bad heat dissipation;
- It is recommended to use a 8-layer board or more to increase the copper of the board as much as possible. It is recommended to use a copper thickness of 1oz, and try to use much ground layers as possible. Other layers should follow the power and signal routing rules, and try to place as much ground copper as possible, with the help of a large area of copper for dissipates heat;
- RK3588 VDD_LOGIC, VDD_GPU, VDD_NPU, VDD_CPU, VCC_DDR, VDD_LIT have relatively large currents, the routing or copper must meet the current-carrying capacity, otherwise it may increase the temperature rise;
- For chips with EPAD, drill as many vias as possible on the EPAD, the neighboring layer must be a ground layer, and the copper on the back side should be as complete as possible. It is recommended that the copper on the back should be bare copper, which is good for heat dissipation;
- The GND pins of RK3588 chip is routed in "井" shape on the top layer and are cross-connected. It is recommended that the trace width is 10mil, which is beneficial to the heat dissipation of the chip;
- For the GND pin of RK3588 chip, it is recommended to try to ensure that each ball has a corresponding ground via. At least ensure that every 1.5 ball corresponds to one via to increase the heat conduction path. The neighboring layer must be a ground layer, which is good for heat dissipation of the chip;
- For decoupling capacitor ground pad on the back of RK3588 chip, it is recommended to use full copper covering, do not use flower holes to connect, try to make the ground copper as complete as possible to improve heat dissipation;
- In empty areas, without damaging the power layer, try to increase ground vias and increase heat conduction paths to improve heat dissipation.

5 ESD/EMI Protection Design

5.1 Overview

This chapter provides ESD/EMI protection design suggestion for RK3588 product design to help customers to improve anti-static and anti-electromagnetic interference ability of product.

5.2 Terms Interpretation

Terms of this chapter are explained as below:

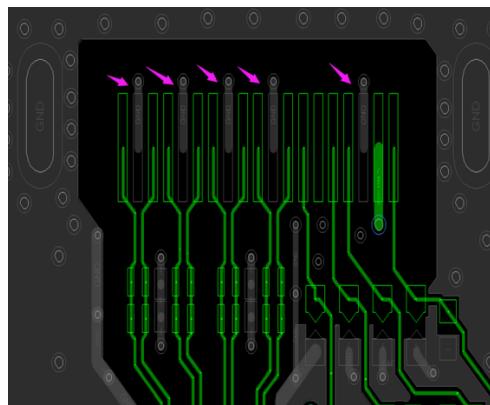
- ESD: Electro-Static discharge
- EMI: Electromagnetic Interference, including conduction interference and radiation interference

5.3 ESD Protection

- Ensure reasonable mold design, retract connectors in the shell as much as possible, so that the distance from static electricity to the internal circuit becomes longer and the energy becomes weaker. The test standard changes from contact discharge conditions to air discharge, etc.
- Protect and isolate sensitive components in PCB layout.
- Try best to put the RK3588 and core components in the center of PCB layout. If it may not be able to put them in the center, ensure that the shielding cover has 2mm distance at least from the board edge and is connected to GND safely
- PCB layout is based on function module and signal flow direction, sensitive components should be mutually independent, and it is better to isolate the parts that are easy to produce interference;
- Place ESD components reasonably. Generally place them near the source, that is, place ESD components in the junction or where electrostatic discharge.
- The layout of the components should be far away from the edge of the board and a certain distance from the connector
- The PCB surface should have a good GND loop, and each connector should be with good GND connection loop on the surface. If there is a shielding cover, it should be connected to the surface ground as much as possible, and drill as much ground vias at the soldering place of the shielding cover as possible. In order to do this, it is required that each connector should not be routed on the surface, and there should not be traces with surface copper cut off in a large area;
- Do not go through the edge of surface layer and make as many ground vias as possible.
- Isolate signal from ground if necessary.
- Expose GND copper of PCB as much as possible, in order to strengthen the electrostatic discharge effect, or to facilitate to add foam and other remedial measures
- If there is a board-to-board connection through the connector, it is recommended that all signals be connected in series with a certain resistance (between 2.0ohm-10ohm, as long as it can meet the SI test), and reserved TVS devices, which can improve antistatic surge capacity
- The 100nF capacitor of the nPOR pin of RK3588 must be placed close to the pin, and the ground pad of

the capacitor must be with a 0402 ground vias. It is recommended to use more than two grounding vias for better grounding if space allowed.

- The distance between key signals such as Reset, clock, interrupt and other sensitive signals from the edge of the board should not be less than 5mm
- If other peripheral chips have Reset pins, it is recommended to add a 100nF capacitor close to the pin. The ground pad of the capacitor must be with a 0402 ground vias. It is recommended to use more than two grounding vias for better grounding if space allowed.
- When the whole device is designed as a ground-floated device, it is recommended not to design each interface with separate ground.
- When the device casing is metal, with a three holes power, and the metal casing must be well connected to the ground.
- Reserve the shielding cover position. The shielding cover should be connected to the surface ground as much as possible, and drill as much ground vias at the soldering place of the shielding cover as possible. In order to do this, it is required that each connector should not be routed on the surface, and there should not be traces with surface copper cut off in a large area.
- Isolate from PCB, so that static electricity can only be released in some areas, such as the ground pin of the connector is connected with the inner layer through a separate vias, keep out the surface PCB, and keep the surface ground copper and pins as far away as possible, that is, keep sensitive signals away from electrostatic discharge areas (surface copper), etc., as shown in the figure, isolate the distance between HDMI signal and GND on the surface.



5.4 EMI Protection

- Electromagnetic interference has three factors: interference sources, coupling channels and sensitive devices. We have no way to deal with sensitive devices, so EMI problem can only start with interference sources and coupling channels. The best way to resolve EMI issues is to eliminate interference source. If it cannot eliminate, try to cut off coupling channels or avoid antenna effect;
- It is difficult to eliminate interference source on PCB. We can take actions such as filtering, grounding, balancing, resistance controlling, improving signal quality (e.g. termination connection) etc. Generally several methods will be applied together, but the basic requirement is good grounding;
- The commonly used EMI materials include shielding cover, special filter, resistor, capacitor, inductor, magnetic bead, common mode choke/magnetic ring, wave-absorbing material, spread frequency device

etc;

- The rules to select filters: if the load (receiver) is high resistance (regular single ended signal interface is high resistance, such as SDIO, RBG, CIF etc.), select capacitive filter components and parallel connect to circuit; if the load (receiver) is low resistance (such as power output interface), select inductive filter component and serial connect to circuit. After using the filter device, the signal quality cannot exceed its SI permission. Differential interface usually uses common mode choke to suppress EMI;
- The shielding measures on PCB should have good grounding, otherwise it will cause radiation leakage or form antenna effect. The shielding of connectors should comply with relevant technical standards;
- RK3588 spread spectrum function is divided into modules. The degree of spreading depends on the signal requirements of the relevant part. See RK3588 spreading instructions for detailed measures;
- It is recommended to keep the matching resistance of all clocks connected in series, which will provide matching impedance, and improve the improvement measures of signal quality;
- At the DC power input, the common mode inductance or EMI filter of the power supply can be reserved if possible;
- Add reserved common mode inductance or filter circuit at USB, HDMI, VGA, screen connector and other interfaces;
- When a radiator is added, it should be noted that the radiator may also couple EMI energy and generate radiation. When selecting a radiator, in addition to meeting the thermal design requirements, it should also meet the EMI test requirements. Grounding conditions should be reserved for the radiator. When grounding is required, the radiator should be grounded. It is not easy to clarify the number of grounding points and how to choose the grounding point. It needs to be adjusted according to the actual test of the first version of hardware in the laboratory.
- EMI has the same high requirement as ESD on layout. The ESD Layout requirements described above are mostly suitable for EMI protection. Besides, add the following requirements:
 - Try best to ensure the integrity of the signal;
 - Differential line should in equal length and be tight coupling to ensure the symmetry of the differential signal, minimize the misplacement of differential signals to avoid EMI problems caused by phase mismatch;
 - Components with metal shell such as plug-in electrolytic capacitors should avoid coupling interference signals to radiate. Also need to avoid component interference signals coupling from shell to other signal lines;
 - The matching resistors of all clocks connected in series should be placed close to CPU (source end), and traces between CPU pins and the resistors must be controlled within 400 mils;
 - If the PCB exceeds 4 layers, it is recommended that all clock signals go to the inner layer as much as possible;
 - To prevent power radiation, the copper of the power supply layer must be retracted, with one H (the thickness of the medium between the power supply and ground) as the unit, and it is recommended to indented by 20H.

6 Soldering Process

6.1 Overview

RK3588 are ROHS certified products, that is, they are all Lead-free products. This chapter regulates basic temperature settings of each period when customers use the chipset to SMT. It mainly introduces process control when using RK3588 chipset to do reflow soldering: lead-free process and mixed process.

6.2 Terms Interpretation

Terms in this chapter are explained below:

- Lead-free: Lead-free process;
- Pb-free: Pb-free process, all devices (main board, all ICs, resistors and capacitors, etc.) are lead-free devices, and the lead-free solder paste are used in the pure lead-free process;
- Reflow profile: reflow soldering
- Restriction of Hazardous Substances (ROHS): instructions for restricting use of certain hazardous components in electrical and electronic equipment;
- Surface Mount Technology(SMT);
- Sn-Pb: Sn-Pb mixing process refers to using lead solder paste and a mixed soldering process with both lead-free BGA and lead IC;

6.3 Reflow Soldering Requirements

6.3.1 Solder Paste Composition Requirements

The proportion of solder alloy and flux is 90%: 10%; volume ratio: 50%: 50%, solder paste refrigerating temperature is 2~10°C, it should be returned to normal temperature before use, and the return time should be 3~4 hours and the time should be recorded.

The solder paste needs to be stirred before brushing, manual stirring for 3 to 5 minutes or mechanical stirring for 3 minutes. After stirring, it will flow naturally.

6.3.2 SMT Profile

Since RK3588 chipset are made of environmental protection materials, Pb-Free process is recommended. The reflow profile shown below is only recommended for JEDEC J-STD-020D process requirements, and customers need to adjust according to actual production conditions.

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak		
Temperature min (T_{smin})	100 °C	150 °C
Temperature max (T_{smax})	150 °C	200 °C
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L)	183 °C	217 °C
Time at liquidous (t_L)	60-150 seconds	60-150 seconds
Peak package body temperature (T_p)*	See classification temp in Table 4.1	See classification temp in Table 4.2
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Figure 6-1 Reflow Soldering Profile Classification

Package Thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Figure 6-2 Heat Resistance of Lead-Free Process Device Packages Standard

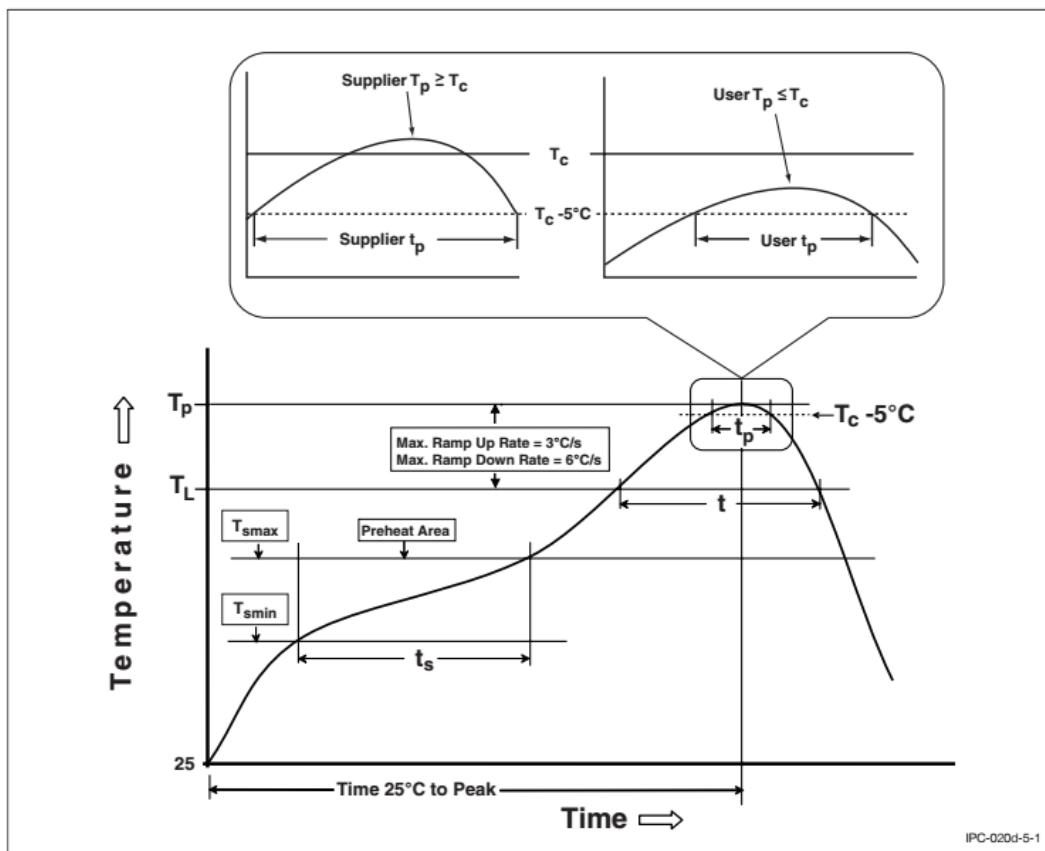


Figure 6-3 Lead-free Reflow Profile

6.3.3 SMT Recommendation Profile

The SMT profile recommended by RK is shown in Figure 6-4:

Step 1 Board Preheat	Step 2 Soak Time	Step 3 Peak Reflow & Time Above 220 °C	Step 4 Cool Down
Start with solder joint temp \leq 40°C	After nozzle is lowered prior to peak reflow (Soak Time: Paste dependant; consult paste manufacturer)	Solder Joint Temp 230 – 250°C Above \geq 217°C 60 – 90 sec Max delta-t of solder joint temperature at peak reflow \leq 10°C	Substrate MAX Temperature \leq 260°C Die Peak Temperature \leq 300°C
Rising Ramp Rate 0.5 – 2.5° C/ Sec.	Solder Joint Temp: 200 to 220°C		Cooling Ramp Rate -0.5 to – 2.0°C/sec
Board Preheat Solder Joint Temp: 125 – 150°C	Critical Ramp Rate (205 to 215°C): 0.35 – 0.75°C/sec.	Peak Temp Range, and Time Above \geq 217°C spec's met.	PCB land/pad temperature needs to be at 100 – 130°C \pm 5°C when removing board from rework machine bottom heater at end of component removal operation or \leq 80°C when using stand alone PCB Pre-Heater for PCB land/pad site dress operation.
Preheat with bottom heater, before nozzle is lowered	Nozzle has lowered to reflow component	Nozzle is down during peak reflow	Nozzle raises to home position when solder joint reaches peak temp range

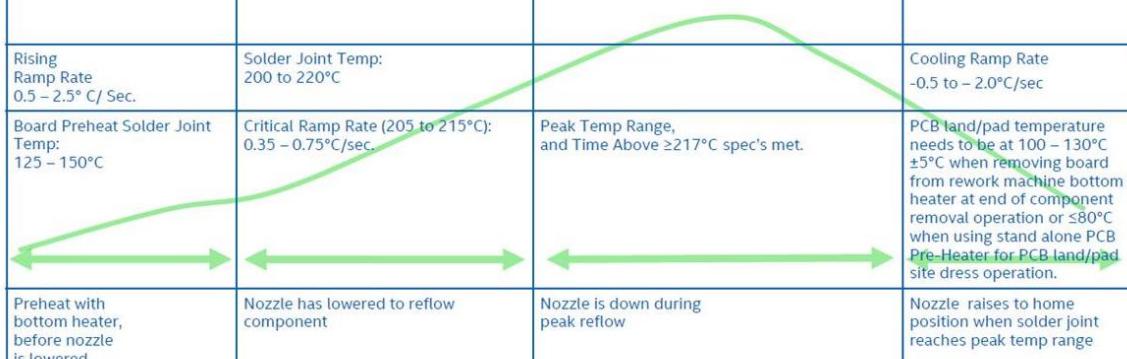


Figure 6-4 Lead-Free Reflow Soldering Process Recommended Profile Parameters

7 Packages and Storage Conditions

7.1 Overview

This chapter introduces the storage and directions for RK3588 usage to ensure the safety and correct usage of products.

7.2 Terms Interpretation

Terms in this chapter are explained below:

- Desiccant: a material used to adsorb moisture
- Floor life: the maximum time products are allowed to be exposed to environment, from before unpacking moisture barrier bag to reflow soldering
- HIC: Humidity Indicator Card
- MSL: Moisture Sensitivity Level
- MBB: Moisture Barrier Bag
- Rebake: to bake again
- Solder Reflow
- Shell Life
- Storage environment

7.3 Moisture Packages

The dry vacuum package material of product is shown as follows:

- Desiccant
- Six-point humidity card
- Moisture barrier bag: aluminum foil, silver opaque, with a mark of moisture sensitivity level

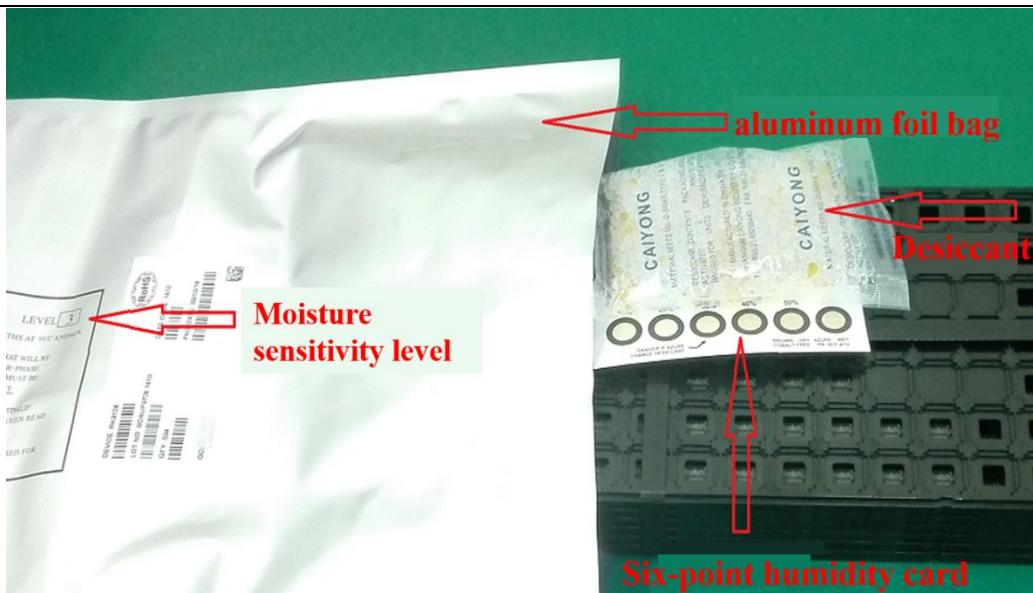


Figure 7-1 Chipset Dry Vacuum Package

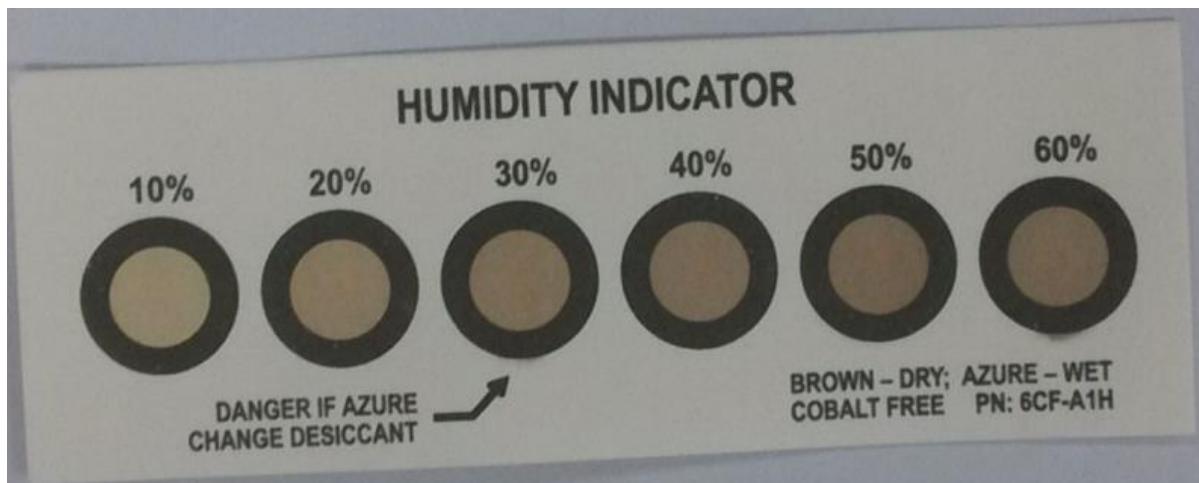


Figure 7-2 Six-Point Humidity Card

7.4 Product Storage

7.4.1 Storage Environment

The product is stored in vacuum packaging, and the storage time can reach 12 months when the temperature is $\leq 40^{\circ}\text{C}$ and the relative humidity is $<90\%$.

7.4.2 Exposure Time

For environmental conditions: $<30^{\circ}\text{C}$ and humidity 60%, please refer to Table 7-1 below.

The MSL level of RK358

8 chipset is 3 and is very sensitive to humidity. If package is not used in time after unpacking, and if it is not baked and directly SMT after being left for a long time, there will be a high probability of chip failure.

Table 7-1 Moisture Sensitivity Levels (MSL)

MSL Level	Exposure time Factory environmental conditions: $\leq 30^{\circ}\text{C}$ /60%RH	
	Unlimited at $\leq 300^{\circ}\text{C}$ /85 %RH	
2	1 year	
2a	4 week	
3	168 hours	
4	72 hours	
5	48 hours	
5a	24 hours	
6	Mandatory bake before use, and must be reflowed within the time limit specified on the label	

7.5 Usage of Moisture Sensitive Products

After RK3588 packages are opened, it must meet the following conditions before reflow soldering:

- Continuous or cumulative exposure time is within 168 hours, and factory environment is $\leq 30^{\circ}\text{C}/60\%$ RH;
- Stored in $<10\%$ RH environment;

Chips must be baked to remove internal moisture under the following conditions to avoid layered or popcorn problems during reflow:

- When humidity indicator card is at $23 \pm 5^{\circ}\text{C}$, $>10\%$ points have changed color. (Please refer to humidity indicator cards for color change);
- Does not meet the specifications of 2a or 2b;

Please refer to Table 7-2 below for the time for chip re-baking:

Table 7-2 RK3588 Re-bake Reference Table

Package Body	MSL	High Temp Bake @ 125°C $+10/-0^{\circ}\text{C}$		Medium Temp Bake @ 90°C $+8/-0^{\circ}\text{C}$		Low Temp Bake @ 40°C $+5/-0^{\circ}\text{C}$	
		Exceeding Floor Life by $> 72\text{h}$	Exceeding Floor Life by $\leq 72\text{h}$	Exceeding Floor Life by $> 72\text{h}$	Exceeding Floor Life by $\leq 72\text{h}$	Exceeding Floor Life by $> 72\text{h}$	Exceeding Floor Life by $\leq 72\text{h}$
Thickness $\leq 1.4\text{mm}$	3	9 hours	7 hours	33 hours	23 hours	13 days	9 days



Note

The Table shows the minimum baking time necessary after damp.

Low temperature baking is preferred.