VERIFICATION PLAN

AHB-Lite Interface

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AHB-Lite Protocol:

AHB-Lite implements the features required for HIGH-performance, HIGH clock frequency systems including:

- burst transfers.
- single-clock edge operation.
- non-tristate implementation.
- wide data bus configurations, 64, 128, 256, 512, and 1024 bits.

The most common AHB-Lite slaves are internal memory devices, external memory interfaces, and HIGH bandwidth peripherals. Although LOW-bandwidth peripherals can be included as AHB-Lite slaves, they typically reside on the AMBA Advanced Peripheral Bus (APB) for system performance reasons. Bridging between this HIGHer level of bus and APB is done using a AHB-Lite slave, known as an APB bridge. The bus interconnect logic consists of one address decoder and a slave-to-master multiplexor. The decoder monitors the address from the master so that the appropriate slave is selected and the multiplexor routes the corresponding slave output data back to the master. Figure 1-1 shows a single master AHB-Lite system design with one AHB-Lite master and three AHB-Lite slaves.

- **Global Signals:**

Name	Destination	Description
HCLK	Clock source	Clock source for all operations on the protocol. Input signals are sampled at rising edge and changes in output signals happen after the rising edge
HRESTn	Reset Controller	Asynchronous primary reset for all bus elements

- **Master Signals:**

Name	Destination	Description
HADDR [31:0]	Slave and Decoder	Address bus of 32 bits
HBURST [2:0]	Slave	Indicates the type of burst signal including wrapping and incrementing bursts
HSIZE [2:0]	Slave	Indicates the size of transfer from 8 bits to 1024 bits

- **Slave Signals:**

Name	Destination	Description
HRDATA [31:0]	Multiplexor	Read data bus to transfer the data from

		a Slave's location to the Master via multiplexor
HREADYOUT	Multiplexor	Indicates transfer has finished on the bus and is used to extend the data phase
HRESP	Multiplexor	Provides additional information that the transfer was successful or failed

- **Decoder Signals:**

Name	Destination	Description
HSELx Note: x is a unique identifier for AHB lite slave	Slave	Indicates current transfer is for intended for selected slave

- **Multiplexor Signals:**

Name	Destination	Description
HRDATA [31:0]	Master	Read data bus to rout to Master
HREADY	Master and Slave	Indicates completion of previous transfer
HRESP	Master	Transfer response

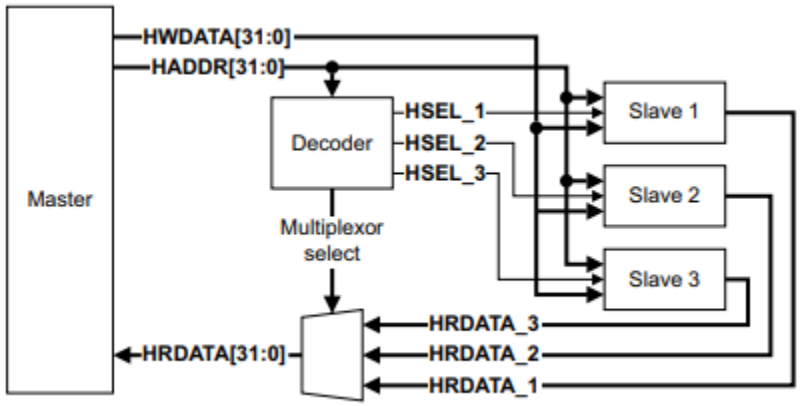
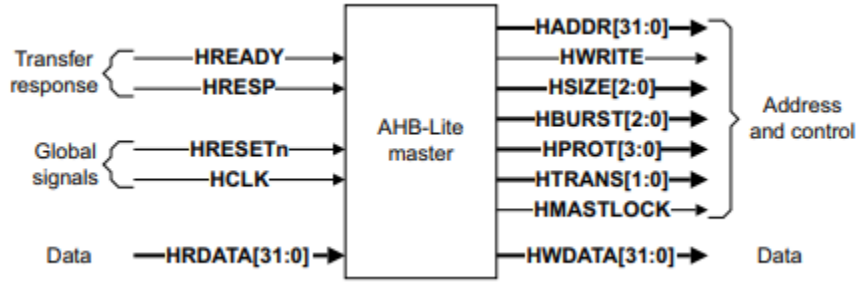


Figure 1.1



Working Protocol:

The transfer is started by the master when it drives the address and control signals. These signals provide information about the address, direction, width of the transfer, and indicate if the transfer forms part of a burst.

Transfers can be of different types for example: single, incrementing bursts that do not wrap at address boundaries, wrapping bursts that wrap at particular address boundaries, etc. The write data bus moves data from the master to the destination slave, and the read data bus moves data from a slave towards the master.

Every transfer consists of two phases:

1. **Address phase**: one cycle for address and control
2. **Data phase**: one or more cycles for the data.

The address phase is for only one cycle. A slave cannot request for the address phase to be extended. Therefore all slaves must be capable of sampling the address during this time. However, a slave can request that the master extends the data phase by using HREADY. This signal when LOW, causes wait states to be inserted into the transfer and enables the slave to have extra time to process or sample data.

The slave uses a response signal HRESP to indicate the success or failure of a transfer.

Verification Plan:

No.	Feature	Test Description	Ref.	Type	Results	Comments
1	Write Transfer from Master to Slave	When **HWRITE** is HIGH then the Master will broadcast the data on the HWDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping types.	3.1	TR		Successful write. **HRESP** should be LOW **HREADY** should be HIGH
2	Read Transfer from Slave to Master	When **HWRITE** is LOW then the slave must generate the data on the HRDATA [31:0] bus for individual burst types i.e., HBURST [2:0] including incrementing and wrapping type.	3.1	TR		Successful read. **HRESP** should be LOW **HREADY** should be HIGH
3	Write-Read Transfer	Write transfer followed by Read transfer at a particular address A.	3.1	TR		**HRESP** is LOW, **HREADY** is HIGH The address location must have the updated

						value
4	Read-Write Transfer	Read transfer followed by Write transfer at a particular address A.	3.1	TR		**HRESP** is LOW, **HREADY** is HIGH The slave must return the previous Data (A).
5	Continuous writing to the same slave (same address)	When **HWRITE** is HIGH, the Master will broadcast the data packets on the HWDATA [31:0] bus.	3.1	TR		Successful write. **HRESP** should be LOW **HREADY** should be HIGH for the successive data packets
6	Continuous reading from the same slave (same address)	When **HWRITE** is LOW, the slave must generate the data packets on the HRDATA [31:0] bus.	3.1	TR		Successful read. **HRESP** should be LOW **HREADY** should be HIGH for the successive data packets
7	Global Signal: **HCLK**	A clock signal is generated in the top module	7.1.1	A		All input signals must be sampled at the rising edge of the clock and changes in the output signals must occur after the rising edge.
8	Global Signal: **HRESTn**	It is an active LOW signal. When asserted then it must reset all bus elements. Note: Slaves must ensure that **HREADYOUT** is HIGH. **HTRANS** [1:0] must indicate **IDLE**.	7.1.2	TR		All previous binary information in the bust elements will be lost.
9	Master Signal: IDLE HTRANS [1:0] =b00	When **IDLE** transfer is inserted to an address, the slave should not do any action on that address for the IDLE signal.	3.2	TR		The **HREADY** must be LOW during the **IDLE** transfer. The transfer must be ignored by the slave. Slave must provide an **OKAY** response.
10	Transfer type changed during waited states: Scenario 1	Transfer type changes from **IDLE** to **NONSEQ** during waited states. The HTRANS signal must be kept constant after the transition until **HREADY** is HIGH	3.6.1	A		Successfully transfer type changed. Slave must give **OKAY** response.
11	Transfer type changed during waited states:	Transfer type changes from **BUSY** to **SEQ** during waited states for fixed length bursts.	3.6.1	A		Successfully transfer type changed. Slave must give an

	Scenario 2	The **HTRANS** signal must be kept constant after the transition until **READY** is HIGH				**OKAY** response.
12	Transfer type changed during waited states: Scenario 3	Transfer type changes from BUSY to any other type during waited states for undefined length burst. The burst continues if an **SEQ** transfer is performed but terminates if an **IDLE** or **NONSEQ** transfer is performed.	3.6.1	A		Successfully transfer type changed. Slave must give an **OKAY** response.
13	Transfer type changed during waited states: Scenario 4	Any scenario other than scenario 1 2 and 3 for example Transfer type changed from **IDLE** to **SEQ**.	3.6.1	A		Slave will give an **ERROR** response.
14	Slave response: Transfer done	Transfer is completed successfully.	5.1.1	A		Slave must give **HREADY** HIGH **HRESP** OKAY
15	Slave response: Transfer pending	Transfer is pending	5.1.2	A		Slave must give **HREADY** LOW **HRESP** OKAY
16	Slave response: transfer failed	Transfer is not completed successfully	5.1.3	A		**HRESP** must be HIGH. Two cycle response is required for an error condition.
17	HREADYOUT	When HIGH the transfer has finish on bus	2.3	A		When HIGH, the HREADYOUT signal indicates that a transfer has finished on the bus. This signal can be driven LOW to extend a transfer.
18	HREADY	When HIGH, the HREADY signal indicates to the master and all slaves, that the previous transfer is complete	2.5 6.1.1	A		If the transfer is extended than the master must hold the valid data until the transfer completes, as indicated by HREADY HIGH