A Robust 12-Transistor Hybrid GDI D-Flip-Flop in 16nm CMOS via Channel Length Engineering

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***Abstract*—The relentless scaling of semiconductor technology has intensified the demand for area- and power-efficient digital circuits for AI and IoT applications. This paper proposes a novel 12-transistor hybrid D-Flip-Flop (DFF) using the Gate Diffusion Input (GDI) technique. The architecture combines GDI multiplexers with CMOS inverters to achieve the area benefits of GDI while ensuring a full-swing output. A key contribution of this work is a detailed investigation into the circuit's robustness on advanced process nodes. We demonstrate that using the minimum channel length in a 16nm High-Performance (HP) process leads to circuit failure. As a solution, we show that by engineering the transistor geometry—specifically by increasing the channel length to 22nm while remaining on the 16nm HP process—these detrimental short-channel effects are mitigated. This optimized design achieves robust operation and demonstrates superior performance in power and area compared to both conventional CMOS and standard GDI implementations, achieving a 99.5% power reduction and 94.3% area reduction over the standard CMOS baseline.**

***Index Terms*—Gate Diffusion Input (GDI), D-Flip-Flop, Low-Power Design, Short-Channel Effects, 16nm CMOS, VLSI, Transistor Sizing.**

I. Introduction

With the proliferation of high-performance SoCs in IoT, wearable devices, and AI, the key performance indicators of operating speed, power consumption, and chip area have become critical design constraints. In many modern processors, sequential logic elements like D-Flip-Flops (DFFs) can consume over 20% of total power and occupy up to 40% of the total chip area. Therefore, optimizing DFF design is paramount for achieving power and area efficiency in complex digital systems. Conventional DFFs in standard cell libraries are typically implemented using tri-state gate (TSG) or pass-transistor gate (PTG) logic, requiring between 24 and 28 MOS transistors. The Gate Diffusion Input (GDI) technique presents an alternative logic design methodology. However, GDI suffers from degraded voltage swing. To address this limitation, we propose a novel *hybrid GDI D-Flip-Flop* that utilizes GDI multiplexers with CMOS inverters to restore a full voltage swing. This innovative structure requires only 12 transistors and does not require an inverted clock (CLKB) signal, simplifying the clock distribution network.

II. Background: GDI vs. Standard CMOS

The GDI method is a novel technique for low-power digital circuit design. A basic GDI cell consists of a single NMOS and PMOS transistor, as shown in Fig. 1(b), unlike a standard CMOS inverter (Fig. 1a). The primary drawback of pure GDI logic is its vulnerability to threshold voltage (V_T) drop, which compromises signal integrity. Our hybrid approach directly solves this problem by using CMOS inverters as an output buffer to restore the full rail-to-rail signal swing.

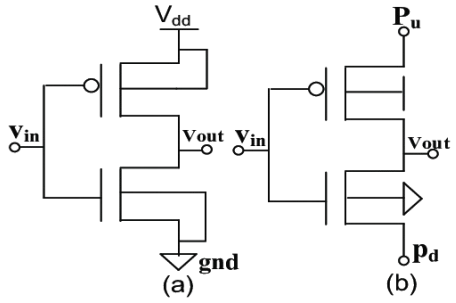

Fig. 1. Comparison of (a) a standard CMOS Inverter and (b) a basic GDI cell.

III. Proposed Hybrid D-Flip-Flop Architecture

To harness the benefits of GDI while mitigating its drawbacks, we employ a hybrid architecture for our DFF design. The proposed DFF is built on a master-slave topology, as shown in the block diagram in Fig. 2. The core of this design consists of two GDI multiplexers (MUXs) and two pairs of cross-coupled CMOS inverters. The entire DFF is implemented with only 12 transistors. When the clock (CK) is low, the master stage passes the input signal D; when CK transitions high, a slave stage passes the stored value to the output Q. This structure uses CMOS inverters to ensure a full VDD-to-GND swing, restoring signal integrity.

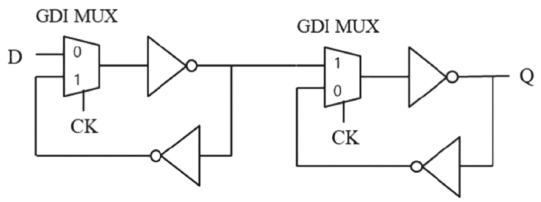

Fig. 2. Block diagram of the proposed 12-transistor Hybrid GDI D-Flip-Flop.

IV. Implementation and Results

The proposed design was implemented and simulated to verify its performance. The transistor-level implementation of the architecture from Fig. 2 is shown in Fig. 3. This section details the critical choice of process technology and transistor geometry, presenting the final optimized performance benchmarks.

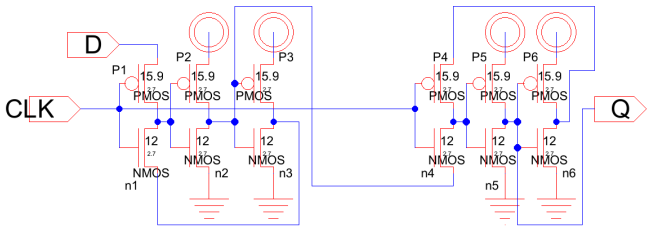

Fig. 3. Transistor-level implementation of the Hybrid GDI D-Flip-Flop.

A. Process and Transistor Geometry Analysis

A key finding of this work is that the hybrid GDI topology's performance is highly dependent on both the chosen process technology and the transistor channel length (L). Our analysis reveals a trade-off between the benefits of technology scaling and the challenges of short-channel effects.

First, we found that **Low-Power (LP) process models consistently failed** across all nodes. LP processes use a higher threshold voltage (Vth0) to save power, which weakens transistor drive strength. In our sensitive GDI circuit, these weaker transistors could not hold the output state firmly against leakage and noise, leading to distorted waveforms.

Second, an important discovery was made when using **High-Performance (HP) models**. While the 32nm and 22nm HP processes worked with adjusting the length, simulating the design on the **16nm HP process with its minimum channel length ($L = 16$nm) resulted in circuit failure**, as shown in Fig. 5. Despite the high drive current of HP transistors, the extremely short channel length led to severe leakage and threshold voltage problems, causing a collapse in signal integrity.

To solve this, we engineered the transistor geometry. By fabricating the design on the **16nm HP process but increasing the channel length to $L = 22$nm**, we successfully mitigated the detrimental short-channel effects. The longer channel reduces leakage current and restores signal integrity, resulting in a clean, robust waveform as seen in Fig. 4. This optimized approach allows us to leverage the speed and density of the 16nm process while ensuring the circuit's functional correctness.

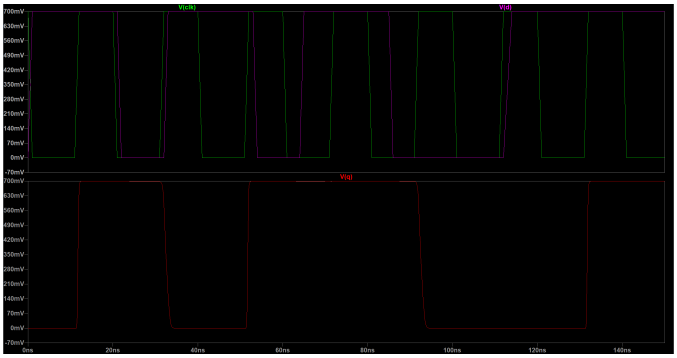

Fig. 4. Successful operation on 16nm HP process with channel length engineered to L=22nm.

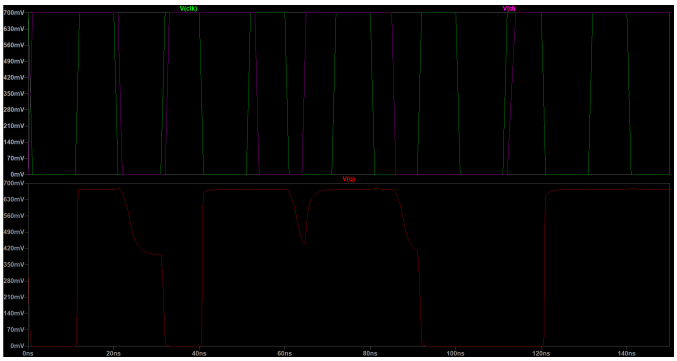

Fig. 5. Circuit failure on 16nm HP process with minimum channel length (L=16nm) due to signal integrity collapse.

B. Performance Benchmarks

The final design was simulated in LTspice using the selected 16nm HP process with a 22nm transistor channel length. Table I presents a three-way comparison of our optimized Hybrid GDI design against baseline values for a standard GDI design and a conventional CMOS design. The results clearly show the superiority of our approach in the critical metrics of power and area, especially considering our design operates at a much lower voltage of 0.7V.

The percentage improvements are summarized in Table II. The power-delay trade-off is a key aspect of this design. The significant reduction in power consumption is primarily due to the lower operating voltage and the use of longer channel transistors, which reduces leakage.

TABLE I
Performance Comparison of D-Flip-Flop Designs

Parameter	Standard CMOS (1.2V)	GDI (1.2V)	Hybrid GDI (0.7V)
Transistor Count	24-28	14-16	**12**
Power (Dynamic)	304.56 μW	65.57 μW	**1.58 μW**
Delay (Clock to Q)	760.67 ps	589.5 ps	**3540 ps**
Layout Area	7.5 μm^2	3.0 μm^2	**0.429 μm^2**

TABLE II
PERCENTAGE IMPROVEMENT OF HYBRID GDI DESIGN

Parameter	vs. Standard CMOS	vs. GDI (Baseline)
Power (Dynamic)	99.5% Reduction	97.6% Reduction
Layout Area	94.3% Reduction	85.7% Reduction

However, these same factors increase the propagation delay, as the transistors have a weaker drive strength at a lower voltage and take longer to charge and discharge load capacitances. This trade-off is fundamental in low-power design, where achieving minimal power often comes at the cost of speed.

C. Layout Implementation

The layout for the 12-transistor hybrid GDI DFF was created using the Electric VLSI Design System and is shown in Fig. 6. The final layout dimensions are 800nm x 536nm, yielding an exceptionally small area of 0.429 μm^2. During the layout phase, the transistor widths were fine-tuned from the initial schematic values (i.e., Wp/Wn of 15.9/12) to new scaled values (16.1 for PMOS, 12.3 for NMOS) to compensate for parasitic capacitances and resistances introduced by the physical interconnects, ensuring the post-layout performance matched the design goals. Post-layout simulations, shown in Fig. 7, verify that the circuit maintains correct functionality after these adjustments.

Detailed timing analysis from the post-layout simulation reveals a clock-to-Q rise time ($T_{CQ,rise}$) of 2.06 ns and a fall time ($T_{CQ,fall}$) of 3.54 ns. This asymmetry is expected and arises from the different electrical paths the signal takes during a low-to-high versus a high-to-low output transition. The effective resistance and capacitance of the pull-up network (dominated by PMOS transistors) and the pull-down network (dominated by NMOS transistors) are not identical in this complex sequential cell, leading to the variance in propagation delay.

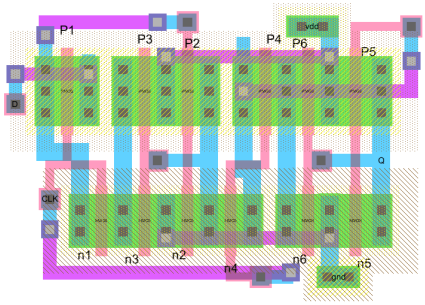

Fig. 6. Layout of the 12-transistor Hybrid GDI D-Flip-Flop.

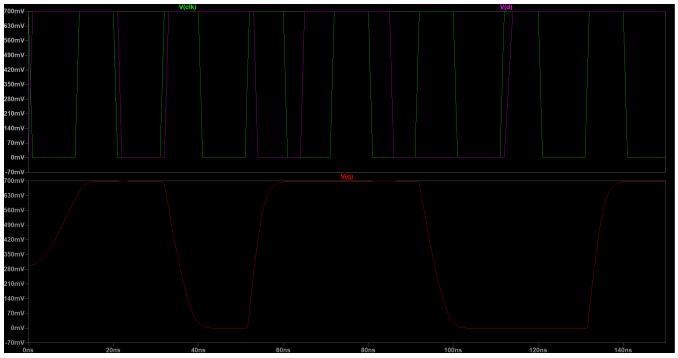

Fig. 7. Post-layout simulation waveform of the optimized GDI D-Flip-Flop.

V. DESIGN PHILOSOPHY AND APPLICATIONS

The design methodology presented in this paper intentionally targets a specific corner of the power-performance-area (PPA) design space. Rather than seeking a balanced compromise, our approach aggressively prioritizes the minimization of dynamic power and physical area. The resulting increase in propagation delay is a calculated trade-off, positioning this D-flip-flop as a highly specialized solution. Consequently, it is exceptionally well-suited for energy-starved applications where device longevity and form factor are the primary figures of merit, and high-speed operation is a secondary concern. Such use cases are prevalent in battery-powered IoT devices, wearable sensors, and various embedded microcontroller systems.

VI. CONCLUSION

This paper presented a novel 12-transistor hybrid GDI D-Flip-Flop and demonstrated a critical design methodology for implementing such sensitive topologies on advanced CMOS nodes. We confirmed that simply scaling to a smaller process node with minimum feature sizes is not always viable; our initial design failed on the 16nm HP process due to severe short-channel effects. The key contribution of this work is our proposed solution: by engineering the transistor geometry and increasing the channel length to 22nm while utilizing the 16nm HP process, we successfully overcame the signal integrity issues. This optimized approach creates a robust DFF that benefits from the high performance of the 16nm node while mitigating its drawbacks. The final design achieves an exceptional 94.3% reduction in layout area and a 99.5% reduction in power compared to its standard CMOS equivalent, proving that thoughtful co-design of circuit topology and transistor geometry is essential for developing next-generation, ultra-low-power circuits.

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