BIRZEIT UNIVERSITY

FACULTY OF ENGINEERING & TECHNOLOGY
ELECTRICAL AND COMPUTER ENGINEERING DEPARTMENT
ADVANCED DIGITAL DESIGN ENCS3310
COURSE PROJECT

Instructors: Abdellatif Abu-Issa & Elias Khalil

Objective:

The task is to design a structural comparator for signed and unsigned number and then to write a complete code for verification. You should search for information about the needed logic/circuits to implement a comparator for signed and unsigned numbers.

The Task:

Your task is to structurally create a comparator for signed numbers (2's complement representation) and unsigned numbers. The circuit will have the following main inputs and outputs

1- First number A: 6 bits
2- Second number B: 6 bits
3- Selection S: 1 bit to select how to consider the numbers (signed or unsigned) and thus how comparator will work
4- First output "Equal" : will produce 1 if A=B.
5- Second output "Greater": will produce 1 if A>B.
6- Third output "Smaller": will produce 1 if A< B.

The Comparator is to be built **structurally from a library of gates**, which contains the following devices:

Gate\ID	0	1	2	3	4	5	6	7	8	9
INV	1	2	1	2	3	4	3	1	4	2
NAND	2	3	3	4	4	5	5	5	6	7
NOR	2	3	4	4	4	5	5	5	6	7
AND	3	4	4	5	6	7	8	6	9	8
OR	3	4	5	5	6	7	8	6	9	8
XNOR	4	5	6	7	8	9	10	8	10	9
XOR	5	6	7	8	9	10	12	9	13	10
Your UDP (Max inputs = 4)	6	7	8	9	10	11	12	10	13	12

All combinational parts of your design should be built structurally from these basic gates and the defined delays (consider that the delay will not change even if the gate has more than 2 inputs).

After that registers should be added to the inputs/outputs of the circuit to make the circuit synchronous (thus, we need to add more inputs such as clk).

You should determine the maximum latency of the comparator. And therefore, what is the maximum frequency of the clock that can be applied to the registers. You should verify that your system is working for all possible values of the inputs. Also, you should introduce

an error in your design and to do a verification that will discover the error and write it to the console screen.

Format of the report:

This project should be written as **formal report.** The report should include sections on the following:

- Brief introduction
- Brief theoretical overview
- Design philosophy
- Simulation Results
- Conclusion and Future works

The report shouldn't exceed **10 pages (excluding the code)** with

- 1.5 line spacing.
- Times new roman.
- Font = 12 point

The code and report should be sent on Ritaj before deadline.

Key Points:

- Any type of plagiarism will be penalized by **0** mark, and the cheaters will be treated according to the university laws.
- The design description should include a block diagram of the design, and give a justification of the decisions made.
- Technical achievement in design is linked to the degree of functionality that was attempted.
- Technical achievement in implementation is based on the quality of your Verilog code. This includes issues such as legibility of code, use of meaningful variable names, good comments, clear structure, and modifiability of the design.
- Technical achievement in evaluation is based on the quality of your simulation results.

Deadline:

- The report + Code should be submitted before the end of Sunday 22/12/2024.
- Late submission is penalized at a rate of 10% marks per day. Late Submission is open till Wednesday 1/1/2025.

Assessment Form (Feedback) :

The following is the assessment form for this project.

Computer Systems Engineering Department
Project Assessment Feedback
Advanced Digital Design (ENCS3310)
Instructors: Abdellatif Abu-Issa & Elias Khalil

	Marks
Report Presentation (10%) Language (Spelling and Grammar), style of the report, caption of figures, page numbering…etc.	
Design Process and Outcome (70%)	
• Description of the system and design process **(20%)**	
• Technical Achievement in System Design and Evaluation **(50%)**	
Judgement and Creativity (20%) Demonstration of good judgment, imagination and creativity in selecting and applying design methods. Good discussion and analysing of the system and suggested improvements.	
Total Mark (Out of 100)	
Deducted Marks: ☐ late days * 10% per day	
FINAL ALLOCATED MARK (Out of 100)	

Any evidence for any type of cheating: yes no