DEPT. OF ELECTRICAL AND COMPUTER ENGINEERING AMERICAN UNIVERSITY OF BEIRUT

EECE320 – Digital Systems Design QUIZ II – FALL 2009

NAME:			
ID:			

INSTRUCTIONS:

- THE EXAM IS CLOSED BOOK/CLOSED NOTES.
- THE DURATION IS 2.0 HOURS.
- CALCULATORS ARE NOT ALLOWED.
- CELL PHONES ARE NOT ALLOWED IN THE EXAMINATION ROOM.
- WRITE YOUR NAME AND ID NUMBER IN THE SPACE PROVIDED ABOVE.
- PROVIDE YOUR ANSWERS IN THE SPACE PROVIDED ON THE QUESTION SHEET.
- THE SCRATCH BOOKLET WILL NOT BE CONSIDERED IN GRADING.
- BE AS NEAT AND CLEAR AS POSSIBLE.

Problem	Total Points	Earned Points
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
9	10	
10	10	
	100	

1.	Use a 1 to 8 de-multiplexer to build a 3-input decoder.
•	Here the decoder from problem 1 and OD cotes to implement a 2 hit prime number detector sireuit. Deminder the
2.	Use the decoder from problem 1 and OR gates to implement a 3-bit prime number detector circuit. Reminder: the number 1 is not prime.
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2.	The number 1 is not prime.
2.	the decoder from problem 1 and OK gates to implement a 3-out prime number detector effects. Reminder, the number 1 is not prime.

3.	A) Draw a tri-state buffer and explain how it works.B) Draw a 1-bit transceiver and its control and explain how it works.
	b) Draw a 1-bit transcerver and its control and explain now it works.
4	Consider a 4x1 PLA with 4 product terms.
.,	Minimize and implement using this PLA the sum of product function $S_{w,x,y,z}(1,3,4,5,9,11,12,13,14,15)$

5.	Let A and B be two 8 outputs a 1 when A is	3-bit positive binary nuis larger or equal to B.	mbers. Use an itera	tive circuit to design	ı a magnitude comp	parator that

6.	Show how to build a D fli	p-flop using a T flip-flo	p with enable and com	binational logic.

7.	Explain the concept of metastability in S-R flip-flop. Give an example.
8.	Show how to build an edge-triggered S-R flip-flop using an edge-triggered D flip-flop and combinational logic Assume that a combination of S=1 and R=1, does not change the state.
	The same that the same and the same and the same same.

9.	Design a synchronous state machine with two inputs x and y. The output z is to be '1 when the inputs x and y ar the same a multiple of 3 times.

10.	Design a synchronous state machine with one input signal x and one output signal y. The state machine is to detect a sequence of '1100 on input x and to output a '1 for one cycle on y when the sequence is detected.