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Design of Pass Transistor-Based Low-Power Approximate Adders for DSP Application

Khaled Hasan[1], Sidrat Muntaha Nur Pranto[2], Shuvankar Biswas[3], Fajla Rabby[4], Md. Atiqur Rahman[5], Md. Anwarul Abedin[6]
[1,2,3,4,5,6]*Department of Electrical and Electronic Engineering*
Dhaka University of Engineering & Technology, Gazipur, Bangladesh
khaledbd61@gmail.com, prantosid@gmail.com, shuvankar85@outlook.com, rfajla7@gmail.com, atiqurrahman.et.1997@gmail.com, abedin@duet.ac.bd

***Abstract*— This paper presents a low-power, and energy-efficient pass transistor-based full adder, along with two other approximate adders sharing the same constructional pattern. Initially, three conventional full adders are analyzed, namely the mirror adder, XOR and XNOR-based adder circuits. Based on these circuits, a new energy-efficient 12T full adder is designed that consumes much less power compared to conventional full adder circuits. The design is implemented in 45nm technology with a +0.8 V supply voltage. Schematic simulations in Cadence Virtuoso tools showed a 60%-85% improvement in power consumption compared to previously stated conventional adders. Furthermore, the research extends to the development of two innovative approximate adder designs that demonstrate remarkable improvements in power efficiency while maintaining an acceptable level of accuracy. Finally, a comparative analysis of conventional approximate full adders proved our proposed approximate adders outperformed existing ones, in terms of power consumption, power delay product, and bit error rate.**

Keywords*— Low power, Power Delay Product, Approximate Adders, Bit Error Rate.

I. Introduction

In recent years, advancements in technology have led to a surge in the popularity of portable electronic devices such as smartphones, laptops, and personal gadgets. This has made it essential to prioritize low-power, high-speed, and small-chip areas in VLSI circuits and systems. Arithmetic units are a vital part of all stated devices and full adder circuits are the building blocks of most of the arithmetic units. Hence, developing the performance of a full adder can have a significant impact on the advancement of integrated circuits (IC) [1].

In widespread applications where precision and reliability are essential, the conventional full adder is commonly employed. However, for purposes of optimizing energy efficiency or speed, an alternative approach can be utilized called approximate adder, which deliberately introduces errors. Approximate computing trades accuracy for efficiency and is gaining prominence for applications like digital signal processing (DSP), multimedia, audio processing, and wireless communication [2]. Most of the DSP applications use algorithms that generate either an image, audio, or video visual for human observation. The limited perception of the human sense of visuals or sounds allows the relaxation of exactness in DSP signals and impreciseness in the output [3]. On the other hand, despite Moore's law predicting double transistors every two years, challenges arise due to quantum effects and leakage currents. Amidst these transistor node advancements, approximate computing stands out, offering performance gains of 20% to 200% without technological leaps [4].

A large number of papers have been published regarding the design of full adder circuits and several studies introduced approximate computing in adder circuits for better performance, prioritizing it over accuracy. These include approximate mirror adders (AMAs) [5], XOR/XNOR-based approximate adders (AXAs) [6], and transmission gate-based approximate adders (TGAAs) [7]. Where AMAs and AXAs are designed from a logical reduction at the transistor level from the mirror adder [8] and pass transistor-based XOR/XNOR adders [9]. This paper proposes a synergistic new full adder circuit, along with two approximate adder circuits. As different comparative matrices introduced in previous studies, in this paper, power consumption, delay, power delay product (PDP), transistor number, and bit error rate (BER) are measured to compare the efficiency and performance of the circuits [10]. Simulation results are provided to show the performance of the proposed designs.

This paper is organized as follows. Section II provides a brief review of different adder circuits. Section III presents the proposed full adder and two approximate adders followed by a comparative analysis in section IV. A conclusion is given in section V.

II. Review of Adders

An accurate full adder is a digital circuit that is designed to precisely and reliably calculate the sum and carry outputs based on binary inputs. The sum (S) and carry-out (C_{out}) equations for an accurate full adder can be derived based on the binary addition rules. If A, B, and C_{in} represent the binary inputs, and S, C_{out} represents the sum and carry-out, respectively. The equations are as follows:

$$S=A \oplus B \oplus C_{in}, \quad (1)$$

$$C_{out}=(A \cdot B) + (C_{in} \cdot (A \oplus B)) \quad (2)$$

In Boolean sum-of-products (SOP),

$$S=\sum 1,2,4,7 \text{ and } C_{out}=\sum 3,5,6,7 \quad (3)$$

On the other hand, an approximate adder deliberately deviates from this conventional SOP algorithm and produces inaccurate '1' and '0' outputs. This intentional introduction of errors enables significant energy and delay savings compared

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to accurate adders. Its compromises for enhanced efficiency make it suitable for applications where slight inaccuracies are acceptable.

In this section, three accurate full adder designs are observed in detail alongside a brief introduction of some other accurate full adder and approximate adder circuits. Furthermore, different matrices for comparative analysis will be briefed.

A. Accurate Full Adder

The design of the mirror adder (MA) uses the same number of transistors as the CMOS full adder circuits, yet it consumes less power. While the pull-up network (PMOS) and pull-down network (NMOS) complement each other in opposite formations in a CMOS circuit, they completely replicate each other formation in the mirror adder circuit, as shown in Fig. 1 [8].

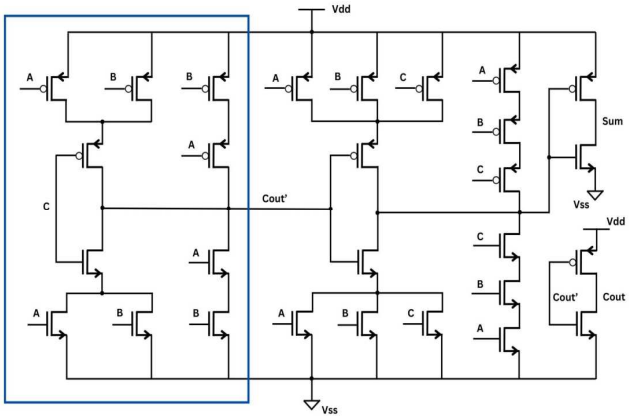
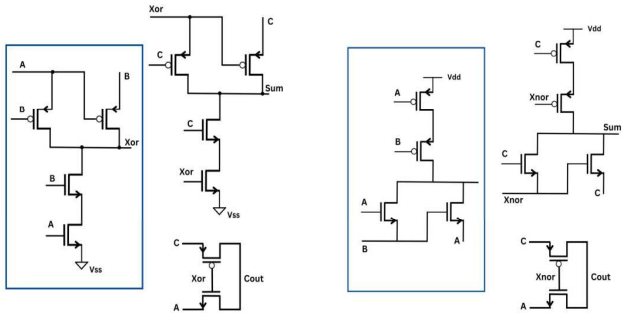


Fig. 1. Schematic view of the mirror adder (MA).

The XOR/XNOR-based full adder namely, static energy-recovery full adder (SERF) uses only 10 transistors, which has the least number of transistors to build a full adder circuit and consumes less power compared to the mirror adder, shown in Fig. 2 [9]. Many low-power adders apply the same pass transistor techniques to build circuits with a smaller number of transistors and less power consumption. But, such low-power adders have the problem of threshold loss, i.e., the logical value of '0' and '1' is not perfectly V_{SS} and V_{DD}, respectively. However, they are very useful in building up larger circuits.



(a) (b)

Fig. 2. (a) Schematic view of XOR full adder (SERF-XA) and (b) XNOR full adder (SERF-XNA).

A transmission gate-based full adder (TGA) is introduced in another paper. The circuit of TGA consists of three modules, including two XOR gates and one MUX circuit [11].

In recent times, the hybrid logic-based adder design has gained significant interest due to its numerous advantages over the single logic full adder. The full adder circuit designed by Bhattacharyya et al. [12] is a hybrid full adder build of CMOS and transmission gate. On the other hand, Tirumalasetty et al. [13] and Hasan et al. [14] have proposed pass transistor and transmission gate-based hybrid full adder circuits. In addition, Nirmalraj et al. [15] provided a gate diffusion input (GDI) technique to design an energy-efficient full adder circuit.

B. Approximate Full Adder

In this paper, three types of approximate full-adder designs are reviewed. These are AMAs, AXAs, and TGAAs. AMAs are designed based on the circuit of MA and have three consecutive circuits, namely AMA1, AMA2, and AMA3 are built of 16, 14, and 11 transistors, respectively [5]. On the other hand, AXAs are designed based on the SERF-XNA adder circuit and the author proposed three consecutive circuits, namely AXA1, AXA2, and AXA3 contain 8, 6, and 8 transistors, respectively [6]. The foundation of TGAAs follows the design of the TGA circuit and it has proposed two approximate adder circuits, namely TGAA1 and TGAA2 are built of 16 and 22 transistors, respectively [7].

For these circuit designs, some matrices must be used to assess the performance and additionally, approximate adder circuits require measuring the inexactness of computing. Previous studies introduced average transient power, static power, delay, power delay product and energy-delay product as the matrices of performance analysis. PDP provides an overall view of the circuit's performance. To perform the accuracy analysis, some authors used error distance and some others used the error rate technique, while the error rate is comparatively more informative than the error distance [16].

III. Proposed Circuits

In this section, an accurate adder is proposed based on MA and SERF XOR-based adder design, along with two approximate adder circuits designed on the same foundation.

A. Proposed Accurate Adder

The proposed accurate adder is a pass transistor-based 12T full adder that follows the construction of the left portion of MA, shown in the box in Fig. 1. While the pull-up network followed the pattern of XOR adder and the pull-down network followed the pattern of XNOR adder, marked in the box in Fig. 2. This pass transistor process repeats in all parallel section of the circuit and finally the results obtain 'sum', as shown in Fig. 3. A minor extension of this circuit, involving input from sub-sections of the previous circuit, provides the carry output. Taking input from the sub-section of the circuit decreases the high-frequency capability of the circuit, limiting the circuit's operating frequency below 10 KHz. However, it provides the idea of creating approximate adders in this manner.

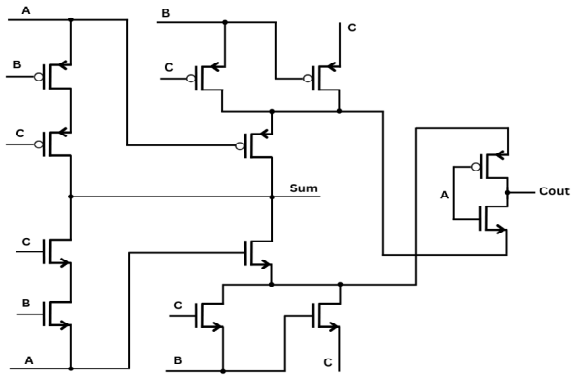


Fig. 3. Schematic view of the proposed 12T full adder.

B. Proposed Approximate Adder

Proposed Approximate Adder 1 (PAA1) is a 10T circuit with the same pattern of pass transistor to generate sum and carry. Two transistors at the end were added to level up the logical value of carry for the 101-input signal. Overall, 6T were used for sum generation and 4T for carry, as shown in Fig. 4. The advantage of PAA1 is having less number of transistors with low power consumption and PDP. The disadvantage includes a slightly higher delay. PAA1 has two error combinations in sum output at 001 and 101 as shown in Table I. The sum and carry-out for PAA1 in Boolean SOP are-

$$S=\sum 2,4,5,7 \text{ and } C_{out}=\sum 3,5,6,7 \quad (4)$$

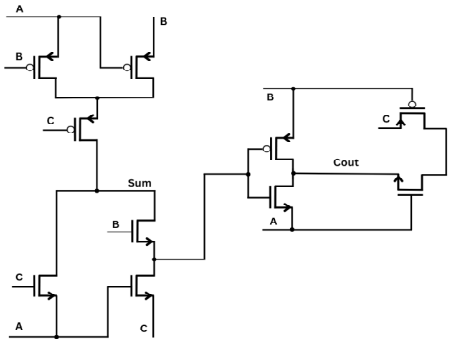


Fig. 4. Schematic view of proposed approximate adder 1.

Proposed Approximate Adder 2 (PAA2) consists of an 11T pass transistor circuit. Overall, 6T were used to generate carry and 5T for sum, as shown in the Fig. 5.

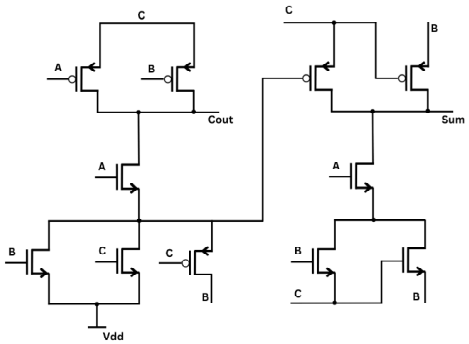


Fig. 5. Schematic view of proposed approximate adder 2.

TABLE I. THE TRUTH TABLE OF PROPOSED APPROXIMATE ADDERS

A	B	Cin	Accurate		PAA -1		PAA -2	
			Sum	Carry	Sum	Carry	Sum	Carry
0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	1
0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	1	1
1	0	0	1	0	1	0	1	0
1	0	1	0	1	1	1	0	1
1	1	0	0	1	0	1	0	1
1	1	1	1	1	1	1	1	1

The advantage of PAA2 is having low power consumption and PDP along with less number of transistors. BER is slightly higher than PAA1 but comparatively better than most of the existing approximate adder circuits. PAA2 faces a bit of a longer delay at 000 and 111 for carry output. It has two error combinations for sum output at 001 and 011, and one error for carry output at 001, as shown in Table I. The Boolean SOP for sum and carry-out are-

$$S=\sum 2,3,4,7 \text{ and } C_{out}=\sum 1,4,5,6,7 \quad (5)$$

IV. SIMULATION & COMPARATIVE ANALYSIS

Simulation is performed using Cadence virtuoso in the gpdk 45nm process to analyse the power consumption and delay of the circuit. On the other hand, the BER of the approximate adders is analyzed by MATLAB Simulink.

Before the simulation, certain design specifications such as supply voltage, the width of pmos and nmos, minimum pulse width, rising and falling time and body connection had to be determined to construct the circuit.

In this study, the choice of supply voltage is critical as it significantly impacts delay and power consumption. On the other hand, every specific process node has a limited range of supply voltage. Hence, voltage scaling is necessary to choose the efficient supply voltage [17]. In this paper, +0.8V is used as the standard supply voltage (V_{DD}). Regarding transistor sizing, the width of the transistors plays a pivotal role in determining delay, power consumption, and area. This study has applied 120nm width of NMOS and 145nm width of PMOS to gain a balanced impact on both delay and power.

In terms of body connection, all the bodies of PMOS and NMOS were connected to V_{DD} and V_{SS}, respectively. The minimum pulse width applied in the simulation is 1 ms and both the rising and falling time are set as 5% of the minimum pulse width. Additionally, Input pulses applied in the circuits are 0V~0.8V.

There are two major power dissipation in digital CMOS circuits, which are transient power and static power dissipation. In this study, Both power consumption is derived by using Cadence's calculator and parametric analysis tools. All possible 64 combinations of input pulses are considered to get the transient power consumption. On the other hand, static power consumption occurs due to the leakage current of the circuit when input pulses are in a static state.

In this simulation, the delay is taken as the time delay between input and output pulse at 0.4V using Cadence's calculator tool. All possible 8 states are considered and the nominal delay is used to have a comparative analysis. The

improvement rate of existing and proposed full adders has been presented compared to conventional MA.

Following all these mentioned criteria, the proposed full adder circuit is designed in Cadence virtuoso schematic editor, as shown in Fig. 6, and the transient waveform is found after running the simulation that is shown in Fig. 7.

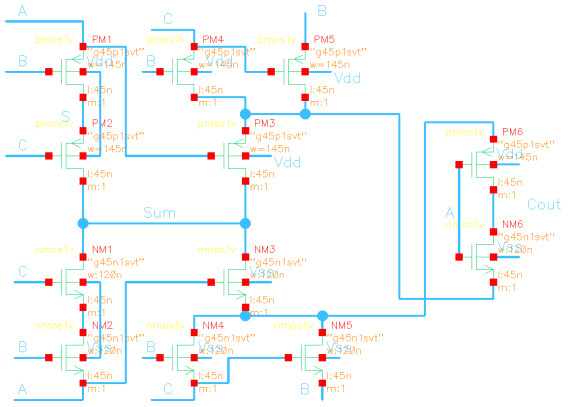


Fig. 6. Schematic implementation of the proposed accurate adder.

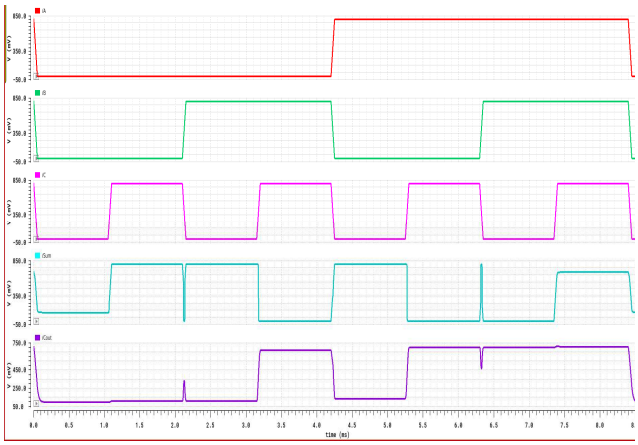


Fig. 7. Simulated transient waveform of the proposed accurate adder.

Table II provides a comprehensive summary of the performance analysis of existing and proposed full adder circuits. It is clear that the proposed full adder consumes the lowest power compared to the other mentioned accurate adders. However, it does incur a slightly higher delay than the others, resulting in an overall average PDP.

The improvement rate in Table II shows that the proposed full-adder gains 85% power and 50% PDP improvement compared to the conventional MA circuit.

The TGA circuit consumes the highest power but it significantly gains the least delay, which makes it best in PDP comparison. This full adder circuit is good for high-speed operation. However, TGA consumes high power and it needs more area than others as the number of transistors used in this circuit is more than most of the conventional full adders.

On the other hand, an approximate adder can be more energy-efficient than conventional full adders. It can gain better PDP and low power consumption while trading some bit errors in operation. In this study, the same specifications are used to design and simulate the approximate adder circuits. Additionally, the same matrices of full adder circuits are used to conduct the performance analysis of approximate adders. Cadence Virtuoso including the calculator and parametric analysis tools are used to get power and delay of the circuits and MATLAB Simulink is used to get BER.

The simulation results given in Table III illustrate the performance summary and comparative analysis among approximate adders. It shows that the least number of transistors are used by AXAs and the second least is our proposed approximate adder designs, while AMAs and TGAAs need more transistors to construct the circuit. The simulated transient waveform of proposed approximate adders, PAA1 and PAA2 are shown in Fig. 8 and Fig. 9, respectively. The simulation results also justify the information given in Table I.

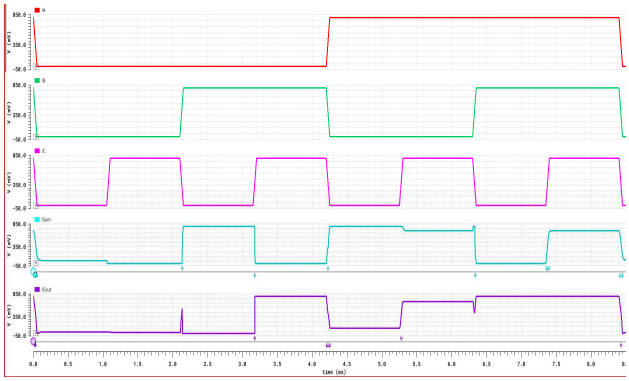


Fig. 8. Simulated transient waveform of PAA1.

TABLE II. PERFORMANCE COMPARISON OF ACCURATE ADDERS

Accurate Full Adders	No. of Trans-istors	Avg. Transient Power (pW)	Static Power (pW)	Delay (ns)		PDP ($\times 10^{-18}$)		Avg. PDP ($\times 10^{-18}$)	Improvement rate (%)	
				Sum	Carry	Sum	Carry		Power	PDP
MA [8]	28	648.31	15.24	467.4	17.0	310.1	11.3	160.7	0.00	0.00
SERF-XNA [9]	10	226.07	10.12	28.8	664.5	6.8	157.0	81.9	64.41	49.05
SERF-XA [9]	10	299.25	0.03	94.1	183.5	28.1	54.9	41.5	54.90	74.16
TGA [11]	20	1188.50	20.24	8.8	6.4	10.6	7.8	9.2	-82.16	94.30
Bhattacharyya's [12]	16	583.09	14.78	122.7	11.2	73.3	6.7	40.0	9.90	75.09
Tirumalasetty's [13]	16	776.42	112.48	130.4	0.7	115.9	0.6	58.3	-33.96	63.76
Hasan's [14]	22	862.33	21.86	308.2	411.4	272.5	363.7	318.1	-33.25	-97.93
Nirmalraj's [15]	10	662.94	3.15	1.9	113.7	1.2	75.7	38.5	-0.38	76.06
Proposed FA	12	94.15	0.53	1007.8	695.9	95.4	65.9	80.7	85.73	49.82

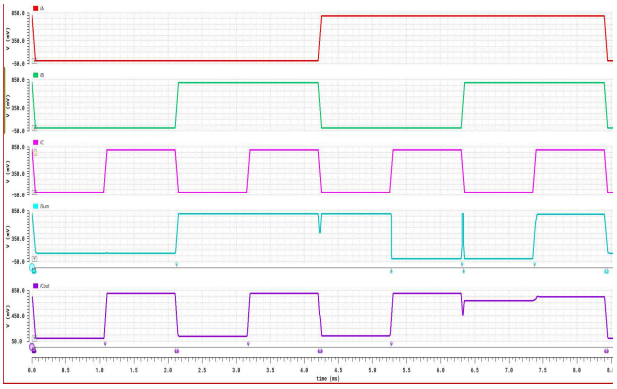


Fig. 9. Simulated transient waveform of PAA2.

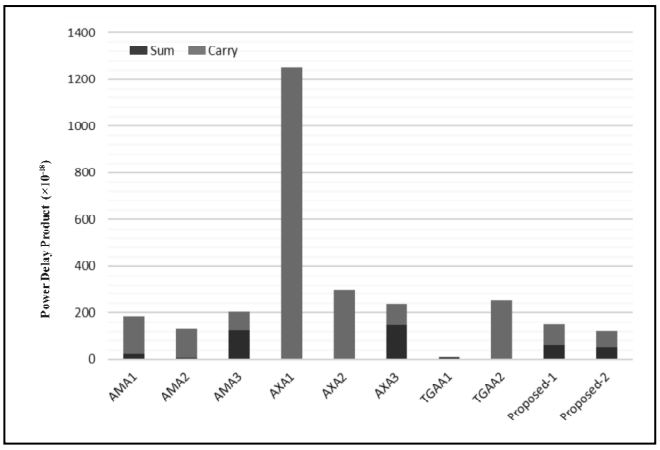


Fig. 10. PDP comparison of approximate adders (both sum and carry).

It is evident that the proposed approximate adders, PAA1 and PAA2 do not maintain a good high '1' or good low '0' in every state. However, they perfectly maintain the 20% to 80% range of changing state in each case.

Simulation results shown in Table III demonstrate that PAA1 and PAA2 consume the least power in terms of both transient and static compared to other conventional approximate adders. Additionally, AXA3 also consume less power, while TGAAs, AMA1, and AXA1 consume high power comparatively. Other approximate adders consume an average amount of power, nearly 300 pW. AXA1 has no delay for the sum as it passes the C_{in} input pulse directly as output, but it has the highest delay at carry output. AMAs and TGAAs have less delay and our proposed approximate adders incur higher delay than others. However, the performance of a circuit depends on both power and delay; hence the product of power and delay is necessary.

Fig. 10 delineates the PDP for both sum and carry, where carry is stacked up on the sum value, producing an overall PDP view for the approximate adder designs. The overall information describes that the delay of the carry signal has significant impacts on all of these circuits as it incurs a higher delay in most of the approximate adder circuits than the sum. As it is a product of power and delay, the unit of PDP is generally expressed as picojoules-second (pJ.s) or femtojoules-second (fJ.s).

On the other hand, power consumption has a substantial impact on PDP for both sum and carry. The PDP comparison in Fig. 10 shows that the proposed approximate adders, PAA1 and PAA2 significantly gained lower value after the TGAA1 approximate adder design. On the other hand, AXA1 has the highest PDP as it has higher power consumption and delay in carry signal. All the other circuit has an average decent value of PDP, nearly 0.2 to 0.3 fJ.s.

The BER of an approximate adder is a significant criterion for designing and implementing circuits in real applications. In this study, BER is analyzed using MATLAB Simulink which provides a more realistic idea of inexactness. In a real application, the input data has no pattern but rather a random input pulse will apply. In this paper, 10 million random binary input pulses were generated and applied to both approximate and accurate full adder. Then, the collected output was compared and finally, the error rate was generated for random input signals. To implement that model in MATLAB Simulink, a resemble of transistor-based accurate adder and approximate adder is converted into a logic gate-based design. It can be done using RTL conversion or it can be done manually by Boolean conversion from the output waveshape of the circuits. The model of MATLAB Simulink implementation is shown in Fig. 11.

TABLE III. PERFORMANCE SUMMARY OF APPROXIMATE ADDERS

Design	No. of Trans-istors	Avg. Transient Power (pW)	Static Power (pW)	Total Power Consumption (pW)	Delay (ns)		PDP ($\times 10^{-18}$)		BER (%)	
					Sum	Carry	Sum	Carry	Sum	Carry
AMA1 [5]	16	649.69	12.00	661.69	29.9	252.1	19.8	166.8	49.57	9.6
AMA2 [5]	14	338.80	7.42	346.22	12.7	370.8	4.4	128.4	28.06	0
AMA3 [5]	11	312.02	8.93	320.95	395.0	243.2	126.8	78.1	37.58	9.59
AXA1 [6]	8	468.88	85.86	554.74	0.0	2257.1	-	1252.1	47.97	33.6
AXA2 [6]	6	271.55	8.03	279.58	11.3	1058.0	3.2	295.8	59.9	0
AXA3 [6]	8	107.04	5.460	112.50	1303.9	804.7	146.7	90.5	68.83	0
TGAA1 [7]	16	657.31	15.42	672.73	15.2	0.0	10.2	-	24.05	24.15
TGAA2 [7]	22	795.51	23.45	818.96	2.0	308.3	1.6	252.5	19.16	64.84
Proposed AA1	10	59.88	0.29	60.17	998.7	1525.8	60.0	91.8	24.07	0
Proposed AA2	11	60.20	0.79	60.99	838.8	1207.8	51.2	73.7	23.94	9.58

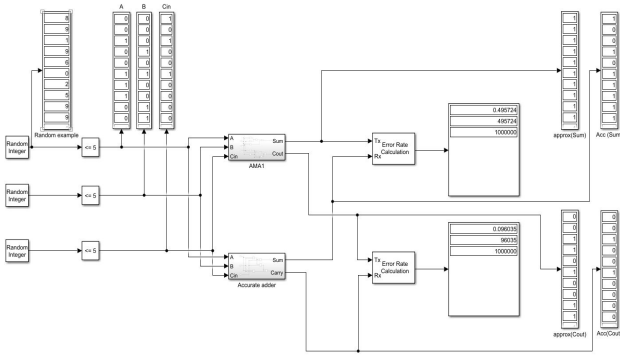


Fig. 11. MATLAB Simulink model of BER comparison.

This simulation requires real-time data flow, hence, no gate delay should be considered here, as the main object of this simulation is to determine bit errors. Fig. 12 shows the BER summary in the percentage of all mentioned approximate adders. The bit error rate of carry is stacked up on the bit error rate of the sum to provide an overall visual of the comparative results of all circuits. It is clear that the proposed approximate adders, PAA1 and PAA2 have the lowest BER, nearly 20% to 30%. AMA2 also shows significantly better results. In contrast, other approximate adders have an average BER between 50% to 80%.

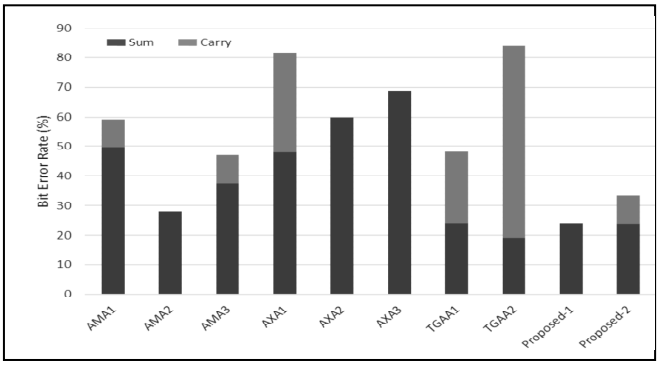


Fig. 12. Bit error rate of approximate adders (both sum and carry).

While BER refers to an approximation of the adder circuit, power delay product refers to the performance of the circuit. An approximate adder is designed to perform with some inexactness to gain better PDP, but both of these factors need to be in balance to perform its arithmetic operation. In terms of bit error rate, our proposed approximate adders show an excellent performance than other mentioned approximate adders.

V. Conclusion

In this paper, we have presented a full adder design and an approach to approximate adders with comparative analysis. Extensive analysis in Cadence tools and MATLAB Simulink provided empirical evidence of the performance of the proposed circuits. The power consumption found least among other conventional adder circuits, 94.68 pW for a 1-bit full adder. Additionally, our designed approximate adders consume less power compared to other accurate and approximate adders, around 60 pW total power, which is 2 to 14 times lower than other approximate adder circuits. On the other hand, the proposed circuits obtained remarkable values of PDP and BER compared to other circuits. However, the propagation delay is slightly higher in these circuits.

In summary, our research provides valuable insights into the design of energy-efficient accurate and approximate full adders that could be viable alternatives for designing more efficient arithmetic units for DSP applications, which have lower accuracy tolerance but need more power efficiency and high performance.

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