

DESIGN OF ENERGY-SAVING AND HIGH-SPEED APPROXIMATE ADDERS FOR DSP APPLICATIONS

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ABSTRACT

Approximate adders allow for a trade-off between accuracy and efficiency by introducing controlled errors or approximations during the addition process. The concept emphasises the value of error correction techniques in keeping accuracy within reasonable bounds. The difficulties humankind has in addressing the rising need for high-performance, energy-efficient digital technology, spark interest in this research.

The study shows that as compared to accurate adders, approximation adders dramatically reduce power consumption, increase computational efficiency, and decrease circuit complexity. The growth of approximate computing is aided by these discoveries, which have the potential to be advantageous in several areas, including machine learning, signal processing, and approximation computing architectures.

The research studies several methods, including voltage scaling, reduced bit precision, pass transistors method to integrate controlled errors or approximations while minimising the trade-off between accuracy, delays, power loss, and transistor count. With a focus on decreased delays and energy consumption, we have suggested three approximation adder architectures. The error rate is kept within a safe range, whereas specific designs purposefully create controlled mistakes. The power dissipation and delay analysis are done by using Cadence virtuoso and spectre tools. On the other hand, the bit error analysis is completed using MATLAB software. The design is implemented by 45nm technology considering the supply voltage +0.8 V.

The desired outcome of the study was to discuss comparative analysis of different matrices. Considering power dissipation, delay, PDP and BER comparison, the outcome shows that, proposed EFAAs have provided significantly better results compared to other existing approximate adders. The PDP we found is within 4 to $5.5 (\times 10^{-5})$ and BER is within safe range.

However, the possibility of accuracy loss, the complexity of error correction was considered for DSP applications.

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ACRONYMS & ABBREVIATION

DSP	- Digital Signal Processing
ALU	- Arithmetic Logic Unit
VOS	- Voltage Over Scaling
DWT	- Discrete Wavelet Transform
RCA	- Ripple Carry Adder
MRED	- Mean Relative Error Distance
ER	- Error Rate
BER	- Bit Error Rate
PDP	- Power Delay Product
EDP	- Energy Delay Product
EDA	- Electronic Design Automation
ADE	- Analogue Design Environment
AMA	- Approximate Mirror Adder
AXA	- Approximate XOR/XNOR Adder
TGA	- Transmission Gate Approximate Adder
EFAA	- Effective and Faster Approximate Adder
GAAFET	- Gate-All-Around Field-Effect Transistor
CNFET	- Carbon Nanotube Field-Effect Transistor

Chapter 1

Introduction

1.1 Introduction

The concept of approximate computing, sacrificing computational quality for computation efforts, has recently emerged as a promising design approach [1]. Approximate computing is motivated by the large and growing class of applications that demonstrate inherent error resilience, such as DSP, multimedia (image/audio/video), graphics, wireless communication, and emerging workloads such as recognition, mining, and synthesis. These applications usually process large, redundant data sets containing significant noise using statistical or probabilistic computations [2-4].

The heart of an integrated circuit (IC) is the arithmetic logic unit (ALU), and the heart of the arithmetic logic units (ALUs) is the adder circuit. The performance and efficiency of integrated circuits (ICs), particularly arithmetic logic units (ALUs), can be enhanced by developing the performance and efficiency of the full adder. In the analogue circuit design, the full adder can be designed by transistors. Designing smaller ICs using MOSFETs becomes increasingly challenging as time passes while ensuring a year-over-year performance and efficiency improvement [5-7].

According to Moore's Law, which has been a driving force in the semiconductor industry for decades, the quantity of transistors on a chip double on average every two years. However, there are issues with Moore's Law's possible slowdown or constraints [8]. Challenges develop as transistors get smaller because of things like quantum effects, leakage currents and increasing variability. The continuation of conventional transistor scaling is seriously affected by these issues. The semiconductor industry has investigated many technologies and tactics to address this problem and boost computing performance. It entails researching novel transistor designs like nanowires and FinFETs and creating novel materials and fabrication methods [9].

While the semiconductor industry looks for more advanced technologies to meet the demands of IC development, there are a few techniques to improve computing performance without any technological advancement. Among these, approximate computing is one of the procedures that can improve performance and energy-saving development by 20% to 200%[10]. The concept of the approximate adder is gaining popularity in analogue IC development because it can boost speed and efficiency while compromising the precision of ICs. It benefits

applications like digital signal processing (DSP), which demand big data analysis but are efficient and faster [11].

Approximation adders aim to balance accuracy and energy efficiency. Traditional adders prioritise accuracy but can be computationally expensive and energy-intensive. In contrast, approximation adders sacrifice some precision to achieve an increased energy economy. Techniques like operand bypassing and reduced bit-widths are used to minimise power consumption. However, this trade-off introduces a degree of error in the output. The energy efficiency of an approximation adder depends on design choices and the extent of the precision compromise [12-14].

An approximation adder often operates more quickly than a precise adder in terms of delay. The critical path of the circuit can be shortened, resulting in shorter propagation delays, by simplifying the circuit or skipping some bits. As a result, additional operations could be completed more quickly, allowing for increased throughput in applications that need speedy processing [15-16].

The approximation adder may convert binary input operands to reduce precision or change values. The traditional existing approximate adders based on analogue circuit designs are approximate mirror adder, XOR/XNOR and transmission gate based approximate adders [2] [17-18]. However, this situation is more severe in the case of adders. Since the delay and power of adders increase significantly with bit-width(N), we have to trade a lot of power/delay for a modest improvement [19]. These include voltage scaling, decreased bit precision, and statistical approximations. Voltage scaling decreases supply voltage to save energy, but voltage dips might cause errors. The addition uses fewer bits, sacrificing accuracy for speed. Statistical approximations calculate totals using probability. Probabilistic statistical approximations estimate sums [20-22]. Voltage scaling, statistical approximations, and lower-bit accuracy are a few examples of these methods. Voltage scaling reduces energy use by lowering supply voltage; however, voltage dips might cause errors. For speed, lower bit accuracy limits the number of bits used for addition. The sum is calculated using probabilistic methods in statistical approximations. Statistical approximations estimate sums using probabilistic methods [23].

1.2 Motivation

Moore's Law's problems are a major driving force behind research in approximation adder design for DSP systems. According to Moore's Law, the number of transistors on integrated circuits doubles roughly every two years. The exponential growth that has driven the development of computing technology is getting harder to sustain as transistors approach their physical limits. This restriction, sometimes known as the “end of Moore's Law,” has led researchers to consider alternate strategies for advancing computer systems' performance and efficiency. Therefore, research in approximate adder design for DSP systems, driven by the implications of Moore's Law, plays a crucial role in enabling the continued advancement of DSP technology.

Modern DSP systems must carefully consider how much energy they use, especially for battery- and portable-powered applications. Due to their precise calculations, traditional adder designs need much power. Even so, in many DSP applications, a certain amount of approximation is allowed without affecting the overall system performance. We can drastically cut power usage, increase battery life, and advance green technology by creating energy-efficient approximation adders.

Real-time DSP applications like audio and video processing demand fast computation to meet latency constraints. Traditional adders' complex processing operations limit their operating frequency. Approximation adders, which sacrifice computation precision for speed, may allow real-time processing of data-intensive DSP applications at higher clock rates.

Not every DSP application needs exact calculations. Human perception may be forgiving of little mistakes in some situations, such as processing images and sounds. We may use approximation adders to significantly boost performance while retaining an acceptable degree of accuracy by utilising the inherent error resilience of these applications. By making this trade-off, we can maximise the speed and efficiency of DSP systems and reach their maximum potential.

There is much potential for research and innovation in the field of approximation computing, which is still relatively new. A multidisciplinary approach combining knowledge in digital design, computer architecture, algorithm optimisation, and performance assessment is necessary to create and analyse energy-efficient and fast approximation adders for DSP applications. By focusing on this study field, we may progress approximation computing methods and open the door for future developments in DSP system design.

1.3 Aim and Objectives

This study focuses on creating and assessing fast, energy-efficient approximation adders that are mainly made for digital signal processing (DSP) applications. Using approximation techniques is intended to optimise the efficiency and performance of DSP systems by achieving a balance between computational accuracy, energy use, and processing speed.

- To analyse different existing approximate adders.
- To design energy saving, less delay approximate adders.
- To make a comparative analysis of approximate adders with respect to the power dissipation, delay and bit error rate.

1.4 Thesis Organisation

This thesis consists of five chapters. A brief introduction to the approximate adder and its comparative matrices such as power dissipation, delay and error rate is discussed in Chapter 1. In chapter 2, several literatures related to design and analysis of approximate adders, power consumption and delay optimisation of digital circuits are discussed. Chapter 3 describes the fundamental concepts of basic MOSFET and adder circuits. Design and comparative analysis with existed approximate adders and proposed approximate adders are discussed in the chapter 4. Finally, Chapter 5 concludes the outcomes of this work and discusses the scope of extending this work in the future.

Chapter 2

Literature Review

2.1 Introduction

This literature review chapter explores various studies and aspects of approximate computing and approximate adders. It explains previous works on approximation circuit modelling, evaluation methodologies, different types of approximate adders, power reduction techniques, and performance analysis. The chapter discusses the strengths and limitations of each proposed approach and compares their performance metrics, including power dissipation, area utilisation, delay, accuracy, and error rates. It is worth noting that some papers lack detailed information on the methodologies used or comparisons with other designs. Additionally, the chapter primarily focuses on digital designs using logic gates, while the potential benefits of analogue designs are mentioned. Further research is needed to explore the applicability of these designs in advanced technology nodes and their performance in real-world applications.

2.2 Literature Review

The paper offers a thorough review of existing approximate adders such as Equal Segmentation Adder (ESA), Error-Tolerant Adder type II (ETAIL), Speculative Carry Select Adder (SCAA), Accuracy-Configurable Approximate Adder (ACAA), Almost Accurate Adder (ACA) and Lower-Part-OR Adder (LOA). It mentions two ways to develop the desired approximate computation by contrasting voltage-over-scaling (VOS) and logic circuit redesign. Simulation results indicate that the Equal Segmentation Adder (ESA) is the most hardware-efficient design. Still, it has the lowest accuracy in terms of error rate (ER) and means relative error distance (MRED). The Error-Tolerant Adder Type II (ETAIL), Speculative Carry Select Adder (SCSA), and Accuracy-Configurable Approximate Adder (ACAA) show similar accuracy performance when the same parameters are used. Among them, ETAIL incurs the lowest power-delay-product (PDP). The Almost Correct Adder (ACA) is the most power-consuming scheme among the evaluated designs, with moderate accuracy. The Lower-Part-OR Adder (LOA) is the slowest design but demonstrates high efficiency in power dissipation. Nonetheless, the paper does not provide explicit information about the software used for the evaluation. As a review paper, it is mainly focused on comparative analysis and results [1].

The paper proposes different designs for approximating a mirror adder circuit, which can be used in implementing discrete wavelet transform (DWT) hardware for image processing

applications. The study demonstrates that power and layout area can be reduced by eliminating certain transistors in the mirror adder circuit. The authors compare the performance of four approximation levels for mirror adder circuits (AMA1, AMA2, AMA3, and AMA4). The trade-off level 3 and level 4 designs show the best results regarding power dissipation and area reduction. The proposed design is implemented using 180 nm technology. The designs also incorporate a voltage-scaling approach to reduce power requirements further. By scaling down the power supply voltage, they observe a decrease in average transient power and average DC power. The trade-off level 3 and level 4 designs show the lowest power dissipation when the supply voltage is scaled down to 3.3 V. They justify the design by offering a marginal reduction in signal-to-noise ratio but significant reductions in layout area and power consumption. The paper evaluates the image quality degradation caused by approximation by calculating the peak signal-to-noise ratio (PSNR) before and after approximation. The trade-off level 3 design exhibits the best PSNR among all levels of approximation, indicating a higher image quality than other designs. Although the paper evaluates power dissipation, area utilisation, and PSNR, it would be beneficial to include additional performance metrics such as speed or latency to provide a more comprehensive assessment of the proposed designs. Again, with the rapid advancements in semiconductor technology, it would be helpful to explore the applicability and performance of the designs in more advanced technology nodes [2].

The paper proposes four approximate adders for DSP processors, which can reduce power dissipation compared to existing approximate adders. The proposed approximate adder circuits were simulated using the Cadence Virtuoso tool under 45 nm CMOS technology with a supply voltage of 0.5 V. The study provides a comprehensive overview of existing approximate adder circuits, comparing and discussing their pros and cons. The author optimised the power dissipation and accuracy regarding transistor count, power delay product and error distance. The proposed adders show promising results with reduced power dissipation and improved accuracy. Despite that, the paper lacks detailed information about the methodology used to design and optimise the proposed adders. The author did not provide any precise cause for choosing a voltage scaling of 0.5V, which is close to the threshold voltage of 45nm technology. The evaluation of the proposed adders is limited to simulation results; experimental validation is not provided [3].

The paper proposes a system-level design approach that combines voltage over scaling (VOS) with unequal error protection to achieve error resiliency in digital signal processing (DSP) systems. The proposed approach adapts the degree of VOS in each system block based on user

specifications, the severity of process variations, and channel noise to minimise system power while maintaining the desired quality and robustness. The paper demonstrates the effectiveness of the proposed approach in a DCT/IDCT system, showing significant power benefits (up to 69%) while tolerating errors induced by varying operating conditions. The application of the proposed approach to a DCT/IDCT system, which is widely used in multimedia applications, demonstrates its practical relevance and potential impact. However, the evaluation of the proposed approach is limited to a DCT/IDCT system, and its applicability to other DSP systems is not explored [4].

The paper presents four Approximate Full Adders (AFAs) designed for high-performance and energy-efficient approximate computing. The main objective of the proposed AFAs is to reduce carry propagation length while minimising the error rate. The proposed AFAs exhibit similar error probabilities, allowing for the design of “N-bit” approximate adders with similar error characteristics. The paper presents analytical models for estimating the proposed AFAs' delay, power, and area, which significantly improved compared to a conventional Ripple Carry Adder (RCA). AFA#1 and AFA#2 outperform the other AFAs in terms of delay, power, area, and PDAP. The normalised delay of ApproxADD decreases with bit-width at a rate of approximately $1/N$, indicating bit-width-aware constant delay. Proposed ApproxADD improve dynamic power consumption by 46.31% and area by 28.57% compared to RCA. The Mean Relative Error Distance (MRED) of ApproxADD decreases with bit-width but saturates for $N \geq 9$, while the Error Rate (ER) increases rapidly with bit-width, reaching approximately for $N \geq 13$. The paper suggests the effectiveness of the proposed approach in image compression and decompression by replacing conventional addition operations in Discrete Cosine Transform (DCT) and Inverse Discrete Cosine Transform (IDCT) modules with the proposed adder. Nevertheless, the study was entirely based on the digital design of approximate adders using logic gates, while the analogue design could be more efficient. On the other hand, the paper lacks a comparison with other approximate adders, limiting the understanding of the proposed design's competitiveness. The author suggests that the proposed approximate adders may be unsuitable for applications with low error resilience due to their high MRED and increasing ER [5].

The paper presents a new approach to leveraging error tolerance during circuit design, which can lead to improved circuit area, delay, and yield. The logic synthesis approach proposed by the authors effectively exploits the given error rate threshold to achieve significant reductions in the circuit area. Experimental results demonstrate that their approach achieves an average of

9.43% literal reductions for all targeted benchmarks with an error rate threshold of 1%, indicating its effectiveness in reducing circuit complexity. However, the paper does not analyse the trade-offs between error rate thresholds, circuit area reductions, and other performance metrics [7].

The paper provides a history of Moore's Law, which describes the exponential growth in the number of components integrated into a semiconductor circuit (until 2010). Moore's Law has expanded beyond its original intentions and has been interpreted in various ways, potentially losing its meaning and usefulness. The author discusses the technological drivers behind the observed trends in Moore's Law, including increasing chip area, decreasing feature size, and improving device and circuit designs. The paper highlights the bifurcation of Moore's Law into memory and logic trend lines, with memory chips advancing faster than logic chips. The economic advantages of Moore's Law were attributed to improved circuit density and transistor performance rather than increased functions per chip. The shrinking transistor size became a crucial aspect of Moore's Law value [8].

The paper discusses the history and future of Si microelectronics, focusing on the scaling of solid-state devices and the limitations of planar CMOS transistor scaling. It mentions that scaling has been a driving force in improving microelectronics' cost, performance, and power for the past 40 years (till 2006). The paper explores potential alternatives to Si transistors, such as nonclassical CMOS, spintronics, single electron devices, and molecular computing. However, it suggests that these options will unlikely replace Si transistors in the foreseeable future. It emphasises that Si CMOS technology still has a significant lifespan and will likely continue as the dominant technology for mainstream logic applications. The paper highlights the economic advantages of scaling and the continuous reduction in the cost per transistor over the years. However, the paper was published in 2006, so it may not reflect the most up-to-date information and developments in the field. It did not extensively discuss recent advancements or emerging technologies beyond planar CMOS and strained Si. The study does not provide information about other possible materials (e.g., Ge, Carbon nano-tube) to replace Silicon. Some statements are subjective and based on the authors' opinions, which may not necessarily align with current perspectives in the field [9].

The paper proposes the use of an approximate reverse carry propagate adder (RCPA) for power reduction and speed improvement in digital processing units, particularly in portable systems. The proposal of the approximate RCPA introduces a novel approach to approximate computing, offering potential benefits in terms of power, speed, and accuracy. The paper introduces three

different mechanisms for generating the forecast signal (F) in the RCPA, aiming to optimise accuracy and performance. In the comparative analysis with other approximate full adders, the RCPA shows less vulnerability to delay variation than conventional adders, making it a promising solution for energy-efficient DSP applications. Nonetheless, While the paper introduces three mechanisms for generating the forecast signal (F) in the RCPA, it does not provide a comparative analysis of their effectiveness or evaluate their impact on accuracy and performance. The study is entirely based on digital circuit design, while other analogue approximate adders exist. On the other hand, the paper does not thoroughly discuss potential limitations or trade-offs associated with the proposed RCPA or its implementation in practical DSP systems [11].

MACACO, an approximation circuit modelling, addresses the need for a comprehensive analysis framework for approximate computing. It evaluates the approximate and equivalent untimed circuits using worst-case error, average-case error, error probability, and error distribution metrics. The methodology covers timing-induced approximations (such voltage over-scaling or over-clocking) and functional approximations (logic complexity reduction). The author computes timing-induced and functional approximations using conventional Boolean analysis tools (SAT solvers and BDDs) and statistical techniques (Monte-Carlo simulation) to achieve analytical results. The studies have focused primarily on the trade-offs and behaviour of approximate arithmetic units. However, the methodologies encourage approximative computing in digital design (using logic gates), although the analogue design may be energy-efficient and can perform better. On the other hand, it did not comprehensively analyse the circuit's "voltage over-scaling" method [12].

The paper discusses the challenges that can be faced by future nanoelectronic devices, including increased power consumption, performance saturation, variability, and reliability limitations. The study focuses on various nanoscale FETs, including multigate nanodevices, nanowires, tunnel transistors, ferroelectric FETs, and hybrid nanocomponents using phase change materials or nanofilaments. The author proposes several promising solutions for these challenges, such as using novel materials and innovative device architectures. Different materials and structures, such as ultra-thin films, 2D and 1D nanostructures, and heterostructures using strained or III-V materials, are explored to boost nanotransistors' performance. The author acknowledges the support from the EU H2020 NEREID European Project on Nanoelectronics Roadmapping and the Sinano Institute Members. Nevertheless, the paper does not provide detailed experimental results or data for the proposed solutions. It

mainly focuses on discussing concepts and theoretical simulations. This study mainly focused on different material comparisons to achieve high performance and low power operation of IC [13].

The study provides a comprehensive overview of approximate computing, covering various aspects, from programming languages to transistor-level designs. This paper discusses several existing adders, including approximate mirror adders, XOR/XNOR-based adders, lower-part-OR adders, speculative adders, error-tolerant adders, and dithering adders and their trade-offs between precision, energy consumption, and performance. Different paradigms have been discussed, such as approximate computing and stochastic/probabilistic computing, highlighting their distinctive features and applications. While approximate computing uses statistical data and algorithms to produce imprecise results using deterministic design, stochastic computing uses random binary bit streams. It introduces metrics for evaluating the precision and dependability of approximate adders, including error rate/frequency, error significance/magnitude, error distance, mean error distance, and normalised error distance. Nevertheless, the paper focuses primarily on hardware-level designs and may not provide an in-depth analysis of higher-level algorithmic techniques for approximate computing. Although it introduces several transistor-designed approximate adders, it does not explain the transistor's nanometer technology or the functionality of the software they used [15].

The paper discusses the issue of power dissipation in integrated circuit design using nanometric CMOS technology, and it proposes three new approximate adders (AXAs) based on XOR/XNOR gates implemented by pass transistors to reduce power consumption. The AXAs are evaluated and compared to energy consumption, delay, area, and power delay product (PDP) using Cadence's Spectre simulation in TSMC 65nm process. The simulation results show that the proposed AXAs consume less power and perform better (lower propagation delay) than the accurate XOR/XNOR-based adder. However, the paper does not comprehensively compare with other approximate adder designs. The reliability assessment based on the error distance metric is limited to single-bit adders, and it would be helpful to evaluate the AXAs on larger multi-bit adders to assess their performance in more complex circuits. The voltage over-scaling method is not introduced in this study [17].

The paper proposes two new transmission gate-based approximate adders (TGA1 and TGA2) for low-power imprecise applications using a logic reduction at the gate level. The use of transmission gates in the designs of the adders is a novel approach which offers advantages regarding reduced complexity and critical path delay. The proposed adders show benefits in

terms of power dissipation compared to accurate adders and recently proposed approximate adders. An image processing application is presented to evaluate the efficiency of the proposed adders in terms of power and delay at the application level. However, no transistor technology nor any energy, delay or accuracy assessment technique has been explained clearly in this article. Performance characteristics have not been observed deeply regarding the trade-off between accuracy and power/delay [18].

The paper offers valuable insights into the trade-offs between power and performance and introduces an optimisation framework to find the optimal values of V_{dd} and V_{th} for power-efficient design. Low-power techniques include problem reformulation, algorithmic changes, clock gating, power gating, low swing interconnects, dual-threshold technologies, and variability-aware design. It highlights the impact of variability on energy consumption and the need for variability-aware design in modern chips. Nevertheless, the paper lacks specific quantitative data and experimental results to support the findings and claims. Some of the explanations and concepts introduced may be technical and require prior advanced and updated knowledge of CMOS technology, while the study did in 2005 [19].

The paper addresses low-power design in energy-constrained systems, crucial for extending battery and system lifetime. The analysis provides insights into the relationship between voltage supply, threshold voltage, energy dissipation, and performance, helping optimise circuit designs. The paper analyses the performance and energy dissipation of 180nm CMOS circuits operating in the subthreshold region ($V_{dd} < V_{th}$). The analysis shows that subthreshold CMOS circuits can be used in low-to-moderate performance applications (10kHz-100MHz) while achieving significant energy savings. The paper explores the trade-offs between energy and performance and identifies the optimal V_{dd} - V_{th} operating points for different circuit designs. The minimum energy point is found at $V_{dd} = 130$ mV and $V_{th} = 370$ mV. The energy per clock cycle is 0.19 fJ/gate, and the ring oscillator clock frequency is 69 kHz. However, it is essential to note that operating at this minimum energy point sacrifices performance, as it is suitable for applications with deficient performance requirements. It can be inferred that lower V_{dd} voltages (in the hundreds of millivolts range) tend to perform better in energy dissipation. However, the findings are based on simulations using BSIM3 models for a specific process (180 nm) and may not generalise to other technology nodes or circuit designs. The paper does not discuss the potential limitations or challenges of implementing subthreshold CMOS circuits in real-world applications [20].

The paper presents a design methodology for voltage-scalable, process variation-aware motion estimation based on significance-driven computation. The authors propose a statistical technique to identify significant and non-significant computations at the algorithmic level, allowing for modifying the underlying architecture. Variable latency arithmetic is employed at the architecture level to achieve voltage scalability while ensuring error-free computation for significant computations. The paper introduces an adaptive quality compensation block that adjusts the algorithm and architecture based on the degree of voltage over-scaling and process variations. Simulation results demonstrate an average power savings of approximately 33% compared to conventional implementations in the 90 nm CMOS technology, with a maximum loss in Peak Signal Noise Ratio (PSNR) of around 1 dB and no throughput penalty. The simulation results show better power savings without compromising output quality, making the proposed approach a viable solution for low-power video processing systems. However, the paper focuses primarily on the voltage-scalability and process variation tolerance aspects, and it would be beneficial to provide more insights into other potential design considerations, such as area overhead or computational complexity. The comparison with conventional implementations is based on the 90 nm CMOS technology, which may limit the generalizability of the findings to more advanced technologies. On the other hand, the paper does not discuss potential trade-offs or challenges in implementing the adaptive quality compensation block, leaving room for further exploration and analysis [21].

The paper proposes design techniques for improving meta-function scalability in approximate computing, explicitly focusing on multimedia, recognition, and data mining algorithms. Two design techniques are introduced: dynamic segmentation with multi-cycle error compensation and delay budgeting for chained data path components. Extensive transistor-level simulations demonstrate that the optimised meta-function implementations consume up to 30% less energy at iso-error rates and achieve up to 27% lower error rates at iso-energy compared to their baseline counterparts. System-level simulations for three applications (motion estimation, support vector machine-based classification, and k-means-based clustering) show the impact of the improved meta-functions at the application level. The combination of transistor-level and system-level simulations provides a comprehensive analysis and demonstrates the benefits of the proposed design techniques. However, the paper lacks specific details about the dynamic segmentation and error compensation techniques. More information about these techniques' scaling implementation and operation would be helpful. The paper does not discuss potential limitations or trade-offs of the proposed design techniques; detailed observations could be more

helpful. On the other hand, it did not mention any mosfet technology nor any specific voltage range of threshold or supply voltage that can be applied [22].

2.3 Conclusion

In conclusion, the literature reviews provide valuable insights into the field of approximate computing and the design of approximate adders. The reviewed papers present various methodologies, circuit designs, and evaluation metrics for approximate computing. They highlight the trade-offs between accuracy, power dissipation, area utilisation, and performance in different approximate adder designs.

The papers demonstrate the effectiveness of approximate computing in reducing power consumption and improving energy efficiency. They propose novel circuit designs, such as MACACO, mirror adders, transmission gate-based adders, and approximate full adders, which offer advantages in terms of power dissipation, layout area, and delay.

However, some limitations are observed across the literature reviews. There is a lack of comprehensive analysis of higher-level algorithmic techniques for approximate computing, as most of the studies focus on hardware-level designs. The evaluation methodologies vary, and some papers do not provide explicit information about the software or simulation tools used for evaluation.

Furthermore, while the digital designs of approximate adders using logic gates are explored extensively, there is limited discussion on the applicability and performance of analogue designs. The impact of nanometer technology and voltage over-scaling methods on circuit performance is not thoroughly addressed in some papers.

Overall, the literature reviews contribute to the understanding of approximate computing and provide valuable insights into the design and evaluation of approximate adders. However, further research is needed to address the limitations and explore the potential of approximate computing in more advanced technology nodes and diverse application domains.

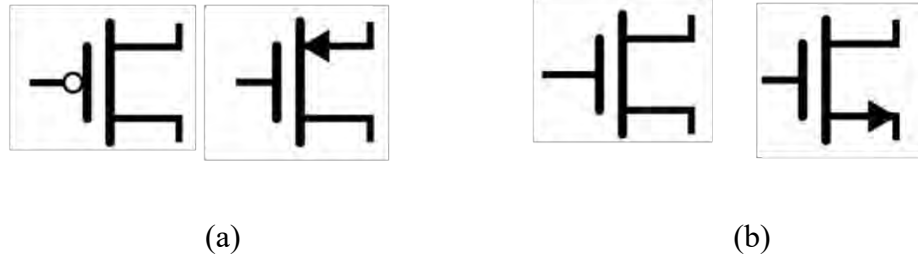


Figure 02: Symbols of (a) PMOS and (b) NMOS

3.2.1 Effect of Threshold Voltage

The threshold voltage of a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) is the minimum voltage that needs to be applied to the gate terminal to establish a conducting/Inversion channel between the source and drain regions of the transistor.

Equation of threshold voltage is $V_{th} = V_{to} + \gamma(\sqrt{|V_{sb}|})$

Where,

- V_{th} = Threshold voltage.
- V_{to} is the threshold voltage with no substrate bias ($V_{sb} = 0$).
- γ is the body effect coefficient, which depends on the MOSFET's characteristics and the substrate's doping concentration.

It establishes the time at which the transistor activates and begins to carry a sizable current. The MOSFET remains in an off-state, and only very little current flows through the channel when the gate voltage is below the threshold value. A sizable current can flow between the source and drain terminals after the MOSFET activates when the gate voltage surpasses the threshold value. The threshold voltage without substrate bias is shown in Figure 03 below-

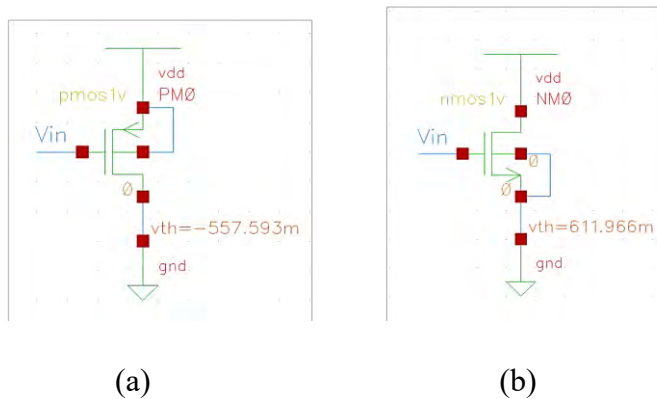


Figure 03: The threshold voltage (V_{th}) of 45nm (a) PMOS and (b) NMOS

3.2.2 Supply Voltage and Gate Voltage Scaling

Gate voltage scaling is often accompanied by supply voltage scaling. The supply voltage is reduced to match the reduced threshold voltage and maintain the desired performance levels. By decreasing V_{dd} , the dynamic power consumption, which is proportional to the square of V_{dd} , can be significantly reduced. However, lowering V_{dd} poses challenges in maintaining circuit performance, such as signal integrity and speed.

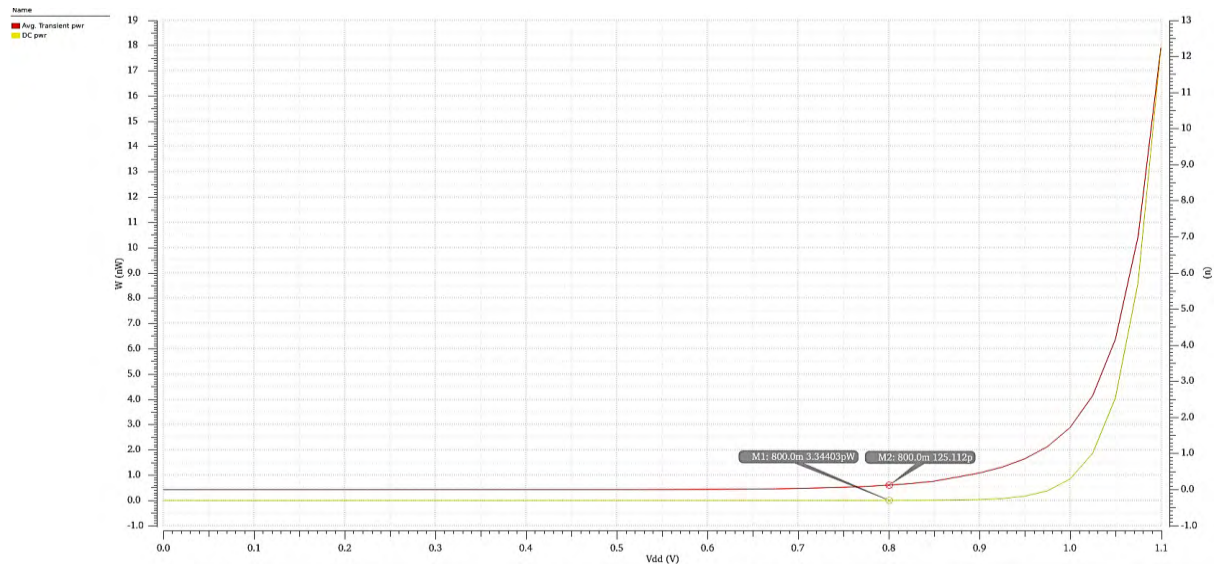


Figure 04: Average transient power and DC power vs Supply voltage

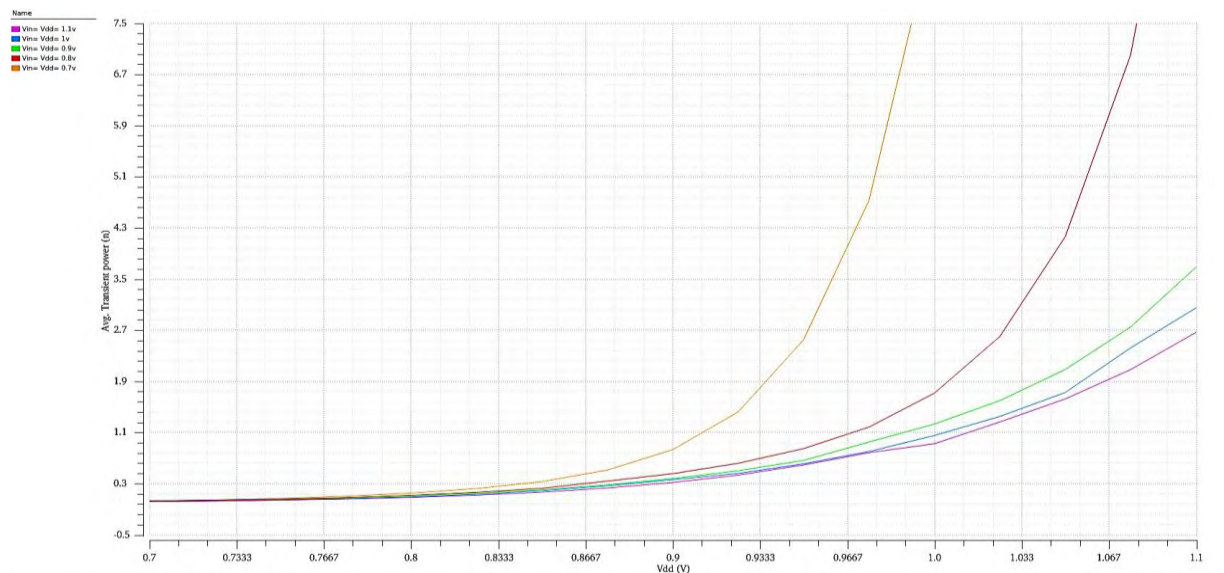


Figure 05: Parametric Average Transient power vs Supply voltage ($V_{dd}=V_{in}$)

- Considering the threshold voltage (3.2.1), voltage scaling (3.2.2), and from Figures 3,4 & 5, it can be said that the safest and less power-consuming supply voltage and gate voltage can be taken as 0.8 V.

3.2.3 Body Effect

The body effect, also known as the substrate bias effect or back-gate effect, refers to how the voltage applied to the substrate affects the transistor's behaviour. It influences the width of the depletion region between the source and drain regions, affecting the threshold voltage.

In an NMOS, a negative substrate bias widens the depletion region and source-to-body voltage increases. Hence the threshold voltage of the NMOS increases. It means that a higher gate voltage is needed to turn on MOSFET. In a PMOS, a positive substrate bias has a similar effect of increasing threshold voltage.

$$V_{th} = V_{th0} + \gamma(\sqrt{|V_{sb}|})$$

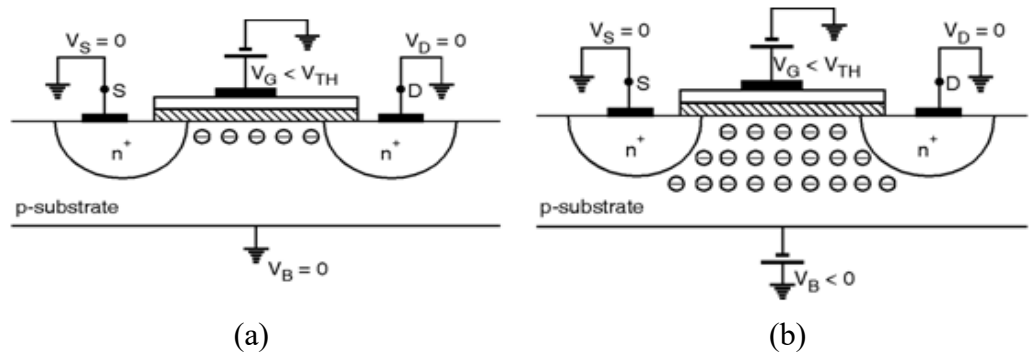


Figure 06: Depletion region of NMOS (a) without body effect and (b) with body effect

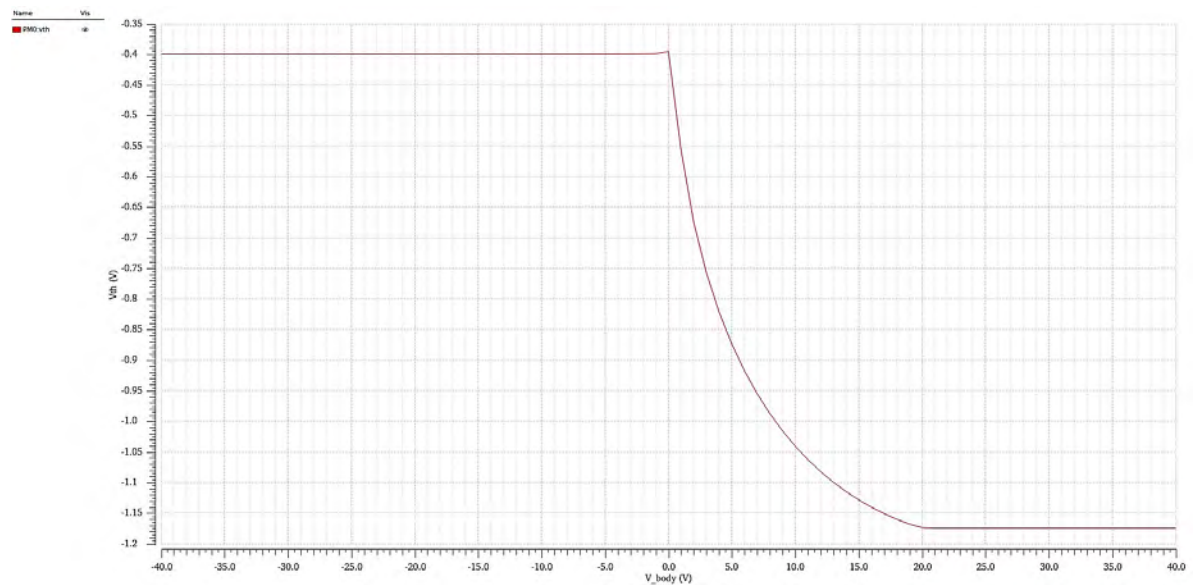


Figure 07: Change of threshold voltage of PMOS by body effect ($V_{dd}=0.8$ V)

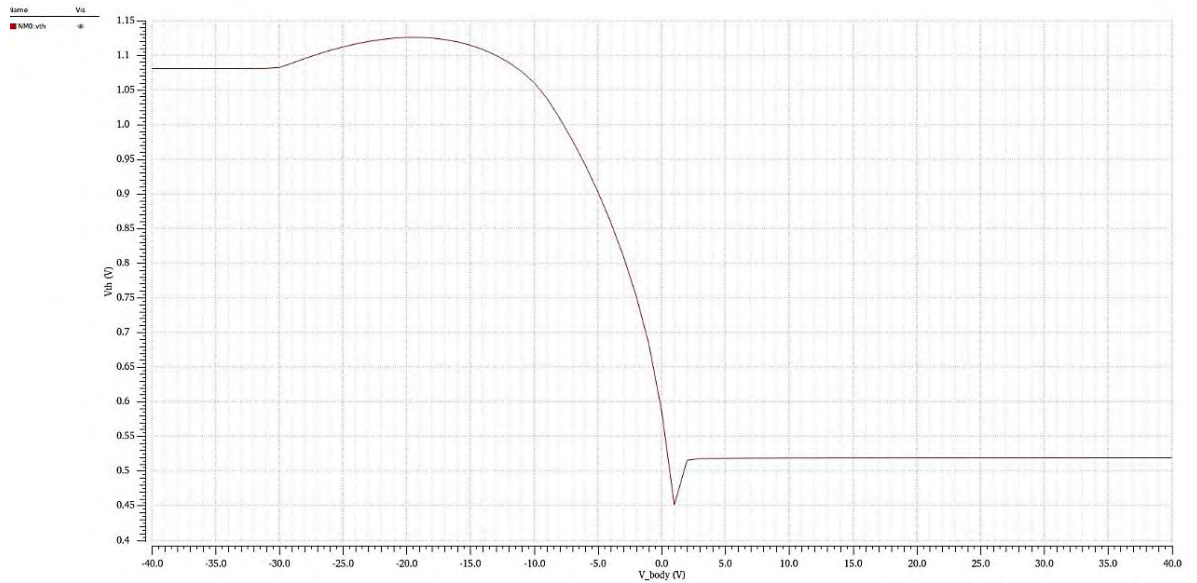


Figure 08: Change of threshold voltage of NMOS by body effect ($V_{dd}=0.8$ V)

3.2.4 Substrate Leakage Current

Substrate leakage current refers to the current that flows between the source/drain regions and the substrate of a MOSFET. In a MOSFET, the PN junction is formed between the semiconductor substrate and the heavily doped regions called source and drain, as shown in the figure below-

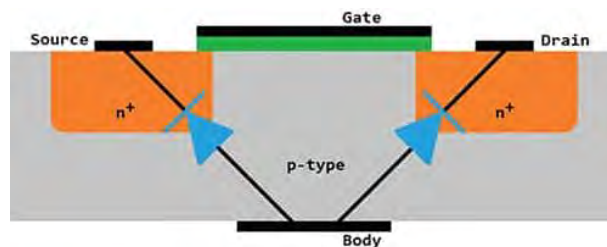


Figure 09: Formation of Body to Drain/Source PN junction in an NMOS

In an NMOS, if the body terminal is connected to a higher potential than the source/drain terminal, then a substrate leakage current starts to flow, which increases unwanted power dissipation. The Same happens for the PMOS when its body is connected to a lower potential than the source/drain terminal. The curve of Figure 10 and Figure 11 shows that the substrate leakage current (i_{sb}) and the internal MOSFET's power dissipation change by the substrate biasing voltage change. The curve was obtained by applying $V_{dd}=0.8$ v and varying substrate voltage that is shown below-

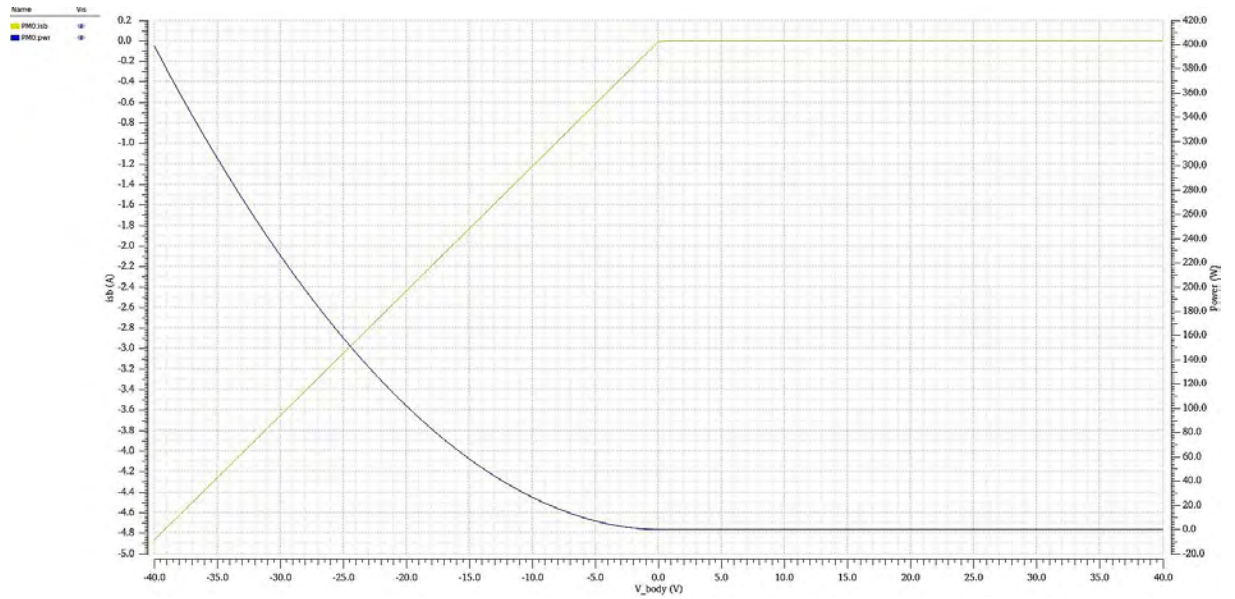


Figure 10: Substrate leakage current (i_{sb}) and power dissipation vs body terminal voltage curve of PMOS

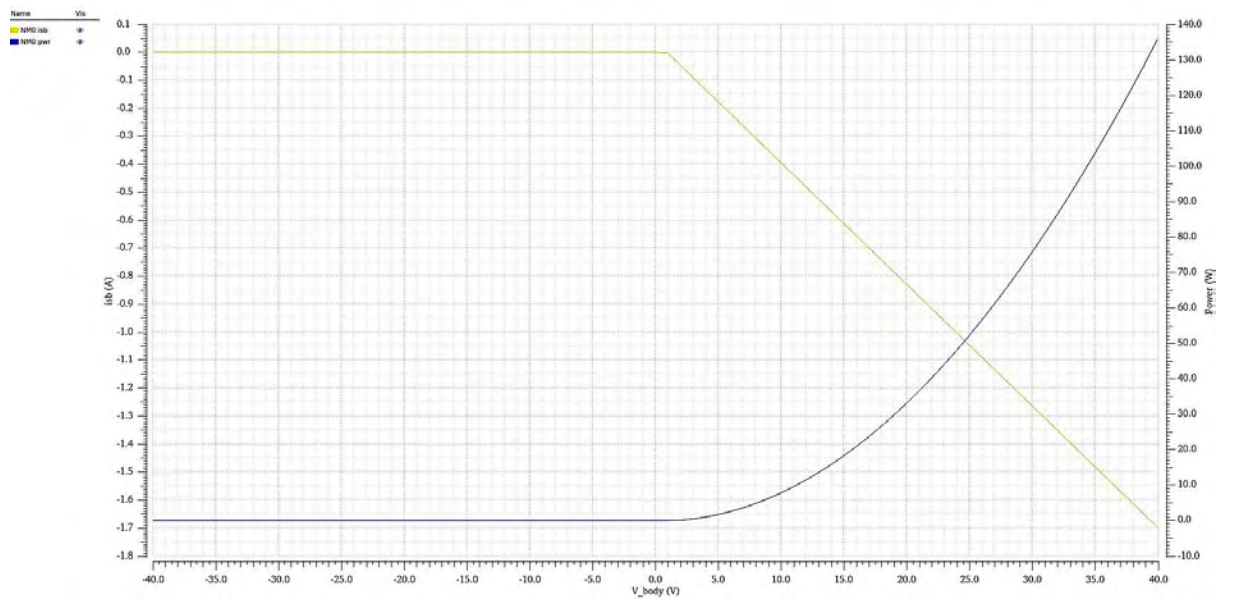


Figure 11: Substrate leakage current (i_{sb}) and power dissipation vs body terminal voltage curve of NMOS

- Considering the body effect (3.2.3) and substrate leakage current (3.2.4), and from Figures 7, 8, 10 & 11, it can be said that the safest way to design a MOSFET circuit is to connect all the PMOS body terminals to the V_{dd} and all the NMOS body terminals to the ground. In this way, there will remain a possibility of body effect and hence threshold voltage might change a little, but it will remain in the safe zone regarding leakage current flow or unwanted power dissipation.

3.3 CMOS Circuit

A popular technology for creating digital integrated circuits is CMOS (Complementary Metal-Oxide Semiconductor). Key elements of these circuits are CMOS transistors, whose operation and properties are designed by complementary pairs of PMOS and NMOS. These transistors are referred to as complementary because of how well their behaviours complement one another. This circuitry process perfectly utilises the “good high” and “good low” character of respective PMOS and NMOS. Complex digital circuits can be designed using CMOS technology, which has low power requirements, excellent noise immunity, and scalability. For a variety of uses, such as microprocessors, memory chips, and other integrated circuits, it has emerged as the industry standard.

3.3.1 CMOS Logic Operation

NMOS and PMOS transistors are combined in CMOS logic circuits to implement various digital operations. It is possible to build logic gates like AND, OR, NAND, NOR, and XOR by connecting the transistors in particular ways.

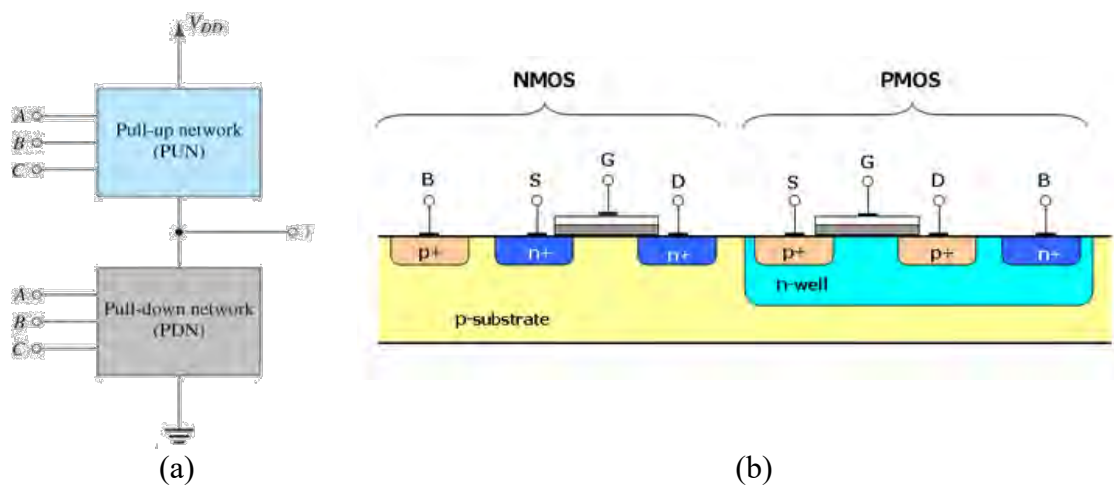


Figure 12: General (a) Schematic diagram and (b) Layout concept of CMOS circuit

The complementary nature of the transistors in CMOS logic enables both high noise immunity and low power consumption. An NMOS transistor functions as a closed switch, allowing current to flow when its input is high (logic “1”). On the other hand, when a PMOS transistor's input is high, it functions as an open switch and blocks current flow. This behaviour reduces power loss by ensuring the current only flows briefly during switching.

3.3.2 CMOS Inverter

The CMOS inverter comprises a PMOS transistor and an NMOS transistor coupled in series, with the sources and drains of each transistor connected to the other. Both transistors' gates receive the input, and their heads and gutters are connected to Vdd and Vss and joined at the output location, as shown in the figure below-

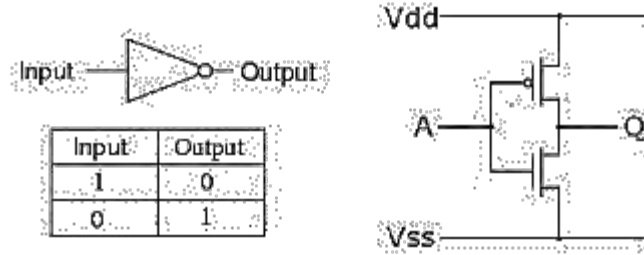


Figure 13: Inverter symbol, truth table and circuit diagram

The PMOS transistor conducts when the input is low (logic “0”), creating a low-resistance path to Vdd (positive power supply). The NMOS transistor is turned off concurrently, resulting in high resistance to the ground. The output is increased as a result (logic “1”).

The NMOS transistor conducts when the input is high (logic “1”), creating a low-resistance channel to the ground. The PMOS transistor is turned off simultaneously, resulting in a high resistance to Vdd. The output is thus low (logic “0”).

3.3.2.1 Inverter RC Model

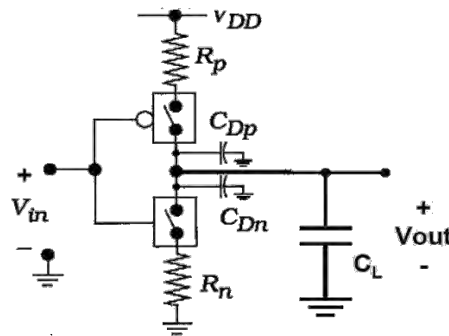


Figure 14: Equivalent RC model of CMOS inverter

The internal resistance and capacitance of the PMOS are denoted as R_p and C_{Dp} , respectively. Samely, for NMOS, it is denoted as R_n and C_{Dn} . Where,

$$R_n = 1/[\beta_n(V_{dd} - V_{tn})] \dots\dots\dots (i)$$

$$R_p = 1/[\beta_p(V_{dd} - |V_{tp}|)] \dots\dots\dots (ii)$$

$$C_{out} = C_{Dn} + C_{Dp} + C_L \dots\dots\dots (iii)$$

Here, β is the beta-effective of the MOSFET and $\beta = \mu \cdot C_{ox}(W/L)$

3.3.2.2 Rise Time, Fall Time and Delay Time of CMOS Inverter

Rise time, fall time, and delay time are a few factors that explain MOSFETs' switching behaviour. These variables are crucial in describing MOSFET-based circuits' timing and speed capabilities. Rise time and fall time with the RC effect are shown in the figure below-

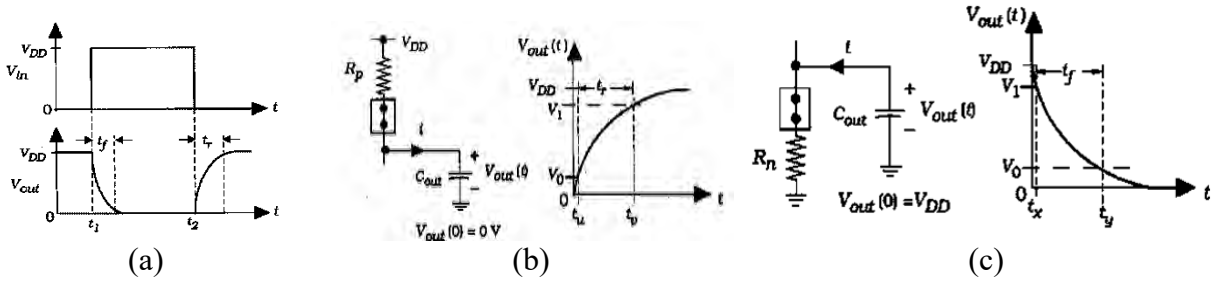


Figure 15: (a) Rise time and fall time in timing diagram (b) Rise time when PMOS active (c) Fall time when NMOS active

Rise time (t_r):

$$i = C_{out} \left(\frac{\partial V_{out}}{\partial t} \right) = \frac{V_{dd} - V_{out}}{R_p} \quad \dots \dots \dots (iv)$$

initially, $V_{out}(0) = V_{dd}$ and

at t time, $V_{out}(t) = V_{dd} [1 - e^{-t_r/\tau_p}]$; where, $\tau_p = R_p C_{out}$

$$\therefore t_r = \tau_p \ln \frac{V_{dd}}{V_{dd} - V_{out}} \quad \dots \dots \dots (v)$$

For the range of 20% to 80%, $V_{out} = 0.2 V_{dd} \sim 0.8 V_{dd}$

$$\text{So, } t_r = \tau_p \left[\ln \frac{V_{dd}}{V_{dd} - 0.8V_{dd}} - \ln \frac{V_{dd}}{V_{dd} - 0.2V_{dd}} \right]$$

$$\therefore t_r = 1.386 \tau_p \quad \dots \dots \dots (vi)$$

Fall time (t_f):

$$i = - C_{out} \left(\frac{\partial V_{out}}{\partial t} \right) = \frac{V_{out}}{R_n} \quad \dots \dots \dots (vii)$$

initially, $V_{out}(0) = V_{dd}$ and

at t time, $V_{out}(t) = V_{dd} e^{-t_f/\tau_n}$; where, $\tau_n = R_n C_{out}$

$$\therefore t_f = \tau_n \ln \frac{V_{dd}}{V_{out}} \quad \dots \dots \dots (viii)$$

For the range of 20% to 80%, $V_{out} = 0.2 V_{dd} \sim 0.8 V_{dd}$

$$\text{So, } t_f = \tau_n \left[\ln \frac{V_{dd}}{0.8V_{dd}} - \ln \frac{V_{dd}}{0.2V_{dd}} \right]$$

$$\therefore t_f = -1.386 \tau_n \quad \dots\dots\dots (ix)$$

The negative sign indicates the downward slope of the falling edge.

Propagation delay (t_p):

$$\text{Propagation delay} = \frac{1}{2} (t_r + t_f) = 0.69 (\tau_p + \tau_n)$$

For simplicity, we consider designing the CMOS circuit as the rise time equal to the fall time.

Hence,

$$t_r = t_f$$

$$\Rightarrow R_p C_{out} = R_n C_{out}$$

$$\Rightarrow \beta_n V_{tn} = \beta_p V_{tp} \quad [\text{from equation (i) \& (ii)}]$$

$$\Rightarrow \mu_n C_{ox} (W_n/L_n) V_{tn} = \mu_p C_{ox} (W_p/L_p) V_{tp} \quad [\text{as, } \beta = \mu C_{ox} (W/L)]$$

$$\Rightarrow W_p = W_n \times \mu_n / \mu_p \times V_{tn} / V_{tp} \quad [L_n = L_p = 45\text{nm technology}]$$

The default minimum width of the NMOS in 45nm technology is 120nm. The width of the PMOS will be greater than NMOS to get an equal delay. Applying parametric analysis of the width of the PMOS from 120nm to 300nm, it is found that the inversion voltage ($V_{inv} = 0.5 V_{dd}$) was achieved at 145nm width when $V_{dd}=0.8\text{V}$.

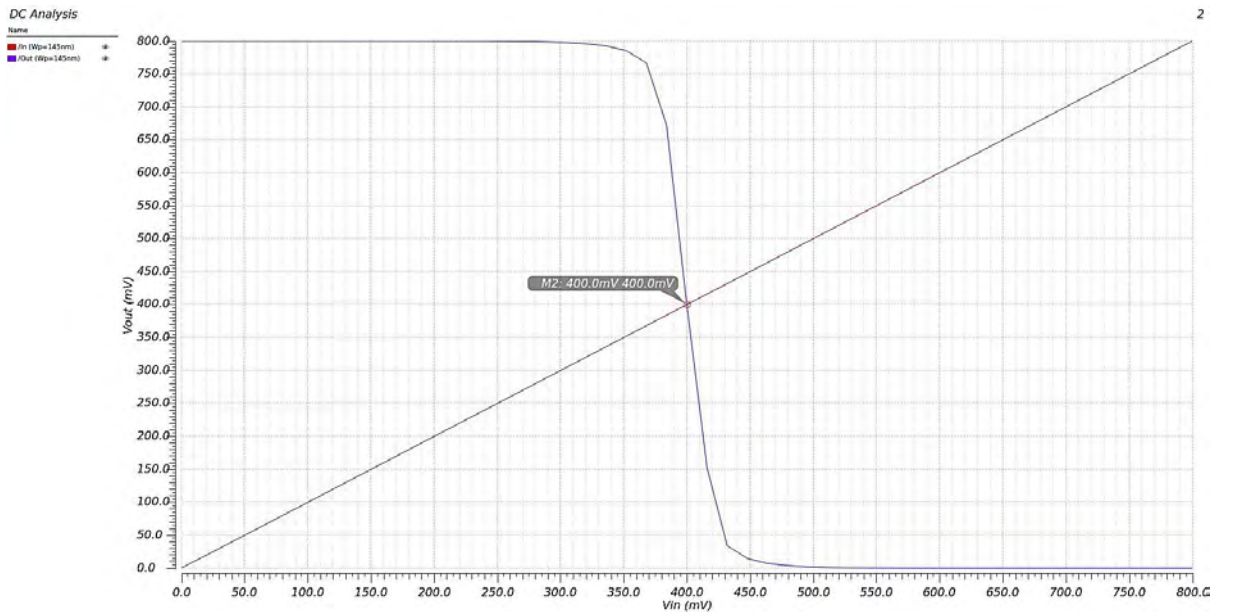


Figure 16: Inversion curve for PMOS width = 145nm

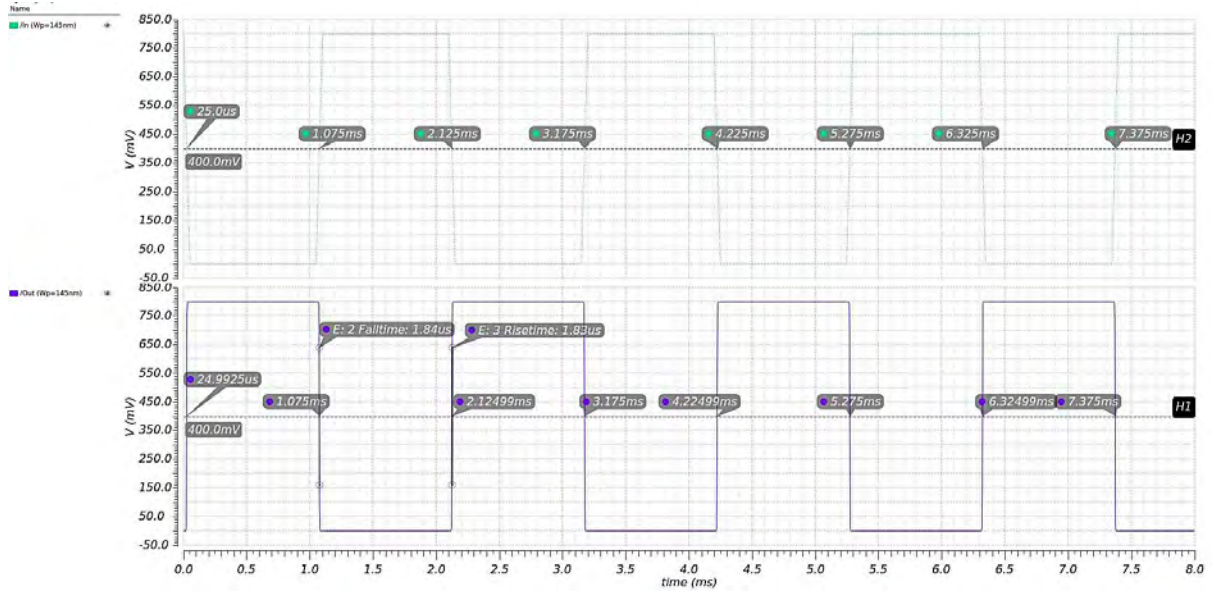


Figure 17: Equal fall time and rise time of an inverter

Applying $W_n = 120\text{nm}$ and $W_p = 145\text{nm}$ at transient analysis, it is found that the fall time and rise time are equal within the 20% to 80% range. On the other hand, it provides the lease delay at $\frac{1}{2} V_{dd}$.

- Considering fall time, rise time, and delay time (3.3.2.2), including figures 16 & 17, it can be said that the optimal way to get less delay in a CMOS circuit can be obtained by applying $W_n = 120\text{nm}$ and $W_p = 145\text{nm}$. Here, we have considered the CMOS inverter as the standard circuit. It might vary for the other circuit. Nevertheless, this study will apply $W_n = 120\text{nm}$ and $W_p = 145\text{nm}$ to maintain simplicity. Again, it is observed that the delay can easily be obtained at $\frac{1}{2} V_{dd}$ (0.4V) by comparing the input and output signal edges.

3.3.3 Power Dissipation of Inverter

The amount of power transformed into heat while a Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is functioning is referred to as power dissipation. As electronic switches or amplifiers, MOSFETs are frequently utilised in various applications.

Static and dynamic power dissipation are the two halves of the power dissipation in a MOSFET.

3.3.3.1 Static Power Dissipation

The MOSFET's steady-state status might be fully ON or OFF, causing static power dissipation or DC power loss. Even though no signal is applied to the gate terminal, a tiny current still flows through the MOSFET in the ON state. Power is lost due to this current, also called

leakage current. Static power dissipation can also occur in the OFF state, where there may still be a slight leakage current.

Static Power Dissipation, $P_{DC} = I_{DDQ} V_{DD}$

Where,

V_{DD} = supply voltage of the MOSFET

I_{DDQ} = quiescent leakage current (mainly due to leakage at substrate junctions for minority charge carrier).

3.3.3.2 Dynamic Power Dissipation

The switching activity of the MOSFET causes a component of power dissipation known as dynamic or transient power dissipation. Dynamic power dissipation is caused by the energy used during the charging and discharging. It takes a moment for the input and output capacitances of the MOSFET to charge or discharge when it switches between the ON and OFF states. The frequency of switching and the load capacitance both affect dynamic power dissipation in a direct proportion.

Dynamic Power Dissipation, $P_{dyn} = \alpha C_{out} V_{DD}^2 f$

Where,

F = switching frequency of MOSFET.

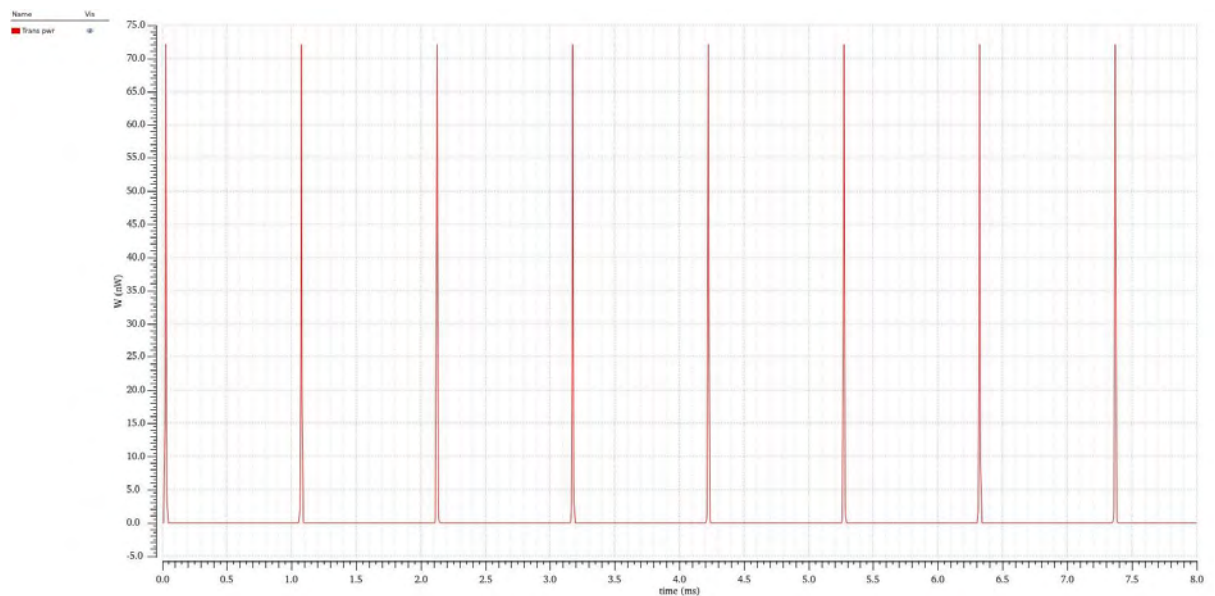


Figure 18: Transient power dissipation of CMOS inverter (45nm, $V_{DD} = 0.8$ V)

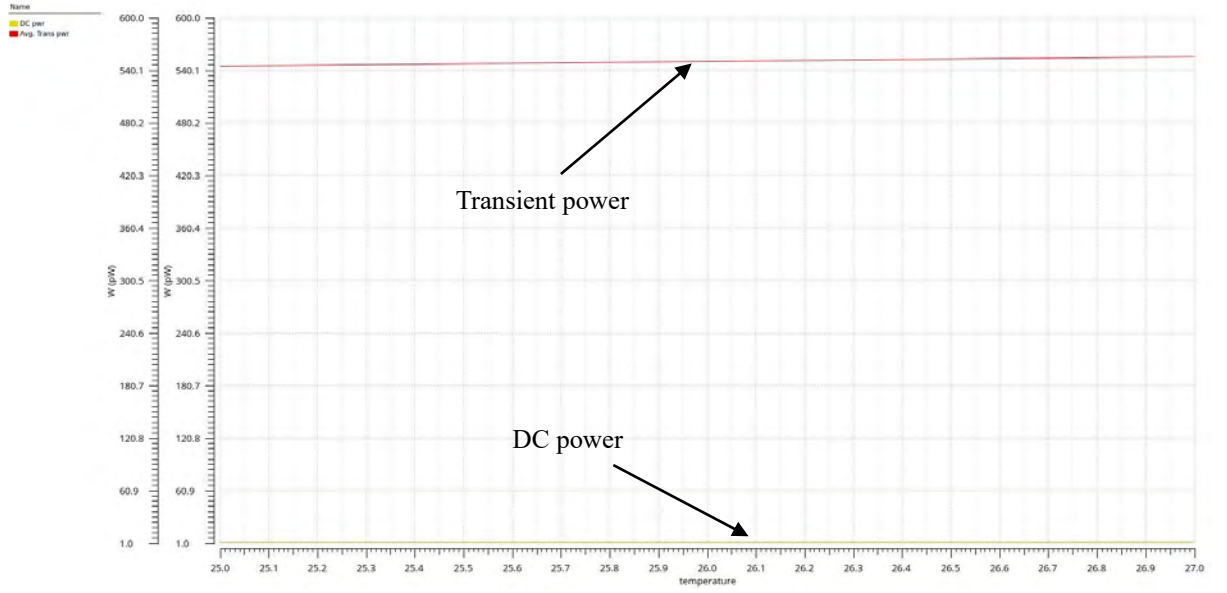


Figure 19: Average transient power and DC power dissipation of CMOS inverter

- Considering the power dissipation of the inverter (3.3.3) and Figures 18 and 19, it is observed that DC power dissipation has a lower impact, but transient power dissipation has more impact on power loss. We can achieve excellent efficiency by saving switching loss. Hence, this study will focus more on transient power dissipation.

3.4 Pass Transistor

A pass transistor, a transmission gate, is a fundamental electronic component for signal switching and amplification. It is typically implemented using complementary metal-oxide-semiconductor (CMOS) technology, consisting of both an N-channel MOSFET (NMOS) and a P-channel MOSFET (PMOS) connected in parallel.

The pass transistor allows signals to pass through from the input to the output terminal in the “ON” state, acting as a low-resistance path. Conversely, when the pass transistor is in the “OFF” state, it acts as an open switch, isolating the input from the output.

3.4.1 NMOS Pass Transistor

Let us consider a simple circuit where the input signal V_{in} is connected to the drain terminal of the NMOS pass transistor, and the output signal V_{out} is taken from the source terminal.

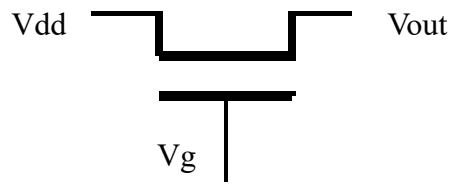


Figure 20: NMOS pass transistor working function

Operation:

1. ON Mode:

- When a positive voltage ($V_g > V_{th}$) is applied to the gate terminal, the NMOS transistor is turned on.
- The transistor channel forms a low-resistance path between the drain and source terminals.
- The input signal can pass through the transistor to the output terminal V_{out} without a significant voltage drop.
- The output signal, V_{out} , replicates the input signal, V_{in} .

2. OFF Mode:

- When no voltage or a low voltage ($V_g < V_{th}$) is applied to the gate terminal, the NMOS transistor is turned off.
- The transistor acts as an open switch, disconnecting the input and output terminals.
- The input signal V_{in} is isolated and does not reach the output terminal V_{out} .
- The output voltage remains unchanged or may be influenced by other components in the circuit.

By controlling the applied voltage to the gate terminal, the pass transistor can be switched between the ON and OFF modes, allowing or blocking the signal flow between the input and output terminals.

3.4.2 PMOS Pass Transistor

Let us consider a simple circuit where the input signal V_{in} is connected to the drain terminal of the PMOS pass transistor, and the output signal V_{out} is taken from the source terminal.

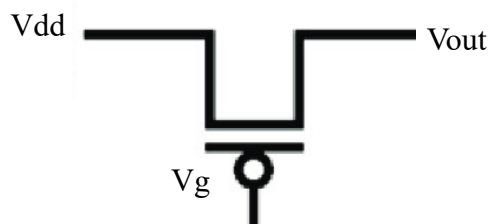


Figure 21: PMOS pass transistor working function

Operation:

1. ON Mode:

- When a negative voltage ($V_g < V_{th}$) is applied to the gate terminal, the PMOS transistor turns on.
- The transistor channel forms a low-resistance path between the drain and source terminals.
- The input signal can pass through the transistor to the output terminal V_{out} without a significant voltage drop.
- The output signal, V_{out} , replicates the input signal, V_{in} .

2. OFF Mode:

- When a positive voltage ($V_g > V_{th}$) is applied to the gate terminal, the PMOS transistor turns off.
- The transistor acts as an open switch, disconnecting the input and output terminals.
- The input signal V_{in} is isolated and does not reach the output terminal V_{out} .
- The output voltage remains unchanged or may be influenced by other components in the circuit.

By controlling the voltage applied to the gate terminal, the PMOS pass transistor can be switched between the ON and OFF modes, allowing or blocking the signal flow between the input and output terminals.

3.4.3 Comparison Between CMOS and PASS Transistors

CMOS circuits use complementary pairs of MOSFETs, while pass transistor circuits primarily use pass transistors. CMOS circuits have low power consumption during transitions and are fast, suitable for complex systems. Pass transistor circuits consume less power overall but have higher delays and are better for more straightforward or low-power applications. CMOS circuits have good noise immunity, while pass transistor circuits may be more susceptible to noise. The choice depends on specific requirements.

3.4.3.1 CMOS XNOR Design

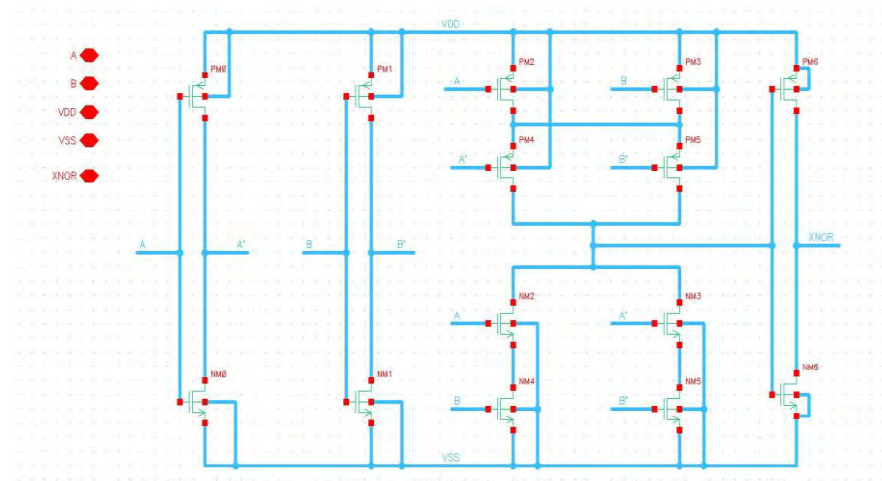


Figure 22: CMOS XNOR circuit

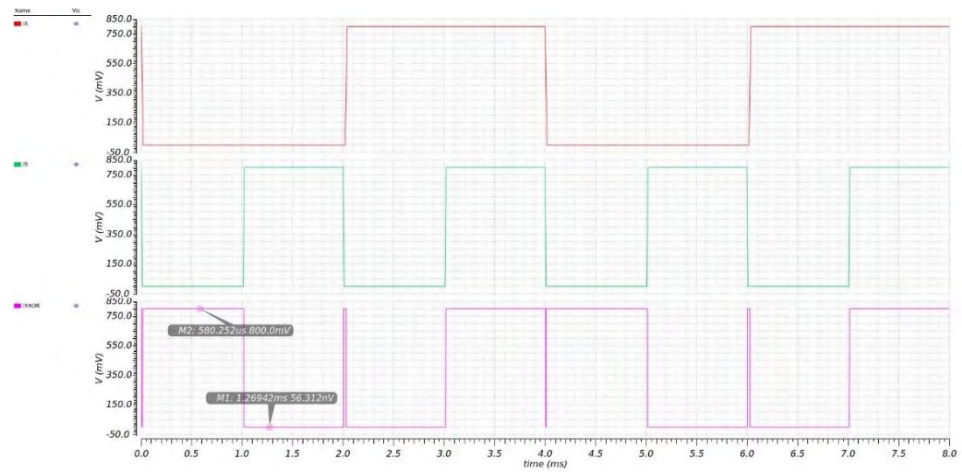


Figure 23: Timing waveform of CMOS XNOR circuit

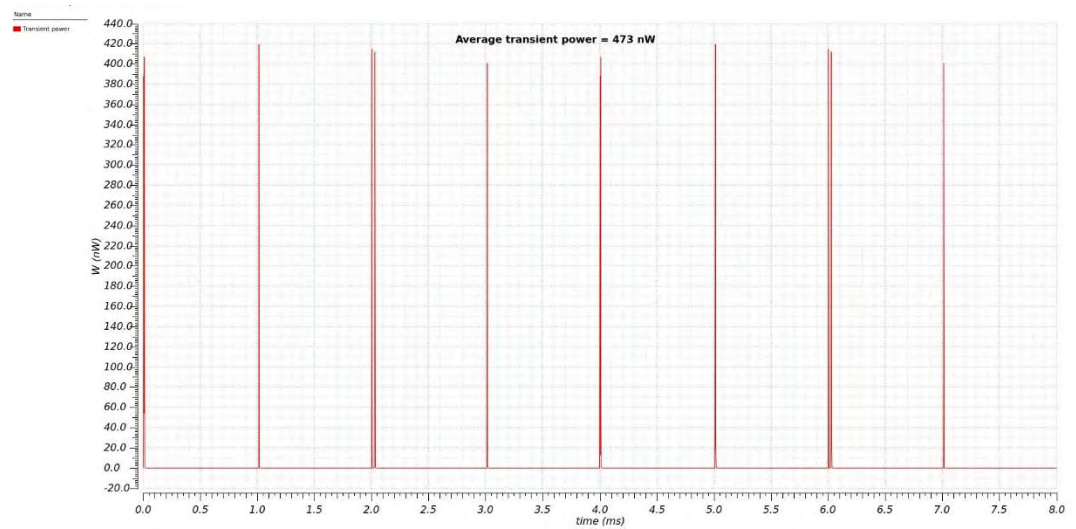


Figure 24: Transient power dissipation of CMOS XNOR circuit

3.4.3.2 Pass Transistor-Based XNOR Design

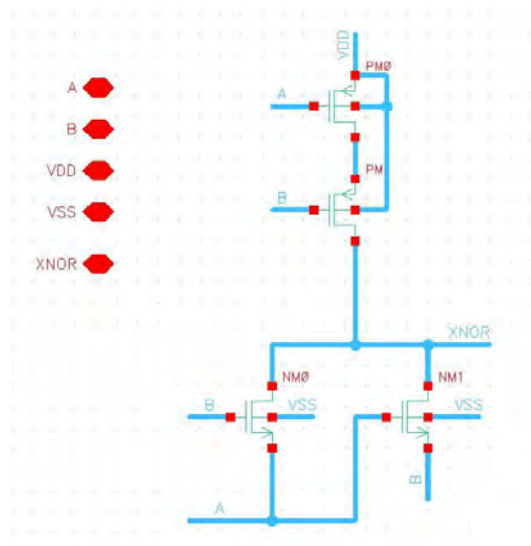


Figure 25: Pass transistor-based XNOR circuit

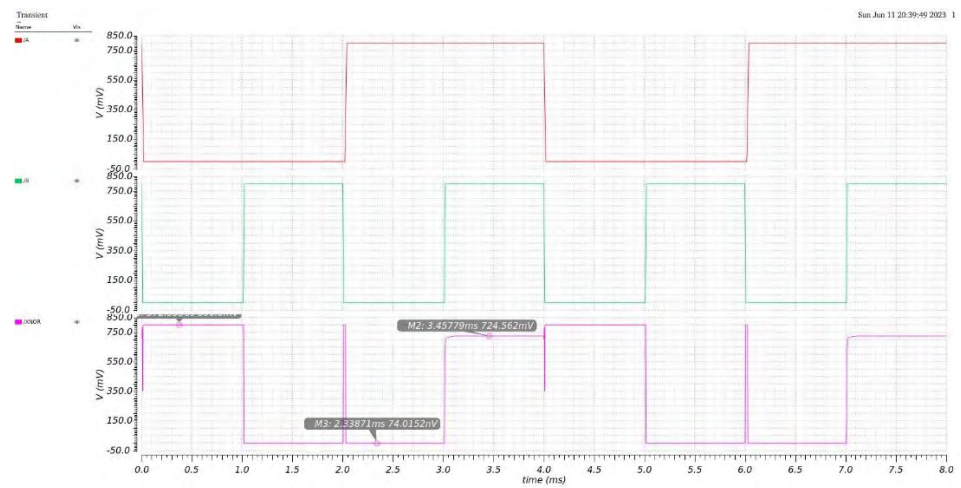


Figure 26: The timing diagram of pass transistor-based XNOR circuit

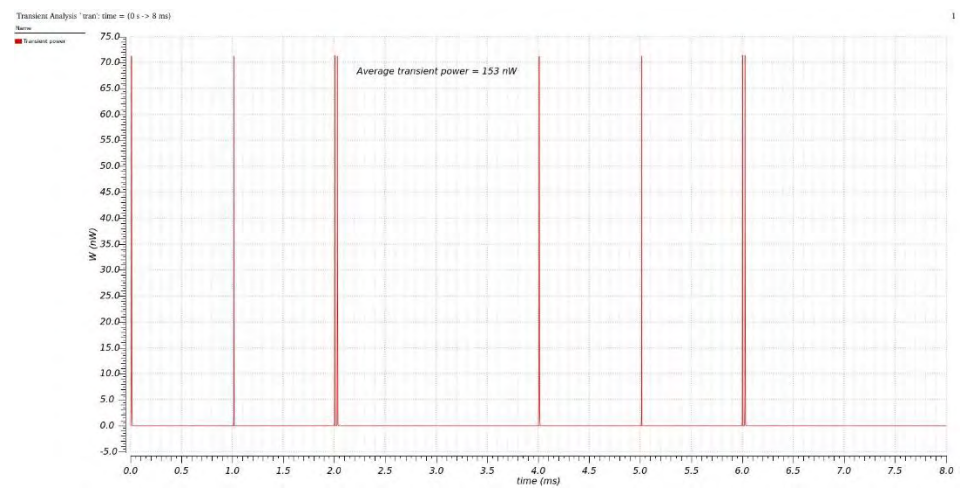


Figure 27: Transient power dissipation of XNOR pass circuit

Pass transistors have lower power dissipation in comparison to CMOS transistors. Fig (c) shows that CMOS dissipated 473nw, and from Fig (f) pass transistor dissipated 153 nw for the XNOR gate. CMOS uses 14 transistors, and the pass transistor circuit needs only four transistors for the same course. So that it dissipates low power, if the same transistor is required for CMOS and PASS transistor, then the pass transistor can be dissipated higher or lower energy than CMOS.

Another comparison is voltage level. CMOS has a proper voltage level, as shown in Fig (b). Pass transistors do not have predefined voltage levels like CMOS logic shown in Fig(e) and cannot pass good '1' or good '0'. Instead, the voltage levels in a pass transistor circuit depend on the input signal and the power supply voltages. Pass transistors operate in a continuous analogue range, allowing the input signal to pass through without significant distortion or voltage drop when the transistor is in the "ON" state.

CMOS logic operates with distinct voltage levels representing logic "1" and "0," where pass transistors operate in a continuous analogue range, closely following the input signal voltage.

Compatibility: CMOS technology, commonly utilised in contemporary digital integrated circuits, is frequently employed to implement pass transistors. Low power consumption, good noise immunity, and compatibility with various voltage levels are all features of CMOS technology.

The following restrictions should be considered when utilising pass transistors: Voltage restrictions: To maintain correct operation and prevent damage, the voltage levels applied to the pass transistor must be within its permitted range.

Pass transistors add resistance and capacitance, which can alter the signal propagation delay and impair the efficiency of the circuit.

Size and layout: When using multiple-pass transistors, the physical size of the transistors can impact the circuit's overall size and design.

Pass transistors provide effective signal routing and data transfer capabilities, which is why they are fundamental to the design of digital circuits. They are the essential building pieces that enable logic operations and signal to switch in various electronic devices.

3.5 Adder

An adder is a primary digital circuit that executes the addition arithmetic function. The addition of binary digits is a joint operation in many digital devices, including microprocessors, calculators, and digital signal processors.

An adder takes two binary input values and provides output by adding those numbers. Depending on the breadth of the binary integers being added, the adder can work on single or multiple bits simultaneously.

Half Adder: The simplest type of adder that can combine two single bits is a half adder. A and B serve as its two inputs, and S and C act as its two outputs. The half adder generates a carry output C if adding the input bits results in a carrier and the sum of the two input bits as the output S otherwise.

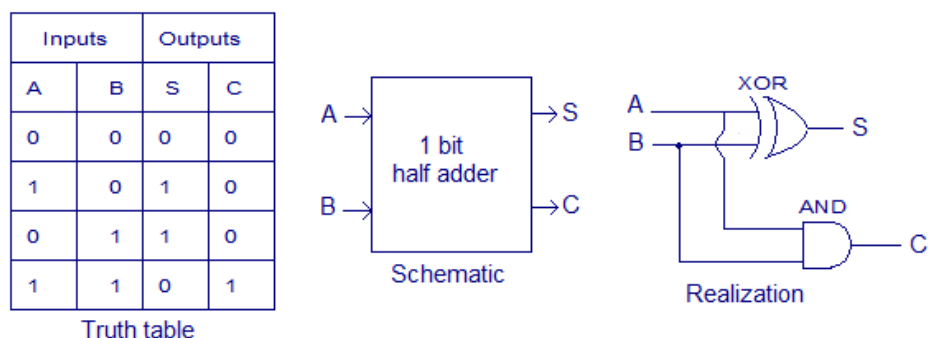


Figure 28: Half adder circuit and truth table

Full Adder: A full adder is a development of the half adder that can add two single bits in addition to an extra carry input. It has two outputs, the sum (S) and the carry output (C_{out}) and three input operands as A, B, and the carry input (C_{in}). The sum of the three inputs and a carry output are produced by the full adder, which also accounts for the carry from the preceding bit operation.

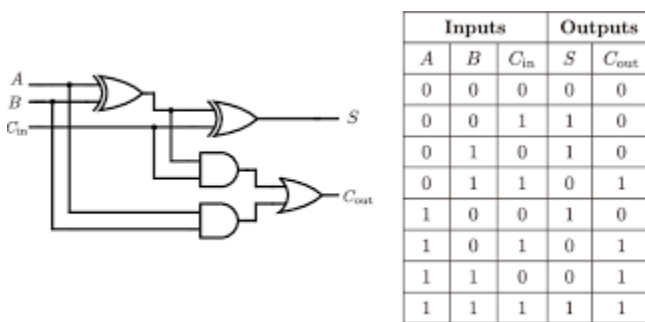


Figure 29: Full adder circuit and truth table

3.5.1 N-Bit Adder

An N-bit adder is a digital circuit that can add two N-bit binary numbers. It produces an N-bit sum and a carry-out bit. The adder consists of individual full adders connected in a cascade fashion. Each full adder takes three inputs: two bits from the added numbers and a carry-in from the previous stage.

The output of each full adder consists of the sum bit and a carry-out bit. The carry-out bit from one full adder becomes the carry-in bit for the next full adder, ensuring that carry propagation occurs through each stage.

3.5.1.1 Ripple Carry Adder

A ripple carry adder is a circuit that adds binary values with multiple bits. Because the carry bit ripples across each step of the adder from the least significant bit (LSB) to the most significant bit (MSB), it is known as a “ripple carry” adder

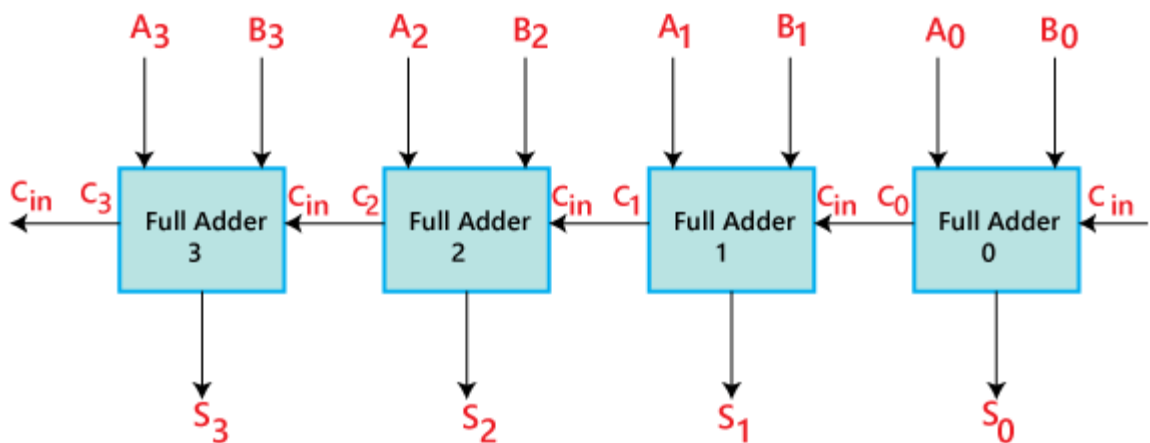


Figure 30: Ripple carry adder circuit

Inputs:

- The N-bit adder takes two N-bit binary numbers as input typically denoted as A and B.
- Each bit of the numbers ($A[0]$, $A[1]$, ..., $A[N-1]$) and ($B[0]$, $B[1]$, ..., $B[N-1]$) represents the individual bits to be added.

Stage-by-Stage Addition:

- The N-bit adder works stage-by-stage, starting from the least significant bit (LSB) and moving towards the most significant bit (MSB).

Full Adders:

- A full adder adds three inputs at each stage, the corresponding bits of A and B and the carry-in from the previous step (initially set to 0 for the LSB stage).
- The full adder consists of two main components: the sum output (S) and the carry-out (C_{out}).

Sum Bit:

- The sum bit (S) from each full adder represents the addition result of the corresponding bits of A and B, along with the carry-in from the previous stage.
- The sum bits form the N-bit output of the adder.

Carry Bit:

- Each full adder's carry-out (C_{out}) represents the carry generated while adding the corresponding bits.
- The carry-out from each stage becomes the carry-in for the next step, ensuring that carry propagation occurs across all bits.

Output:

- The final output of the N-bit adder consists of the N-bit sum ($S[N-1], S[N-2], \dots, S[0]$) and the carry-out (C_{out}) from the most significant bit stage.

3.5.1.2 Carry Look-Ahead Adder

For reducing the carry propagation delay, carry look ahead (CLA) is a technique that binary adders utilise to accelerate the addition process. A traditional ripple carry adder requires the carry bit to propagate through each step, which makes adding operations slow for wider bit-widths. With no need for carry propagation, take look-ahead adders to get around this restriction by concurrently calculating the carry signals for each bit location.

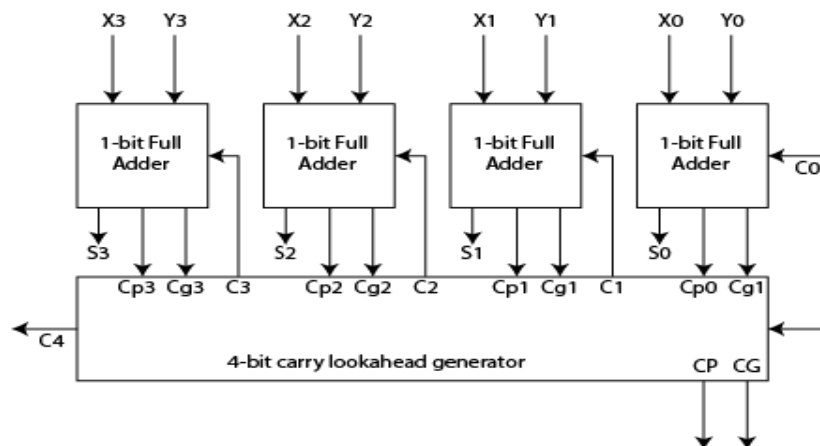


Figure 31: 4-bit carry look-ahead adder circuit

The carry bit for each bit position depends on the inputs and carries bits of the lower-order locations, as is the basis for the Carry look-ahead approach. Based on the information and take bits, it performs logic operations to construct the carry signals in advance. Due to the simultaneous availability of the carry signals, adding can proceed more quickly.

The carry bits are predetermined through carry look-ahead, regardless of inputs and take bits from lower-order positions. Because ripple moves, propagation is no longer necessary, the overall delay decreases and the addition speed increases.

3.5.1.3 Carry Skip Adder

Reduce the carry propagation latency to increase the efficiency of binary adders by using carry skip adders, carry special adders, or carry bypass adders. An overview of each is provided below.

A carry skip adder seeks to shorten the propagation delay for the carry by adding more parallel pathways for the carry. To accomplish this, fast carry-skip logic is used between these groups to link together several consecutive adder stages. If there is neither a carry-in nor a carry-out in a given group of adder stages, the carry can skip over those adder stages using the carry-skip logic. Decreasing the number of steps waiting for the carry signal to propagate aids in hastening the addition process. In contrast to other adder architectures, Carry Skip Adders might have a larger area and greater complexity.

3.5.1.4 Carry Look-Ahead Adder with Select Inputs

A carry-lookahead adder with select inputs, often called a carry-lookahead adder with selects, combines the benefits of ripple carry and carry-lookahead adders. Two sets of sum and carry outputs are produced for each group once the adder is divided into many groups. The carry input to the group is either assumed to be '0' in one set or '1' in the other, depending on the model. A multiplexer (select circuit) chooses the proper group of outputs by the actual carry input value. As a result, the carry propagation time is decreased by enabling the concurrent creation of the sum and carry signals. Carry Select Adders are more sophisticated than ripple have adders, which take up more space since they need additional multiplexer circuitry.

3.5.1.5 Carry Bypass Adder

A Carry Bypass Adder, also called a Carry-Save Adder, is a method that shortens the time it takes for a carry to propagate by storing intermediate carry values rather than instantly reproducing them. Two portions, one for carry generation and the other for carry propagation, comprise the adder stages. The carry values for every step are created and stored in registers in

the carry-generating portion. The held carry values and sum outputs are combined to make the final carry and sum outputs in the carry propagation step. Because the carry values can be computed individually and in parallel, saving the intermediate carry values reduces the carry propagation delay. Carry Bypass Adders are frequently employed in high-speed arithmetic circuits but need extra registers to hold the intermediate carry values.

3.6 Approximate Adder

A type of digital adder known as an approximation adder sacrifices precision for increased performance, power efficiency, or more minor size requirements. Approximate adders strive to achieve a near approximation of the total while minimising the complexity and resources required for the addition operation instead of producing precise addition results.

The concept behind approximate adders is founded on the fact that exact precision and results may be optional in many applications. Approximate adders can benefit from advantages like faster operation, less power usage, or simpler circuits by lowering the demand for precise results.

In approximation adder designs, several strategies are employed, including:

Bit Skipping: To minimise the number of calculations needed for the addition operation, bit skipping algorithms selectively skip or approximatively represent specific bits of the operands or the carry chain.

Probabilistic Computing: Probabilistic computing systems include stochastic or probabilistic aspects to approximate addition. These methods use statistical characteristics to deliver an approximation with less effort.

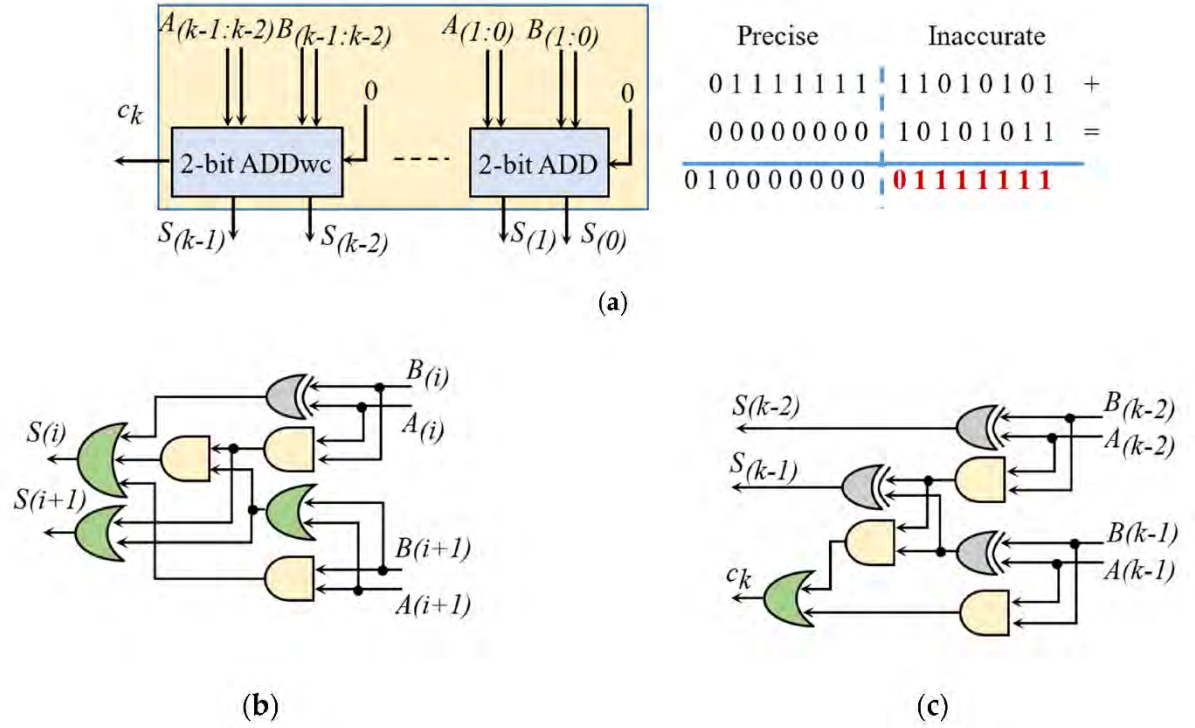


Figure 32: Approximate adder's conceptual figure

Error-Tolerant Logic: Error-tolerant logic techniques leverage the idea that some faults may be tolerable in particular applications by introducing controlled errors in the addition process. These adders can reduce circuit complexity and operate more quickly by enabling controlled defects.

The advantages of approximate adders over traditional accurate adders are faster performance and less power consumption. For applications where precise results are crucial, like necessary numerical computations, the trade-off is a loss of accuracy, which may need to be improved.

When a near approximation of the total is sufficient for the intended purpose, approximate adders are used. Low-power gadgets, audio and picture processing, machine learning techniques, and error-tolerant computers are a few examples.

It's crucial to remember that the specifications of the particular application and the allowed degree of approximation must be carefully considered while designing and implementing approximate adders. The degree of approximation must be weighed against the influence on total system accuracy, anticipated performance advantages, and both.

Chapter 4

Design And Analysis of Approximate Adders

4.1 Introduction

In this chapter, we will discuss the existing analogue circuit-based approximate adders and implement those circuits in 45nm technology. Those circuits will be designed by using the software Cadence. We will use the Cadence Spectre tool for delay and power dissipation analysis. The bit error rate will be analysed by using the MATLAB software. Later, four other efficient and less delayed approximate adders will be proposed, and a comparative analysis will be shown in this study. Information achieved from Chapter 3 will be applied to design and analyse the circuits.

Table 01: A summary of chapter-3 information

V_{dd}	: 0.8V	$V_{body(pmos)}$: V_{DD}
V_{in}	: 0.8V	$V_{body(nmos)}$: gnd
PW	: 1ms	W_n	: 120nm
$t_r(V_{in})$: 5% of PW	W_p	: 145nm
$t_f(V_{in})$: 5% of PW	V_{inv}	: 0.4V

Existing analogue circuit-based approximate adders that will be analysed in this study is: Approximate Mirror Adders (AMAs), XOR/XNOR-based Approximate Adders (AXAs), Transmission Gate based Approximate Adders (TGAs), Pass-transistor based Approximate Adders (PAAs).

4.2 Introduction of Cadence

Cadence Design Systems is a leading EDA software company offering various IC design and verification tools. Cadence tools are used by semiconductor companies, design houses, and individual engineers to design, simulate, and verify complex integrated circuits. Cadence tools provide a comprehensive design environment that covers various stages of the design process, including schematic capture, simulation, layout, and verification.



Figure 33: Cadence Logo

4.2.1 Cadence Virtuoso Tools

Cadence Virtuoso is a widely used electronic design automation (EDA) software tool suite provided by Cadence Design Systems. It is primarily used to design and layout complex integrated circuits (ICs) at both the transistor and block levels. Virtuoso is known for its powerful capabilities, flexibility, and integration with Cadence tools such as Spectre, PVS, Quantus, etcetera. Virtuoso includes a schematic editor that allows engineers to create and modify circuit schematics using a graphical interface. It offers various options for designing and connecting components, defining design rules, and specifying design parameters.

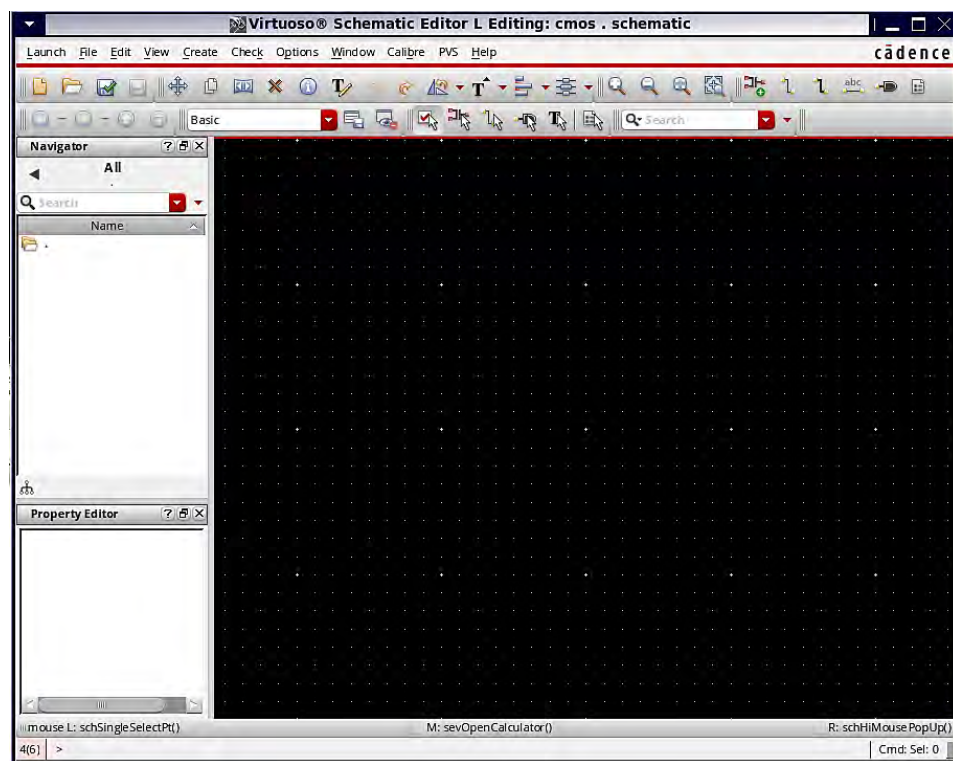


Figure 34: Cadence virtuoso schematic editor

Virtuoso supports using Process Design Kits, which provide process-specific information and guidelines for designing ICs using specific semiconductor technologies. PDKs contain information about device models, layout rules, and other process-related parameters. Additionally, The Virtuoso layout editor enables engineers to create the physical layout of ICs based on the circuit schematics. It provides advanced layout editing capabilities, including component placement, routing, and connectivity.

ADE, or Analog Design Environment, is an analysis tool provided by Cadence Virtuoso. ADE allows engineers to perform various circuit simulations, such as DC, AC, transient, and noise analysis. These simulations help analyse circuit behaviour under different operating conditions,

validate performance, and identify potential issues. The Cadence Virtuoso works combinedly with the spectre tools to accomplish ADE analysis.

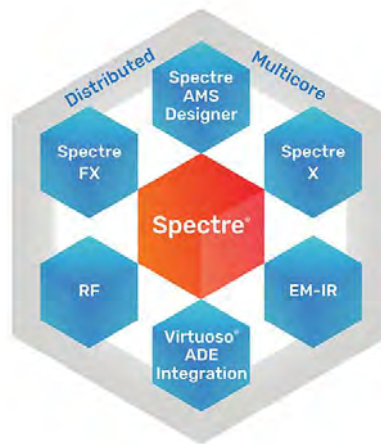


Figure 35: Applications of Cadence Spectre

4.2.2 Transient Analysis

Transient analysis in Cadence refers to the simulation and analysis of analogue and mixed-signal circuits to study their dynamic behaviour over time. It simulates the circuit's response to time-varying input signals and observes the resulting waveforms to determine delay and transient power dissipation.

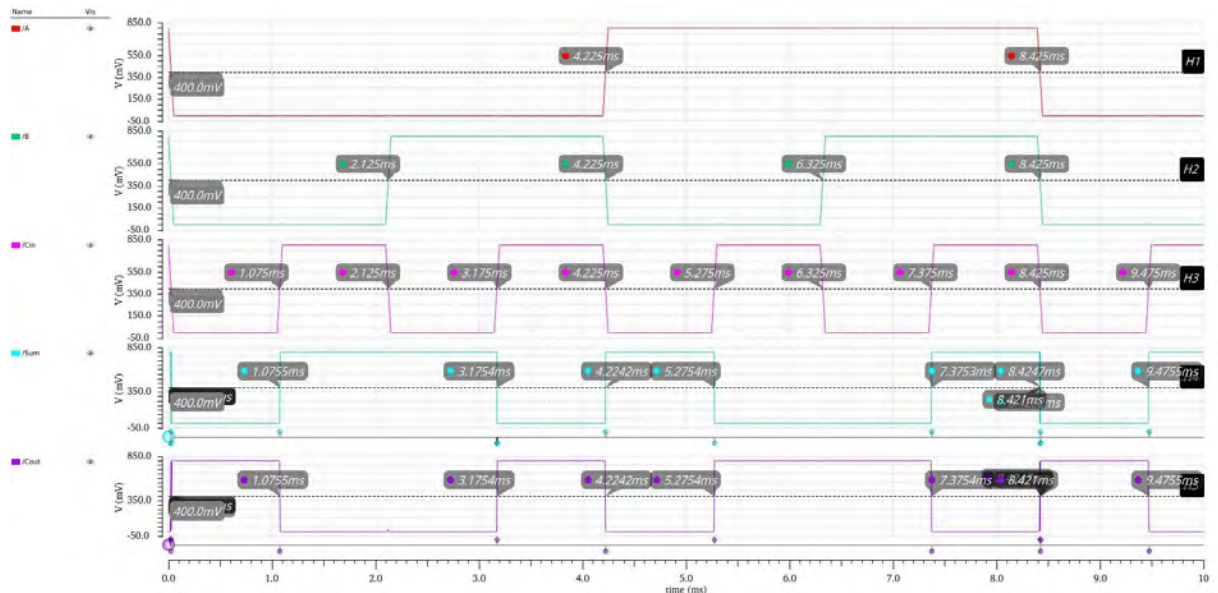


Figure 36: The resulting waveform of an analogue circuit

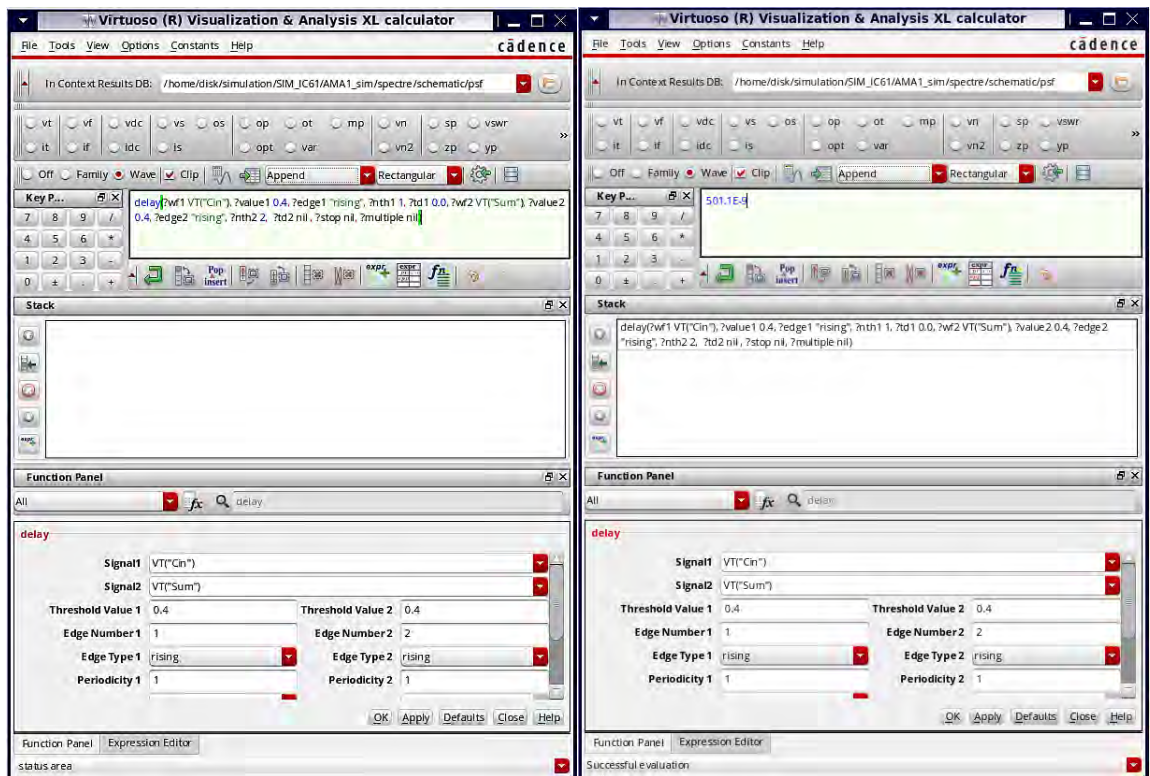


Figure 37: Delay calculation by Virtuoso visualisation & analysis calculator

Delay can be calculated by comparing input and output waveform at $\frac{1}{2} V_{dd}$ using Cadence virtuoso calculator, as shown in Figures 36 and 37.

Transient power analysis can be plotted using Cadence Virtuoso, and the average transient power can be obtained using a virtuoso calculator as shown in the figure below-

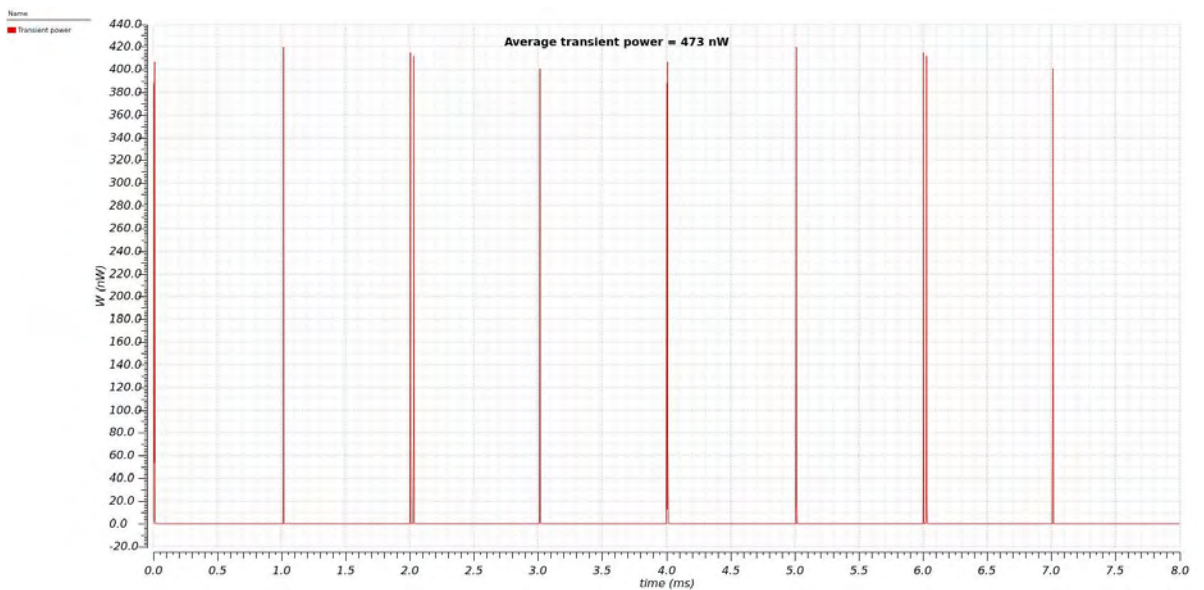


Figure 38: Transient power analysis using Cadence Virtuoso & Spectre

4.2.3 DC Analysis

DC analysis in Cadence refers to the simulation and analysis of analogue and mixed-signal circuits under DC (direct current) conditions. It involves determining the steady-state voltages, currents, and power dissipation in the circuit when all the time-varying signals are assumed to be constant.

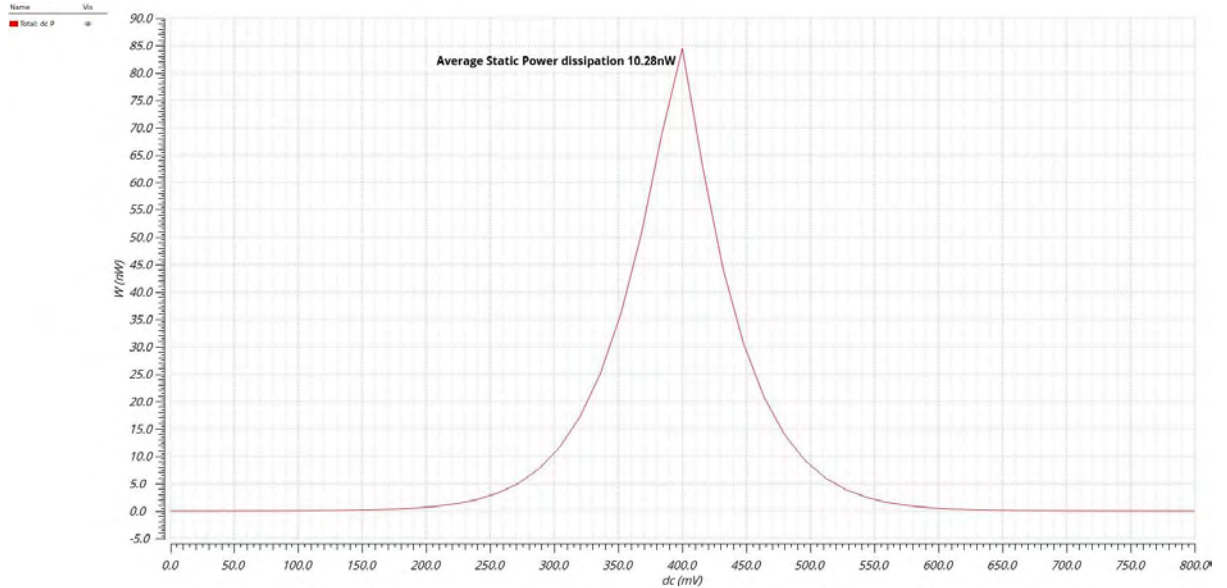


Figure 39: DC power analysis using Cadence Virtuoso & Spectre

DC/Static power dissipation can be plotted using Cadence Virtuoso, and the average static power loss can be obtained using a virtuoso calculator, as shown in Figure 26.

As this study is concerned about delay, transient, and static power dissipation, these three analyses will be done using Cadence Virtuoso & Spectre.

4.3 Introduction to MATLAB/Simulink

MATLAB and Simulink are software tools developed by MathWorks that are widely used in various fields, including engineering, science, and academia. They provide an integrated environment for numerical computation, data analysis, algorithm development, and simulation. Simulink is a graphical programming environment in MATLAB for modelling, simulating, and analysing dynamic systems. It uses a block diagram interface to create models by connecting pre-built blocks representing system components. Simulink supports various domains like control, signal processing, communications, power, and automotive systems. It enables simulation, result visualisation, and system response analysis.

In this study, we will use Simulink to determine the bit error rate of approximate adders.

4.3.1 Bit Error Rate Analysis

In Simulink, BER analysis of an approximate adder circuit involves evaluating the bit error rate of the circuit's output under various input patterns. A Simulink model representing the adder circuit is created, and input signals are generated to simulate different bit patterns. The circuit uses appropriate Simulink blocks, and the output is compared to the expected result. Simulation parameters are set, and the simulation is run to compute the bit error rate. Results are analysed using Simulink's visualisation tools, providing insights into the circuit's error performance.

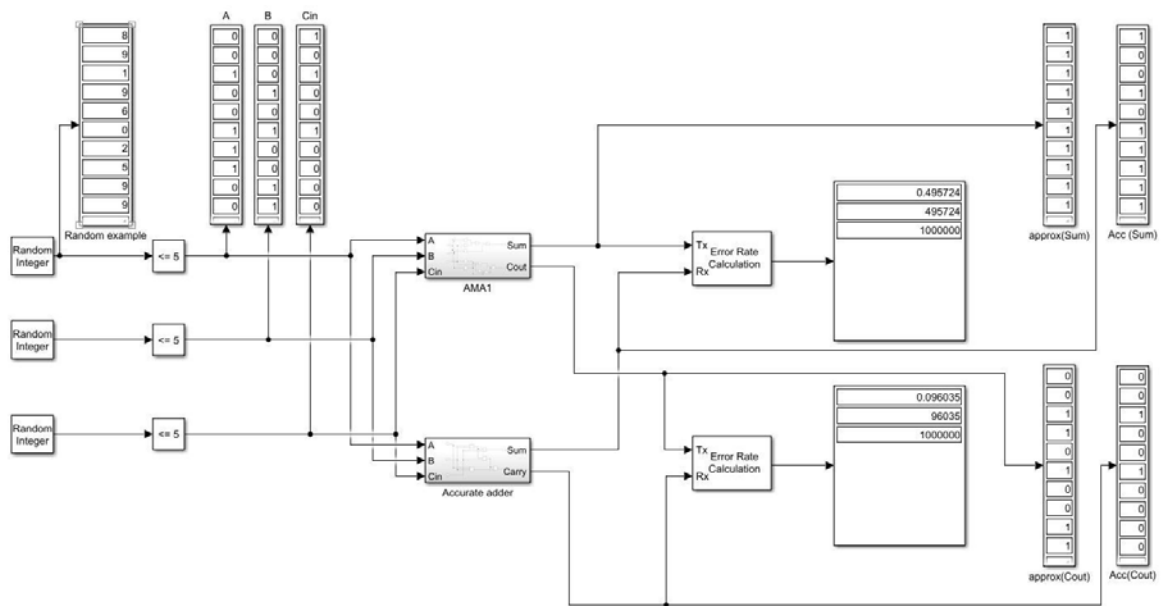


Figure 40: Bit error rate analysis of an approximate mirror adder compared with an accurate adder

Using the MATLAB Simulink, we will apply 10,00,000 randomly generated binary three input data to an approximate and accurate adder. The output gets almost stabilised for this vast amount of random data as the figure shows the BER of sum = 49.57% and BER of carry= 9.6%.

4.4 Existing Approximate Adder Analysis

A study on approximate adders aims to balance achieving performance improvements while maintaining acceptable levels of accuracy for specific applications. Research in approximate adders is ongoing, aiming to explore new techniques and optimisations. Some areas of active research include: developing optimal algorithms, error-resilient arithmetic designs, digital and analogue circuit designs, selective approximation or designing approximate adders for specific error-tolerant applications. This study will discuss analogue circuit-based approximate adders for DSP applications.

4.4.1 Approximate Mirror Adders (AMAs)

The approximate mirror adder is a variation of the conventional mirror adder, a high-speed adder architecture widely used in digital arithmetic circuits. The approximate mirror adder introduces approximation techniques to reduce power consumption and improve performance while sacrificing accuracy.

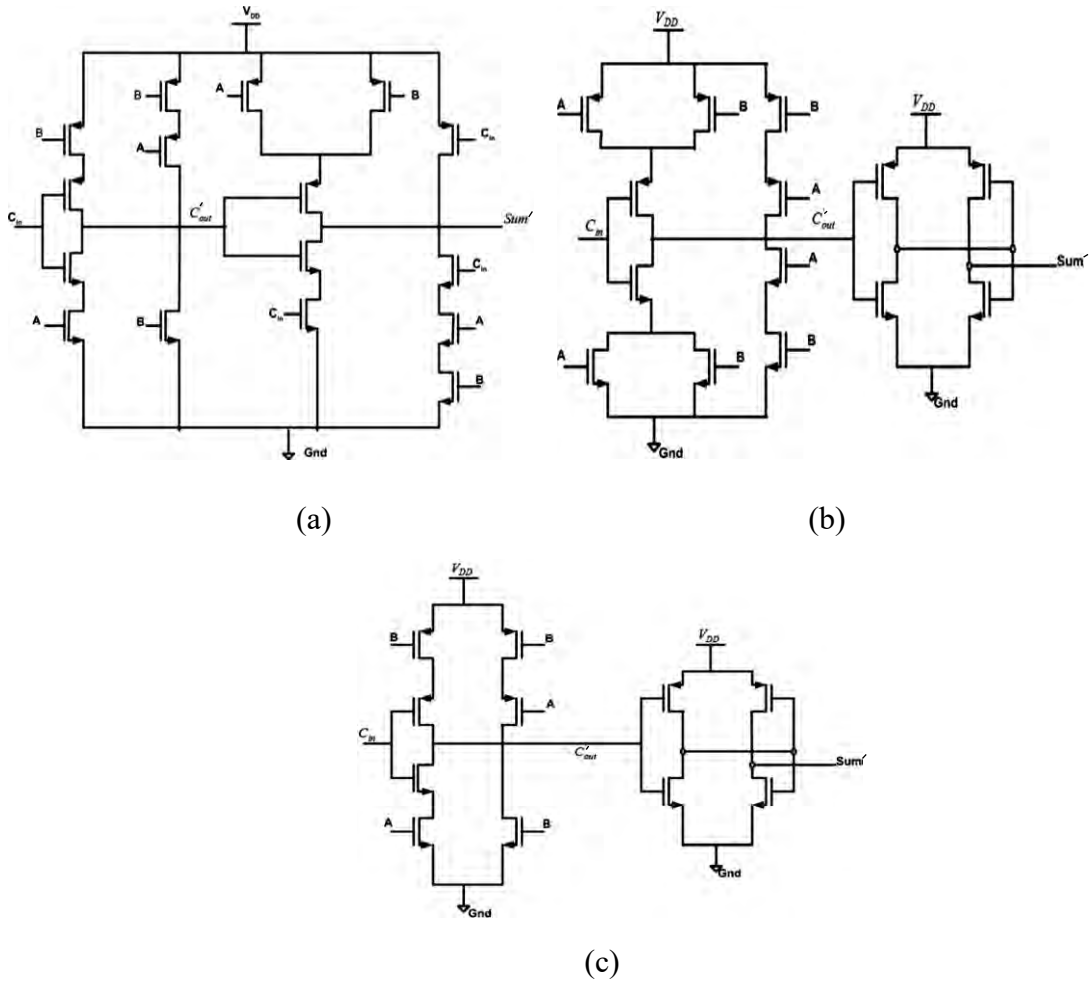


Figure 41: Schematic diagram of (a) AMA1, (b) AMA2 and (c) AMA3

4.4.1.1 Transient and DC Analysis (AMA1)

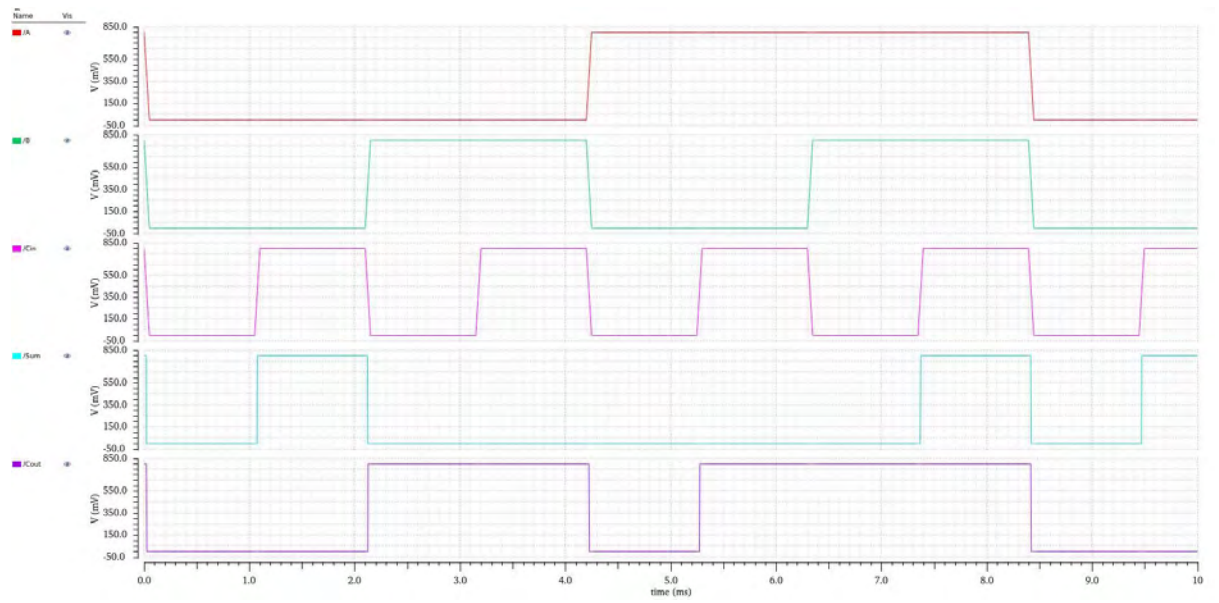


Figure 42: The transient waveform of AMA1

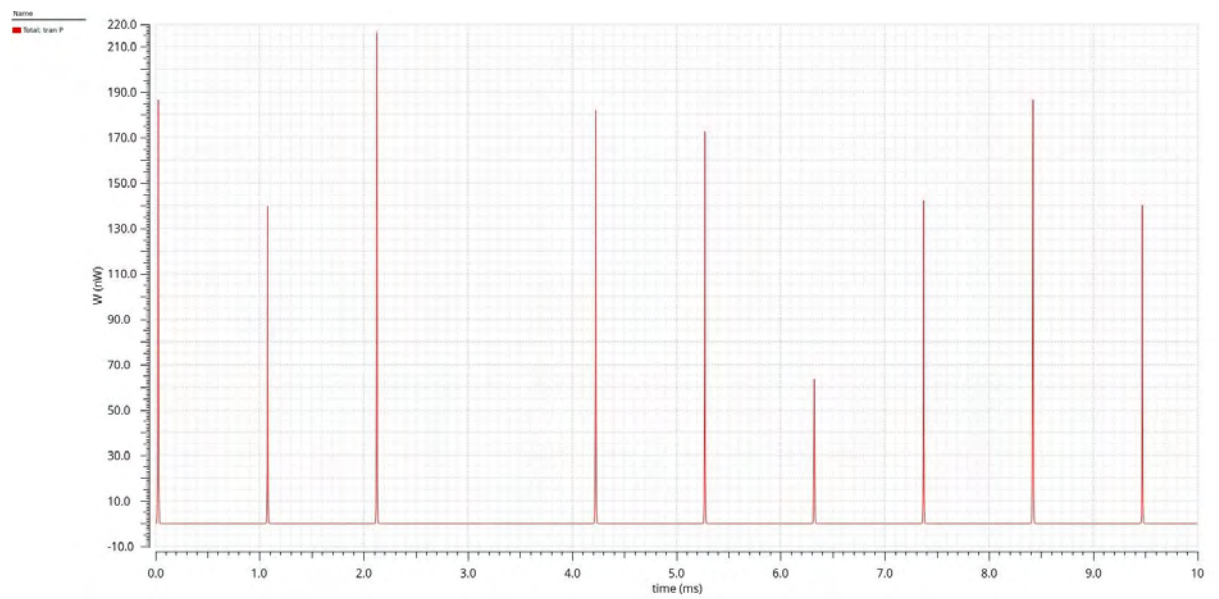


Figure 43: Transient power dissipation of AMA1

From the figure above, it is found that,

- Average transient power dissipation = 698.85 pW
- Delay of sum = 171.19 ns
- Delay of carry = 1.33 μs

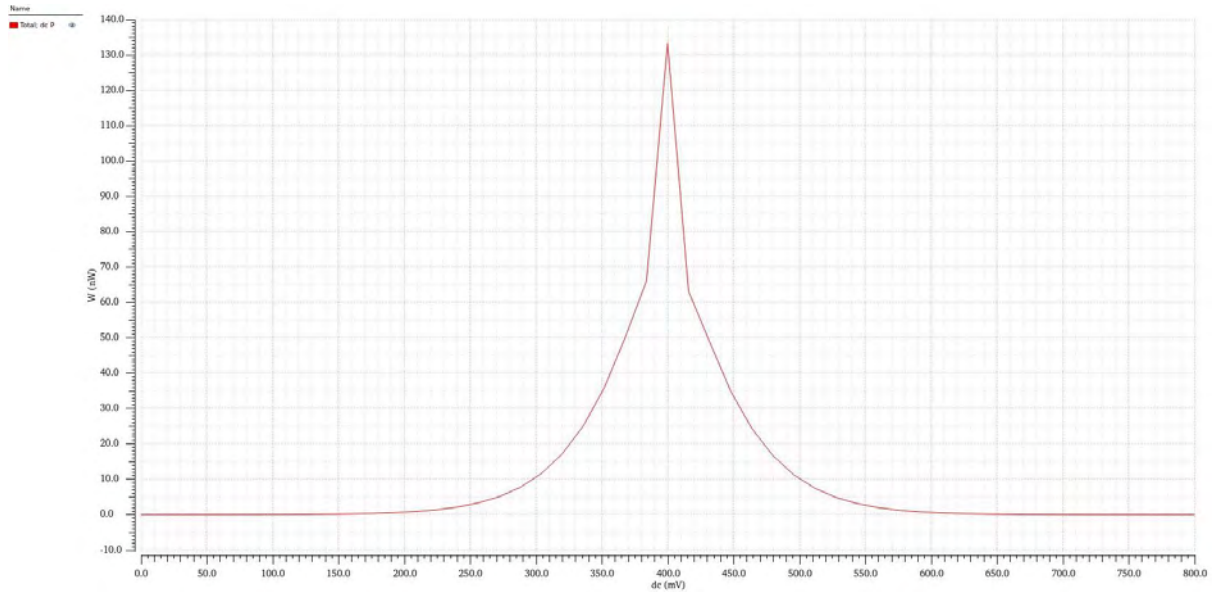


Figure 44: Static power dissipation of AMA1

From the static power dissipation, it is found that,

- Average static power dissipation = 11.635 nW

4.4.1.2 Bit Error Rate Analysis (AMA1)

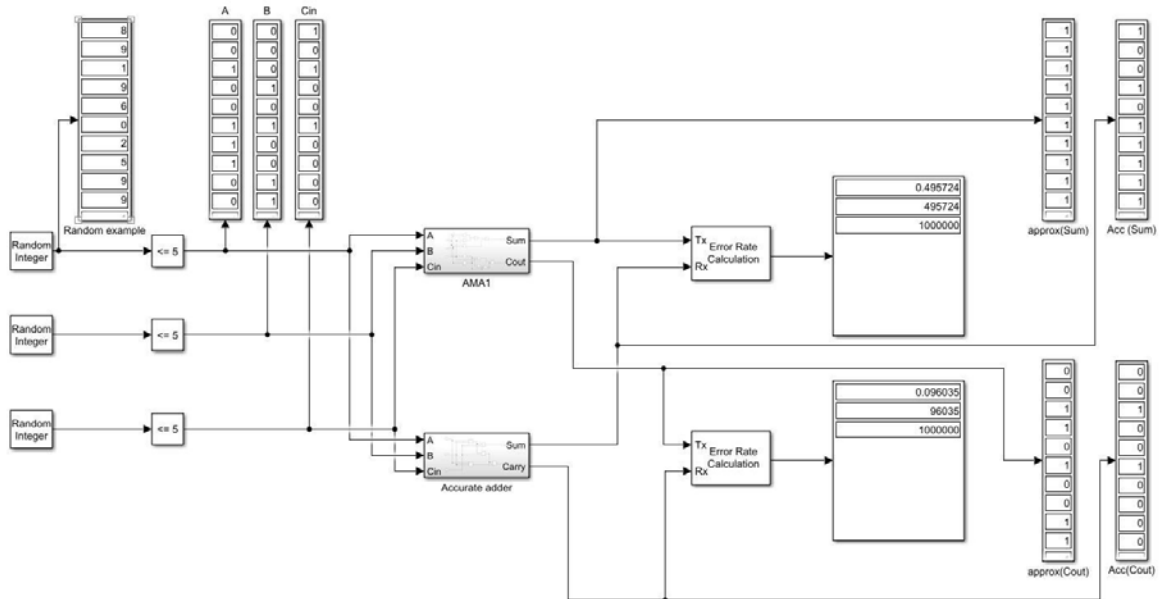


Figure 45: Bit error rate analysis of AMA1

From the figure above, it is found that,

- BER of sum = 49.57%
- BER of carry = 9.6%

4.4.1.3 Transient and DC analysis (AMA2)

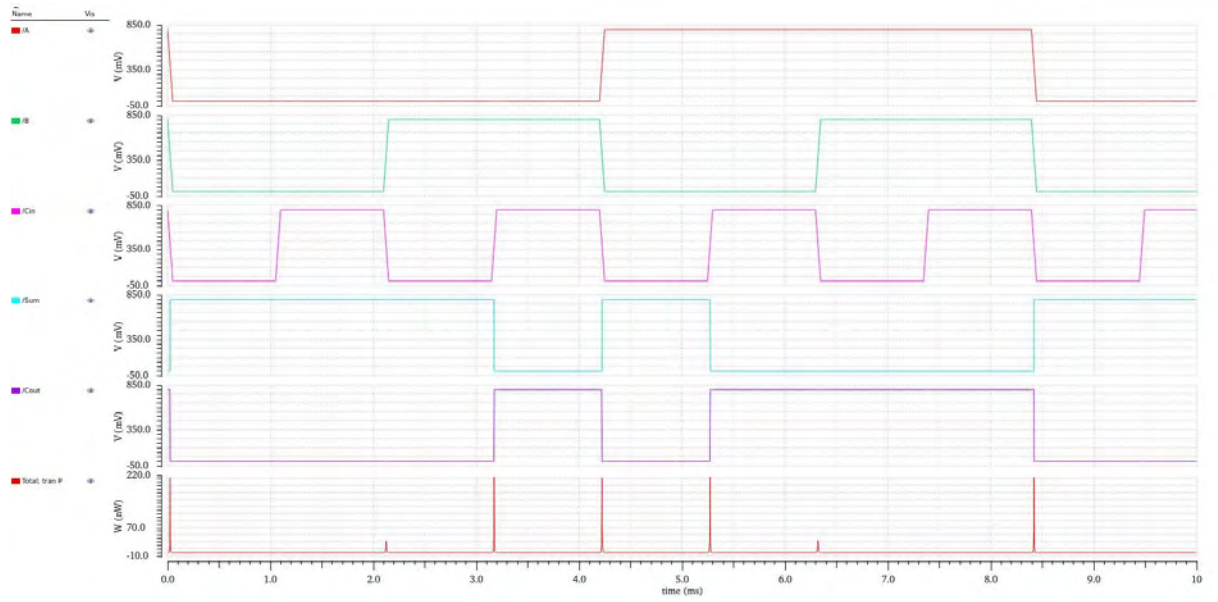


Figure 46: Transient analysis of AMA2

From the transient and dc analysis of AMA2, it is found that,

- Average transient power dissipation = 344.024 pW
- Delay of sum = 9.71 ns
- Delay of carry = 8.8 ns
- Average DC power dissipation = 9.54 pW

4.4.1.4 Bit Error Rate Analysis (AMA2)

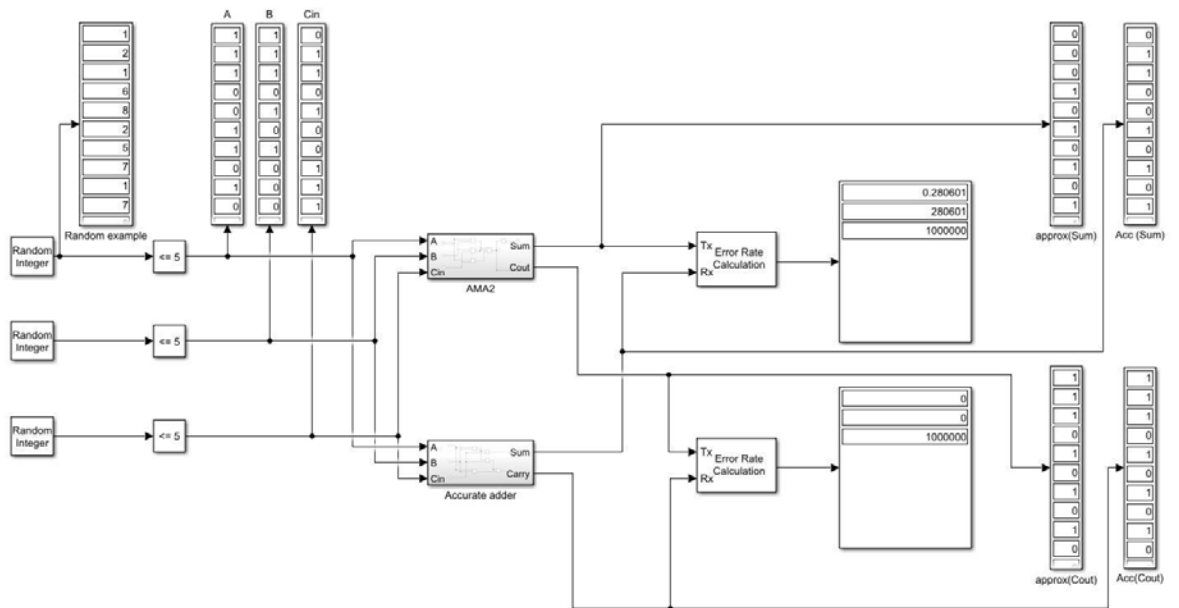


Figure 47: BER analysis of AMA2

- BER of sum = 28.06%
- BER of carry = 0%

4.4.1.5 Transient and DC analysis (AMA3)

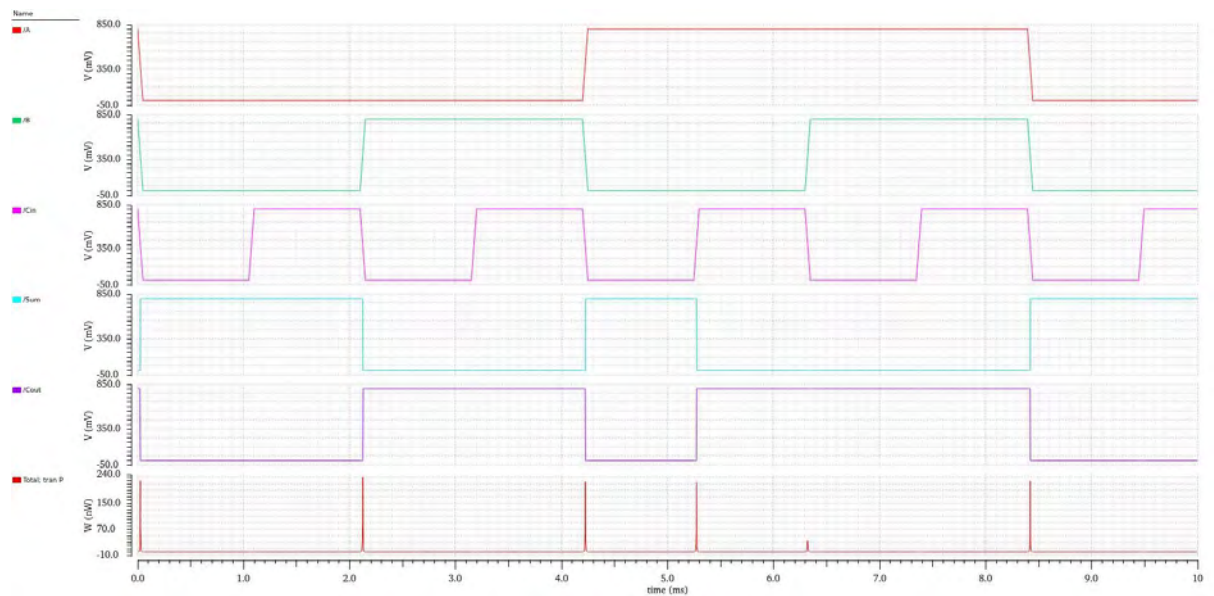


Figure 48: Transient analysis of AMA3

From the transient and DC analysis of AMA3, it is found that,

- Average transient power dissipation = 355.92 pW
- Delay of sum = 1.332 μ s
- Delay of carry = 1.331 μ s
- Average DC power dissipation = 8.37 pW

4.4.1.6 Bit Error Rate Analysis (AMA3)

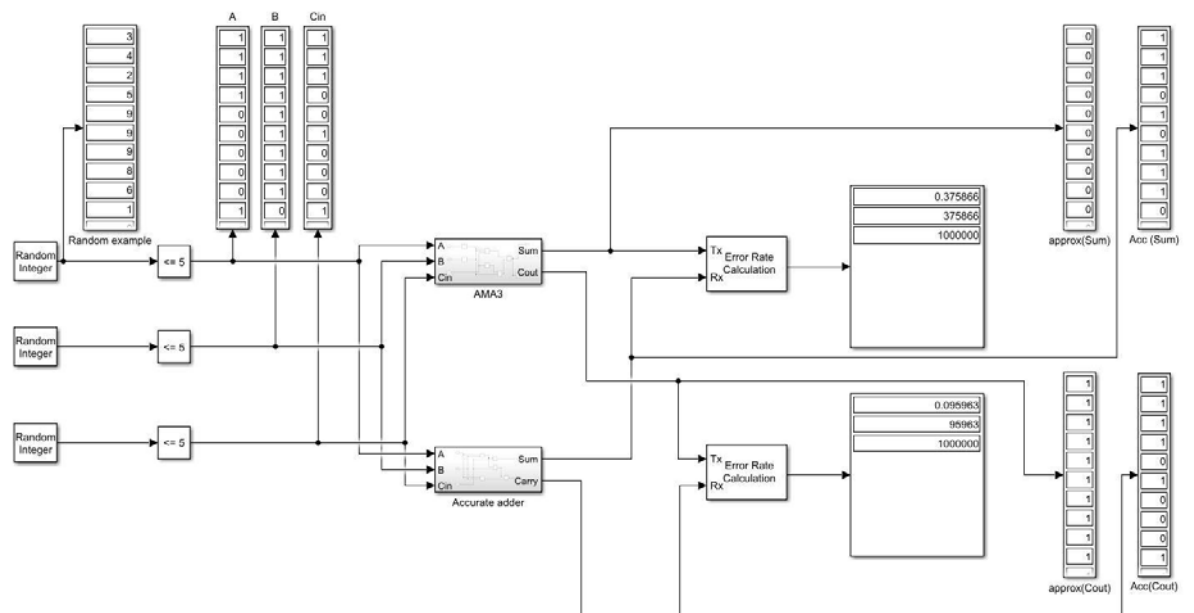


Figure 49: BER analysis of AMA3

- BER of sum = 37.58% BER of carry = 9.59%

4.4.2 XOR/XNOR Based Mirror Adders (AXAs)

The AXA adder is based on exploiting the properties of XOR and XNOR gates to introduce controlled errors in the addition operation and evaluate the trade-offs between accuracy, hardware complexity, and power consumption to determine the appropriate configuration for a given application.

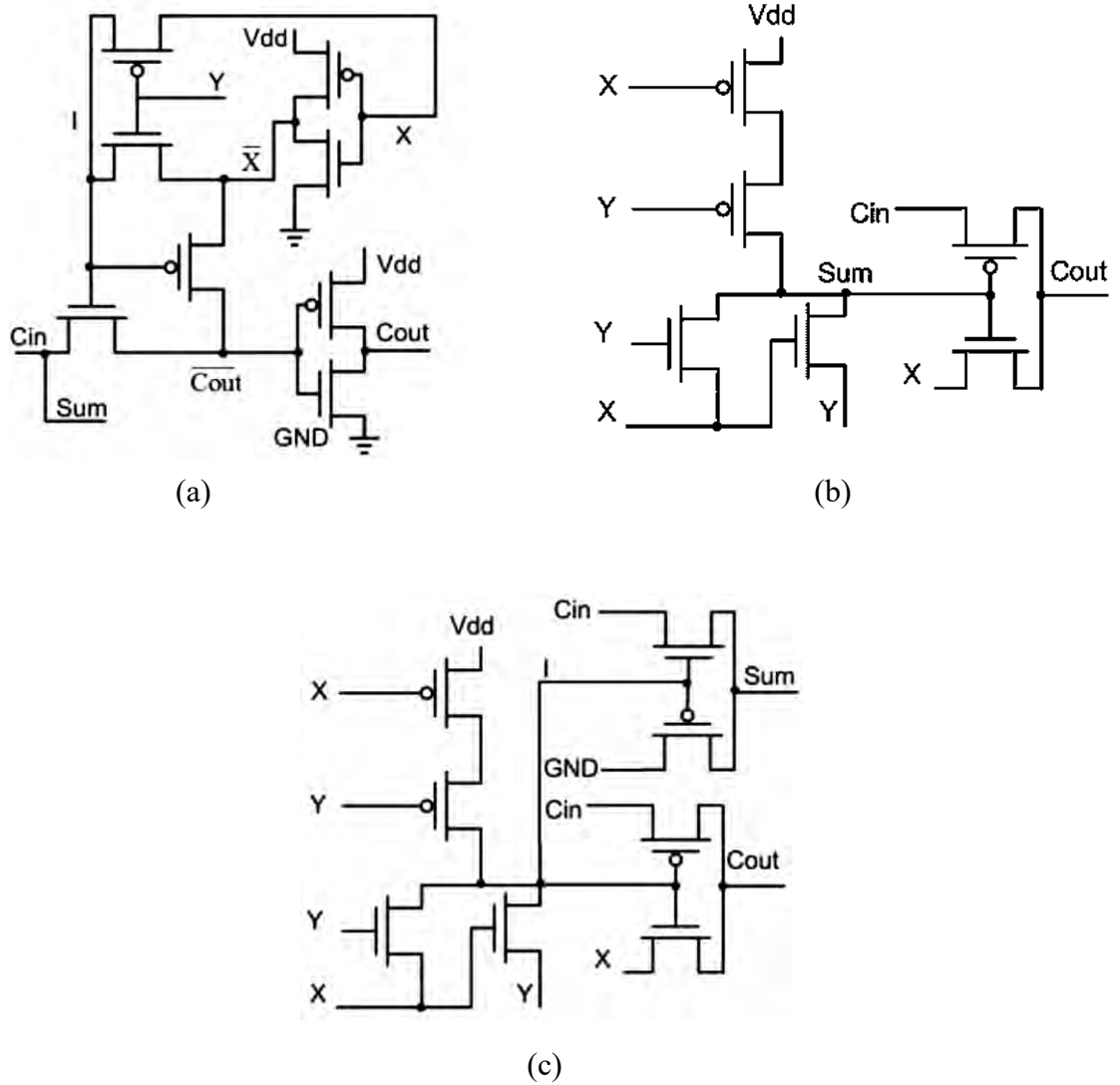


Figure 50: Schematic diagram of (a) AXA1 (b) AXA2 and (c) AXA3

4.4.2.1 Transient and DC Analysis (AXA1)

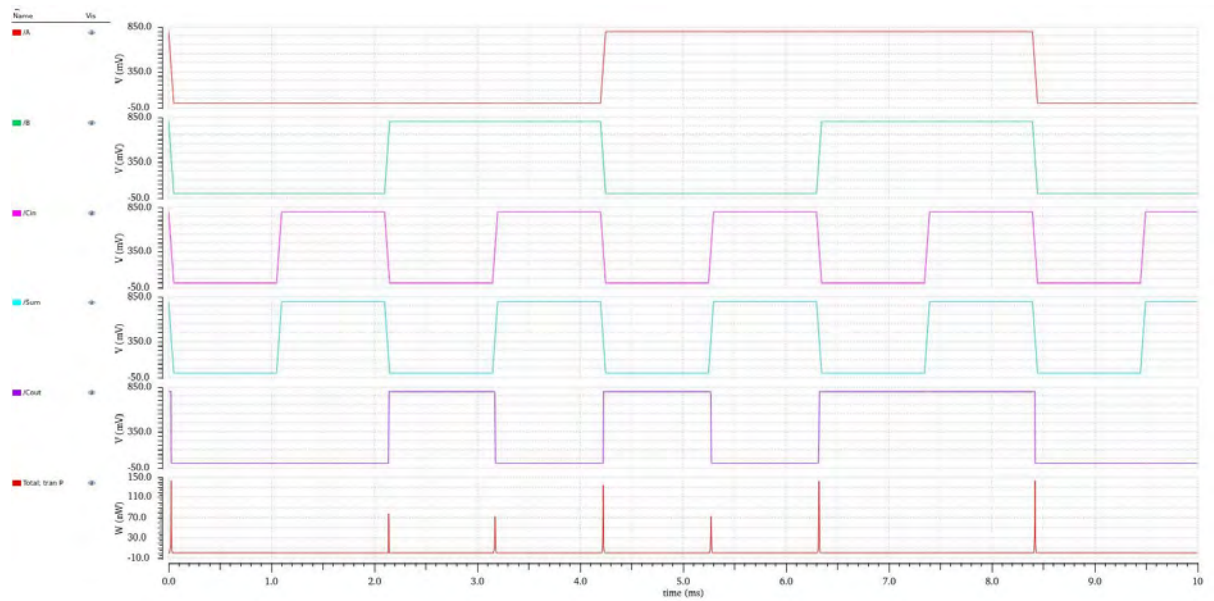


Figure 51: Transient analysis of AXA1

From the transient and DC analysis of AXA1, it is found that,

- Average transient power dissipation = 439.66 pW
- Delay of sum = 0 s
- Delay of carry = 14.7 μ s
- Average DC power dissipation = 104.84 pW

4.4.2.2 Bit Error Rate Analysis (AXA1)

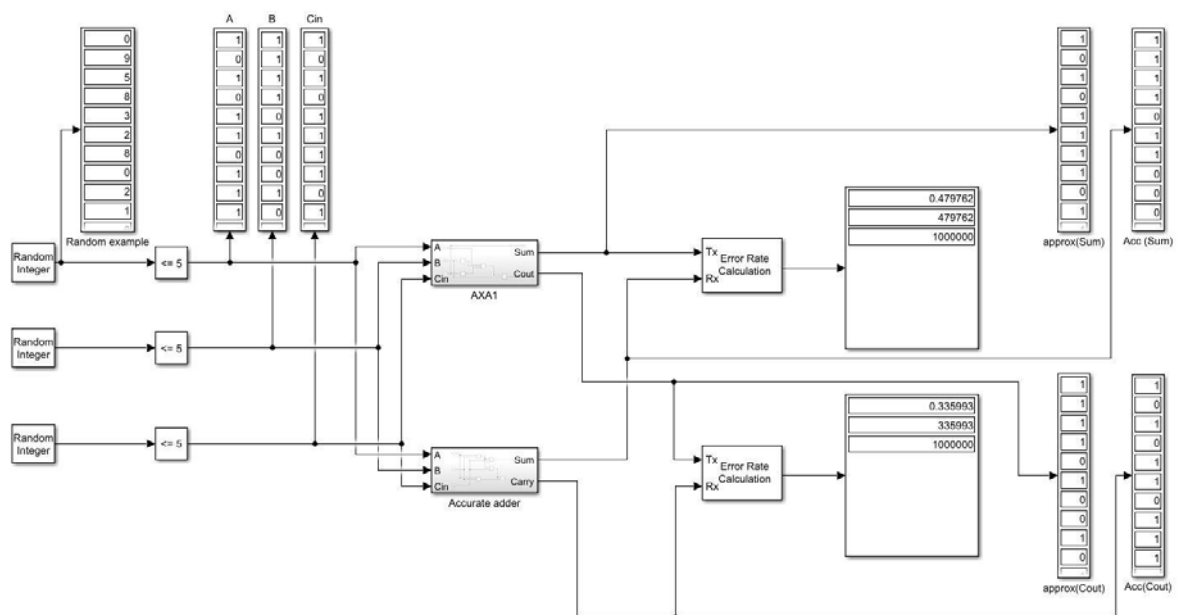


Figure 52: BER analysis of AXA1

- BER of sum = 47.97%
- BER of carry = 33.6%

4.4.2.3 Transient and DC analysis (AXA2)

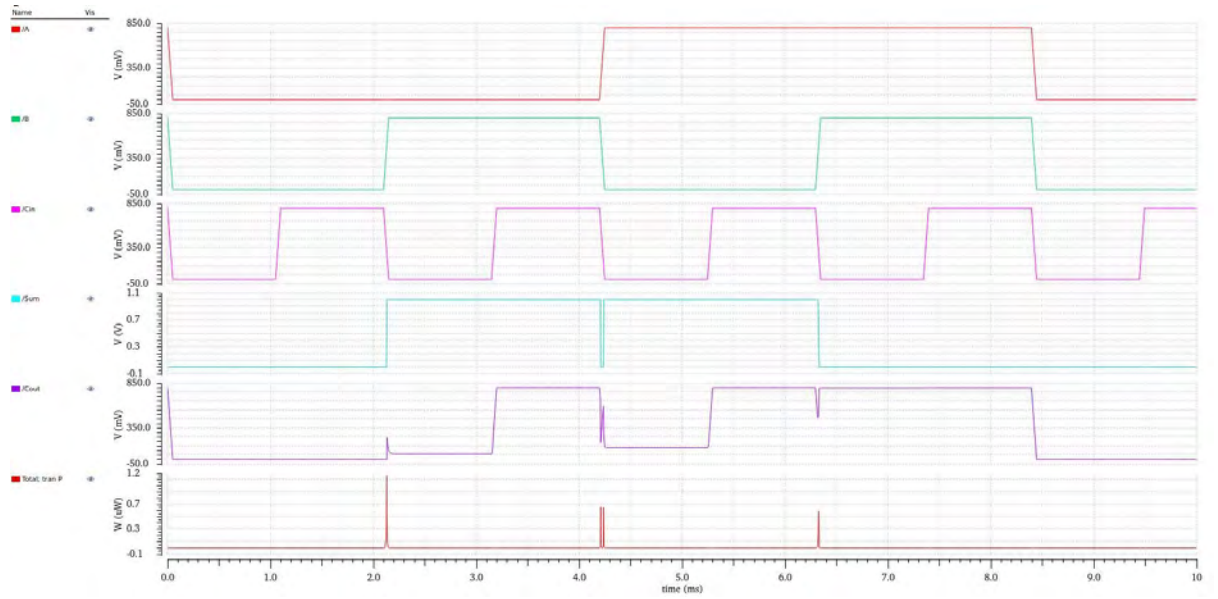


Figure 53: Transient analysis of AXA2

From the transient and DC analysis of AXA2, it is found that,

- Average transient power dissipation = 1.3815 nW
- Delay of sum = 13.08 μ s
- Delay of carry = 13.83 μ s
- Average DC power dissipation = 4.887 pW

4.4.2.4 Bit Error Rate Analysis (AXA2)

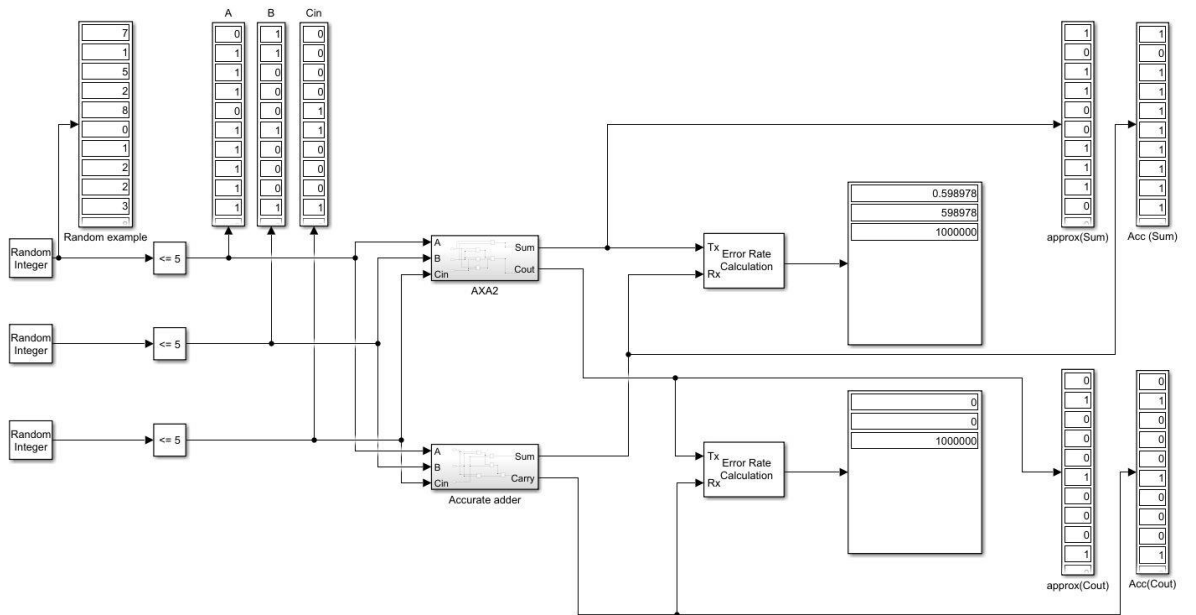


Figure 54: BER analysis of AXA2

- BER of sum = 59.9%

BER of carry = 0%

4.4.2.5 Transient and DC Analysis (AXA3)

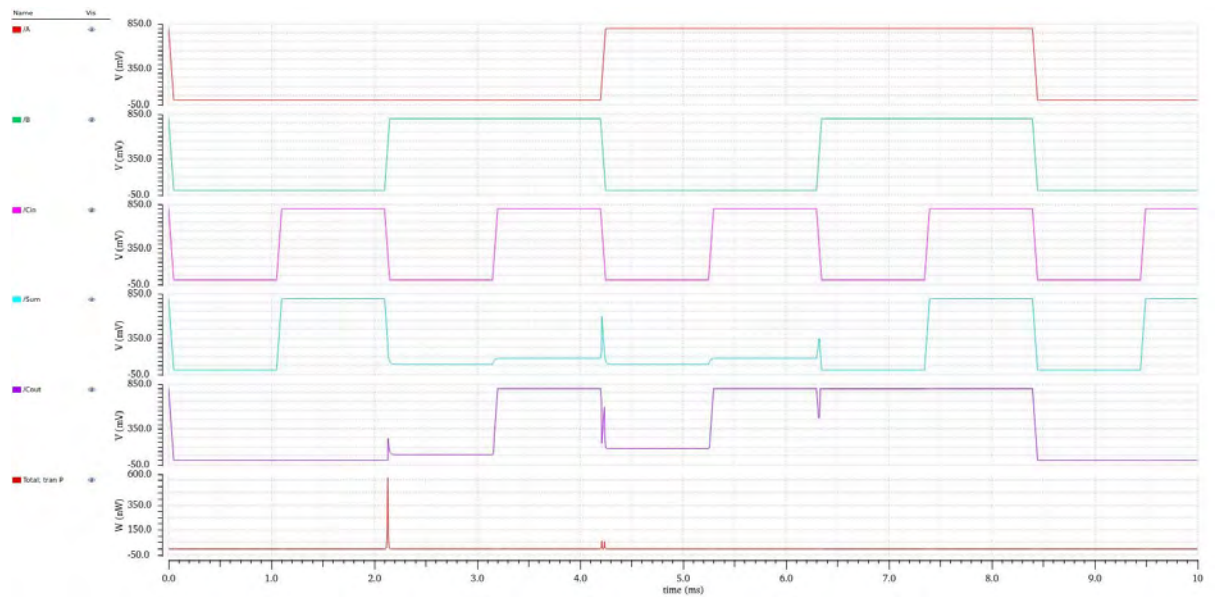


Figure 55: Transient analysis of AXA3

From the transient and DC analysis of AXA3, it is found that,

- Average transient power dissipation = 916.83 pW
- Delay of sum = 13.17 ps
- Delay of carry = 13.84 μ s
- Average DC power dissipation = 1.26 pW

4.4.2.6 Bit Error Rate Analysis (AXA3)

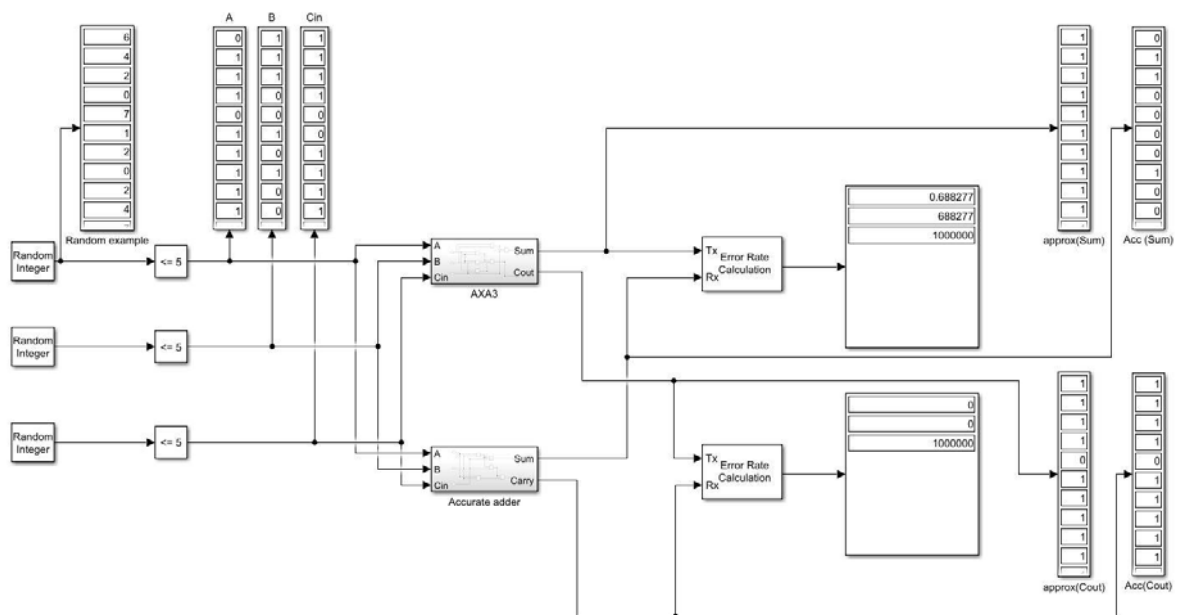


Figure 56: BER analysis of AXA3

- BER of sum = 68.83%

BER of carry = 0%

4.4.3 Transmission Gate-Based Approximate Adders (TGAs)

A transmission gate-based approximate adder is a circuit that uses transmission gates to perform approximate addition. It introduces errors or approximations to trade accuracy for computational efficiency. This can be done by reducing the number of full-adder stages or using approximate logic gates. It is suitable for applications where precision is not critical and can improve performance.

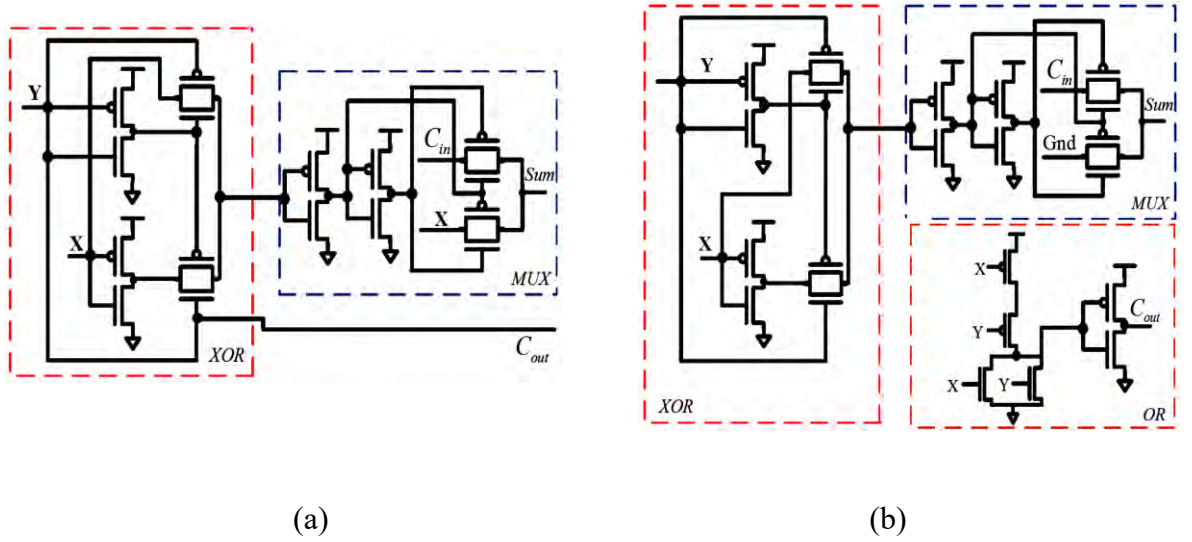


Figure 57: Schematic diagram of (a) TGA1 and (b) TGA2

4.4.3.1 Transient and DC Analysis (TGA1)

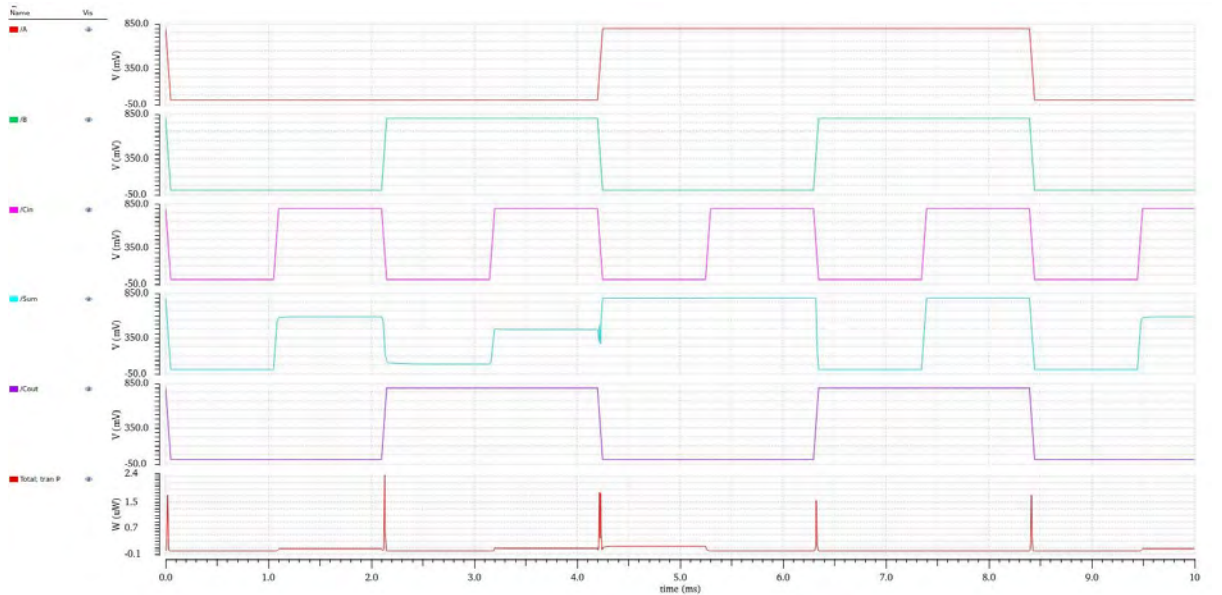


Figure 58: Transient Analysis of TGA1

From the transient and DC analysis of TGA1, it is found that,

- Average transient power dissipation = 38.897 nW
- Delay of sum = 1.719 ns
- Delay of carry = 0 s
- Average DC power dissipation = 1.719 nW

4.4.3.2 Bit Error Rate Analysis (TGA1)

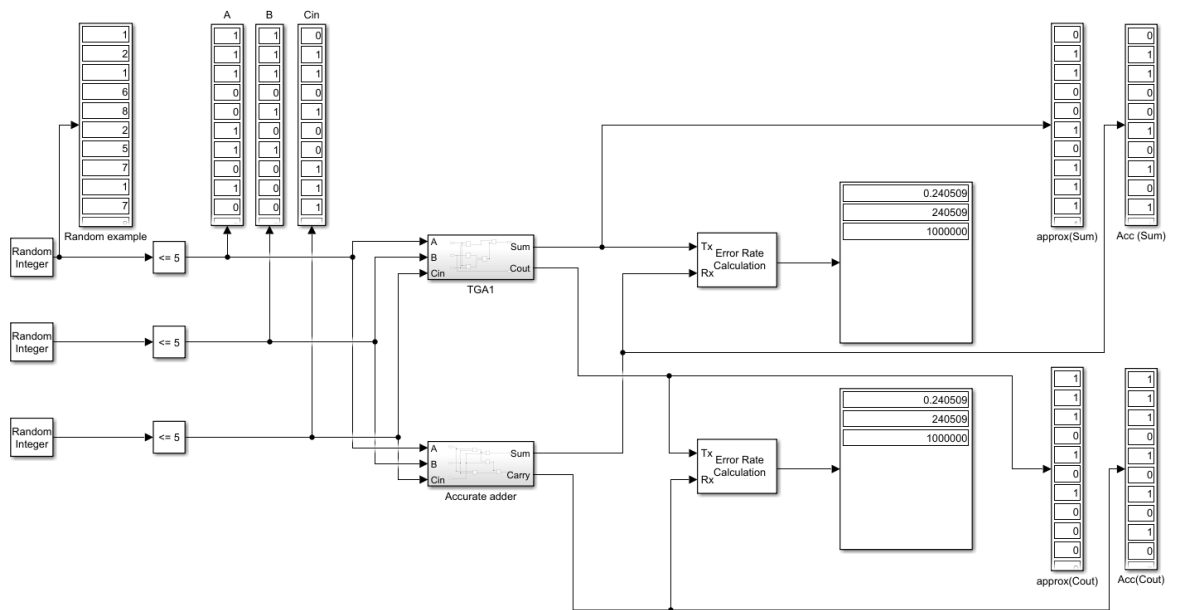


Figure 59: BER analysis of TGA1

- BER of sum = 24.05%
- BER of carry = 24.05%

4.4.3.3 Transient and DC Analysis (TGA2)

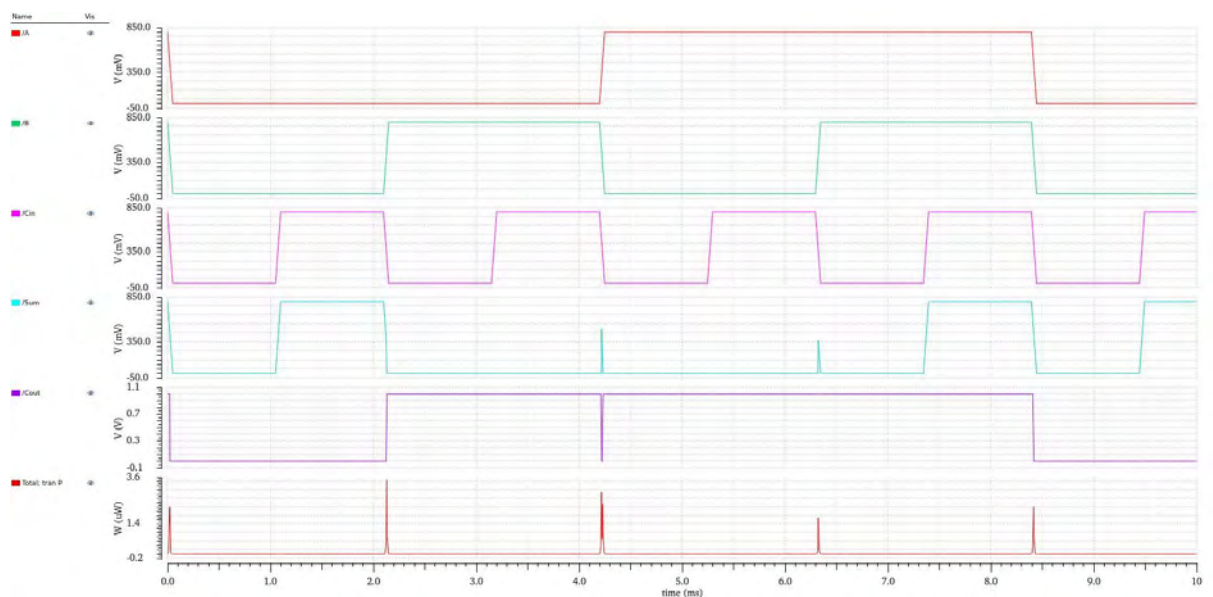


Figure 60: Transient analysis of TGA2

From the transient and DC analysis of TGA1, it is found that,

- Average transient power dissipation = 10.53 nW
- Delay of sum = 15 ps
- Delay of carry = 6.09 μ s
- Average DC power dissipation = 1.95 nW

4.4.3.4 Bit Error Rate Analysis (TGA2)

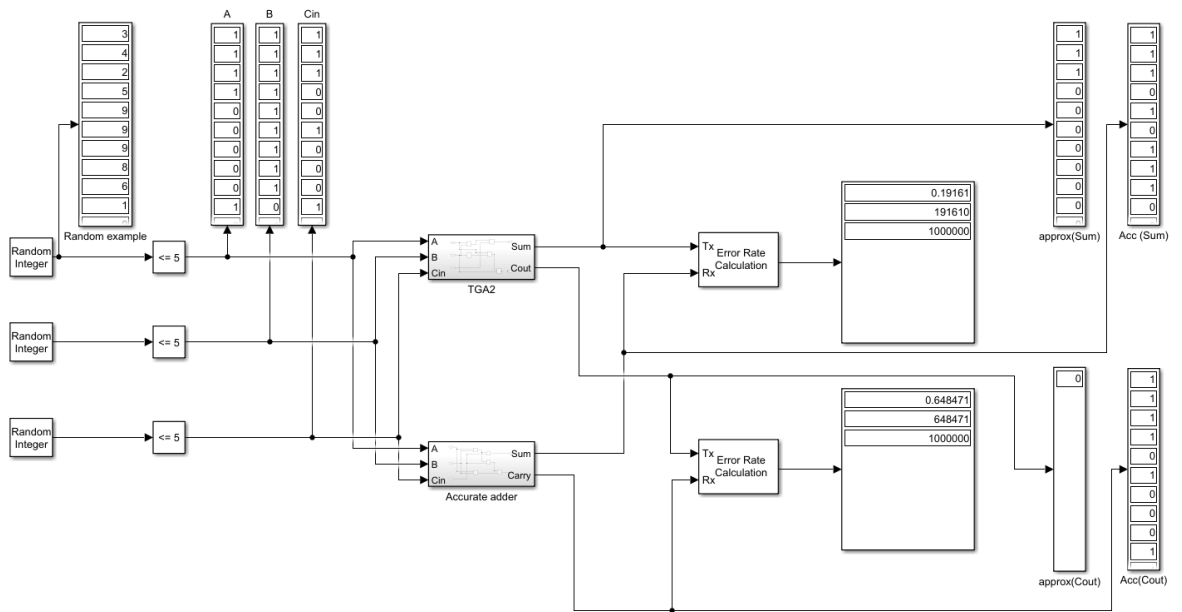
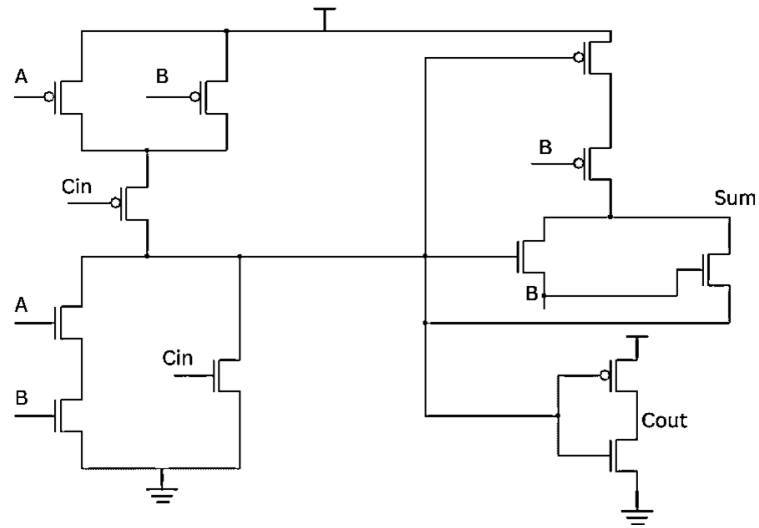


Figure 61: BER analysis of TGA2

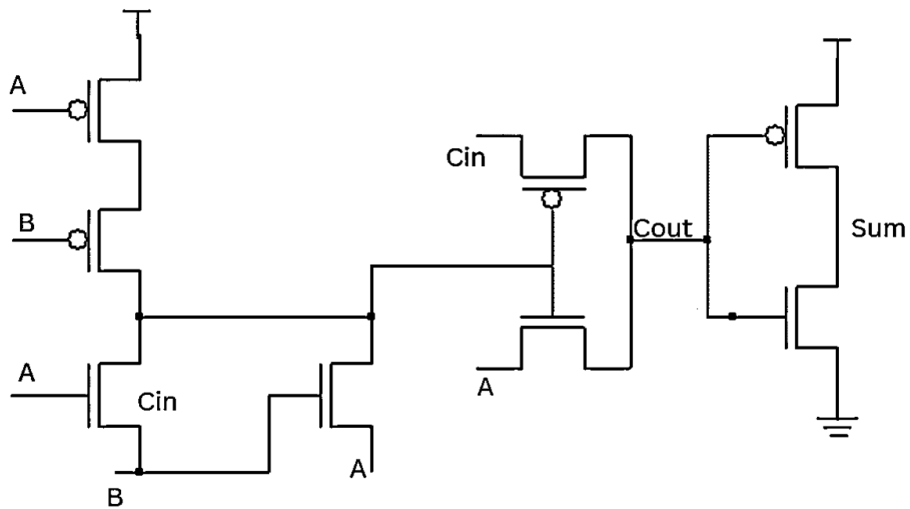
- BER of sum = 19.16%
- BER of carry = 64.84%

4.5 Proposed Approximate Adder

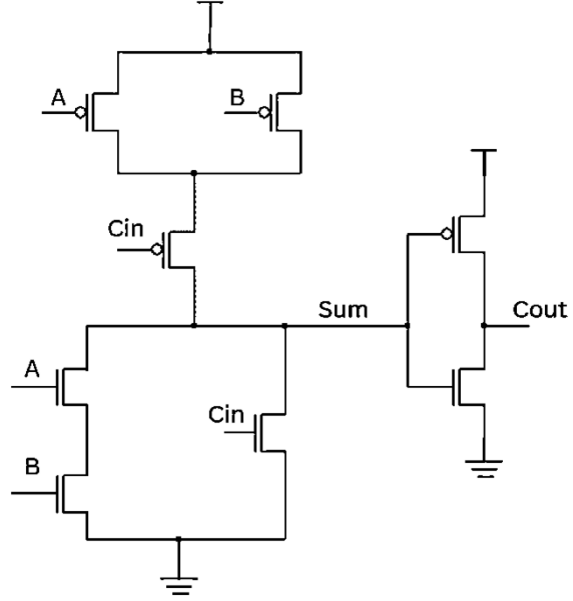
We have proposed four approximate adder designs that prioritise energy efficiency and reduced delay. These designs intentionally introduce controlled errors while ensuring the error rate remains within a safe range. The goal is to trade off accuracy for improved energy consumption and reduced delay. The designs modify the adder's building blocks, such as XOR and XNOR gates, and pass transistor operation to achieve these trade-offs. The proposal includes detailed descriptions, error analysis, energy consumption, delay characteristics, and comparative analytical analysis to support findings. In this study, we named that proposed adders as “Effective and Faster Approximate Adders” (EFAAs), as the schematic diagram of these shown in the figure below-



(a)



(b)



(d)

Figure 62: Proposed schematic diagram of (a) EFAA1 (b) EFAA2 (c) EFAA3

4.5.1 Transient and DC Analysis (EFAA1)

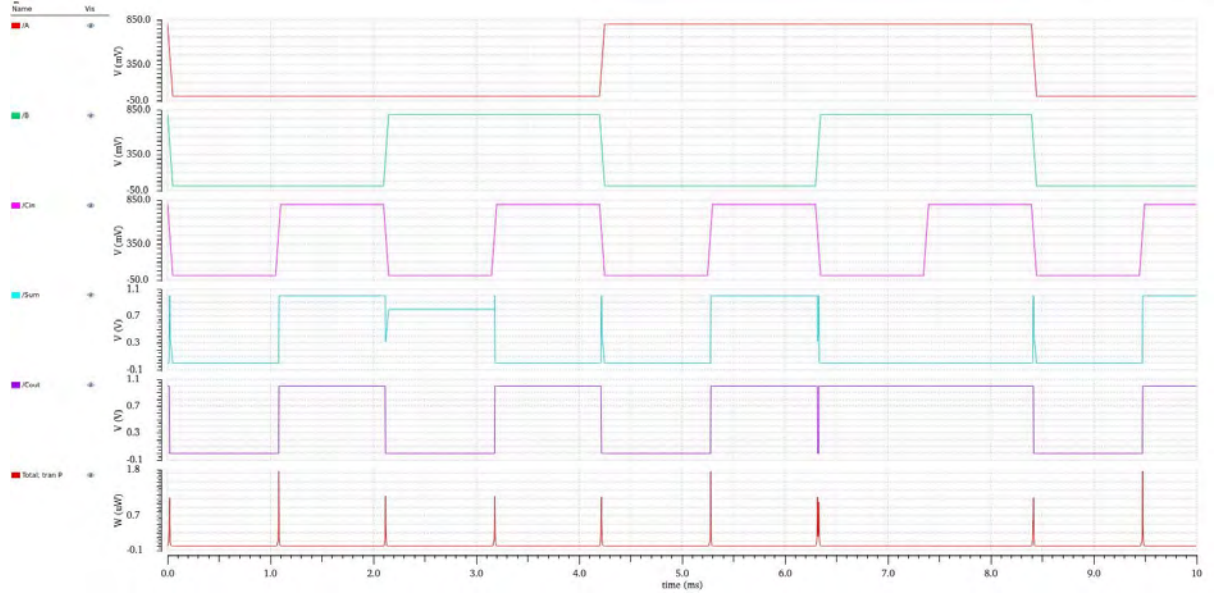


Figure 63: Transient analysis of EFAA1

From the transient and DC analysis of EFAA1, it is found that,

- Average transient power dissipation = 686.78 pW
- Delay of sum = 6.18 μ s
- Delay of carry = 6.16 μ s
- Average DC power dissipation = 187.42 pW

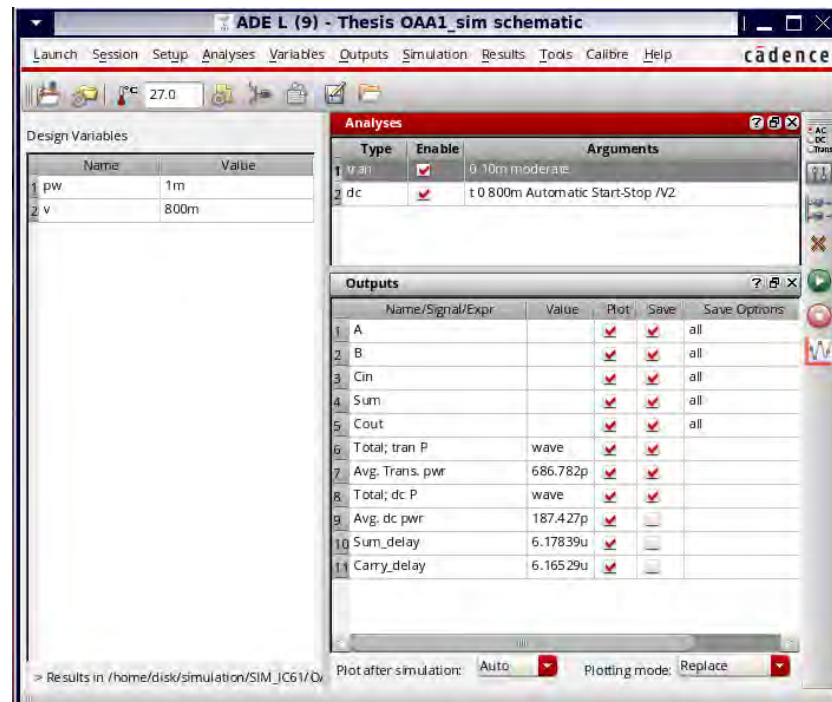


Figure 64: ADE analysis view of EFAA1

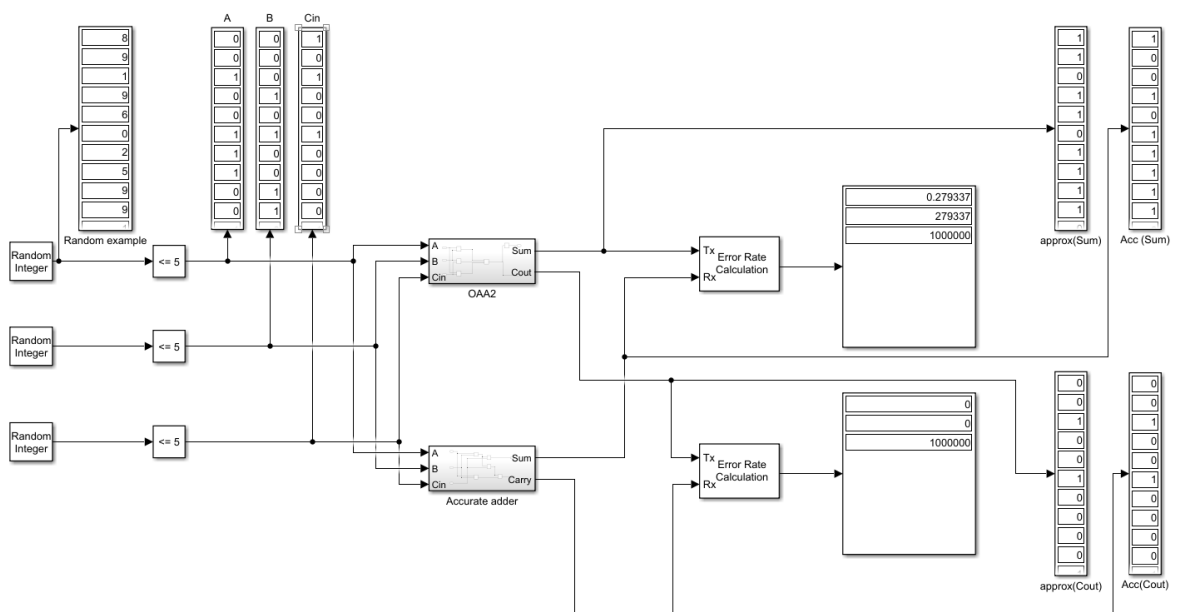


Figure 65: BER analysis of EFAA1

➤ BER of sum = 27.93%

BER of carry = 9.6%

4.5.2 Transient and DC Analysis (EFAA2)

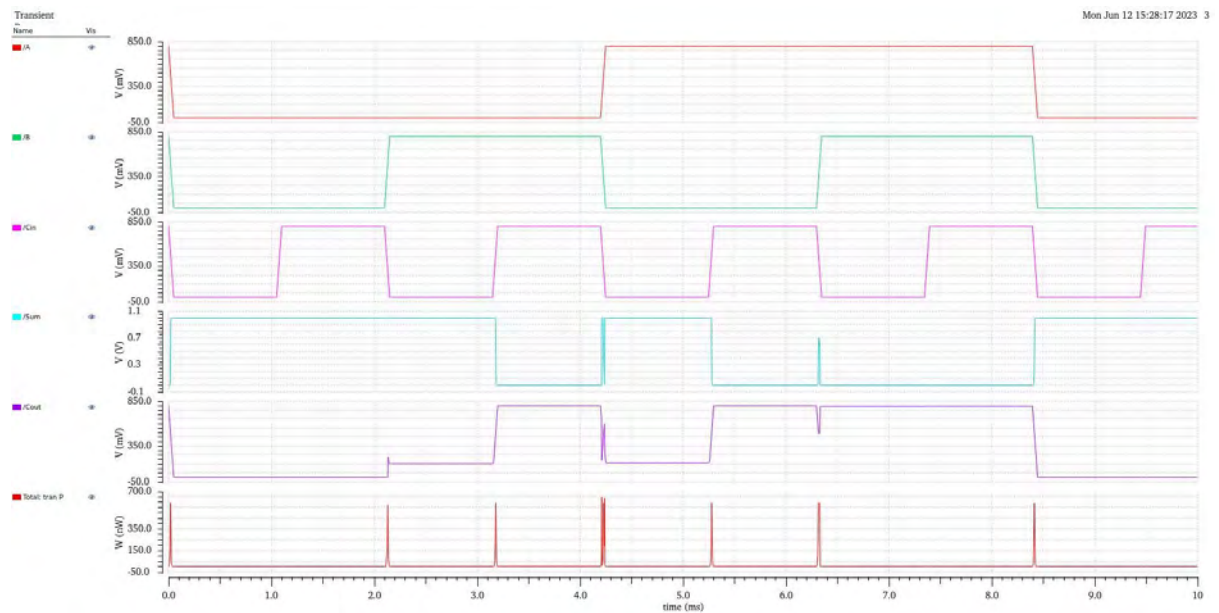


Figure 66: Transient analysis of EFAA2

From the transient and DC analysis of EFAA1, it is found that,

- Average transient power dissipation = 530.74 pW
- Delay of sum = 6.6 μ s
- Delay of carry = 925 ps
- Average DC power dissipation = 100.23 pW

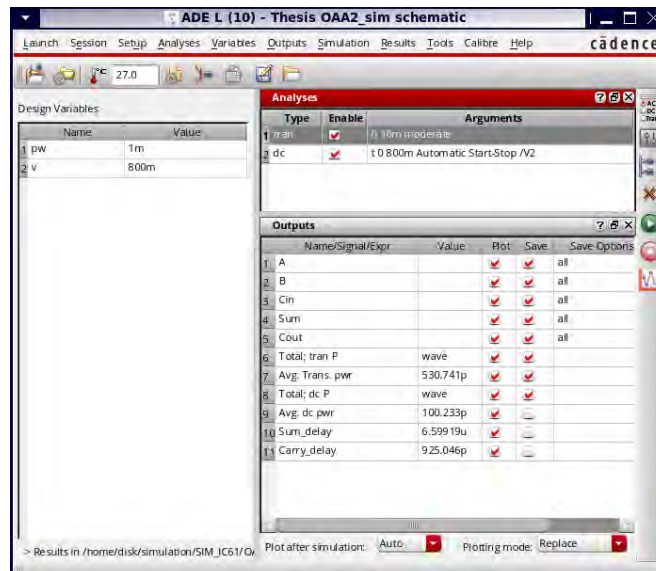


Figure 67: ADE analysis result of EFAA2

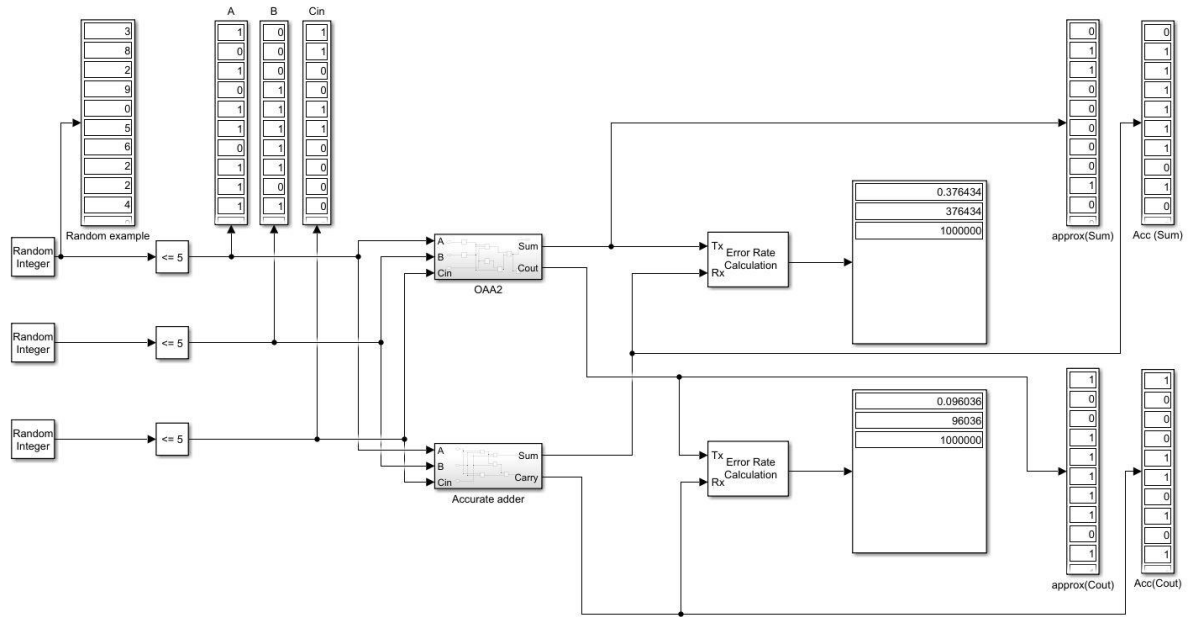


Figure 68: BER analysis of EFAA2

- BER of sum = 37.64%
- BER of carry = 0%

4.5.3 Transient and DC Analysis (EFAA3)

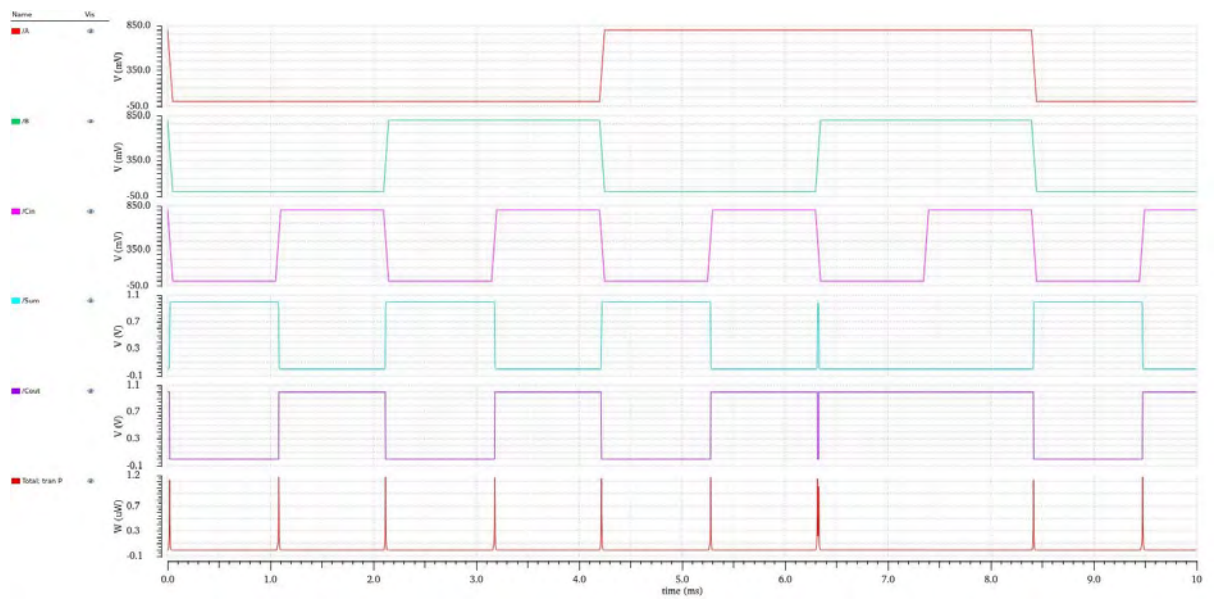


Figure 69: Transient analysis of EFAA3

From the transient and DC analysis of EFAA1, it is found that,

- Average transient power dissipation = 585.291 pW
- Delay of sum = 6.52 μ s
- Delay of carry = 6.16 μ s
- Average DC power dissipation = 102.038 pW

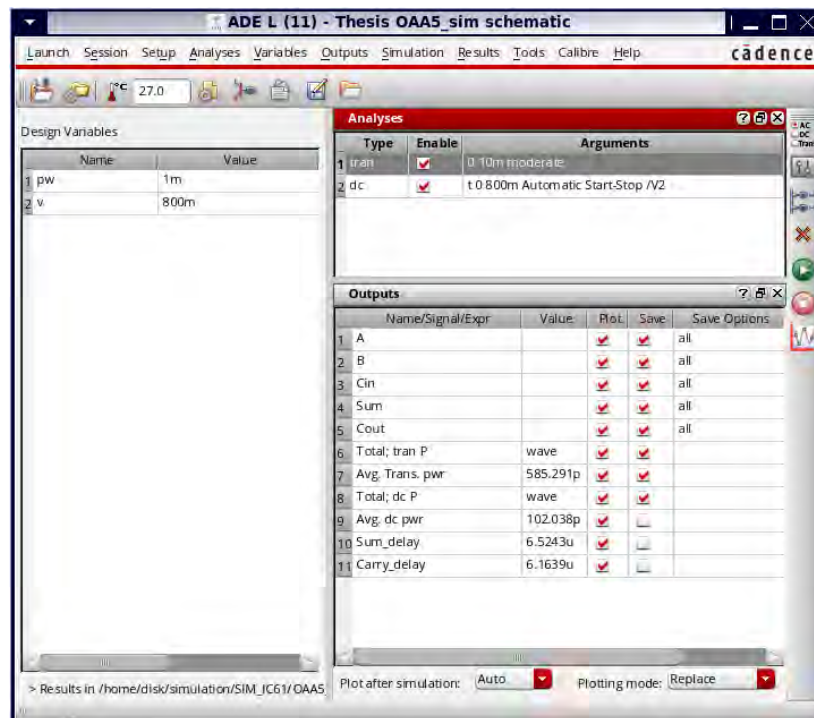


Figure 70: ADE analysis of EFAA3

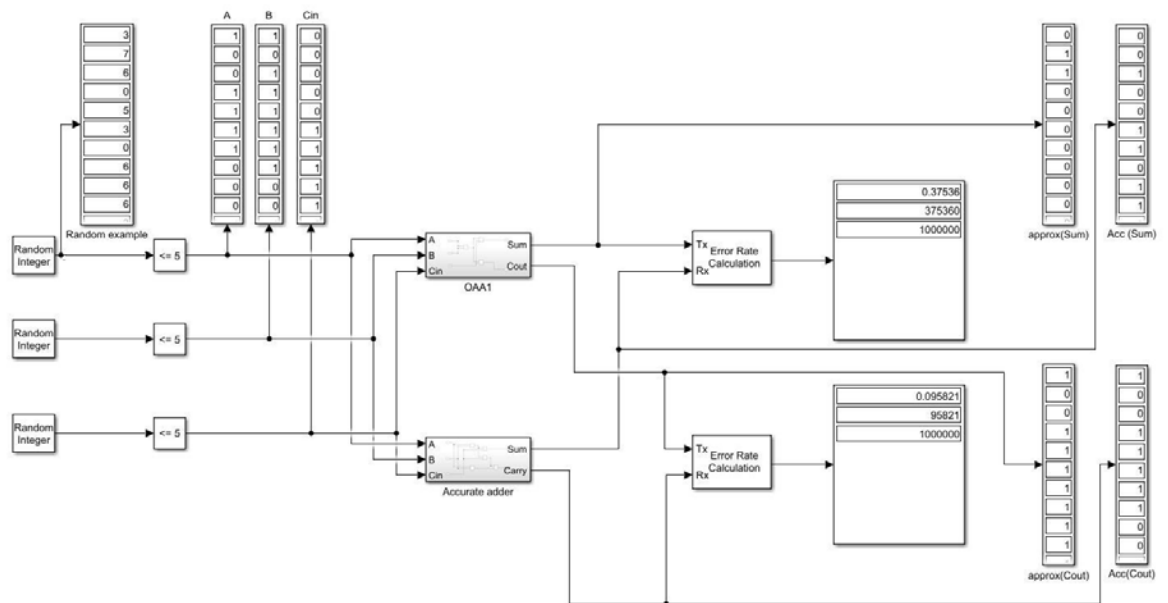


Figure 71: BER analysis of EFAA3

- BER of sum = 37.53% BER of carry = 9.58%

4.6 Results

The comparative analysis of the existing analogue approximate adders and our proposed approximate adders are shown in the table below-

Table 02: Power and delay comparison table

Name of approx. adder	Avg. dynamic power (pw)	Static power (pw)	Total power dissipation (pw)	Delay of sum (ns)	Delay of carry (ns)	Max delay (ns)	PDP $\times 10^{-15}$	EDP $\times 10^{-20}$
AMA1	698.85	11635.00	12333.85	171.20	1330.00	1330.00	16.40	2.18
AMA2	344.02	9.54	353.56	9.71	8.80	9.71	0.01	3.33
AMA3	355.92	8.37	364.29	1332.00	1331.00	1332.00	0.49	0.07
AXA1	439.66	104.84	544.50	0.00	14700.00	14700.00	8.00	11.80
AXA2	1381.50	4.89	1386.38	13080.00	13830.00	13830.00	19.20	26.50
AXA3	916.83	1.26	918.09	0.01	13840.00	13840.00	12.70	17.60
TGA1	38897.00	1719.00	40616.00	1.72	0.00	1.72	0.07	1.20
TGA2	10530.00	1950.00	12480.00	0.02	6090.00	6090.00	76.00	46.20
EFAA1	686.78	187.42	874.20	6180.00	6160.00	6180.00	5.40	3.34
EFAA2	530.74	100.23	630.97	6600.00	0.93	6600.00	4.16	2.75
EFAA3	585.29	102.04	687.33	6520.00	6160.00	6520.00	4.48	2.92

Table 03: Bit error rate comparison table

Name of approximate adder	BER of sum (%)	BER of carry (%)
AMA1	49.57	9.60
AMA2	28.06	0.00
AMA3	37.58	9.59
AXA1	47.97	33.60
AXA2	59.90	0.00
AXA3	68.83	0.00
TGA1	24.05	24.05
TGA2	19.16	64.84
EFAA1	21.65	9.60
EFAA2	37.64	0.00
EFAA3	37.53	9.58

Table-02 shows the power and delay comparison and also PDP & EDP. We see that AMA 2 and AMA 3 have less power dissipation than others, and the value is 353.564 pw & 364.29 pw. Our proposed EFAA have the average power consumption property compared to other approximate adders.

AMA2 and TGA1 show the lowest delay typically values of 9.71 ns and 1.72 ns compared to the remaining approximate adder, as shown in Figure (a). As a result, AMA2, AMA3 and TGA1 have the better value of PDP. As the carry propagation delay is always higher in ripple carry adder (RCA) circuits, our proposed adders will provide significant output results in applying field in RCA models. Our proposed EFAAs gained averagely a better PDP and EDP compared to other existing adders.

Finally, Table-03 shows the bit error rate (BER) for various existing and proposed approximate adders. Although AMA1, AMA2 and TGA1 had good outcome with respect to the PDP, but, considering the BER analysis, AMA3 and TGA1 has mildly higher error than others. On the other hand, EFAAs has lower BER of sum and significantly less BER of carry bits.

Considering power dissipation, delay, PDP and BER comparison, we can say that, alongside the AMA2, our proposed EFAAs have provided significantly better results compared to other existing approximate adders.

Chapter 5

Conclusion

5.1 Summary

The thesis focuses on designing and analysing approximate adders that sacrifice precision for improved performance, power efficiency, or more minor size requirements. The objective is to achieve near-approximations of the sum while minimising the complexity and resources needed for the addition operation.

The thesis explores various strategies in approximate adder designs, including bit skipping, probabilistic computing, and error-tolerant logic. These techniques selectively skip or approximate specific bits of the operands or carry chain, use statistical characteristics to deliver approximations with less effort and introduce controlled errors in the addition process. The advantages of approximate adders over traditional accurate adders are faster performance and lower power consumption. They are suitable for applications where precise results are not critical, such as low-power devices, audio and image processing, machine learning, and error-tolerant computers.

The main work of the thesis focuses on designing and analysing existing analogue circuit-based approximate adders. The circuits are implemented in 45nm technology using Cadence software. Cadence Virtuoso, a widely used electronic design automation (EDA) tool, is employed for schematic capture, simulation, layout, and verification. The analysis includes delay and power dissipation analysis using Cadence Spectre and bit error rate analysis using MATLAB.

The findings of this thesis provide that AMA 2 and AMA 3 have the most negligible power dissipation, and the value is 353.564 pW & 364.29 pW. Our proposed EFAs have the average power consumption property compared to another approximate adder. The total power consumption of EFAs1, EFAs2, and EFAs3 is respectively 874.2 pW, 630.97 pW, 687.329 pW, and all of them have delays around 6 μ s to 6.6 μ s.

Above all, we can say that our proposed EFAs have the average property compared to the existing approximate adder.

5.2 Future Scope

The future scope of the thesis work on approximate adders includes the following possibilities:

- Applying nano-technology: Applying more nano-technology to design must improve the efficiency and performance of approximate adders.
- Material improvement: Changing the MOSFET material or the material's structure can improve the outcome. In that case, GAAFET, CNFET, etc., can be used.
- Integration of approximate adders with advanced technologies: Exploring the integration of approximate adders with emerging technologies like machine learning, neuromorphic computing, or quantum computing can leverage a new dimension in this work.

Overall, the future scope of the thesis work on approximate adders lies in further refining the designs, exploring new techniques, evaluating their performance in different applications, integrating with advanced technologies, hardware implementation, comparative analysis, and exploring hybrid approaches to achieve optimal trade-offs between accuracy, performance, and power efficiency.

5.3 Thesis Management

The key administrative component that records the progress of the thesis and its assessment is the Thesis Management component.

5.3.1 Work Plan in RACI Chart

A RACI chart, also known as a RACI matrix or responsibility assignment matrix, is a visual tool that clarifies roles and responsibilities within a project or organisation. The acronym RACI stands for Responsible, Accountable, Consulted, and Informed, which represents the different levels of involvement for individuals or roles in completing tasks or making decisions.

Table 04: RACI chart for thesis management

Task	Thesis Supervisor	Students		
		Khaled Hasan ID: 172008	Fajla Rabby ID: 172084	MD. Atiqur Rahman ID: 172087
Topic Selection	C, I	R	R	R
Developing Framework	C, I	R, A	R, A	R, A
Circuit Design	C, I	R, A	R, A	R, A
Simulation Framework	C, I	R, A	R, A	R, A
Data/ Report	C, I	R, A	R, A	R, A
Thesis Report Paper	C, I	R, A	R, A	R, A
Presentation Slide	C, I	R, A	R, A	R, A

Table 05: Individual and teamwork list

Team Work Task	Khaled Hasan ID: 172008	Fajla Rabby ID: 172084	MD. Atiqur Rahman ID: 172087
Research / Literature Review	√	√	√
Circuit Design / Selection	√	√	√
Simulation	√	√	√
Data Analysis	√	√	√
Presentation slide Preparation	√	√	√
Report Writing	√	√	√

5.4 SDG Goal Alignment with the Thesis

The Sustainable Development Goals (SDGs) are a set of 17 interconnected goals established by the United Nations (UN) in 2015. They provide a blueprint for achieving a better and more sustainable future for all by 2030. The SDGs address the world's various social, economic, and environmental challenges and aim to promote peace, prosperity, and well-being while safeguarding the planet.



Figure 72: SDG goals provided by the UN

The thesis work on the design and analysis of approximate adders aligns with several Sustainable Development Goals (SDGs) in the following ways:

SDG 7: Affordable and Clean Energy: By focusing on energy-efficient designs, the thesis contributes to the goal of promoting clean and sustainable energy solutions. The use of approximate adders can reduce power consumption, making them suitable for low-power devices and applications.

SDG 9: Industry, Innovation, and Infrastructure: The thesis explores innovative strategies and techniques in designing approximate adders, contributing to advancements in digital circuit design and promoting innovation in computer engineering.

SDG 13: Climate Action: Approximate adders can help reduce energy consumption and carbon emissions by improving power efficiency in digital circuits. It aligns to mitigate climate change and promote sustainable practices.

SDG 4: Quality Education: The thesis contributes to computer engineering education by providing valuable insights into the design and analysis of approximate adders. This knowledge can enhance curriculum development and promote quality education in this area.

SDG 16: Peace, Justice, and Strong Institutions: While not directly related, the research and analysis conducted in the thesis contribute to building solid institutions by promoting advancements in digital circuit design and fostering a culture of research and innovation.

It is important to note that the alignment of the thesis with the SDGs is indirect, as the thesis focuses on technical aspects rather than directly addressing societal or environmental challenges. However, the research outcomes have the potential to contribute to broader sustainability efforts by improving energy efficiency and promoting innovation in digital circuit design.

5.5 Conclusion

The thesis focuses on designing and analyzing approximate adders that trade precision for improved performance, power efficiency, or reduced size requirements. Various strategies for approximate adder designs, such as bit skipping, probabilistic computing, and error-tolerant logic, are explored. These techniques selectively skip or approximate specific bits of the operands or carry chain to achieve faster performance and lower power consumption.

The main work of the thesis involves designing and analyzing existing analog circuit-based approximate adders using Cadence software. Transient, DC, and bit error rate analyses are conducted to evaluate the performance characteristics of the adders.

Comparative analysis of the existing analog approximate adders and the proposed approximate adders is presented in the tables provided. Power and delay comparison, as well as bit error rate (BER) analysis, are used to assess the performance of the adders.

The proposed EFAAs (Effective and Fast Approximate Adders) show average power consumption compared to the other approximate adders. AMA2 and TGA1 exhibit the lowest delay values. EFAA1 and TGA2 demonstrate the lowest BER for the sum.

Overall, the thesis provides insights into the design, analysis, and trade-offs involved in approximate adders. The proposed EFAA adders offer a balance between power consumption, delay, and bit error rate compared to the existing approximate adders.

These findings are valuable for improving performance and power efficiency in applications where precise results are not critical, such as low-power devices, audio and image processing, machine learning, and error-tolerant computers.

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