A three-way Wilkinson power divider at center frequency 2.4 GHz

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This project report is submitted to professor Islam A. Eshrah as a part of [ELC2090] microwaves course.

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I-Introduction

Microwave frequencies have become an essential part of modern communication systems; they are used in everything from phones to satellite communications, moreover, they are used in medical applications, industrial applications and military applications, microwave engineering is a field that involves the study and applications of electromagnetic waves at high frequencies that typically range from 1 GHz to 100 GHz and their corresponding wave length ranges from 0.3 m to 3 mm [1].

In many of the microwaves applications we need to divide the power among multiple devices, and here comes the role of one of the most important passive components in microwaves engineering the "Power Divider". The earliest transmission line power dividers created were just a simple T-junction splitting the input port but this design suffered from very poor isolation between the output ports. Until in 1960, Ernest J. Wilkinson designed the Wilkinson power divider that can split power equally between the output ports as well as maintaining isolation between them and also maintaining matched condition on all ports. The Wilkinson design can also be used as a power combiner under the condition that the 2 input waves to be combined have the same phase [2].

In this project, we will be designing a three-way equal power splitter at frequency 2.4 GHz (for a Wi-Fi application), to achieve acceptable input and output ports matching, isolation between ports and equal power division ratio, in this report's next section we will show different design methodologies, then the proposed design section will contain the implementation of the circuit using ideal transmission lines, Advanced Design System (ADS) will be used for simulating the proposed circuit schematic, next we will implement the proposed design using micro-strip technology and create a layout for the proposed design to be fabricated. In the results section ideal and micro-strip circuit simulations results will be provided and discussed as well as an Electro-Magnetic simulation results. Results of all simulations will be discussed to evaluate the design based on its input and output return loss, isolation between output ports, insertion loss and bandwidth.

II-Types of design

A- 3-way Wilkinson splitters using delta star configuration

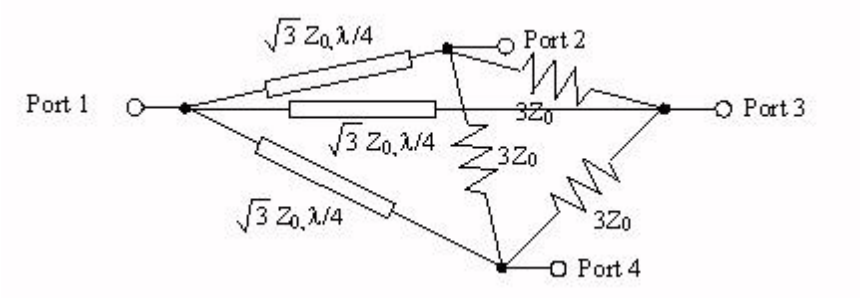


Fig. 1: *3-way Wilkinson power divider with isolation resistors in delta configuration [3].*

The design of a three-way Wilkinson power divider is usually done by adding 3 quarter waves (λ/4) transmission lines in parallel and their characteristic impedance is $\sqrt{3}Z_0$, as shown in Fig.1 the isolation resistors are connected in a delta configuration with a value of $3Z_0$, however, this delta configuration can also be converted to a star configuration [3].

The problem with this design is creating the layout of the circuit to be implemented using micro-strip technology, the third isolation resistor connecting between ports 2 and 4 cannot be realized and has to be removed when creating the layout, and thus the rest of the circuit has to be optimized to get the best results using only 2 isolation resistors.

B- Three-way splitter based on unequal Wilkinson

Another idea for implementing the 3-way Wilkinson power divider is by using a 2-way Wilkinson power divider and splitting the power among its 2 ports unequally such that port 2 gets 2/3 of the power and port 3 gets 1/3 of the power as shown in Fig.2, the values for the transmission lines characteristic impedances are Z_{0A} = 51.5 ohms, Z_{0B} = 103 ohms, Z_{0C} =42.1 ohms, Z_{0D} = 59.5 ohms and the resistor R_W is equal to 106.1 ohms, then adding another Wilkinson at port 2 to divide the two thirds of the power equally into 1/3 over each port this makes the first Wilkinson non-symmetric but the second one is symmetric [4].

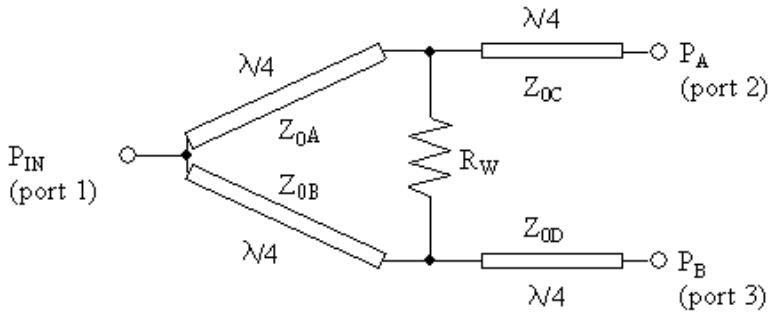


Fig. 2: *2-Way unequal Wilkinson power divider [4].*

III- Proposed Design

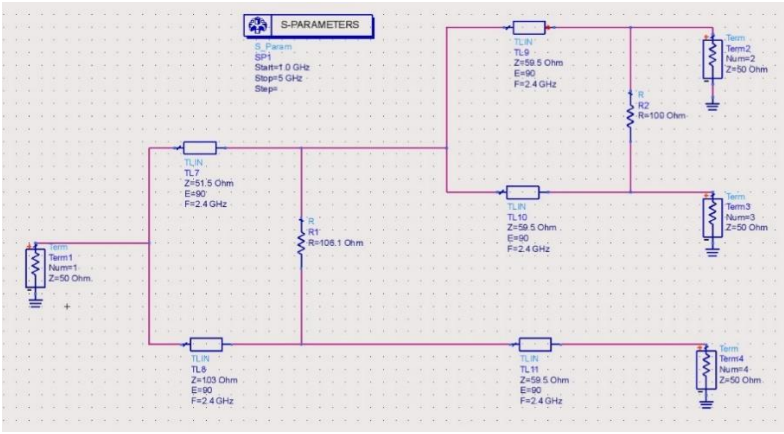


Fig. 3: *3-way Wilkinson power divider circuit schematic using ideal TLs at 2.4 GHz.*

The Advanced Design System (ADS) is used for the design and simulation of the power divider. The proposed design is a 4-port Wilkinson power divider circuit, three ports for output and one input port. Circuit's schematic view is in Fig.3 where port 1 is the input port and ports 2, 3 and 4 are the output ports. The input power is divided among the first 2 branches unequally so that the first branch gets two thirds of the power and the second branch gets one third of the power which is sent to port 4 and then another Wilkinson is added at the first branch to divide the two thirds of the power equally on port 2 and port 3. First step is to simulate using ideal transmission lines and next is to implement the circuit using micro-strip technology using the FR4 substrate with the following parameters and copper thickness 35 um.

FR4 substrate parameters

Dielectric constant $\varepsilon_r = 4.58$

Height = 0.8mm

Loss Tangent = 0.022

First we tested a 50-ohms transmission line of length 1 cm to determine the loss per cm due to the used substrate and it turns out there is a loss of 0.1 dB per cm as shown in fig.4 at design frequency and the used substrate data sheet is shown in fig.5.

With the line calculator tool in ADS shown in fig.6, we were able to calculate the length and width of each transmission line to get the required characteristic impedance at design frequency as shown in table 1, and the circuit schematic is shown in fig.7, then we created the layout for the proposed design but we did not generate the layout from the schematic directly as the circuit is not symmetric so generating the layout is not straight forward we created the layout shown in Fig.8 from scratch to match the acquired lengths and widths and we defined differential ports at resistors terminals to be able to run the EM simulation.

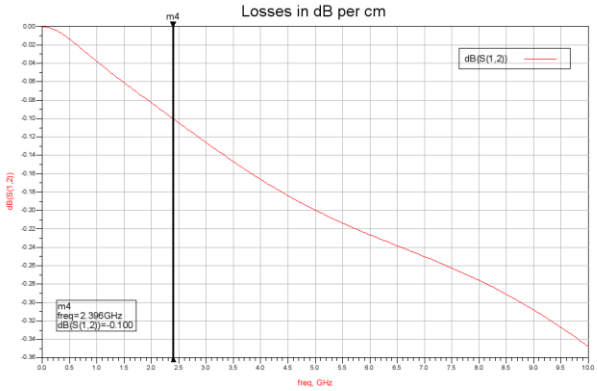


Fig. 4: *loss in dB per cm*

Table 1: *Transmission lines length and width at design frequency (2.4 GHz) and required characteristic impedance.*

Characteristic Impedance	Length	Width
51.5 ohms	17036.500000 um	1385.500000 um
103 ohms	18111.700000 um	274.631000 um
59.5 ohms	17248.700000 um	1063.690000 um

KB

产 品 技 术 资 料

TECHNICAL INFORMATION

KB-6160（ANSI：FR-4.0）

Thin Core Laminate for Multilayer Board 多层电路板用薄内层板材

General Properties 一般特性

Test Item 测试项目	Unit 单位	Test Method (IPC-TM-650) 测试方法	Test Condition 处理条件	Specification (IPC-4101D) 规格值	Typical Value 典型值
Peel Strength (1 oz.) 铜箔剥离强度	N/mm	2.4.8	125℃	≥0.70	1.62
			Float 288℃/ 10 Sec	≥1.05	1.65
Thermal Stress 热应力	Sec	2.4.13.1	Float 288℃/ unetched	≥10	180
Bow / Twist 弯弓度/翘曲度	%	2.4.22.1	A	≤ 1.0	0.17 / 0.18
Flammability 燃烧性	Rating	UL94	UL94	UL94V-0	V-0
Glass Transition (Tg) 玻璃化转变温度	℃	2.4.25	E-2/150 （DSC）	≥130	136
Surface Resistivity 表面电阻	MΩ	2.5.17.1	C-96/35/90	$\geq 1.0\times10^{4}$	1.0×10^{6}
Volume Resistivity 体积电阻	MΩ-cm	2.5.17.1	C-96/35/90	$\geq 1.0\times10^{6}$	1.0×10^{8}
Dielectric Constant 介电常数	—	2.5.5.2	Etched/@1 MHZ	≤5.4	4.58
Loss Tangent 介质损耗	—	2.5.5.2	Etched/@1 MHZ	≤0.035	0.022
Arc Resistance 耐电弧性	Sec	2.5.1	D-48/50+D-0.5/23	≥60	125
Moisture Absorption 吸水率	%	2.6.2.1	D-24/23	≤0.80	0.23
Comparative Tracking Index 相比漏电起痕指数	V	IEC 60112	Etched/0.1% NH_4Cl	AABUS	175
TD	℃	2.4.24.6	TGA	——	305
Dimensional Stability 尺寸稳定性	ppm	3.9.1.2	Warp	±300	-210
			Fill		-180

Remarks: Specimen Thickness:0.51mm 1/1 样品厚度：0.51mm 1/1 (不含铜厚)

A = Keep the specimen originally without any process 保持原样,不作处理

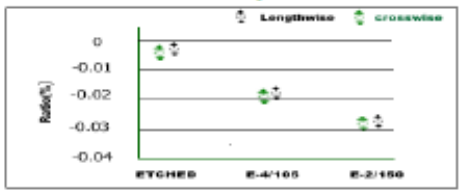
C = Temperature and humidity conditioning 恒温恒湿空气中处理

D = Immersing in distilled water with temperature control. 恒温水中处理

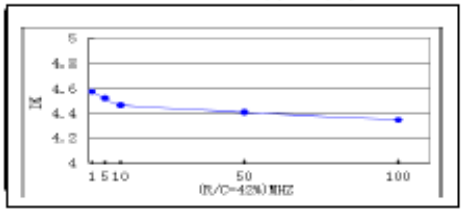
E = Temperature conditioning 恒温空气中处理

Speciality Chart 板材特性图

Dimensional stability 尺寸稳定性



Dielectric constant 介电常数



Purchasing Information 采购信息

Base Color 基板颜色	Thickness 厚度	Copper Cladding 铜箔厚度	Regular Size（mm）常规尺寸
黄色 Yellow	0.05mm ~ 1.2mm	12μm, 18μm, 35μm, 70μm 105μm	940*1245mm （37" * 49"） 1042*1245mm （41" * 49"） 1093*1245mm （43" * 49"）

Note: 1) Other sheet size and thickness could be available upon request.

Fig. 5: *Substrate datasheet.*

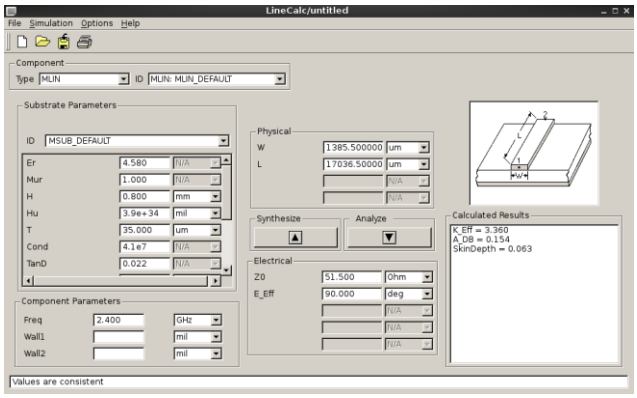


Fig. 6: *Line calculator tool calculating length and width for the TL with Z_O 51.5 ohms.*

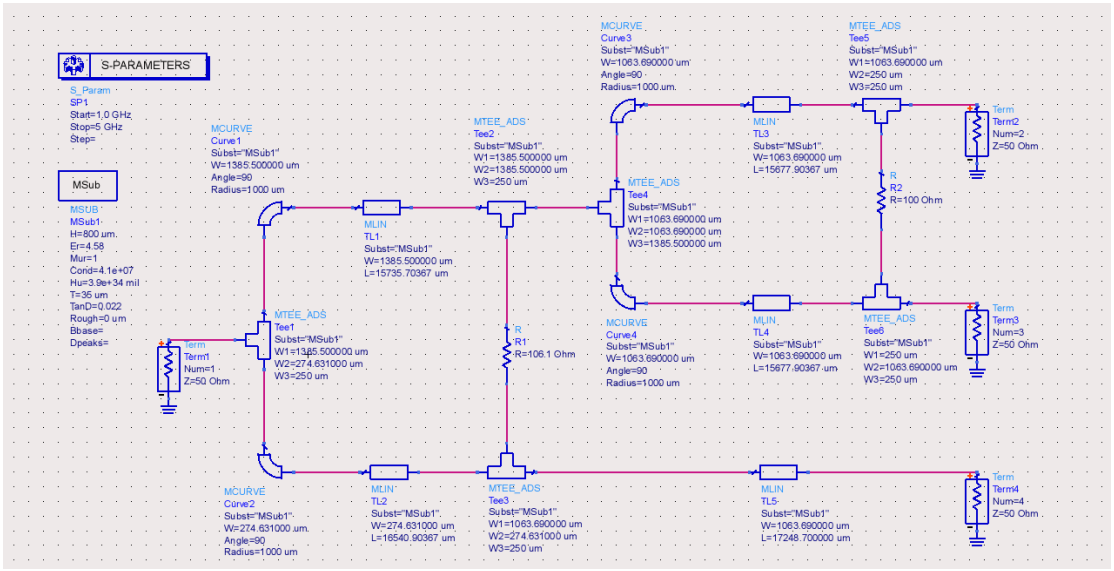


Fig. 7: *Circuit Schematic using micro-strip technology.*

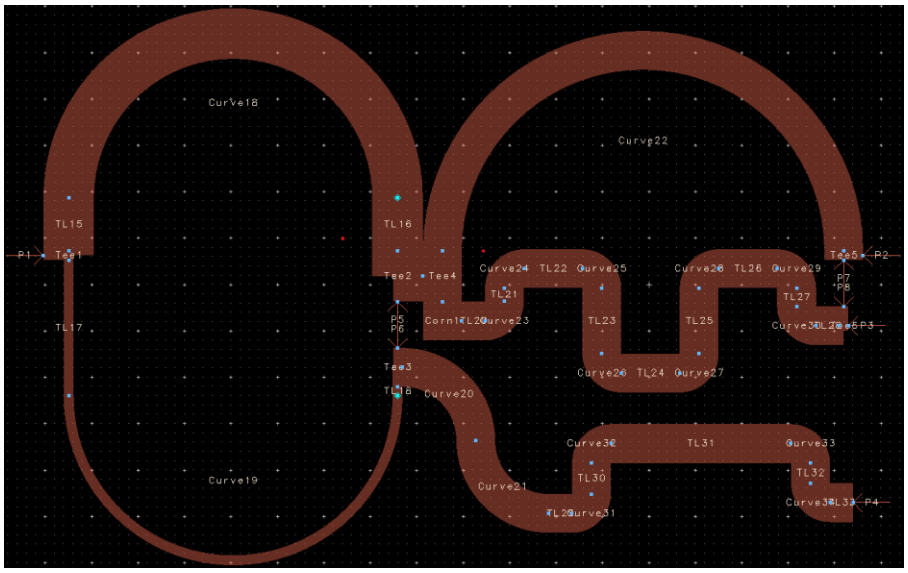


Fig. 8: *Layout diagram for micro-strip 3-way Wilkinson power divider.*

IV- Results and Discussion

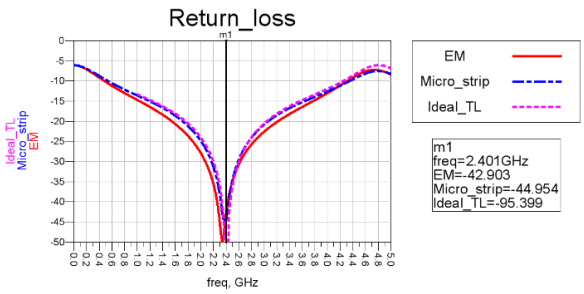


Fig. 9: *Input return loss S(1,1) in dB*

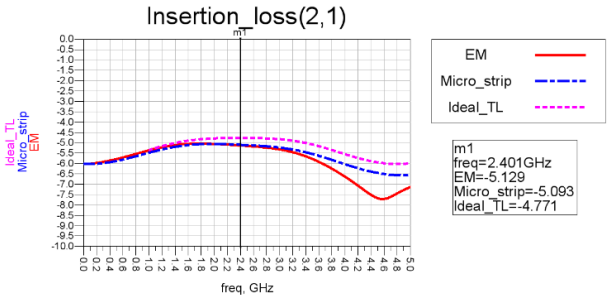


Fig. 10: *Insertion loss S(2,1) in dB*

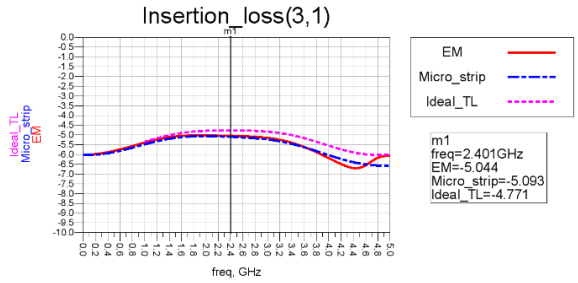


Fig. 11: *Insertion loss S(3,1) in dB*

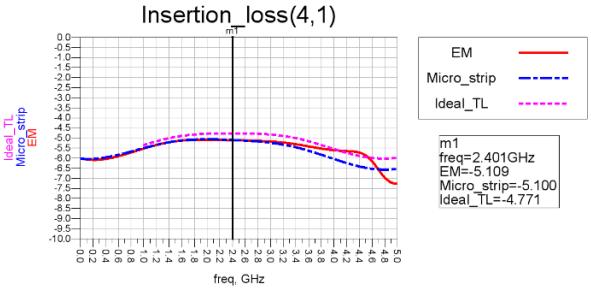


Fig. 12: *Insertion loss S(4,1) in dB*

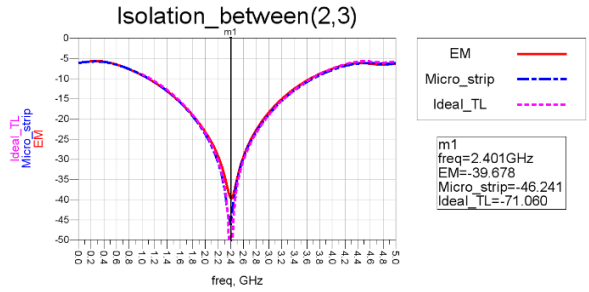


Fig. 13: *Isolation between ports 2 and 3 S(2,3) in dB*

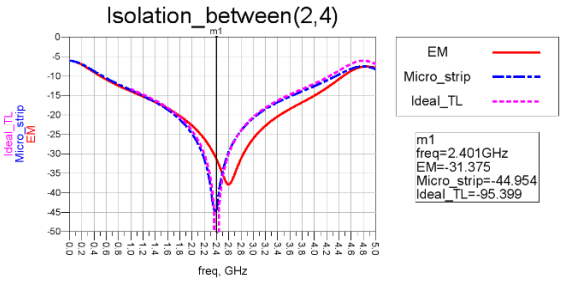


Fig. 14: *Isolation between ports 2 and 4 S(2,4) in dB*

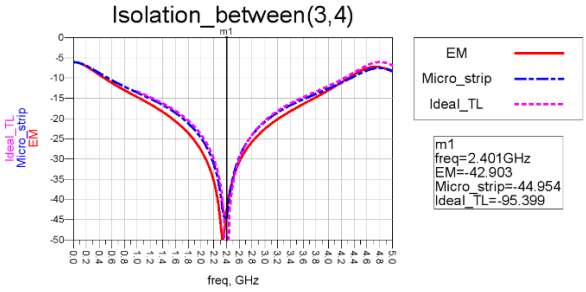


Fig. 15: *Isolation between ports 3 and 4 S(3,4) in dB*

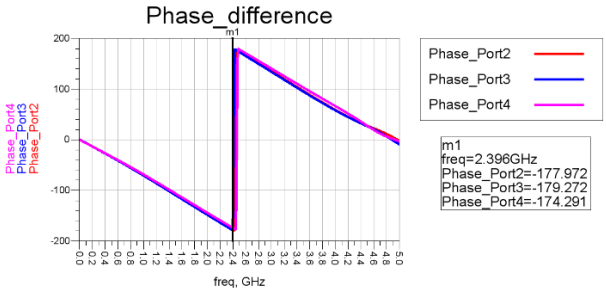


Fig. 16: *Phase difference between ports*

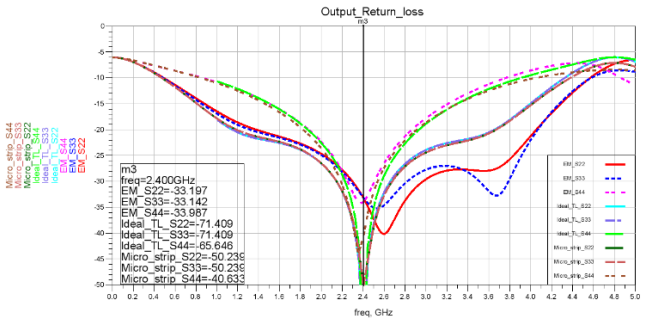


Fig. 17: *Output return loss for all 3 ports (S22, S33, S44)*

From the simulations results we can see that our 3-way Wilkinson power divider design and implementation using micro-strip technology performs well at the design frequency (2.4 GHz), from Fig.9 we can see that the input return loss for the ideal case is 95 dB and for the micro-strip circuit simulation it is 44.9 dB and in the electromagnetic simulation it is 42.9 dB the decrease in the input return loss is because of the high loss material we are using in the micro-strip implementation.

From Fig.10, Fig.11 and Fig.12 we can see the insertion loss for all of the 3 ports, in the ideal case the power division is perfect one third for each port ($IL_{dB} = -10\log(1/3) = 4.771$) as for the micro-strip circuit simulation we can see that there is excess insertion loss because of the high loss material used, we can see that insertion loss for port 2 is equal to 5.093 dB that means that port 2 gets 30.953% of the power and same for port 3, for port 4 the insertion loss is -5.1 dB so port 4 gets 30.903% so the equal power division is approximately satisfied with 7.191% of the input power lost inside the device due to non-ideality in the used material and similar results were obtained in the EM simulation.

From Fig.13, Fig.14 and Fig.15 we can see that the isolation between ports 2,3 in the ideal case is -71.060 dB and the isolation between ports 2,4 and 3,4 is -95.399 dB, in the micro-strip circuit simulation the isolation between ports 2,3 increases to -46.241 dB and the isolation between ports 2,4 and 3,4 increases to -44.954 dB, in the EM simulation the isolation between ports 2,3 increases to -39.678 dB and the isolation between ports 2,4 increases to -31.375 dB and the isolation between ports 3,4 increases to -42.903 dB .

The phase difference between each one of the output ports and the input port in the ideal case is exactly equal to -180 degree for all 3 ports in the ideal case but in the micro-strip circuit implementation the phase difference starts to differ as shown in Fig.16, for port 2 the phase difference is equal to -177.972 degree and for port 3 the phase difference is equal to -179.272 degree and for port 4 the phase difference is equal to -174.291 degrees.

The output return loss for all ports is shown in Fig.17, for port 2 and port 3 the output return loss is 71.402 dB in the ideal case and 50.239 dB in the micro-strip circuit simulation and for the EM simulation port 2 has an output return loss of 33.197 dB and port 3 has an output return loss of 33.142 dB, as for port 4 its output return loss in the ideal case is equal 65.646 dB and for the micro-strip circuit simulation its output return loss is 40.633 dB and the output return loss for the EM simulation is equal to 33.987 decibels, all at design frequency.

Table 2: *obtained values for the input return loss, insertion loss and isolation between ports in bandwidth.*

Parameters	S value	Accepted value
Input return loss	S(1,1)	-15 dB
Insertion loss	S(2,1), S(3,1), S(4,1)	-5.3 dB
Isolation between ports	S(2,3), S(2,4), S(3,4)	-15 dB
Output return loss	S(2,2), S(3,3), S(4,4)	-15 dB

In Fig.18 the bandwidth satisfying the input return loss accepted value is shown, in Fig.19 the bandwidth satisfying Insertion loss for all 3 ports accepted value is shown, in Fig.20 the bandwidth satisfying the isolation between ports accepted value is shown and the bandwidth of the proposed design is obtained by getting the intersection between all 3 graphs as shown in Fig.21, the bandwidth is from 1.6 GHz to 3.2 GHz, the obtained **bandwidth is equal to 66.67%** satisfying the parameters shown in Table 2.

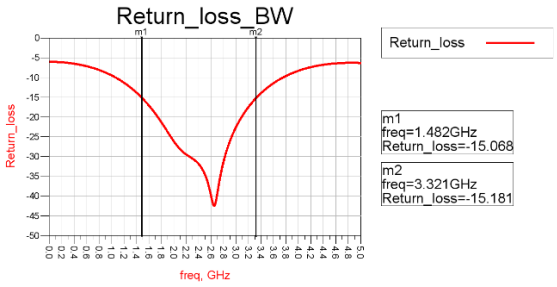


Fig. 18*: Insertion loss bandwidth.*

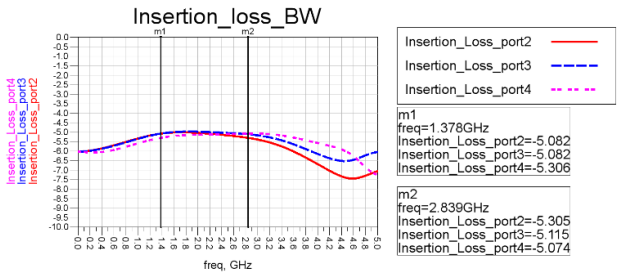


Fig. 19: *Return loss bandwidth.*

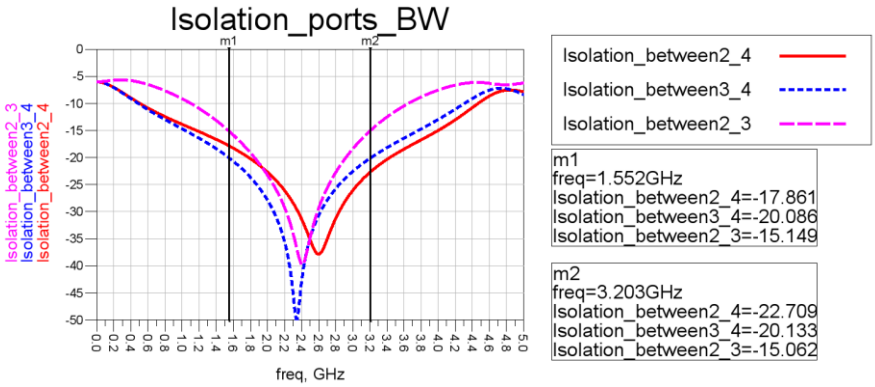


Fig. 20: *Bandwidth for isolation between ports.*

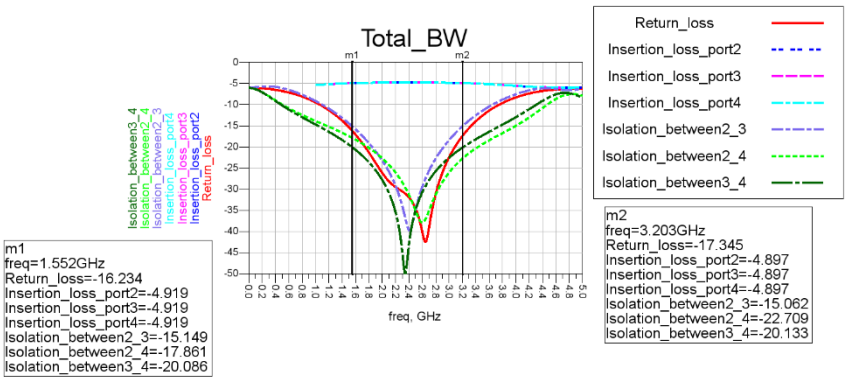


Fig. 21: *The proposed design bandwidth.*

V- Conclusion

In this report, we presented a three-way Wilkinson power divider design and analysis using ideal transmission lines and micro-strip line technology. The ideal transmission line simulation showed perfect power division among the three output ports and excellent input/output matching and isolation between output ports at design frequency 2.4 GHz. In the micro-strip circuit simulation and EM simulation for the layout there is almost equal power division ratio and very good input/output ports matching and isolation between output ports at design frequency with differences between the ideal transmission lines and the micro-strip technology because of the losses in the used materials and substrate.

VI- Future Work

Our next step is to optimize the designed layout to be fabricated and this optimization includes changing resistors values and their assumed sizes in the layout based on the available resistors and also adjusting the input and output ports based on the available connectors, and testing the circuit after fabrication and comparing the obtained values to the obtained results in this report.

References

[1] D. M. Pozar, "Introduction to Microwave Engineering," in *Microwave Engineering*, 2011, pp. 1-10.

[2] M. J. U. M. Jalalifar, "POWER SPLITTER ARCHITECTURES AND APPLICATIONS," *Progress In Electromagnetics Research C,* vol. 18, pp. 231-244, 2011.

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