Lab05 - JK Flip Flops and Sequential Circuits

This lab will focus on learning how to design circuits that utilize memory and a clock in order to achieve so functionality. In previous labs, we learned the fundamentals of creating circuits, in which the circuits have no memory and the inputs are the only things determining the output. This lab introduces the idea of a clock and how combinational circuits outputs at time t + ε, where ε conveys that in real life, the circuit does not happen instantaneously.

A clock is a digital signal that simply alternates between logical one and logical zero (high/low or +5V/0V) with consistent, regular timing, yielding a square wave. A clock sequential circuit achieves memory and combinational circuit functionality. The storage device to a holding a single bit of information is called a flip-flop.

We begin the lab by exploring the IC 7476 which is the hardware for 2 flip-flops. First, we plug in pin 5 to +5V and pin 13 to GND. We also see pins PRE and CLR which allow us to preset and clear the stored value that happens in sync with the clock. For our lab, we plug these on both flip-flops to +5V so they don't affect our experiment. Then I wire the pins 1 and 6 to the function generator that is our CLK for this experiment. To test out the flip-flop, I wire the inputs (J and K) to switches and the output (Q) and CLK to the logic indicator. I find out that it takes at least 1 clock cycle to take on a new value.

In the next part of the lab, we make a Morre circuit. A general model of a Moore sequential circuit consists of two combinational circuits to compute the next state and to compute the output based on the present state. A sequence detector is a circuit that serially examines a string of 0's and 1's and outputs if our sequences match a particular pattern. For this lab, our sequence was 111. The very first step was to draw the Moore diagram for that sequence which consisted of four states. The next step was to draw the next state for the present state in a truth table followed by extending the truth table to

see the output function of the machine. Further, to get boolean expressions we use Karnaugh maps and got 4 separate equations. (picture for this is attached)

Moving forward, we used the IC 7808 AND gate to implement the equation Q0X. The inputs were X (switch 1) and 2Q on the JK flip-flop and the output was given in pin 4 on the JK flip-flop. We use an IC 7404 NOT gate to implement ~X and the output was inserted into as the first input to an IC 7432 OR gate to implement ~X + ~Q1. The second input (~1Q) was from pin 14 on the JK flip-flop. The output from the OR gate was then given to 2K (pin 12) on the JK flip-flop. 2J was connected to switch 1 which was X in this experiment. Then 2Q (pin 11) on the JK flip-flop and 1Q (pin 15) on the JK flip-flop were given as inputs to an AND gate. The output from this gate was then connected to the logic indictor. The CLK pin was also connected to the logic indicator.

After setting up the experiment, we see that it takes three clock cycles for a JK flip-flop to change or flip its value. The experiment thus shows that the power traveling in the circuit does not, in fact, change instantaneously. It does take time for the circuit to be implemented even though it might not seem like it.
The video of the circuit is attached.