CS 281: Computer Systems

Lab 07: Condition Codes

The main purpose of this lab is to build a circuit to save a value for later. In lab 4, you worked in a group to build an ALU which output flags, including the zero flag, sign flag, and overflow flag. As you are soon to find out, these values should remain persistent, saved until the next operation occurs. In this lab, you will choose an appropriate flip-flop and build a logisim subcircuit that saves a flags value until another operation sets it once more. While the end goal of this logisim subcircuit will be used in your final project, enough of these sub circuits connected together results in an 8-bit register.

In the design section, you will apply your knowledge to solve a design challenge. **The lab report should focus solely on your design for the design portion of the lab, but include truth tables and Karnaugh maps where appropriate.**

Design: The Logic

In this first section, we will lay out the problem description. There are two incoming signals, A and B. A represents a signal that when high, should allow the flip-flop to be set to the signal of B. When A is low, the value of Q should not change.

Q1. Which flip-flop would be best to save this 1-bit value? Why?

Regardless of whether you chose a D or JK flip-flop, there is now a third potential input, Q. Set up your truth table appropriately, with A, B, and Q on the left as inputs and your Q_1 and D or J and K on the right as your outputs.

Q2. What is your SOP formula? Note that this will differ depending on which flip-flop you chose.

Use your knowledge of Karnaugh maps and algebraic proofs to reduce your SOP expression.

Q3. What are your simplified formula(s)?

Sketch out your expected combinational circuit, then build this (with your flip-flop) as a subcircuit in Logisim.

Design: Register Data

What was originally intended to save a single bit condition flag (zero, signed, overflow) can be used for so much more. Replicate your subcircuit eight times to build an 8-bit register that saves a full byte of input data.

Deliverables

For this lab, you should work on your own to create 1 Logisim file with one subcircuit and an 8-bit register. You will also write a lab report indicating your design choices and outcomes.