Report

Milestone 2

RISC-V CPU

Computer Architecture

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Implemented Modules:

The RISC-V CPU was structured using various Verilog modules, each responsible for specific functionalities. The key modules included→

Instruction Memory (InstructionMem):

- Responsible for fetching instructions from memory based on the program counter (PC) value.

Control Unit (ControlUnit):

- Generates control signals based on the opcode of the fetched instruction, controlling various CPU operations.

Register File (RegFile):

- Stores and retrieves data from registers, facilitating data manipulation operations.

Arithmetic Logic Unit (ALU):

- Performs arithmetic and logical operations on data operands based on the ALU control signals.

Data Memory (DataMem):

- Stores and retrieves data from memory locations, supporting load and store operations.

Program Counter (PC):

- Manages the program counter value, determining the address of the next instruction to be fetched.

Immediate Generator (Immgen):

- Generates immediate values for instructions requiring immediate operands.

Branch Control Unit (branch_ctrl):

- Controls branch operations and determines branch outcomes based on instruction operands.

Multiplexers (Mux):

- Selects appropriate data inputs based on control signals, facilitating data routing within the CPU.
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Jump Control Unit:

- The Jump Control Unit managed control signals related to jump instructions such as JAL, JALR, and branches.
- It determined the target address for jumps and branches and controlled the program counter accordingly.

Limitations:

- Sh and sb are not working properly.