Katie Hamiter

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SKILLS:

Experience with Multisim, Xilinx Vivado, LTspice, Altium, AutoCad, Linux, C/C++ programming, and Verilog/VHDL programming

EDUCATION:

B.S. Electrical Engineering, San Diego State University Aug 2018 - May 2022
M.S. Computer Engineering, University of Southern California Aug 2023 – May 2026

WORK EXPERIENCE:

Electrical Engineer at Fisica (Formerly L3Harris) Sept 2022 – June 2025 | Simi Valley, CA

- Designed antenna systems
  - Worked with firmware and hardware teams to design a new track receiver
  - Created servo, feed, antenna system controller and pedestal wiring diagrams for existing systems and system upgrades using AutoCad
  - Contributed to design of S, X, and Ka band feed block diagrams
  - Experience testing RF components using spectrum analyzer
  - Performed power analyses on sub-systems to verify that current drawn from components will not exceed system capabilities
  - Developed software I/O definitions based upon antenna system controller and feed designs to support software development
  - Maintained legacy PCBs using Altium
  - Performed site surveys to analyze performance of electronics in existing systems prior to upgrading

Product Engineer I Intern / Product Engineer II at Semtech April 2022 – Sept 2022 | San Diego, CA

- Evaluated capability of ICs in smart phones / smart devices
  - Analyzed test and characterization data to demonstrate product meets marketing requirements
  - Prepared reliability test plans to support new product qualification
  - Performed product testing using ATE (Automatic Test Equipment)

PROJECTS:

UNIX Socket Programming

- Designed library management system using C++ in Linux environment
  - Created 5 servers, “Client”, “Main”, “Science”, “History”, and “Literature” which communicate over TCP and UDP
  - System enables users to submit a book code through the client server to access the main library management server, check its availability within the relative department server which stores information on books offered, and proceed with borrowing the book if available

Multisim/Vivado Projects

- Implemented a divider with cache on Nexys 7 FPGA using VHDL
  - Wrote code for divider, cache, CAM and the LRU stack
  - Used UART to send 4 bit hex number to FPGA representing dividend and divisor, then 4 bit quotient and remainder appeared on FPGA screen after division was carried out
- Designed gray code counter using VHDL
- Designed a 5 stage pipelined CPU using BRAMS in VHDL

Bluetooth Speaker with Class D Amplifier

- Designed 10 W Class D Amp with less than 1% THD
  - Designed, tested, and integrated gate driver circuit and low pass filter circuit
  - Designed PCB using KiCad
  - Evaluated reliability and performance of components such that current spikes of up to 3 A could safely run through circuit
  - Carried out root cause analysis when failure of subsystems or system occurred during each phase of testing