Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Lab Sheet– 5 (20th February 2018)

MEMORY

Pre-lab Work:

1. What is a RAM? List its input output signals?
2. Draw the timing diagram of read and write cycle?
3. What is CAM? How does it operate? Where is it used?
4. How can we improve the efficiency of digital systems through Look Up Tables?

Using Verilog HDL implement the following Implement a 64 Byte RAM using Verilog HDL. Initialize its content from a .txt file and using the ***$readmemeh*** system task. Now read each memory location sequentially and replace it with its 2's complement. You can use dataflow, model to obtain the 2's complement.

****** The End ******