Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Homework Exercise – 3 (30th January 2018)

Gate Level (structural) Modeling Style

HWP05: Implement a ***priority encoder (4 to 2)*** using primitive gates only. There are four inputs ***I0, I1, I2 and I3*** (active high) and the order of priority is from highest (I0) to lowest(I3). There is a two-bit output (active high) ***Y*** which indicates the input asserted based upon the priorities. An additional output signal ***V*** indicates if the output status is valid (at-least one of the inputs is asserted) or not.

HWP06: Implement a serial adder (adds one bit at a time, needs n-cycles to implement a n-bit addition). Necessary components for building this system like parallel in serial out (PISO), Serial in parallel out (SIPO), D-flip-flop, full adder can be modelled using modeling style of your choice (in most cases designers choose behavioral modeling due to its ability to implement both sequential and combinational circuits).

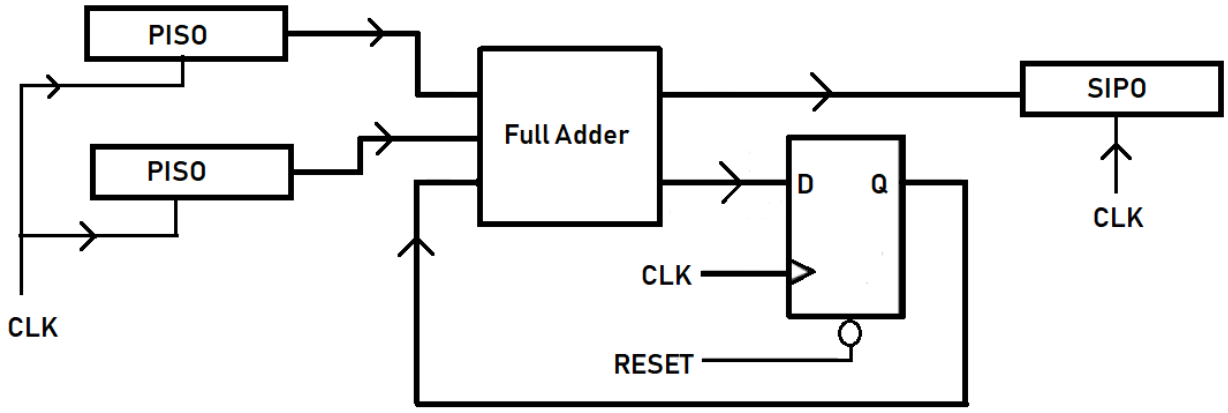

Figure 1 A block diagram of Serial Adder

HWP07: Implement a ***4-bit unsigned binary array multiplier*** using full adders and half adders.

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