Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Homework Exercise – 2 (23rd January 2018)

Behavioral Modeling Style

HWP02: Implement a ***8-bit unsigned multiplier*** using the shift-add algorithm. The module has two 8-bit unsigned inputs ***a,b*** a ***clock*** signal (negative edge), ***reset*** (active high, asynchronous) and a 16-bit output ***prod*** also there is a single bit output ***eop*** (end of operation) which goes high for one clock cycle when the multiplication operation is completed.

HWP03: Implement a ***BCD up/down counter.*** The counter has a two-digit output (remember each BCD digit is 4-bit wide and valid BCD digits are from 0 to 9 only). The counter counts from "00" to "59" if it is counting in ***up*** mode. It will count from "59" to "00" when it is in ***down*** mode. Choose a negative edge clock and asynchronous active low reset for the module. There is a control signal ***up/down*** which determines the mode of operation of the counter. ***Up*** when ***high*** and ***down*** when ***low***.

Example output: count in up mode

00, 01, 02, 03, 04, 05, 06, 07, 08, 09, 10, 11, 12, 13 ..... 59, 00,01 …

HWP04: Implement a ***8-bit signed divider*** using ***repetitive subtraction***. The module has two 8-bit signed inputs ***divisor, dividend*** a ***clock*** signal (negative edge), ***reset*** (active high, asynchronous) and two 8-bit outputs ***remainder and quotient*** also there is a single bit output ***eop*** (end of operation) which goes high for one clock cycle when the division operation is completed.

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