Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Homework Exercise – 4 (07th February 2018)

Finite State Machine (FSM) Modeling

HWP08: Implement a Mealy/Moore type FSM to detect a palindrome of length 3-bits in a serial input bit stream. Example of three bit palindromes 111,101,010,000.

HWP09: When a certain serial binary communication channel is operating correctly, all blocks of 0's is of even length and all blocks of 1's are of odd length. Draw the state diagram (Moore) or table of a machine that will produce an output symbol $z = 1$ whenever a discrepancy from the above pattern is detected. The following is an example.

example.

X : 0 0 1 0 0 0 1 1 1 0 1 1 0 0 · · ·
Z : 0 0 0 0 0 0 1 0 0 0 1 0 1 0 · · ·

HWP10: Implement (FSM based approach) a serial to parallel Excess-3 code to BCD converter. The circuit has a single input line (1-bit) ***sin*** receiving messages in Excess-3 code, and a 4-bit output line ***bcd*** which produces the BCD code corresponding code to input messages. The input arrives serially with LSB first. The outputs are specified only at the occurrence of every fourth input.

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