Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Lab Sheet– 6 (27th February 2018)

System Level Design

Implement a 8 bit multiplier using a four bit multipliers and a suitable adder.

1. Use necessary hardware to finish the job in a single clock cycle.
2. Use only a single multiplier and a single adder. How many clock cycles do you need?
3. Use Pipe-Line approach for this problem.

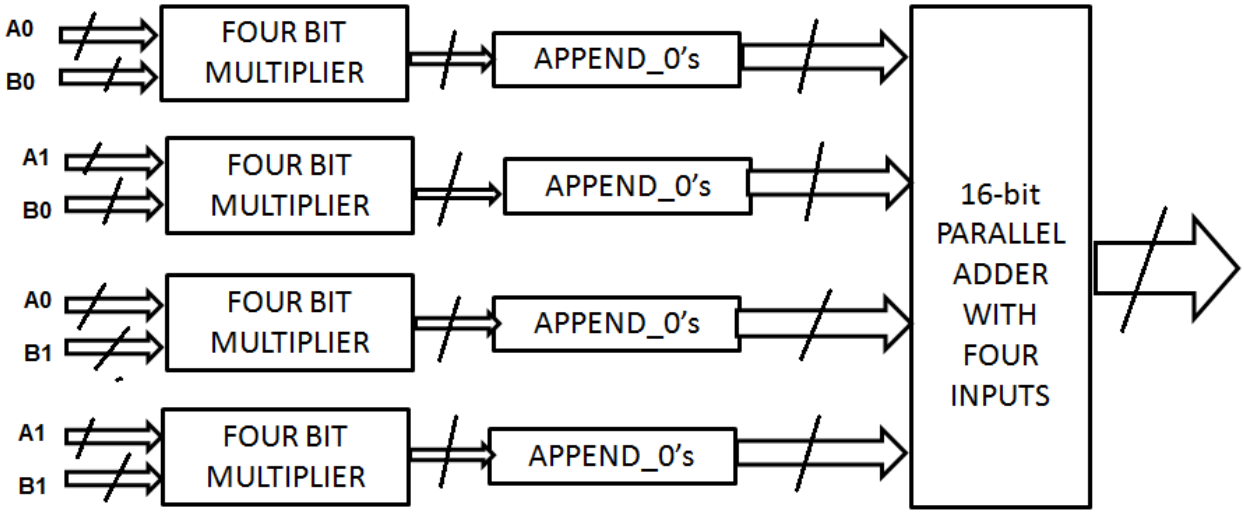

Figure 1 Single Cycle Implementation

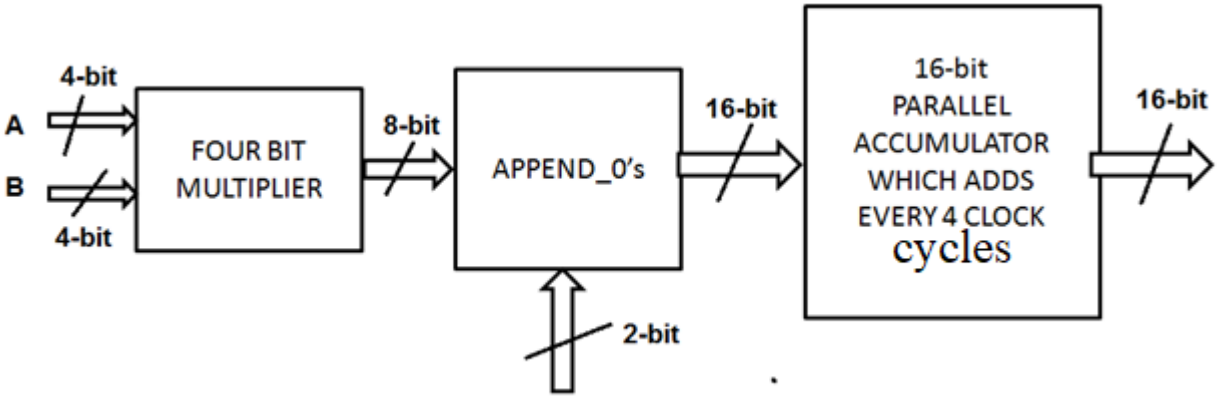

Figure 2 Multi-Cycle Implementation

*** *The End* ***