Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Lab Sheet – 1 (16th January 2018)

Dataflow Modeling Style

In today's lab we shall try to implement a few combinational circuits which we have studied in digital design using dataflow modeling style and verify their functionality using a suitable test bench.

1. Implement a half adder.
2. Implement a full adder.
3. Implement a 2:4 decoder.
4. A four bit ALU. The ALU operates on two four bit operands a and b to produce a four bit output. It can perform eight different operations on the operands.

S.No.	Opcode	function
1	000	A – B
2	001	A + B
3	010	A XOR B
4	011	A AND B
5	100	A OR B
6	101	Shift right A by 1 bit (logical)
7	110	Shit Left A by 1 bit (logical)
8	111	Shift arithmetic right A by 1 bit

****** The End ******