Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Self-Assessment Test-2 (16th February 2018)

Instructions to the candidate

1. Please solve this test on your own, without taking help from any source.
2. This test should be ideally completed in 15 to 20 minutes.

Answer the following questions

1. Look at the Verilog code given below and identify the Boolean function (SOP) implemented by the module.

```
module who_am_I(output y, input a,b,c);
assign w1 = a & b ;
assign w2 = b | a ;
assign f = c ? w2 : w1 ;
endmodule
```

2. What is the difference between ***casex*** and ***casez*** statement in Verilog?

3. Using primitive gates implement a tri-state address bus. The module has a 8-bit input address input ***ad_in*** and a one bit signal ***ale.*** If ale is HIGH then 8-bit output signal ***ad_out*** is assigned with ***ad_in*** while ***ad_out*** is in high impedance state if ***ale*** is LOW.

4. In the following Verilog Code Identify the errors along with proper reason.

```
module trace errors()

wire [2:0]a,b ;
wire [3:0]y ;

always @(a,b)
begin
case({a,b})
3'b2 : y <= a & b ;
3'b1 : half_adder HA(y,a,b);
3'h3 : y = a ^ b ;
end
endmodule
```

****** End of Paper ******