**Birla Institute of Technology and Science Pilani**
**CS F342 Computer Architecture**
**Second Semester 2017-18**
**Lab Sheet– 3 (30th January 2018)**

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## Gate Level (Structural) Modeling Style

*In today's lab we shall implement a few digital systems which we have studied in digital design using gate level (structural) modeling style and verify their functionality using a suitable test bench.*

1. Implement a 4-bit Ripple Carry Adder (RCA) using Full Adders.
2. Implement a synchronous binary mod-10 up counter (counts from 0 to 9). The system has two inputs clock, reset and a 4-bit output count. Use a negative edge triggered d-flip flop with asynchronous active high reset and primitive gates for implementing the design.

****** The End ******