Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Self-Assessment Test-I (04th February 2018)

Instructions to the candidate

1. Please solve this test on your own, without taking help from any source.
2. This test should be ideally completed in 15 to 20 minutes.

Answer the following questions in one word/sentence

1. What is the major advantage of FPGAs over ASIC?
2. What does 'V' stand for in VHDL?
3. The Verilog operator for *logical not* is _____.
4. If *a* is declared as a 3 bit wire, then the size of the signal *{3'd0,a,a[2]}* is____
5. What is the difference between *$display* and *$monitor*?

Identify whether the following statements are true or false

6. Always and initial blocks can be nested.
7. The default size and data type of an uninitialized signal is 32 bit and wire.
8. The declaration *wire [4:-2]d* declares a 8-bit wire.
9. Verification is at software level while testing is at hardware level.

Complete the following Verilog code

10. Complete the following piece of Verilog code (test bench) to generate a *clk* signal of frequency 10MHz and duty cycle ($T_{ON}/T_{ON} + T_{OFF}$) = 40%.

```
`timescale 10ns/1ns;
module clk_gen();
reg clk;
initial #00 clk = 1'b0;
// fill the ----- correctly
always @(--------)
   begin
   -----------
   ----------
   end
endmodule
```

****** End of Paper ******