Birla Institute of Technology and Science Pilani
CS F342 Computer Architecture
Second Semester 2017-18
Homework Exercise – 1 (16th January 2018)

Dataflow Modeling Style

HWP01: Implement a *comparator* which can compare two 8 bit numbers **A** and **B** and has three output signals **AeqB** , **AgtB** and **AltB** which are asserted (active high) when A equals B , A greater than B and A less than B. An additional 1 bit input **signed/unsigned** determines whether the two operands are to be treated as unsigned or signed (2's complement notation). While this input is high the operands are treated as signed and while it is low they are treated as unsigned. Use data flow modeling. You can customize any of the test bench modules provide to you in the lab sheets for testing this module.

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