

# Kshitij KHANDELWAL

## ABOUT ME

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INTERESTS: • Computer Vision, Generative Adversarial Networks, Reinforcement Learning  
• Speech Processing, Biomedical Signal Processing  
WEBPAGE: [khandelwalkshitij.github.io](https://khandelwalkshitij.github.io)  
LANGUAGES: • English (fluent) • French (basic knowledge) • Hindi (fluent) • Marathi (fluent)

## EDUCATION

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*Current* BE. (Hons.) in ELECTRICAL AND ELECTRONICS ENGINEERING  
*Aug '15 - Jul '19 (Exp.)* **Birla Institute of Technology and Science, Pilani**, Pilani, India  
CGPA 8.61/10 (Semester IV)

## INDEPENDENT COURSEWORK (ONLINE)

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### COMPLETED

**Neural Networks for Machine Learning** Geoffrey Hinton, University of Toronto  
**Reinforcement Learning** David Silver, University College London

### ONGOING

**CS231n: Convolutional Neural Networks** Stanford University  
**Deep Learning for NLP** Oxford University

## UNIVERSITY COURSEWORK

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### Electrical Engineering

Electrical Sciences  
Electrical Machines  
Control Systems  
Neural Networks and Fuzzy Logic  
Power Systems (Ongoing)

### Electronics Engineering (Analog)

Electronic Devices  
Micro-electronic Circuits  
Analog VLSI Design  
Analog Electronics (Ongoing)  
Power Electronics (Ongoing)

### Electronics Engineering (Digital)

Digital Design  
Computer Programming  
Microprocessors and Interfacing  
Computer Architecture  
Digital VLSI Design

### Communications Engineering

Signals and Systems  
Communication Systems  
Digital Signal Processing

### Mathematics

Multivariate Calculus & Vector Fields  
Probability & Statistics  
Linear Algebra & Complex Analysis  
Differential Equations  
Optimization

### Sciences

Principles of Economics  
Mechanics, Oscillations & Waves  
General Chemistry  
General Biology  
Thermodynamics

## WORK EXPERIENCE

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### *Current*

APR '17

Control Systems Engineer at [HYPERLOOP INDIA](#), India

Worked on Control Algorithm for Braking and Trajectory of the OrcaPod. Current work involves developing the EM Model for Braking. Hyperloop India is the only Indian team and one of the only 24 University teams worldwide to have presented their Pod at **SpaceX Competition Weekend II, 2017 in Los Angeles, CA**. Hyperloop India is currently working towards the [SpaceX Competition Weekend III, 2018](#).

MAY - JUL '17

Summer Research Intern at SOLID STATE PHYSICS LABORATORY (SSPL - DRDO), New Delhi, India

Worked on designing Microstrip Filters for RF Applications. Designed, simulated and optimized a L-Band Microstrip Low Pass Filter using Agilent ADS.

## PROJECTS

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Current DEC '17	<b>Satellite Image Super-Resolution Using GANs</b> <i>Independent, BITS Pilani, India</i> The Project aims at testing the SR-GAN method for Image Super Resolution on the LANDSAT-7 Satellite Imagery Dataset using Generative Adversarial Networks and thereby develop a computationally efficient technique for Satellite Image Super-resolution
OCT - NOV '17	<b>LPC for Formant Analysis of Concurrent Vowels</b> <i>Course Project (Digital Signal Processing), BITS Pilani, India</i> The project focuses on understanding the effects of noise on the formant representations of both single and concurrent vowels and using Linear Predictive Coding (LPC) and Speech Spectrum Shaped Noise. Further, an attempt was made to understand which vowels (both single and concurrent) are more susceptible to noise. ( <a href="#">Github</a> ) ( <a href="#">Report</a> )
OCT - NOV '17	<b>Actor-Critic Model for Playing Atari Games</b> <i>Course Project (Neural Networks &amp; Fuzzy Logic), BITS Pilani, India</i> The project focuses on developing a comparison between using Actor-Critic Models and Generative Adversarial Networks for learning to play Atari Games. The games used for this purpose were Open-AI Gym's Cartpole-V0 and Lunar Lander.
OCT - NOV '17	<b>Design of a High Gain Two Stage Telescopic Operational Amplifier</b> <i>Course Project (Analog &amp; Digital VLSI Design), BITS Pilani, India</i> The project involved designing a high gain two stage telescopic operational amplifier with a phase margin of 60 degrees, ICMR from 0.9V to 2.2V for a VDD of 2.5V and a 3 dB bandwidth of 100 KHz. The project was completed in LT Spice.
MAY - JUL '17	<b>Design of Low-Pass Microstrip L-Band Filter</b> <i>Internship Project, Solid State Physics Laboratory (SSPL), Defence Research &amp; Development Organization (DRDO), New Delhi, India</i> The Project was towards the fulfillment of a summer research internship at SSPL-DRDO. It involved design of an optimum L-Band Low-Pass Filter, EM Simulation, and fault-analysis of the same. ( <a href="#">Certificate</a> )
JAN - APR '17	<b>Soft Computing in Electromagnetics</b> <i>Study Project (Dr. Navneet Gupta), BITS Pilani, India</i> Optimization of Gain and Directivity of Microstrip Patch Antenna Arrays using Artificial Neural Networks and Bacterial Foraging Optimization. ( <a href="#">Letter of Recommendation</a> )

## SKILLS

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### Programming Languages

- MATLAB • Python (numpy, scikit-image, scikit-learn, tensorflow, openCV, pyGTK)
- Embedded C • Verilog • Assembly (MASM and DebugX) • Shell • Perl • HTML • CSS •  $\text{\LaTeX}$

### Software

- Cadence • Agilent ADS • LTSpice • iVerilog • NI LABVIEW • COMSOL Multiphysics

## AFFILIATIONS

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Current Aug '15 - Present	<b>Chair (Operations) at ACM STUDENT CHAPTER, BITS Pilani, India</b> <ul style="list-style-type: none"><li>• Won the Best Association for Computing Machinery (ACM) India Student Chapter Award, thrice in a row. • Supervised Special Interest Groups on Cryptography and Linux.</li></ul>
Current Aug '17 - Present	<b>Senior Student Representative at CODECHEF CAMPUS CHAPTER, BITS Pilani, India</b> <ul style="list-style-type: none"><li>• Re-established the inactive campus chapter. • Competitive Programming SIG</li></ul>
Aug '15 - Mar '16	<b>Teaching Volunteer at NATIONAL SERVICE SCHEME (NSS), BITS Pilani, India</b> <ul style="list-style-type: none"><li>• Volunteered for Junoon, a nation-wide sports meet for the specially-abled. • Volunteered to set-up the annual Blood Donation Camp, BITS Pilani.</li></ul>