Kshitij Khandelwal

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About me

Address:	Ashok 271, BITS Pilani, Rajasthan - 333031
email:	kshitijgokul@gmail.com | f2015156@pilani.bits-pilani.ac.in
interests:	• Computer Architecture • Digital VLSI • Real Time Systems
languages:	• English (fluent) • Hindi (fluent) • Marathi (fluent)
Date of Birth:	5-Oct-1997 (20 Years Old)
Phone:	(+91) 94218 81230

Education

Current — Senior Year, BE. (Hons.) in Electrical and Electronics Engineering

Aug '15 - Jul '19 (Exp.) — **Birla Institute of Technology and Science, Pilani**, Pilani, India

CGPA: *8.3/10*

University Coursework

Electronics (Digital)
Digital Design
Microprocessors & Interfacing
Digital VLSI Design
Computer Architecture
Real Time Systems

Electronics (Analog)
Electronic Devices
Micro-electronic Circuits
Analog VLSI Design
Analog Electronics

Electrical
Electrical Sciences
Electrical Machines
Control Systems
Power Electronics
Power Systems

Communication
Signals and Systems
Digital Signal Processing
Communication Systems

Mathematics
Multivariate Calculus & Vector Fields
Probability & Statistics
Linear Algebra & Complex Analysis

Miscellaneous
Neural Networks & Fuzzy Logic
Quantum Info. Theory & Computation
Intro. to Astronomy & Astrophysics

Work Experience

Current — Aug '18

Teaching Assistant for CS F342 - Computer Architecture, BITS Pilani, India

Teaching Assistant for the Computer Architecture course for Fall 18-19 being taught by Dr. Sudeept Mohan, BITS Pilani. Tasks involve teaching a Verilog HDL to a batch of 50 students and evaluating their performance regularly.

Current — Feb '18

Lead Engineer, Electrical Power Subsystem at Team Pixxel

Team Pixxel is a student team from BITS Pilani aiming to participate in the IBM Watson AI XPRIZE competition. The team is working on developing a constellation of nanosatellites for remote sensing operations. I worked on designing an Electrical Power System for the satellite and implemented MPPT Control (P&O) using SPV 1040 with 30 triple junction solar cells in 5 configurations along with battery monitoring, charging and regulation. The DoD of the batteries in every cycle was limited to 7 percent .

Jan '18 - May '18

Teaching Assistant for EEE F244 - Microelectronic Circuits, BITS Pilani, India

Teaching Assistant for the Microelectronic Circuits course for Spring 17-18 being taught by Dr. Anu Gupta, BITS Pilani. Tasks involve training a batch of 250+ students in the use of EDA tools. Introduced use of GitHub for maintaining the repository for the course.

Apr '17 - Feb '18

Control Systems Engineer at Hyperloop India, India

Designed and Implemented the Control Algorithm for Braking and Trajectory of the OrcaPod. Hyperloop India is the only Indian team and one of the only 24 University teams worldwide to have presented their Pod at **SpaceX Competition Weekend II, 2017 in Los Angeles, CA.**

May '17 - Jul '17

Research Intern at Solid State Physics Laboratory (SSPL - DRDO), New Delhi, India

Worked on designing Microstrip Filters for RF Applications. Designed, simulated and optimized a L-Band Microstrip Low Pass Filter using Agilent ADS.

Projects

Mar - Apr '18 | Design of a 16-bit Multicycle RISC Microprocessor
Course Project (Computer Architecture), BITS Pilani, India
Designed, implemented & tested an optimized 16 bit multicycle RISC Processor to support a total of 18 instructions including R-Type, memory, jump, branch, logical and shift instructions. The project was coded in Verilog HDL and tested using iVerilog and GTKwave. (GitHub)

Oct - Nov '17 | LPC for Formant Analysis of Concurrent Vowels
Course Project (Digital Signal Processing), BITS Pilani, India
The project focuses on understanding the effects of noise on the formant representations of both single and concurrent vowels and using Linear Predictive Coding (LPC) and Speech Spectrum Shaped Noise. Further, an attempt was made to understand which vowels (both single and concurrent) are more susceptible to noise. (GitHub)

Oct - Nov '17 | Transmission Gate Based Design to Implement Boolean Function
Course Project (Analog & Digital VLSI Design), BITS Pilani, India
Designed and implemented a Transmission Gate based model to implement a Boolean Function while minimizing the area and power consumption.

Oct - Nov '17 | Design of a High Gain Two Stage Telescopic Operational Amplifier
Course Project (Analog & Digital VLSI Design), BITS Pilani, India
Designed a high gain two stage telescopic operational amplifier with a phase margin of 60 degrees, ICMR from 0.9V to 2.2V for a VDD of 2.5V and a 3 dB bandwidth of 100 KHz using LT Spice.

May - Jul '17 | Design of Low-Pass Microstrip L-Band Filter
Internship Project, Solid State Physics Laboratory (SSPL), Defence Research & Development Organization (DRDO), New Delhi, India
The Project involved design of an optimum L-Band Low-Pass Filter, EM Simulation, and fault-analysis of the same using Agilent ADS. (Certificate)

Jan - Apr '17 | Soft Computing in Electromagnetics
Study Project (Dr. Navneet Gupta), BITS Pilani, India
Optimization of Gain and Directivity of Microstrip Patch Antenna Arrays using Artificial Neural Networks and Bacterial Foraging Optimization. (Letter of Recommendation)

Skills

Programming • Verilog • MATLAB • C++ • Assembly (MASM & DebugX) • Python • Perl • HTML • CSS

Software • ModelSim • Microwind • LTSpice • Agilent ADS • iVerilog • Simulink • COMSOL Multiphysics • EagleCAD PCB • Proteus Design Suite • Code Composer Studio

Affiliations

Aug '15 - Apr '18 | Chair (Operations) at ACM Student Chapter, BITS Pilani, India
• Won the Best Association for Computing Machinery (ACM) India Student Chapter Award, thrice in a row. • Supervised Special Interest Groups on Cryptography and Linux.

Aug '17 - Apr '18 | Senior Student Representative at Codechef Campus Chapter, BITS Pilani, India
• Re-established the inactive campus chapter. • Competitive Programming SIG

Awards

Mar '18 | Best Paper Award, Electronics & Communication, APOGEE 2018
Department of Paper Presentation & Evaluation, BITS Pilani

Feb '13 | National Talent Search Examination Scholarship
National Council Of Educational Research And Training, Government of India