Kshitij Khandelwal

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EDUCATION

BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE (BITS), PILANI

BE (Hons) in Electrical and Electronics Engineering
Aug 2015 - Jul 2019 (Expected)
Pilani, Rajasthan, India
CGPA: 8.3/10

Class XII (Maharashtra Board)
Shri Dawale Jr. College, Akola, India
Score: 93.08/100
Grad: May 2015

Class X (Maharashtra Board)
Mount Carmel High School, Akola, India
Score: 97.82/100
Grad: May 2013

COURSEWORK

MOOCS

Introduction to FPGA Design
(Timothy Scherr, Coursera) Building OVM UVM Testbenches
(Ramdas Mozhikunnath M, Udacity)
Neural Networks for ML
(Geoffrey Hinton, Coursera)
Reinforcement Learning
(David Silver, UCL)

UNIVERSITY COURSES

Computer Programming
Digital Design
Microprocessors & Interfacing
Computer Architecture
Microelectronic Circuits
Analog & Digital VLSI Design
Signals & Systems
Communication Systems
Digital Signal Processing
Electrical Sciences
Electrical Machines
Control Systems
Neural Networks & Fuzzy Logic
Power Electronics
Analog Electronics
Power Systems

University Webpage:// **f2015156**
LinkedIn:// **khandelwalkshitij**

EXPERIENCE

DRDO - SOLID STATE PHYSICS LABORATORY (SSPL)

Summer Research Intern
MAY 2017 – JUL 2017 | New Delhi, India

- Designed, simulated and optimized a L-Band Microstrip Low Pass Filter using Agilent ADS.

HYPERLOOP INDIA

Contrl Systems Engineer
APR 2017 – FEB 2018 | Pilani, India | Bengaluru, India

- Worked on Control Algorithm for Braking and Trajectory of the OrcaPod.
- Worked on the Permanent Magnetic Eddy Braking System of the OrcaPod.
- Hyperloop India is the only Indian team and one of the only 24 University teams worldwide to have presented their Pod at SpaceX Competition Weekend II, 2017 in Los Angeles, CA.

EEE F244: MICRO-ELECTRONIC CIRCUITS

Teaching Assistant
SPRING 2018 | BITS Pilani, Pilani, India

PROJECTS

DEEP REINFORCEMENT LEARNING FOR CONTINUOUS CONTROL

Design Project, CEERI, Pilani
JAN 2017 – Present | Pilani, India
Working under Dr. Ing. Jagdish Raheja, Chief Scientist and Group Head, Control and Automation Group, CSIR - CEERI, to develop a robust Deep Reinforcement Learning based algorithm for obstacle avoidance based path planning of robot for medical applications.

DESIGN OF A HIGH GAIN 2-STAGE TELESCOPIC OPAMP

Course Project, Analog & Digital VLSI Design, BITS Pilani
JAN 2017 – May 2017 | Pilani, India
The project involved designing a high gain two stage telescopic operational amplifier with a phase margin of 60 degrees, ICMR from 0.9V to 2.2V for a VDD of 2.5V and a 3 dB bandwidth of 100 KHz. The project was completed in LT Spice.

SKILLS

PROGRAMMING

Verilog • C • MATLAB • Python (numpy, scikit-image, scikit-learn, tensorflow, openCV) • Assembly (MASM and DebugX) • Shell • Perl • HTML • CSS

SOFTWARE

ModelSIM • Cadence • iVerilog • LTSpice • Agilent ADS • NI LABVIEW • Simulink

EXTRA-CURRICULAR

2017-18 Chair (Operations), ACM Student Chapter, BITS Pilani
2017-18 Student Representative, Codechef Student Chapter, BITS Pilani

AWARDS

2013 National Talent Search Examination (NTSE) Scholar, Class X