Kshitij Khandelwal

About me

Webpage:	khandelwalkshitij.github.io
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email (Personal):	kshitijgokul@gmail.com | f2015156@pilani.bits-pilani.ac.in
interests:	• Hyperloop, Nanosatellites
	• Generative Adversarial Networks, Reinforcement Learning, Computer Vision
	• Speech Processing, Biomedical Signal Processing
	• Computer Architecture, Digital VLSI Design
languages:	• English (fluent) • French (basic knowledge) • Hindi (fluent) •Marathi (fluent)

Education

Current Aug '15 - Jul '19 (Exp.)	BE. (Hons.) in Electrical and Electronics Engineering **Birla Institute of Technology and Science, Pilani**, Pilani, India CGPA *8.61/10* (Semester IV)

University Coursework

Electrical Engineering	Electronics Engineering (Analog)	Electronics Engineering (Digital)
Electrical Sciences	Electronic Devices	Digital Design
Electrical Machines	Micro-electronic Circuits	Computer Programming
Control Systems	Analog VLSI Design	Microprocessors and Interfacing
Neural Networks and Fuzzy Logic	Analog Electronics (Ongoing)	Computer Architecture
Power Systems (Ongoing)	Power Electronics (Ongoing)	Digital VLSI Design

Communications Engineering	Mathematics	Sciences
Signals and Systems	Multivariate Calculus & Vector Fields	Principles of Economics
Communication Systems	Probability & Statistics	Mechanics, Oscillations & Waves
Digital Signal Processing	Linear Algebra & Complex Analysis	General Chemistry
	Differential Equations	General Biology
	Optimization	Thermodynamics

Independent Coursework (Online)

Completed
Neural Networks for Machine Learning	Geoffrey Hinton, University of Toronto
Reinforcement Learning	David Silver, University College London

Ongiong
CS231n: Convolutinal Neural Networks	Stanford University
Deep Learning for NLP	Oxford University

Work Experience

Current Apr '17	Control Systems Engineer at Hyperloop India, India Worked on Control Algorithm for Braking and Trajectory of the OrcaPod. Current work involves developing the EM Model for Braking. Hyperloop India is the only Indian team and one of the only 24 University teams worldwide to have presented their Pod at **SpaceX Competition Weekend II, 2017 in Los Angeles, CA.** Hyperloop India is currently working towards the SpaceX Competition Weekend III, 2018.
May - Jul '17	Summer Research Intern at Solid State Physics Laboratory (SSPL - DRDO), New Delhi, India Worked on designing Microstrip Filters for RF Applications. Designed, simulated and optimized a L-Band Microstrip Low Pass Filter using Agilent ADS.

PROJECTS

Current DEC '17	**Satellite Image Super-Resolution Using GANs** *Independent, BITS Pilani, India* The Project aims at testing the SR-GAN method for Image Super Resolution on the LANDSAT-7 Satellite Imagery Dataset using Generative Adversarial Networks and thereby develop a computationally efficient technique for Satellite Image Super-resolution
OCT - NOV '17	**LPC for Formant Analysis of Concurrent Vowels** *Course Project (Digital Signal Processing), BITS Pilani, India* The project focuses on understanding the effects of noise on the formant representations of both single and concurrent vowels and using Linear Predictive Coding (LPC) and Speech Spectrum Shaped Noise. Further, an attempt was made to understand which vowels (both single and concurrent) are more susceptible to noise. (Github)
OCT - NOV '17	**Actor-Critic Model for Playing Atari Games** *Course Project (Neural Networks & Fuzzy Logic), BITS Pilani, India* The project focuses on developing a comparison between using Actor-Critic Models and Generative Adversarial Networks for learning to play Atari Games. The games used for this purpose were Open-AI Gym's Cartpole-V0 and Lunar Lander.
OCT - NOV '17	**Design of a High Gain Two Stage Telescopic Operational Amplifier** *Course Project (Analog & Digital VLSI Design), BITS Pilani, India* The project involved designing a high gain two stage telescopic operational amplifier with a phase margin of 60 degrees, ICMR from 0.9V to 2.2V for a VDD of 2.5V and a 3 dB bandwidth of 100 KHz. The project was completed in LT Spice.
MAY - JUL '17	**Design of Low-Pass Microstrip L-Band Filter** *Internship Project, Solid State Physics Laboratory (SSPL), Defence Research & Development Organization (DRDO), New Delhi, India* The Project was towards the fulfillment of a summer research internship at SSPL-DRDO. It involved design of an optimum L-Band Low-Pass Filter, EM Simulation, and fault-analysis of the same. (Certificate)
JAN - APR '17	**Soft Computing in Electromagnetics** *Study Project (Dr. Navneet Gupta), BITS Pilani, India* Optimization of Gain and Directivity of Microstrip Patch Antenna Arrays using Artificial Neural Networks and Bacterial Foraging Optimization. (Letter of Recommendation)

SKILLS

Programming Languages

• MATLAB • Embedded C • Verilog • Python (numpy, scikit-image, scikit-learn, tensorflow, openCV, pyGTK)
• Assembly (MASM and DebugX) • Shell • Perl • HTML • CSS • LaTeX

Software

• Cadence • Agilent ADS • LTSpice • iVerilog • NI LABVIEW • COMSOL Multiphysics

AFFILIATIONS

Current Aug '15 - Present	**Chair (Operations) at ACM STUDENT CHAPTER, BITS Pilani, India** • Won the Best Association for Computing Machinery (ACM) India Student Chapter Award, thrice in a row. • Supervised Special Interest Groups on Cryptography and Linux.
Current Aug '17 - Present	**Senior Student Representative at CODECHEF CAMPUS CHAPTER, BITS Pilani, India** • Re-established the inactive campus chapter. • Competitive Programming SIG
Aug '15 - Mar '16	**Teaching Volunteer at NATIONAL SERVICE SCHEME (NSS), BITS Pilani, India** • Volunteered for Junoon, a nation-wide sports meet for the specially-abled. • Volunteered to set-up the annual Blood Donation Camp, BITS Pilani.