Kshitij Khandelwal

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About me

Webpage:	khandelwalkshitij.github.io
Address:	GN 3116, BITS Pilani, Rajasthan - 333031
email:	kshitijgokul@gmail.com | f2015156@pilani.bits-pilani.ac.in
interests:	• Reinforcement Learning • Computer Vision • Digital Electronics • Computer Architecture
languages:	• English (fluent) • French (basic knowledge) • Hindi (fluent) • Marathi (fluent)
Date of Birth:	5-Oct-1997 (20 Years Old)
Phone:	(+91) 94218 81230

Education

Current
Aug '15 - Jul '19 (Exp.)

III Year, BE. (Hons.) in Electrical and Electronics Engineering
Birla Institute of Technology and Science, Pilani, Pilani, India
CGPA: *8.3/10*

University Coursework

Electrical Engineering
Electrical Sciences
Electrical Machines
Control Systems
Neural Networks and Fuzzy Logic
Power Systems (Ongoing)

Electronics Engineering (Analog)
Electronic Devices
Micro-electronic Circuits
Analog VLSI Design
Analog Electronics (Ongoing)
Power Electronics (Ongoing)

Electronics Engineering (Digital)
Digital Design
Computer Programming
Microprocessors and Interfacing
Computer Architecture
Digital VLSI Design

Communications Engineering
Signals and Systems
Communication Systems
Digital Signal Processing

Mathematics
Multivariate Calculus & Vector Fields
Probability & Statistics
Linear Algebra & Complex Analysis
Differential Equations
Optimization

Physics
Mechanics, Oscillatinos & Waves
Theory of Relativity (Ongoing)
Introductory Astronomy (Ongoing)
Introductory Astrophysics (Ongoing)
Quantum Info. Theory (Ongiong)

Independent Coursework (Online)

Completed	**Neural Networks for Machine Learning**	Geoffrey Hinton, University of Toronto
	Reinforcement Learning	David Silver, University College London
Ongiong	**CS231n: Convolutinal Neural Networks**	Stanford University
	Deep Learning for NLP	Oxford University

Work Experience

Current
Jan '18

Teaching Assistant for EEE F244 - Microelectronic Circuits, BITS Pilani, India

Teaching Assistant for the Microelectronic Circuits course for the Spring 17-18 being taught by Dr. Anu Gupta, Professor, Department of Electrical & Electronics Engineering, BITS Pilani. Tasks involve training a batch of 150+ students in the use of LT Spice Simulation.

Apr '17 - Feb '18

Control Systems Engineer at Hyperloop India, India

Designed the pneumatically actuated permanent magnetic linear eddy braking system for team's current Hyperloop pod. Worked on Control Algorithm for Braking and Trajectory of the OrcaPod. Developed the EM Model for Braking. Hyperloop India is the only Indian team and one of the only 24 University teams worldwide to have presented their Pod at **SpaceX Competition Weekend II, 2017 in Los Angeles, CA.**

May '17 - Jul '17

Research Intern at Solid State Physics Laboratory (SSPL - DRDO), New Delhi, India

Worked on designing Microstrip Filters for RF Applications. Designed, simulated and optimized a L-Band Microstrip Low Pass Filter using Agilent ADS.

Projects

Current / Dec '17 — Satellite Image Super-Resolution Using GANs
Independent, BITS Pilani, India
The Project aims at testing the SR-GAN method for Image Super Resolution on the LANDSAT-7 Satellite Imagery Dataset using Generative Adversarial Networks and thereby develop a computationally efficient technique for Satellite Image Super-resolution

Oct - Nov '17 — LPC for Formant Analysis of Concurrent Vowels
Course Project (Digital Signal Processing), BITS Pilani, India
The project focuses on understanding the effects of noise on the formant representations of both single and concurrent vowels and using Linear Predictive Coding (LPC) and Speech Spectrum Shaped Noise. Further, an attempt was made to understand which vowels (both single and concurrent) are more susceptible to noise. (Github)

Oct - Nov '17 — Actor-Critic Model for Playing Atari Games
Course Project (Neural Networks & Fuzzy Logic), BITS Pilani, India
The project focuses on developing a comparison between using Actor-Critic Models and Generative Adversarial Networks for learning to play Atari Games. The games used for this purpose were Open-AI Gym's Cartpole-V0 and Lunar Lander.

Oct - Nov '17 — Design of a High Gain Two Stage Telescopic Operational Amplifier
Course Project (Analog & Digital VLSI Design), BITS Pilani, India
The project involved designing a high gain two stage telescopic operational amplifier with a phase margin of 60 degrees, ICMR from 0.9V to 2.2V for a VDD of 2.5V and a 3 dB bandwidth of 100 KHz. The project was completed in LT Spice.

May - Jul '17 — Design of Low-Pass Microstrip L-Band Filter
Internship Project, Solid State Physics Laboratory (SSPL), Defence Research & Development Organization (DRDO), New Delhi, India
The Project was towards the fulfillment of a summer research internship at SSPL-DRDO. It involved design of an optimum L-Band Low-Pass Filter, EM Simulation, and fault-analysis of the same. (Certificate)

Jan - Apr '17 — Soft Computing in Electromagnetics
Study Project (Dr. Navneet Gupta), BITS Pilani, India
Optimization of Gain and Directivity of Microstrip Patch Antenna Arrays using Artificial Neural Networks and Bacterial Foraging Optimization. (Letter of Recommendation)

Skills

Programming • MATLAB • C++ • Verilog • Python (numpy, scikit-image, scikit-learn, tensorflow, openCV) • Assembly (MASM and DebugX) • Shell • Perl • HTML • CSS

Software • Cadence • Agilent ADS • LTSpice • Simulink • iVerilog • NI LABVIEW • COMSOL Multiphysics

Affiliations

Current / Aug '15 - Present — Chair (Operations) at ACM Student Chapter, BITS Pilani, India
• Won the Best Association for Computing Machinery (ACM) India Student Chapter Award, thrice in a row. • Supervised Special Interest Groups on Cryptography and Linux.

Current / Aug '17 - Present — Senior Student Representative at Codechef Campus Chapter, BITS Pilani, India
• Re-established the inactive campus chapter. • Competitive Programming SIG

Aug '15 - Mar '16 — Teaching Volunteer at National Service Scheme (NSS), BITS Pilani, India
• Volunteered for Junoon, a nation-wide sports meet for the specially-abled. • Volunteered to set-up the annual Blood Donation Camp, BITS Pilani.