# Kshitij Khandelwal

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## EDUCATION

### BIRLA INSTITUTE OF TECHNOLOGY AND SCIENCE (BITS), PILANI

BE (Hons) in Electrical and Electronics Engineering
Aug 2015 - Jul 2019 (Expected)
Pilani, Rajasthan, India
CGPA: 8.61/10

Class XII (Maharashtra Board)
Shri Dawale Jr. College, Akola, India
Score: 93.08/100
Grad: May 2015

Class X (Maharashtra Board)
Mount Carmel High School, Akola, India
Score: 97.82/100
Grad: May 2013

## COURSEWORK

Electronic Devices
Microelectronic Circuits
Analog & Digital VLSI Design
Signals & Systems
Communication Systems
Digital Signal Processing

Computer Programming
Digital Design
Microprocessors & Interfacing
Computer Architecture

Electrical Sciences
Electromagnetic Theory
Electrical Machines
Control Systems
Neural Networks & Fuzzy Logic

## ADDRESS

3116, Gandhi Bhawan,
BITS Pilani, Pilani Campus
Pilani, Rajasthan, India
PIN: 333031

University Webpage:// **f2015156**
LinkedIn:// **khandelwalkshitij**
Github:// **khandelwalkshitij**
Medium:// **@khandelwal**
Twitter:// **@utopianflaws**

## EXPERIENCE

### DRDO - SOLID STATE PHYSICS LABORATORY (SSPL)

Summer Research Intern
MAY 2017 – JUL 2017 | New Delhi, India

- Worked on designing Microstrip Filters for RF Applications.
- Designed, simulated and optimized a L-Band Microstrip Low Pass Filter using ADS.

### HYPERLOOP INDIA

Contrl Systems Engineer
APR 2017 – PRESENT | Pilani, India | Bengaluru, India

- Worked on Control Algorithm for Braking and Trajectory of the OrcaPod.
- Working on Fuzzy Controller based solution for optimizing the Control Algorithm for Braking and Trajectory of the OrcaPod.
- Hyperloop India is the only Indian team and one of the only 24 University teams worldwide to have presented their Pod at SpaceX Competition Weekend II, 2017 in Los Angeles, CA.

## PROJECTS

### SOFT COMPUTING IN ELECTROMAGNETICS

Study Project, BITS Pilani
JAN 2017 – May 2017 | Pilani, India
Study Project under Dr. Navneet Gupta, Head, Department of Electrical and Electronics Engineering, BITS Pilani on Optimization of Gain and Directivity of Microstrip Patch Antenna Arrays using Artificial Neural Networks and Bacterial Foraging Optimization.

### DESIGN AND OPTIMIZATION OF L-BAND MICROSTRIP LOW PASS FILTER

Summer Research Intern, DRDO - SSPL
MAY 2017 – JUL 2017 | New Delhi, India
Worked under Mr. Pritam Kr. Sinha, Scientist 'C', SSPL, DRDO to design, simulate and optimize a L-Band Microstrip Lowpass filter.

## SKILLS

### PROGRAMMING

MATLAB • C • Verilog • Python (numpy, scikit-image, scikit-learn, tensorflow, openCV) • Assembly (MASM and DebugX) • Shell • Perl • HTML • CSS

### SOFTWARE

Cadence • Agilent ADS • LTSpice • iVerilog • NI LABVIEW

## EXTRA-CURRICULAR

2017-18 Chair (Operations), ACM Student Chapter, BITS Pilani
2017-18 Student Representative, Codechef Student Chapter, BITS Pilani
2015-17 Core Team Member, ACM Student Chapter, BITS Pilani
2015-16 Teaching Volunteer, National Service Scheme

## AWARDS

2013 National Talent Search Examination (NTSE) Scholar, Class X
2011 National Talent Search Examination (NTSE) Scholar, Class VIII