

Portland State Aerospace Society

C3 Board

(Command, Control, Communications)

Test Plan, Homework #6

T05 CubeSat C3

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Revision History

Revision	Date	Changes	Authors
1.00	11/21/2015	Initial Release	Shan Quinney
1.01	11/22/2015	RF tests	Shan Quinney, Jake Heath
1.02	11/23/15	JTAG test	Saroj Bardewa
1.03	11/24/2015	GPIO test	Saroj Bardewa

1.0 Introduction

1.1 Purpose

The purpose of this document is to outline a comprehensive test plan for the first version of the CubeSat C3 project. The test plan is intended to be as complete as possible, but with an understanding that all test vectors cannot be possibly covered. There are however four crucial tests that are covered in detail.

1.2 Testing procedure

The members of the team will carry out all of the tests described in this document. An effort will be made to have the entire group present for as many of the tests as possible. This should include the initial power-up of the board and various low-level tests such as measuring the expected voltages at pre-defined nodes and various current levels where applicable. Individual members or smaller groups of the team will likely conduct the functional unit/module tests, as well as, the integration tests.

The entire group will be present to conduct the complete system test. As a note, all of the test results will be documented and displayed on the team's wiki located here: <https://github.com/wrh2/ECE411/wiki>

1.3 Recording of Results, Witnessing, and Authorities

The results of all testing conducted in this test plan will be displayed on the project wiki. The tests will be conducted on a pass/fail basis and any tests that do not pass will be noted in the documentation with an explanation as to why they did not pass. No authorities or witnesses outside of the group will be required to be present during testing.

2.0 Reference Documents

2.1 Design Documentation

The level 1 diagram for the project is displayed above. Here, the main units or modules of the board are displayed along with interconnections between modules. Each module will be given a functional unit test to verify functionality. Interface tests will be conducted to test the interface between adjacent modules.

Note: Other important reference information can be found at the team wiki.

3.0 Overview

3.1 Operational Description

This project has been formed for the Portland State Aerospace Society (PSAS) to build a working communication “break out” board that will be used to communicate between a future ground station and CubeSat satellite. The “break out” capabilities of the board will allow the ground station to communicate via radio to the satellite and have access to features such as UART, I2C, SPI, GPIO, and ADC/DAC. The RF frequency of interest is 436.5 MHz, which falls into the amateur satellite 70 cm radio frequency band. We will demonstrate the radio communication of our system by turning on an LED via RF communication from one board to another.

3.2 Definition of Terminology

70 cm RF band – generally 420 MHz to 450 MHz Regulated by the FCC.
435 MHz to 438 MHz is used for amateur satellite communication

4.0 Pre-test Preparation

4.1 Test Equipment

The equipment needed for the tests is as follows:

- Multimeter
- JTAG connector
- Oscilloscope
- USB to micro-USB cable
- Logic analyzer

4.2 Test Setup and Calibration

Four of the tests listed in this document will contain detailed test case descriptions and documentation. The rest of the tests will include the necessary equipment needed to complete the test and the expected result of the test.

5.0 System Tests

5.1 Module Tests

5.1.1 Power System

5.1.1.1 Battery charger

To test that the battery charger is properly supplying power to the voltage regulator, the following tests can be performed.

If there is a USB connection on the USB port, a voltage of 4.5V – 5.5 V, as specified in the USB protocol, should be measured at the input of the battery charger. The same voltage should be measured at the output of the battery charger.

If the USB connection is absent and the battery is connected, a voltage of approximately 0V should be measured at the input of the battery charger. The voltage of the battery should be measured at the output of the battery charger.

If the USB connection and the battery are both absent, a voltage of 0V should be measured at the output of the battery charger.

If the USB connection and the battery are both present, a voltage of 4.5V – 5.5V should be measured at the input of the battery charger. The output of voltage on the battery charger should be the same.

To test that the battery charger is properly charging the battery, the following test can be performed.

Drain the battery as much as possible and then connect it to the device with a USB connection present. The battery voltage should gradually rise over time. The charger current configuration for the battery charger is 200mA so charge time may be long for the 1000mAh battery.

5.1.1.2 Voltage regulator

To test that the voltage regulator is receiving power from either the battery (if connected) or the USB port, the following tests can be performed.

If there is a USB connection on the USB port, a voltage of 4.5V – 5.5 V, as specified in the USB protocol, should be measured at the input of the regulator. A voltage of 3.3V should be measured at the output of the regulator.

If the USB connection is absent and the battery is connected, a voltage of approximately 3.7V should be measured at the input of the regulator. A voltage of the 3.3V should be measured at the output of the regulator.

If the USB connection and the battery are both absent, a voltage of 0V should be measured at the input of the regulator.

If the USB connection and the battery are both present, the USB power overrides the battery power and a voltage of 4.5V – 5.5V should be measured at the input of the regulator. The output of voltage on the regulator should still be 3.3V

The maximum current output of the regulator is 500mA regardless of the input voltage. All measurements should be made using a multimeter.

5.1.2 USB2UART

To test the power to the USB2UART chip, the following test can be performed.

Plug in a USB connection to the device and measure the voltage of the RGIN pin. It should be 4.5V – 5.5V. The voltage on the VDD pin should be 3.3V. There are test points on the PCB to accommodate this test.

To test the functionality of the USB2UART chip, the following test can be performed.

Connect a logic analyzer to the RX and TX lines on the chip, and have a USB connection present. Send a byte via USB and observe that byte with the logic analyzer.

5.1.3 GPIO

To test the functionality of GPIO, selective testing should be performed. Compile and upload code via JTAG to the MCU flash that makes a couple of pins on each port of the MCU have a 3.3V voltage signal.

5.1.4 JTAG

Test that the JTAG unit is able to talk to the board. To test this module, use JTAG to obtain the MCU Device ID which should be 0x2E2A2A2.

5.1.5 MCU

Test the voltage at the test points connected at the MCU unit. We expect the voltage reading at the power trace points connected to MCU to be about 3.3V. Having this voltage will indicate the MCU is able to power up properly.

Also, through the JTAG, and GPIO tests, we will be able to further test MCU module.

5.1.6 RF Front End

Test the s21 parameter of the front end. Here, we expect to have a pass band capable of passing our 436.5 MHz signal. Do to the nature of the passive network and large pass band of our filter, we expect to see some s21 loss at 436.5 MHz. Previous testing has shown that approximately 1dB loss or less is achievable. Note: this is not a finite test. We are simply testing to see how well our filter behaves based on expected results and previous modular tests. We will be able to adjust component values if necessary to improve these results.

We expect to attenuate the 2nd harmonic by 40dB or more.

By connecting the network analyzer to the SMA connector on the main board we will be able to test the s21 parameter. The VNA will need to be calibrated using the calibration kit in the lab. This calibration will include the proper frequency range needed for our signal. A useful range will be to set the minimum frequency to 100 MHz and the maximum frequency to 1GHz. This will allow us to measure the response of the filter of our desired 436.5 MHz signal and the 2nd harmonic of this signal.

Test Writer:		Shan Quinney				
Test Case Name:		RF Front End	Test ID#:		RFFE	
Description:		The purpose of this test is to measure the frequency response of the RF filter.	Box Type:		white box black box	
Tester Information						
Name of Tester:			Date:			
Hardware Version:		Board Rev.1, Filter Rev.1	Time:			
Setup:			Calibrate the VNA to give a 2-port response reading. The frequency range of interest is from 100 MHz to 1 GHz. Attach one end of the SMA cable to the VNA. Attach the other end of the SMA cable to the SMA connector of the board.			
Step	Action	Expected Result	Pass	Fail	N/A	Comments
1	Use the cursor to locate the 436.5 MHz frequency of interest.	The 436.5 MHz frequency falls within the pass band of the filter. Make a comment on the s21 parameter reading.				
2	Use a second cursor to locate the 2 nd harmonic of the frequency of interest. This should be 873 MHz.	The 873 MHz frequency is attenuated by 40dB below the fundamental frequency. Make a comment on the s21 parameter reading.				
Overall Test Result:						

5.1.7 RF Antenna

Test the antenna's ability to transfer data over the intended RF band at a specified distance. Here, we expect to have a signal transmitted and received from both boards in the 436.5MHz range over the distance of about 5-6 meters. The antenna length will then be altered based on the strength of the signal and its ability to stay within the range of our intended frequency. Note: this is not a finite test. We are simply testing to see how well the antenna behaves based on expected results and previous modular tests.

We can perform this test using the network analyzer to determine the frequency range and gain of our antennas directly, and then perform another test to confirm that the boards are capable of communication with each other once we've confirmed their length with the VNA. The second test will likely have to wait until the firmware for the board is developed to send a ping and will likely be one of the final tests of the project.

Test Writer:				James Heath			
Test Case Name:		RF Antenna		Test ID#:		RFANT	
Description:		The purpose of this test is to measure the antenna’s communication capability.		Box Type:		white box black box	
Tester Information							
Name of Tester:				Date:			
Hardware Version:		Board Rev.1, Filter Rev.1, Wire antenna		Time:			
Setup:				Calibrate the VNA to give a 2-port response reading. The frequency range of interest is form 100 MHz to 1 GHz. Attach one end of the VNA cable to a SMA connector and test the antenna’s frequency range. Once frequency range is confirmed, we can confirm communication between the boards through direct testing between the boards.			
Step	Action	Expected Result	Pass	Fail	N/A	Comments	

1	Use the cursor to locate the 436.5 MHz frequency of interest.	The 436.5 MHz frequency falls near the middle of the passband in for the antenna. Also gain should be decent enough to send signal at least 6 meters.				
2	Perform the same test on the other board.	The 436.5 MHz frequency falls near the middle of the passband in for the antenna. Make a comment on the s21 parameter reading.				
3	Test Board communication via ping signal	Once the ping is received the receiver board LED should light up indicating a received signal.				
4	Test Board communication for other board	Once the ping is received the receiver board LED should light up indicating a received signal.				
Overall Test Result:						

5.2 Interface Tests

5.2.1 RF Front End to Integrated Transceiver

Test the functionality of the integrated PA. This test will need to be performed in steps where the PA's power is increased in incremental steps so that the result can be carefully measured. The data sheet states that a maximum of 13dBm is achievable with this setup.

The s11 parameter will test how well the impedance of the front-end matches the impedance of the transceiver. In previous tests we have been able to achieve approximately 90% match to the desired 50 ohm. Note: We may be able to achieve a better impedance match by alternating some of the component values in the filter. This will be an iterative process and will include both documentation and test results.

5.2.2 JTAG to MCU

Test the interface between JTAG and MCU. We will connect JTAG header to the board, which will be our main channel to communicate to MCU unit. The tri-colored LEDs on the board should light up when JTAG is connected. This will further indicate that MCU is able to detect the connection of JTAG.

Test Writer:			Saroj Bardewa				
Test Case Name:		JTAG interface		Test ID#:		RFFE	
Description:		The purpose of this test is to check that there is connection between JTAG and MCU		Box Type:		white box black box	
Tester Information							
Name of Tester:				Date:			
Hardware Version:		Board Rev.1, JTAG Rev.1		Time:			
Setup:				Power up the C3 board. Plug in the JTAG cable on the board			
Step	Action	Expected Result	Pass	Fail	N/A	Comments	
1	Reset the device	This should bring the board to a known initial state indicated by blinking of tri-colored LEDs.					
2	Probe for the device ID	This should return the device ID to the host computer.					
Overall Test Result:							

5.2.3 MCU to GPIO

Test the interface between MCU and GPIO. Here we will write, compile and feed in C code to make the signal on some selected GPIO pins go high. We will use a multimeter to check the voltage level at those pins. Having a high voltage level on the signal will indicate that the interface between MCU and the GPIO pin is properly setup.

Test Writer:			Saroj Bardewa			
Test Case Name:		GPIO connection		Test ID#:		CST
Description:		The main purpose of this test is to examine the interface between GPIO and MCU		Box Type:		white box black box
Tester Information						
Name of Tester:				Date:		
Hardware Version:		Board Rev.1, JTAG Rev.1		Time:		
Setup:				Connect C3 board on a computer via a JTAG. Compile commands for MCU in the computer and feed in through the JTAG connection. In the C code, use the following algorithm to test JTAG to MCU interface.		
Step	Action	Expected Result	Pass	Fail	N/A	Comments
1	Read 0x400F_F088 register	We expect to read the content of Port Clear Output register (GPIOC_PCOR).				

2	Write 0x2h to 0x400F_F088 register	We expect to reset the PTC1 port through this operation				
3	Read 0x400F_F090 register	It should give us a pointer to the beginning of Port Data Direction Register (GPIOC_PDDR)				
4	Write 0x2h to 0x400F_F090 register	Writing 0x2h to GPIOC_PDDR register should set PTC1 port as an output internally.				
5	Read 0x400F_F084 Register	It should give us an access to read the content of Port Set Output Register (GPIOC_PSOR).				
6	Write 0x2h to 0x400F_F084 Register	This action should set the content of PTC1 pin go high				

7	Read 0x4000F_F080 register	This operation should set a pointer to the beginning of Port Data Output Register (GPIOC_P DOR)				
8	Write 0x2h to 0x4000F_F080	This operation should set the output of PTC1 pin go high. We should be able to measure 3.3 V on the PTC1 port using a multimeter after this operation.				
Overall Test Result:						

5.3 Complete System Test

Test the ability to send a RF signal from one board to another to turn on an LED.
This test will be conducted after all of the other test have been successfully tested.