**CUBESAT C3 Board**



Test Plan, Homework #6

T05 CubeSat Radio

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**Table of Contents**

**Revision History 2**

**1.0 INTRODUCTION 2**

**1.1 This Document 2**

**1.2 Conduct of System Tests 2**

**1.3 Recordings of Results, witnessing, and Authorities 2**

**2.0 REFERENCE DOCUMENTS 3**

**2.1 Design Documentation 3**

**3.0 CUBESAT RADIO OVERVIEW 4**

**3.1 Operational Description 4**

**3.2 Definition of Terminology 4**

**3.3 Computational Methods 4**

**4.0 PRETEST PREPERATION 4**

**4.1 Test Equipment 4**

**4.2 Test Setup and Calibration 4**

**5.0 SYSTEM TESTS 4**

**5.1 Module Tests 4**

**5.1.1 Power Management Unit 4**

**5.1.1.1 Voltage Regulator 4**

**5.1.1.2 Battery sourced power 5**

**5.1.1.3 USB sourced power 5**

**5.1.2 USB2UART chip 5**

**5.1.3 GPIO 5**

**5.1.4 JTAG 5**

**5.1.5 MCU 5**

**5.1.6 RF Front End 5**

**5.1.7 RF Antenna 6**

**5.2 Interface Tests 7**

**5.2.1 RF Front End to Integrated Transceiver 7**

**5.2.2 JTAG to MCU 8**

**5.2.3 GPIO to MCU 8**

**5.2.4 USB to MCU 9**

**5.2.5 Voltage Regulator to MCU 9**

**5.2.6 Battery charger chip to Voltage Regulator 10**

**5.2.7 USB to UART 10**

**5.3 Complete System Test 10**

**Revision History**

|  |  |  |  |
| --- | --- | --- | --- |
| **Revision** | **Date** | **Changes** | **Authors** |
| 1.00 | 11/21/2015 | Initial Release | Shan Quinney |
| 1.01 | 11/22/2015 | RF tests | Shan Quinney, Jake Heath |
| 1.02 | 11/23/15 | JTAG test | Saroj Bardewa |
| 1.03 | 11/24/2015 | GPIO test | Saroj Bardewa |

**1.0 Introduction**

**1.1 Purpose of this document**

This text is intended as an exercise to demonstrate the effectiveness of the team to write a comprehensive test plan for the testing and evaluation of the team’s CubeSat Radio project. An effort is made to be as complete as possible, and at least four of these tests will include detailed test descriptions, as directed by the homework instructions.

**1.2 Conduct of System Tests**

The members of the team will carry out all of the tests described in this document. An effort will be made to have the entire group present for as many of the tests as is possible. This should include the initial power-up of the board and various low-level tests such as measuring the expected voltages at pre-defined nodes and various current levels where applicable. Individual members or smaller groups of the team will likely conduct the functional unit/module tests, as well as, the integration tests.

The entire group will be present to conduct the complete system test. As a note, all of the test results will be documented and displayed on the team’s wiki. ***Include link to wiki here.***

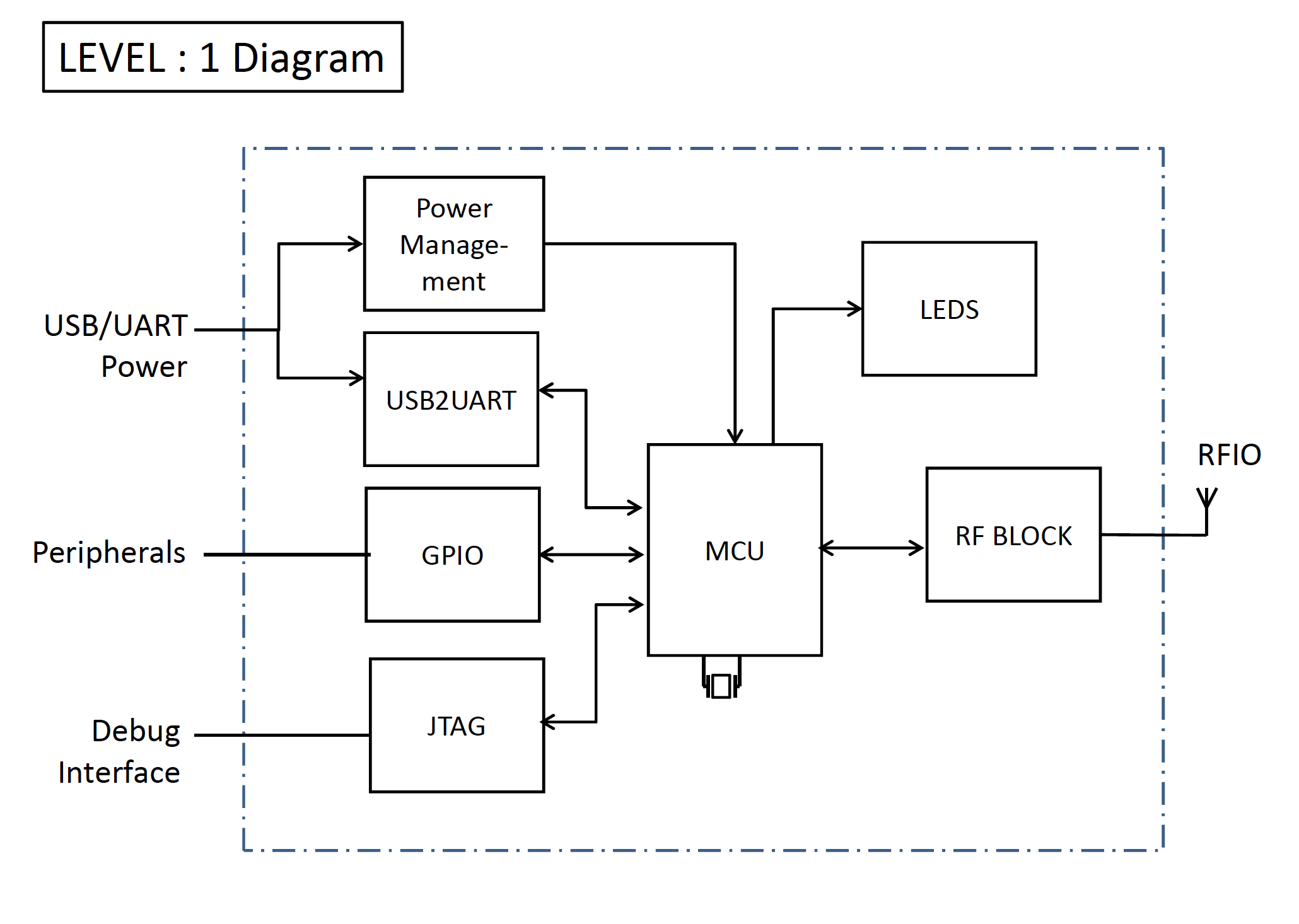
**1.3 Recording of Results, Witnessing, and Authorities**

The results of all testing conducted in this test plan will be displayed on the project wiki. The tests will be conducted on a pass/fail basis and any tests that do not pass will be noted in the documentation with an explanation as to why they did not pass.

No authorities or witnesses outside of the group will be required to be present during testing.

**2.0 Reference Documents**

**2.1 Design Documentation**

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The level 1 diagram for our project is displayed above. Here, the main units or modules of the board are displayed along with interconnections between modules. Each module will be given a functional unit test to verify functionality. Interface tests will be conducted to test the interface between adjacent modules.

*Note: Other important reference information can be found at the team wiki.*

**3.0 CubeSat Radio Project Overview**

**3.1 Operational Description**

This project has been formed on the desire for the Portland State Aerospace Society (PSAS) to build a working communication “break out” board that will be used to communicate between a future ground station and CubeSat satellite. The “break out” capabilities of the board will allow the ground station to communicate via radio to the satellite and have access to features such as UART, I2C, SPI, GPIO, and ADC/DAC. The RF frequency of interest is 436.5 MHz, which falls into to amateur satellite 70 cm radio frequency band. We will demonstrate the radio communication of our system by turning on an LED via RF communication from one board to another.

**3.2 Definition of Terminology**

70 cm RF band – generally 420 MHz to 450 MHz Regulated by the FCC.

435 MHz to 438 MHz is used for amateur satellite communication

**4.0 Pre-test Preparation**

**4.1 Test Equipment**

The equipment used for the tests in this document include:

* Multimeter
* JTAG connector
* Oscilloscope
* USB cable

**4.2 Test Setup and Calibration**

Four of the tests listed in this document will contain detailed test case descriptions and documentation. The rest of the tests will include the necessary equipment needed to complete the test and the expected result of the test.

**5.0 System Tests**

**5.1 Module Tests**

**5.1.1 Power Management**

**5.1.1.1 Voltage regulator**

Test that the voltage regulator is receiving power from either the battery (if connected) or the USB port. If the power is supplied from the USB port, we expect to measure approximately 4.5 VDC – 5.5 VDC at the input of the regulator. If the battery is supplying power (hence, the USB port is disconnected from a power source), we expect to measure a DC voltage in the range of approximately 3.7 V to 3.3V at the input of the voltage regulator.

The output of the regulator, regardless of input condition should be approximately 3.3 VDC. The maximum current output of the regulator is 500mA. All measurements are made using a multimeter.

**5.1.1.2 Battery sourced power**

Test the operation of the battery as a power source. Here, USB should be disconnected. The output of the battery is approximately 3.7VDC – 3.3VDC. This test will be conducted using a multimeter.

**5.1.1.3 USB sourced power**

Test that the board is capable of being powered while connected to USB. We will conduct two test; One with a battery attached to the board and another without a battery attached to the board. USB power should be measured between approximately 4.5 VDC and 5.5 VDC. Both tests will be conducted using a multimeter.

**5.1.2 USB2UART**

Test to examine if the chip powers up when a USB is connected. Here, we the full functionality of the subsystem will not be tested due to time constrain.

**5.1.3 GPIO**

Test the GPIO subsystem. Here, a selective testing will be performed where we will compile and upload code for a couple of pins on each port of the MCU that makes the voltage signal on those pins go high.

**5.1.4 JTAG**

Test that the JTAG unit is able to talk to the board. To test this module, code will be feed into the system using the JTAG connection for lighting the tri-colored LEDs that are placed on the board.

**5.1.5 MCU**

Test the voltage at the test points connected at the MCU unit. We expect the voltage reading at the power trace points connected to MCU to be about 3.3V. We will use a multimeter to test the voltage present at those. Having a voltage drop will indicate the MCU is able to power up properly.

Also, through the JTAG, and GPIO tests, we will be able to further test MCU module.

**5.1.6 RF Front End**

Test the s21 parameter of the front end. Here, we expect to have a pass band capable of passing our 436.5 MHz signal. Do to the nature of the passive network and large pass band of our filter, we expect to see some s21 loss at 436.5 MHz. Previous testing has shown that approximately 1dB loss or less is achievable. Note: this is not a finite test. We are simply testing to see how well our filter behaves basted on expected results and previous modular tests. We will be able to adjust component values if necessary to improve these results.

We expect to attenuate the 2nd harmonic by 40dB or more.

By connecting the network analyzer to the SMA connector on the main board we will be able to test the s21 parameter. The VNA will need to be calibrated using the calibration kit in the lab. This calibration will include the proper frequency range needed for our signal. A useful range will be to set the minimum frequency to 100 MHz and the maximum frequency to 1GHz. This will allow us to measure the response of the filter of our desired 436.5 MHz signal and the 2nd harmonic of this signal.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test Writer: | | Shan Quinney | | | | | |
| Test Case Name: | | RF Front End | | | | Test ID#: | RFFE |
| Description: | | The purpose of this test is to measure the frequency response of the RF filter. | | | | Box Type: | 🞎 white box  ✓ black box |
| Tester Information | |  | | | | | |
| Name of Tester: | |  | | | | Date: |  |
| Hardware Version: | | Board Rev.1, Filter Rev.1 | | | | Time: |  |
| Setup: | | Calibrate the VNA to give a 2-port response reading. The frequency range of interest is form 100 MHz to 1 GHz. Attach one end of the SMA cable to the VNA. Attach the other end of the SMA cable to the SMA connector of the board. | | | | | |
| Step | Action | Expected Result | Pass | Fail | N/A | Comments | |
| 1 | Use the cursor to locate the 436.5 MHz frequency of interest. | The 436.5 MHz frequency falls within the pass band of the filter. Make a comment on the s21 parameter reading. |  |  |  |  | |
| 2 | Use a second cursor to locate the 2nd harmonic of the frequency of interest. This should be 873 MHz. | The 873 MHz frequency is attenuated by 40dB bellow the fundamental frequency. Make a comment on the s21 parameter reading. |  |  |  |  | |
| Overall Test Result: | | |  |  |  |  | |

**5.1.7 RF Antenna**

Test the antenna’s ability to transfer data over the intended RF band at a specified distance. Here, we expect to have a signal transmitted and received from both boards in the 436.5MHz range over the distance of about 5-6 meters. The antenna length will then be altered based on the strength of the signal and its ability to stay within the range of our intended frequency. Note: this is not a finite test. We are simply testing to see how well the antenna behaves basted on expected results and previous modular tests.

We can perform this test using the network analyzer to determine the frequency range and gain of our antennas directly, and then perform another test to confirm that the boards are capable of communication with each other once we’ve confirmed their length with the VNA. The second test will likely have to wait until the firmware for the board is developed to send a ping and will likely be one of the final tests of the project.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test Writer: | | James Heath | | | | | |
| Test Case Name: | | RF Antenna | | | | Test ID#: | RFANT |
| Description: | | The purpose of this test is to measure the antenna’s communication capability. | | | | Box Type: | 🞎 white box  ✓ black box |
| Tester Information | |  | | | | | |
| Name of Tester: | |  | | | | Date: |  |
| Hardware Version: | | Board Rev.1, Filter Rev.1, Wire antenna | | | | Time: |  |
| Setup: | | Calibrate the VNA to give a 2-port response reading. The frequency range of interest is form 100 MHz to 1 GHz. Attach one end of the VNA cable to a SMA connector and test the antenna’s frequency range. Once frequency range is confirmed, we can confirm communication between the boards through direct testing between the boards. | | | | | |
| Step | Action | Expected Result | Pass | Fail | N/A | Comments | |
| 1 | Use the cursor to locate the 436.5 MHz frequency of interest. | The 436.5 MHz frequency falls near the middle of the passband in for the antenna. Also gain should be decent enough to send signal at least 6 meters. |  |  |  |  | |
| 2 | Perform the same test on the other board. | The 436.5 MHz frequency falls near the middle of the passband in for the antenna. Make a comment on the s21 parameter reading. |  |  |  |  | |
| 3 | Test Board communication via ping signal | Once the ping is received the receiver board LED should light up indicating a received signal. |  |  |  |  | |
| 4 | Test Board communication for other board | Once the ping is received the receiver board LED should light up indicating a received signal. |  |  |  |  | |
| Overall Test Result: | | |  |  |  |  | |

**5.2 Interface Tests**

**5.2.1 RF Front End to Integrated Transceiver**

Test the functionality of the integrated PA. This test will need to be performed in steps where the PA’s power is increased in incremental steps so that the result can be carefully measured. The data sheet states that a maximum of 17dBm is achievable with this setup.

The s11 parameter will test how well the impedance of the front-end matches the impedance of the transceiver. In previous tests we have been able to achieve approximately 90% match to the desired 50 ohm. Note: We may be able to achieve a better impedance match by alternating some of the component values in the filter. This will be an iterative process and will include both documentation and test results.

**5.2.2 JTAG to MCU**

Test the interface between JTAG and MCU. We will connect JTAG header to the board, which will be our main channel to communicate to MCU unit. The tri-colored LEDs on the board should light up when JTAG is connected. This will further indicate that MCU is able to detect the connection of JTAG.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Test Writer: | | Saroj Bardewa | | | | | |
| Test Case Name: | | JTAG interface | | | | Test ID#: | RFFE |
| Description: | | The purpose of this test is to check that there is connection between JTAG and MCU | | | | Box Type: | 🞎 white box  ✓ black box |
| Tester Information | |  | | | | | |
| Name of Tester: | |  | | | | Date: |  |
| Hardware Version: | | Board Rev.1, JTAG Rev.1 | | | | Time: |  |
| Setup: | | Power up the C3 board. Plug in the JTAG cable on the board | | | | | |
| Step | Action | Expected Result | Pass | Fail | N/A | Comments | |
| 1 | Reset the device | This should bring the board to a known initial state indicated by blinking of tri-colored LEDs. |  |  |  |  | |
| 2 | Probe for the device ID | This should return the device ID to the host computer. |  |  |  |  | |
| Overall Test Result: | | |  |  |  |  | |

**5.2.3 MCU to GPIO**

Test the interface between MCU and GPIO. Here we will write, compile and feed in C code to make the signal on some selected GPIO pins go high. We will use a multimeter to check the voltage level at those pins. Having a high voltage level on the signal will indicate that the interface between MCU and the GPIO pin is properly setup.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Test Writer: | | Saroj Bardewa | | | | | | | | |
| Test Case Name: | | GPIO connection | | | | | | Test ID#: | | CST |
| Description: | | The main purpose of this test is to examine the interface between GPIO and MCU | | | | | | Box Type: | | 🞎 white box  ✓ black box |
| Tester Information | |  | | | | | | | | |
| Name of Tester: | |  | | | | | | Date: | |  |
| Hardware Version: | | Board Rev.1, JTAG Rev.1 | | | | | | Time: | |  |
| Setup: | | Connect C3 board on a computer via a JTAG. Compile commands for MCU in the computer and feed in through the JTAG connection. In the C code, use the following algorithm to test JTAG to MCU interface. | | | | | | | | |
| Step | Action | Expected Result | Pass | | Fail | N/A | | Comments | | |
| 1 | Read 0x400F\_F088 register | We expect to read the content of Port Clear Output register (GPIOC\_PCOR). |  |  | | |  | |  | | |
| 2 | Write 0x2h to 0x400F\_F088 register | We expect to reset the PTC1 port through this operation |  |  | | |  | |  | | |
| 3 | Read 0x400F\_F090 register | It should give us a pointer to the beginning of Port Data Direction Register (GPIOC\_PDDR) |  |  | | |  | |  | | |
| 4 | Write 0x2h to  0x400F\_F090 register | Writing 0x2h to GPIOC\_PDDR register should set PTC1 port as an output internally. |  |  | | |  | |  | | |
| 5 | Read 0x400F\_F084  Register | It should give us an access to read the content of Port Set Output Register (GPIOC\_PSOR). |  |  | | |  | |  | | |
| 6 | Write 0x2h to 0x400F\_F084  Register | This action should set the content of PTC1 pin go high |  |  | | |  | |  | | |
| 7 | Read 0x4000F\_F080  register | This operation should set a pointer to the beginning of Port Data Output Register (GPIOC\_PDOR) |  |  | | |  | |  | | |
| 8 | Write 0x2h to 0x4000F\_F080 | This operation should set the output of PTC1 pin go high.  We should be able to measure 3.3 V on the PTC1 port using a multimeter after this operation. |  |  | | |  | |  | | |
| Overall Test Result: | | |  |  | | |  | |  | | |

**5.2.4 USB Power to Voltage Regulator**

Test that the interface between USB Power line and Voltage Regulator. We will connect USB and check its voltage output to the system at the test points placed on voltage regulator line. A high voltage reading (approx. 5 V) at the test points will indicate that USB system has a proper interface with voltage regulator.

**5.2.5 Voltage Regulator to MCU**

Test that the voltage between the regulator and MCU is maintained at approximately 3.3 VDC regardless of the power source. This test will include using both using the battery independently as a power source and the USB source to power the board. Either source will supply a voltage greater that the desired 3.3V that is required to power the MCU. We will use a multimeter to test the voltage at the MCU.

**5.2.6 Battery charger chip to Voltage Regulator**

Test the ability of the voltage regulator to properly function when receiving power from the battery charging unit. Here, we are interested in what the battery charging unit is outputting to the voltage regulator when a battery is connected to the board and when a battery is not connected to the board. The expected output of the battery charging unit will depend on the status of the battery (if present) and will fall in the range of (XVDC – YVDC). The

**5.2.7 USB to UART**

Test the interface between USB and UART. Depending on time, we will perform a basic test to examine the interface between USB to UART. We will connect USB from a computer to the board, and feed in C code to set up high voltage on some selective GPIO pins. The high voltage reading at those GPIO pin will show that the USB to UART interface is configured properly.

**5.3 Complete System Test**

Test the ability to send a RF signal from one board to another to turn on an LED. This test will be conducted after all of the other test have been successfully tested.