Soft-Error Resilient Network-on-Chip for Safety-Critical Applications

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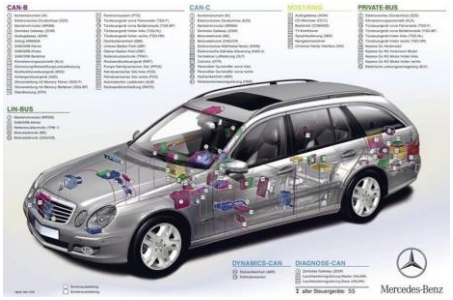
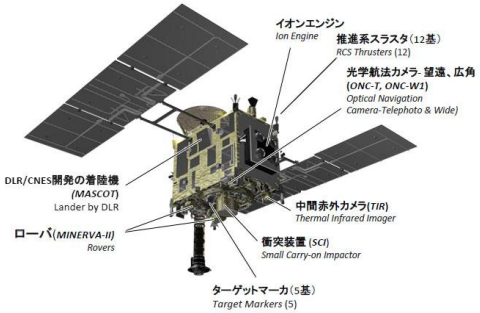
ASL

Era of Many-core: Safety-Critical Applications

- Hundreds of cores integrated on chip
  - Technology scaling
  - 3D integration
  - Examples:
    - STMicro P2012/STHORM
    - picoChip
    - Tilera Tile GX, Tile Pro
    - Scale-out
    - Intel Polari



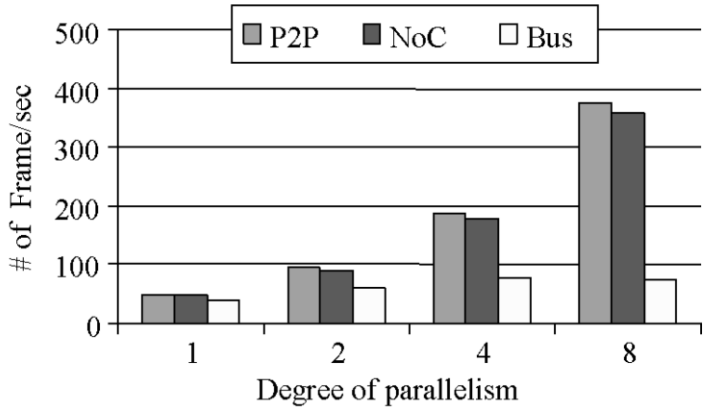


- Complex apps, stringent constraints
  - Massively parallel applications
    - Big-data analytics, graphics, augmented reality, communication etc.
  - Safety-critical applications:
    - Automotive, medical, government/military.
  - Performance, power, scalability, reliability are key challenges

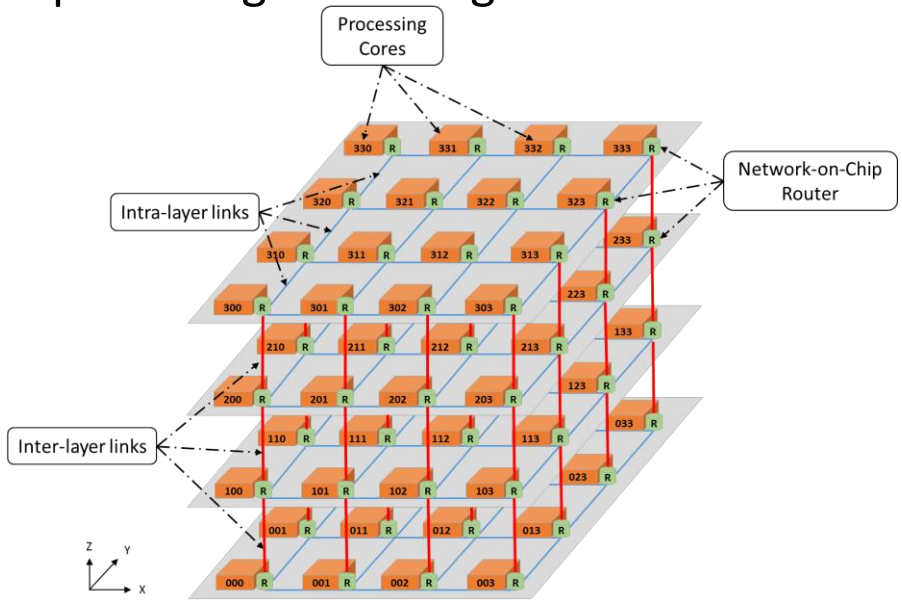
3D Network-on-Chip Paradigm

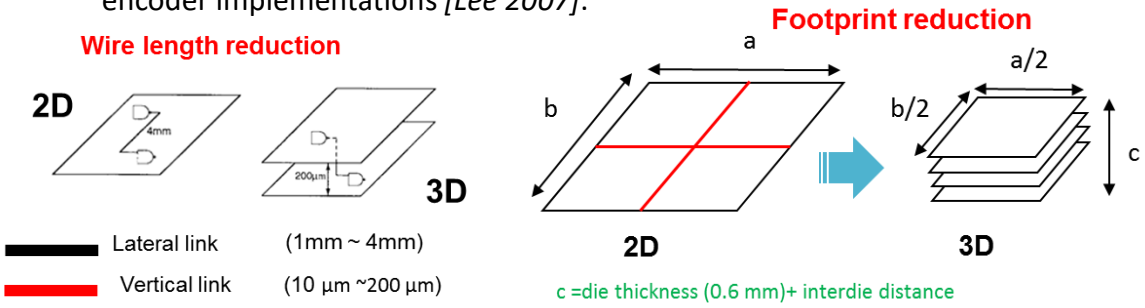
3D Network-on-Chip is the combination of two promising technologies:

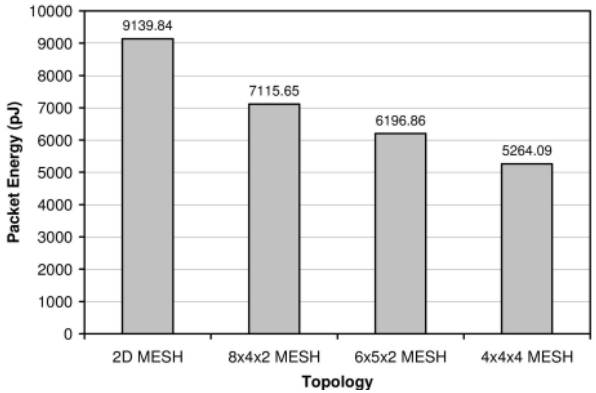
- 3D Integrated Circuit.
- Network-on-Chip.



Point-to-Point (P2P) vs NoC vs Bus: Throughput comparison of various MPEG-2 encoder implementations *[Lee 2007]*.



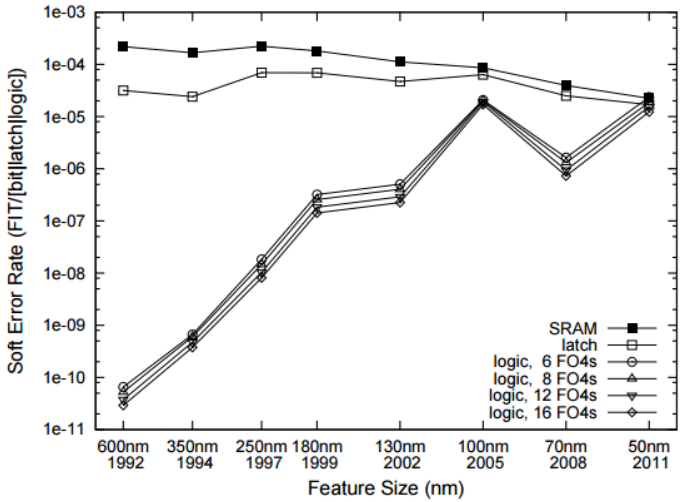




2D-NoC vs 3D-NoC *[Feero 2009]*

=> The 3D NoC paradigm can be the future of many-core era.

Soft Error Rates: Gate-Level and System Level



SER of a single SRAM cell/latch/logic chain for different feature sizes and pipeline depths *[Shivakumar 2002]* .

Tech. (nm)	*Relative SEU rate in FITs/kbit*	Approx. Mbits per microprocessor	Relative uncorrected SEU rate per microprocessor (kFIT)
250	3.2	1.52	5.0
180	3.0	1.52	4.3
130	2.4	3.28	7.9
90	1.0	33.6	33.6
65	0.7	44.3	30.5
40	0.94	71.0	67.0

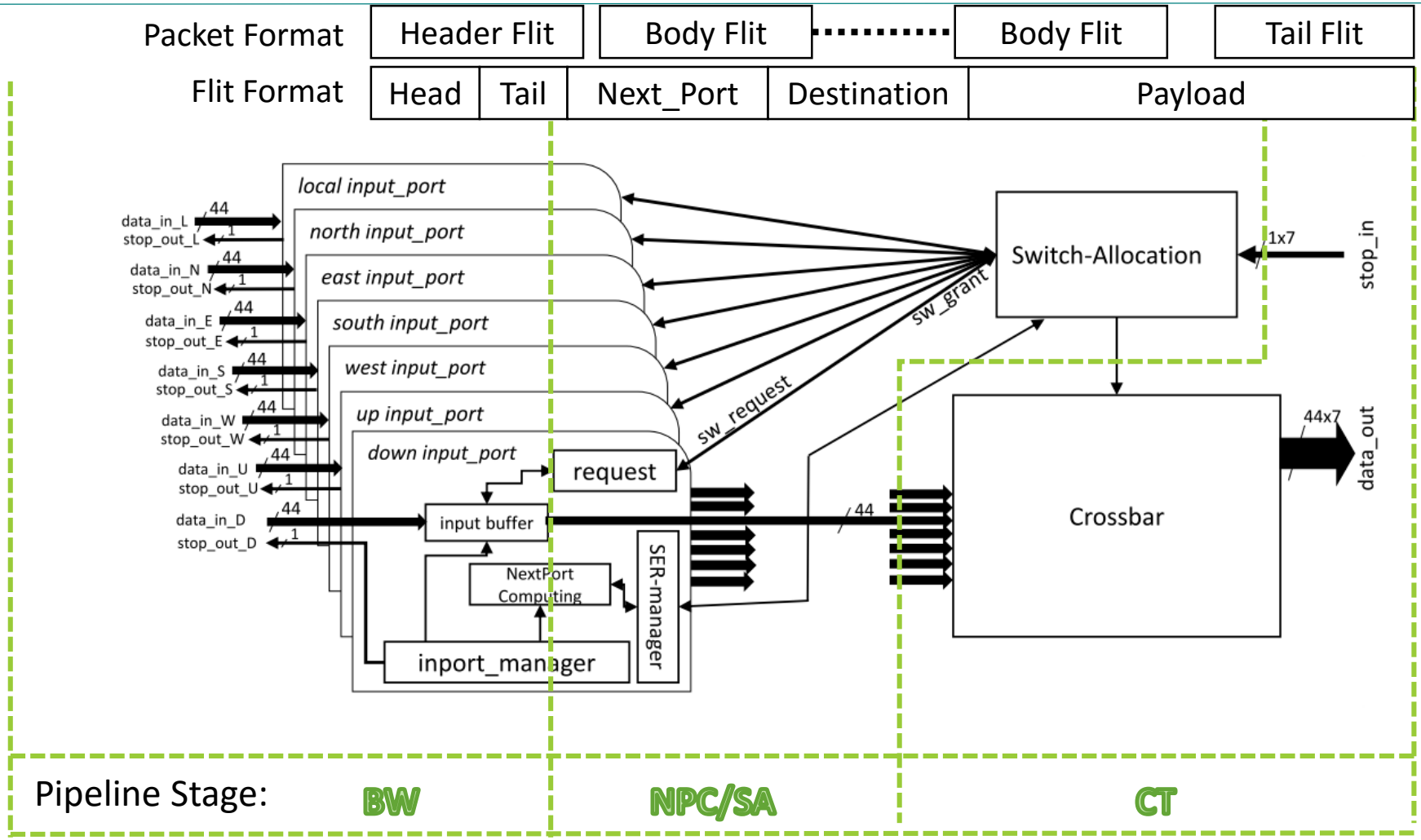
Raw SEU (single event upset) Rate Per Microprocessor *[Dixit 2011].*

Energy(MeV)	3.0	3.5	4.0	4.5	5.5	6.0	7.0	9.0	11.9
Particles	113816	57409	10885	12917	13804	15318	14772	14709	24428
Errors	0	23	378	652	537	491	488	407	254

Report on space research: The energies, the number of particles and the number of errors by Li ion irradiation to the 8 Mbits body-tie PD SOI-SRAM at 90nm technology *[Hazama 2013]*.

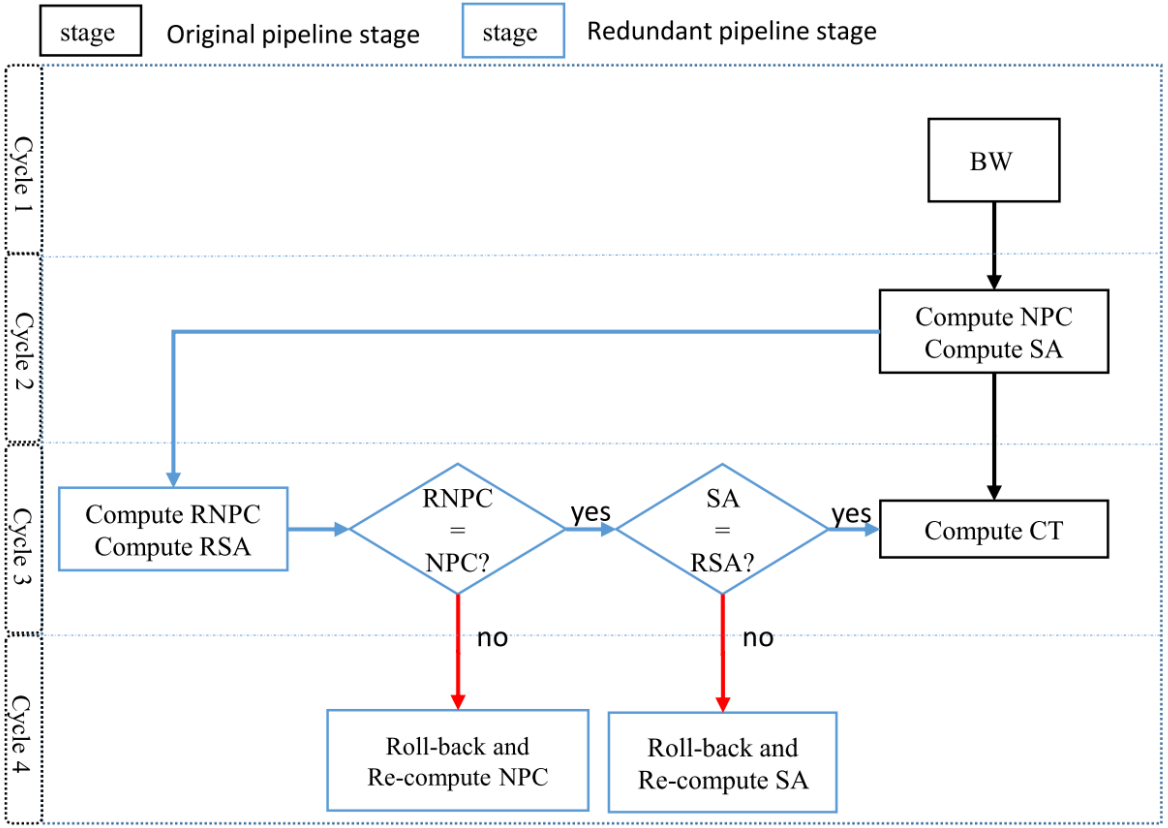
The future safety-critical applications need a sufficient technology to alleviate the increasing of soft errors impact!

Soft Error Resilient 3D-NoC Router Architecture



BW (Buffer-Writing): receives data and stores. **NPC (Next-Port-Computing)**: calculates the output port value. **SA (Switch-Allocation)**: arbitrates input ports → output ports. **CT (Crossbar-Traversal)**: routes data from input ports to output ports.

Pipeline of SER-3DR-NoC router

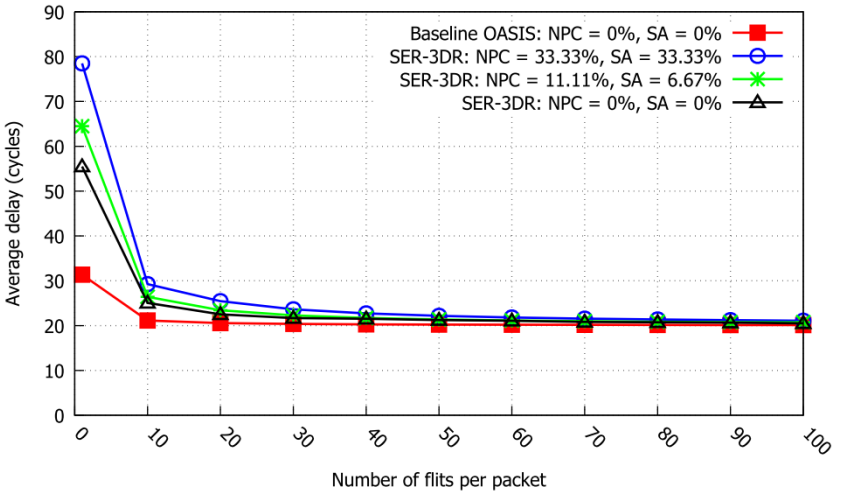


BW (Buffer-Writing): receive data and store.
NPC (Next Port Computing): calculate the outport value.
SA (Switch Allocation): arbitrating inports → outports.
CT (Crossbar Traversal): route data from inports to outports.
RNPC : redundant Next Port Computing.
RSA : redundant Switch Allocation.

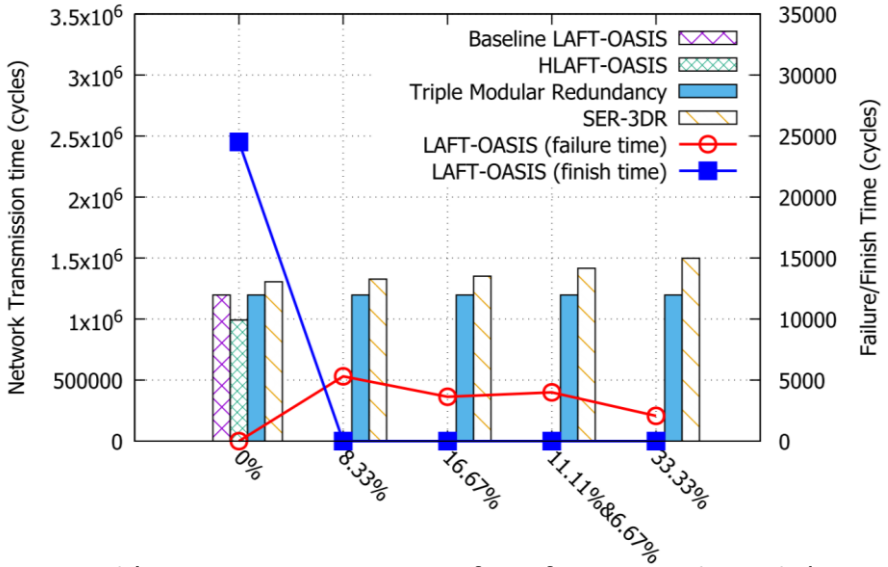
Case	*no fault*	*faulty NPC*	*faulty SA*	*faulty NPC&SA*
Solution	unchanged	correct NPC	correct SA	correct both
Cost *(cycle)*	0	1	1	1

Simulation Results

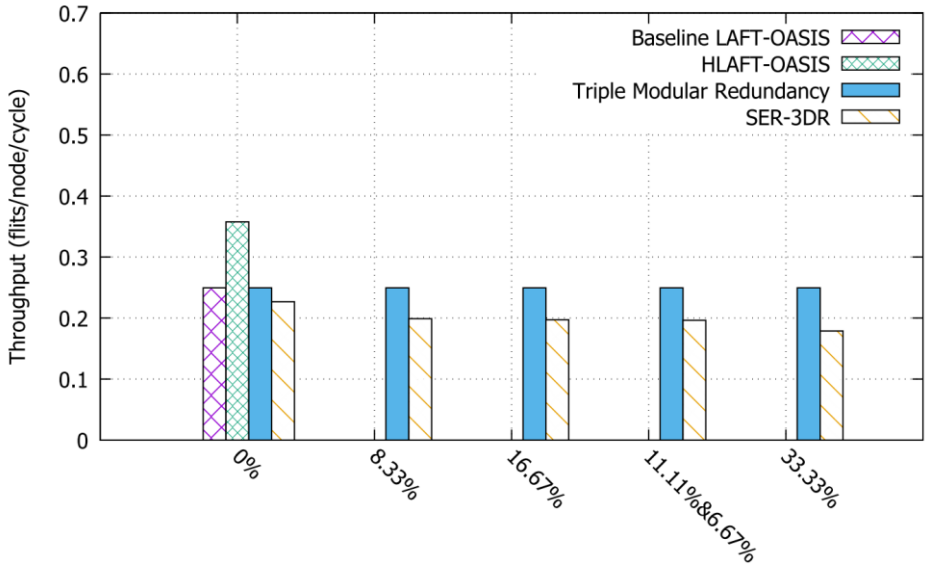
Architectures	LAFT-OASIS *[Ben Ahmed 2014]*	TMR-OASIS *[Dang 2015]*	SER-3DR-NoC
Test-benches	Uniform, Transpose and Matrix-Multiplication		
Flit size	33		
Injection Rates	0%, 8.33%, 16.67%, 11.11%&6.67% and 33.33%		
Packet size	10 flits		
Routing	Switching: Wormhole-like Flow-control: Stop-Go Routing: Look-ahead routing algorithm		



Average End-to-End delay of Transpose Benchmark (4×4×4).



Network's Transmission Time of Uniform Benchmark (4×4×4).

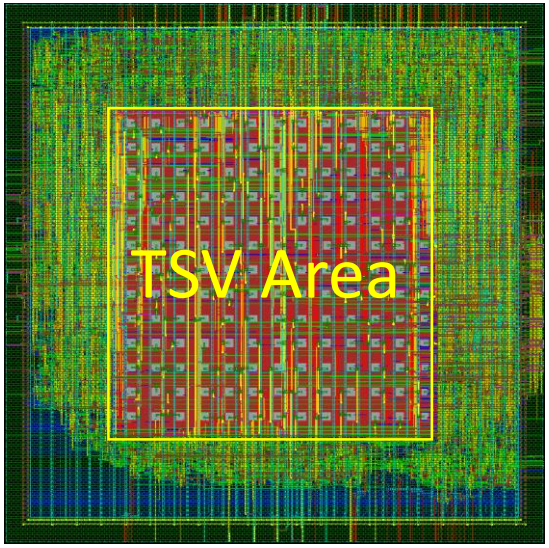


Throughput of Matrix Multiplication Benchmark (3×6×6).

Hardware Complexity

Design	Max Freq. (MHz)	Total Power mW)	Logic's area (μm^2)	# TSVs
LAFT OASIS	801.28	25.62	14,920	164
TMR-OASIS	763.36	30.31	21,664	164
Our proposal	655.74	27.13	17,154	164

Hardware Complexity of a single SER-3DR router.



SER-3DR-NoC's router layout

Network Configuration	
Parameter	Value
Number of TSVs per router	34×2 (data) $(6+1) \times 2$ (handshaking)
Flit size	34
Input Buffer	4
Topology	3D Mesh
Network's Size	$N \times 2 \times 2$
Routing Algorithm	Look-ahead routing
Flow Control	Stall-Go
Forwarding mechanism	Wormhole

Hardware Configuration	
Parameter	Value
Technology	Nangate 45 nm FreePDK3D45
Voltage	1.1 V
Impl. Freq.	500Mhz
Chip's size	$600\mu m \times 600\mu m$
TSV's size	$4.06\mu m \times 4.06\mu m$
TSV pitch	10 μm
Keep-out Zone	15 μm
TSVs' area	$390\mu m \times 390\mu m$

Conclusion

- In this paper, we proposed a soft-error resilient 3D Network-on-Chip architecture targeted for safety critical embedded applications.
- The architecture is designed in 45 *nm* CMOS and *FreePDK3D45* kit.
- Evaluation results show that the proposed system is able to achieve a high level of transient error protection with small degradation in term of performance and power overhead.
- As a future work, an in-depth hybrid soft and hard error protection and recovery mechanism will be implemented for 3D NoC. Moreover, thermal-power study will be also investigated.