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Reliability Assessment and Quantitative Evaluation of Soft-Error Resilient 3D Network-on-Chip Systems

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- Background
- Soft Error Resilient 3D NoC System
- Reliability Assessment Methodology
- Evaluation Result
- Conclusion & future work

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VLSI Design Challenges

For decades, the CMOS technology has been progressed to provide efficient solutions; however, VLSI design nowadays has several challenges:

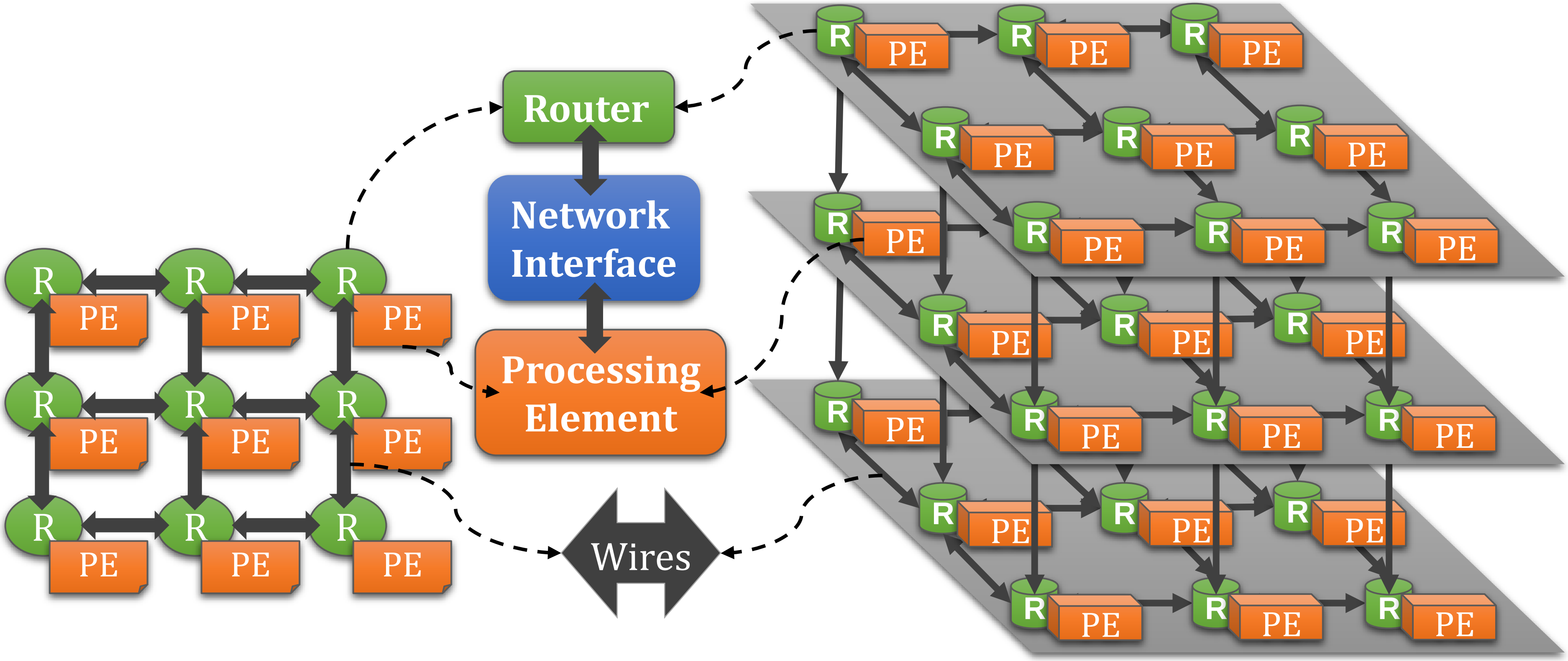
- **Power Wall**: Energy consumption is increased by *~60%* (high computing area) and *~40%* (middle computing area) per year [Chang 2016].
- **Yield Wall**: With the similar process control steps (~420), yield of *5nm* is predicted to be under 55% in compare to *28 nm* (~78%) [Yield].
- **Packaging**: Intel Chip's pin number is expected to increase by *25%* every 2 years (tick-tock period)*[Intel Proc]*.

VLSI Design Challenges (cnt.)

- **Time-to-Market:**
  - One quarter or one year late to market (2 year product life) leads to over 33% or 90% of the revenue loss, respectively[TTM].
- **Reliability**: Exposing to a variety of manufacturing, design, and operation factors makes the future architectures more vulnerable to different types of faults. [Henkel 2013].
  - 10-15°C difference in operation temperature can lead to 2x times difference of MTTF [Shafique 2014].
  - Soft error rate at 0.45 V is 30x times of 0.7 V [Shafique 2014].
  - ⇒ <u>Reliability assessment</u> has been becoming an import part in the design process.

Network-on-Chip

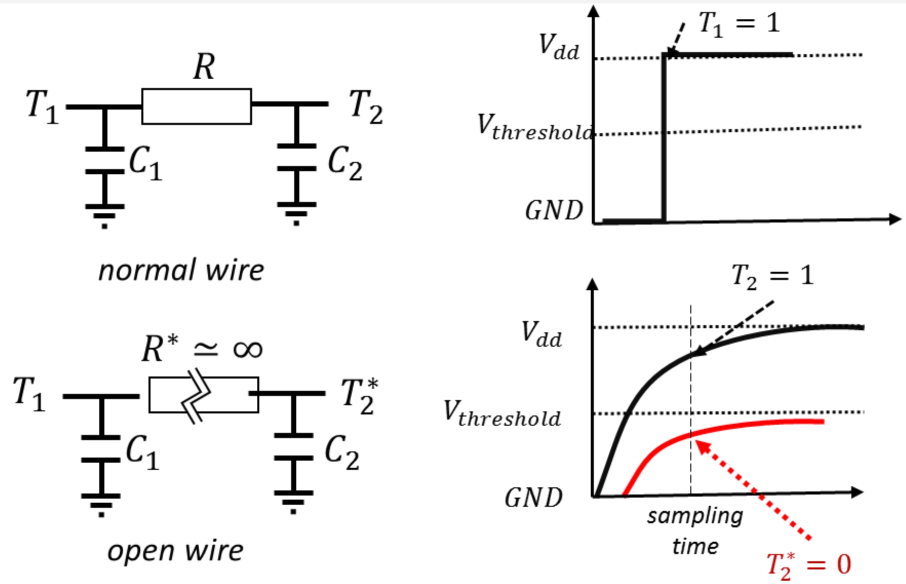
- Network-on-Chip (NoC) is the new paradigm to replace the traditional Bus with benefits:
  - Low power
  - Scalability
  - Reusability
  - Parallelism



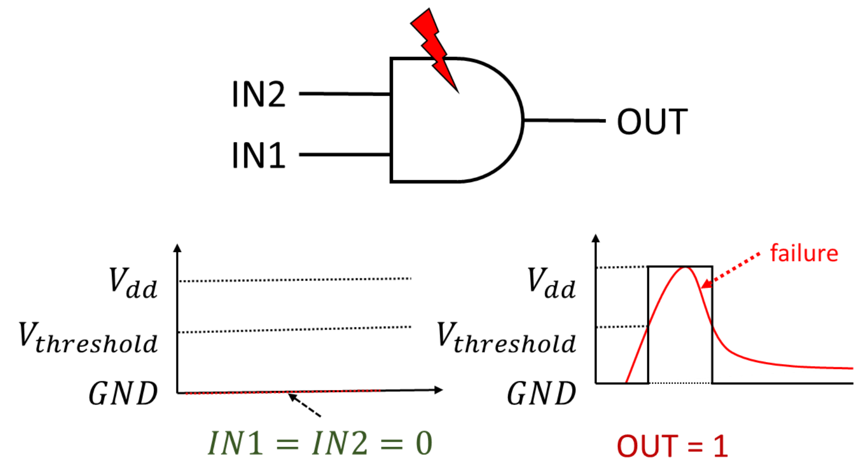
2D Mesh Network-on-Chip

3D Mesh Network-on-Chip

Reliability Challenges



Open wire defect



Single Event Transient by radiation particle

Fault Type	Source
Soft Errors	Cross-talk Radiation particles Cosmic rays Thermal neutrons
Hard Faults	Manufacture defects Time dependent dielectric breakdown Thermal Stress Electro-migration Negative-Bias Temperature Instability

Reliability Challenges (cnt.)

Fault Type	Potential Effects	Possible Solution
S	• Flip-bit (gate/wire) • Data Corruption • Misrouting	• Error Correction Code
Hard Faults	• Stuck at 0/1 • Delay • Data corruption • Packet loss/duplicate/misroute • Locking state	• Spare module/gate for replacements. • Faulty part isolation. • Fault-tolerant routing.

With the increasing of system vulnerability to faults and the critical effects on NoC systems, addressing NoC system reliability is needed.

Reliability Assessment

- Reliability Assessment involves five phases:
  - System Definition
  - Preliminary Design
  - Detailed Design
  - Fabrication, Assembly, Integration and Test (FAIT)
  - Production/Support

Reliability assessment is important for early design stages in order to prevent costly redesigns of the system.

Physical Analysis	Analytical Model	System-Level Simulation
• Requires massive time and computation resource		and high amount of statistic values.

- Analytical model is efficient for the three early stages.
- By analyzing analytically, the critical part can be detected and improved.

Paper Contributions

1. An efficient soft error resilient mechanism and architecture (SER-3DR-NoC) for reliable 3D-NoC systems.
    - Use redundancy of pipeline stage execution to detect.
    - Use three execution results and majority voting to recover the soft error.
2. An formulation of reliability assessment for fault-tolerant system.
    - Base on Mean-Time-Between-Failure.
    - Modeling by Markov-state model.

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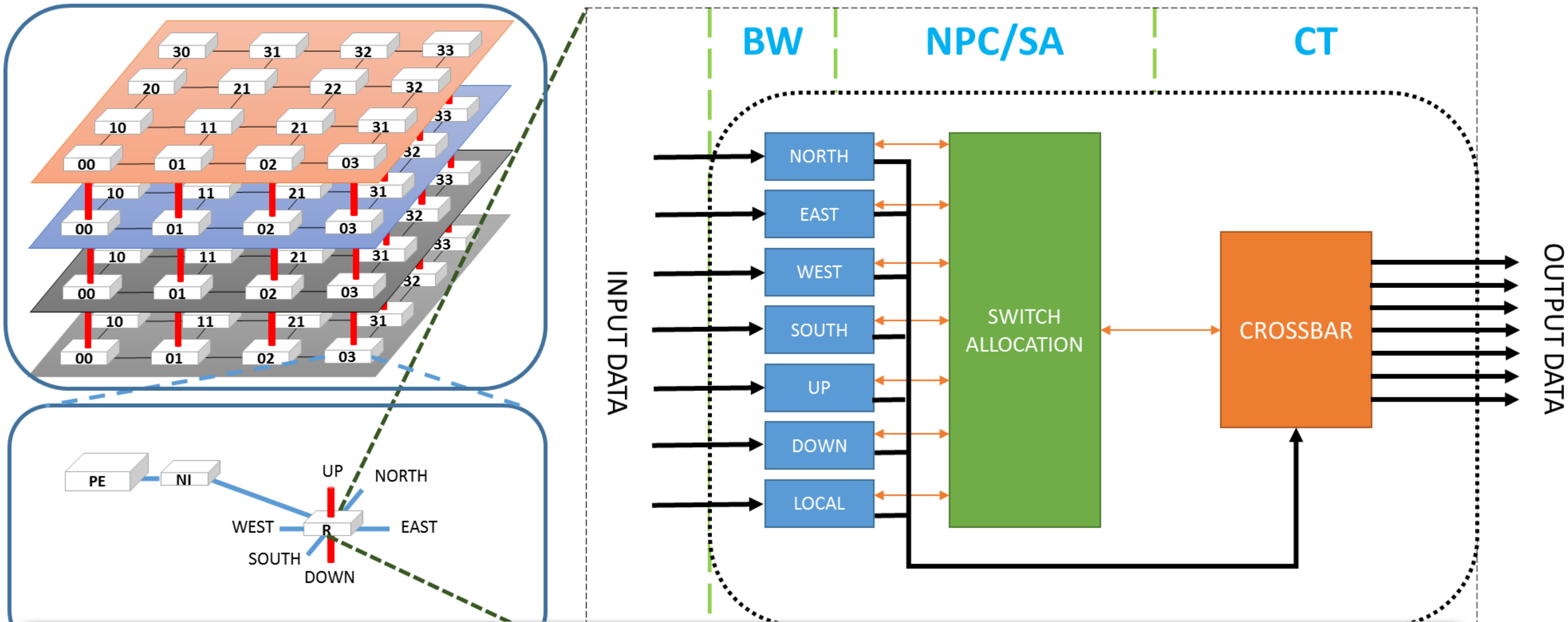
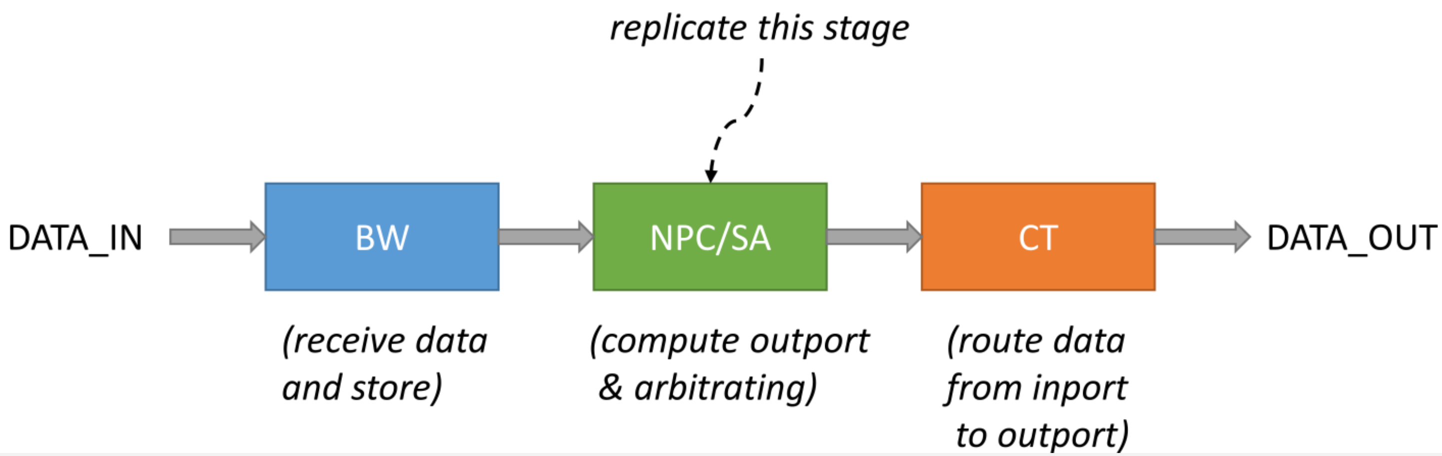
Proposed System Architecture



Incoming flit is stored in the input buffer. Later, the routing information is used to computing routing path and intra-router arbitration. Flits will be forwarded through the crossbar.

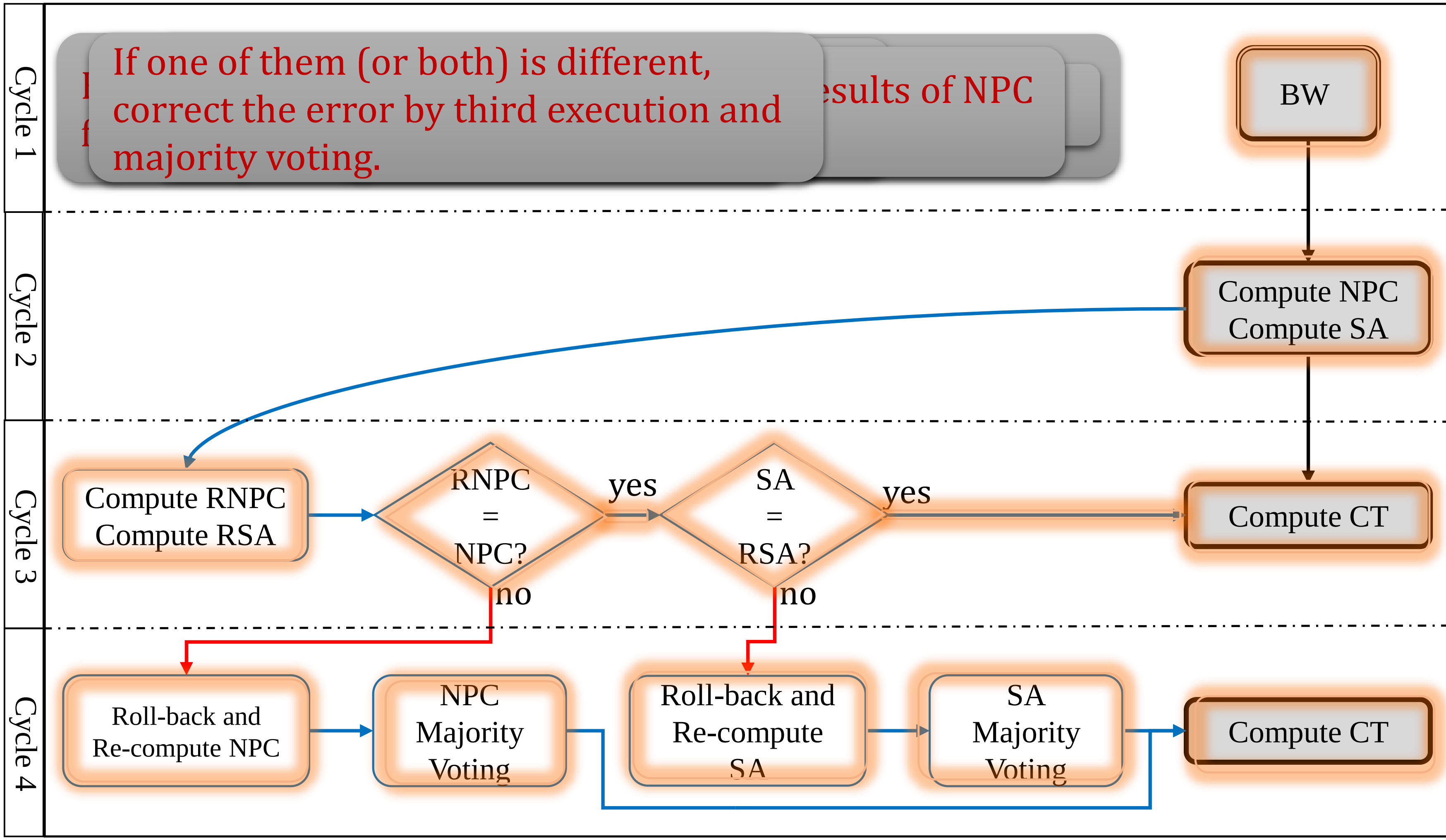
Soft Error Resilience Method

- Approach:
  - Replicate the execution of the pipeline state.
  - Compare two consecutive results: different ⇔ fault occurred.
  - Correct by executing the third time and using a majority voting.
- Target:
  - The routing (NPC) and arbitrating (SA) units role an import part in side the network.
  - A soft error in NPC or SA can lead to misrouting, loss/duplicated packet or even locking states.
  - NPC and SA are selected to be protected.



Soft Error Resilience Algorithm

stage Original pipeline stage stage Redundant pipeline stage



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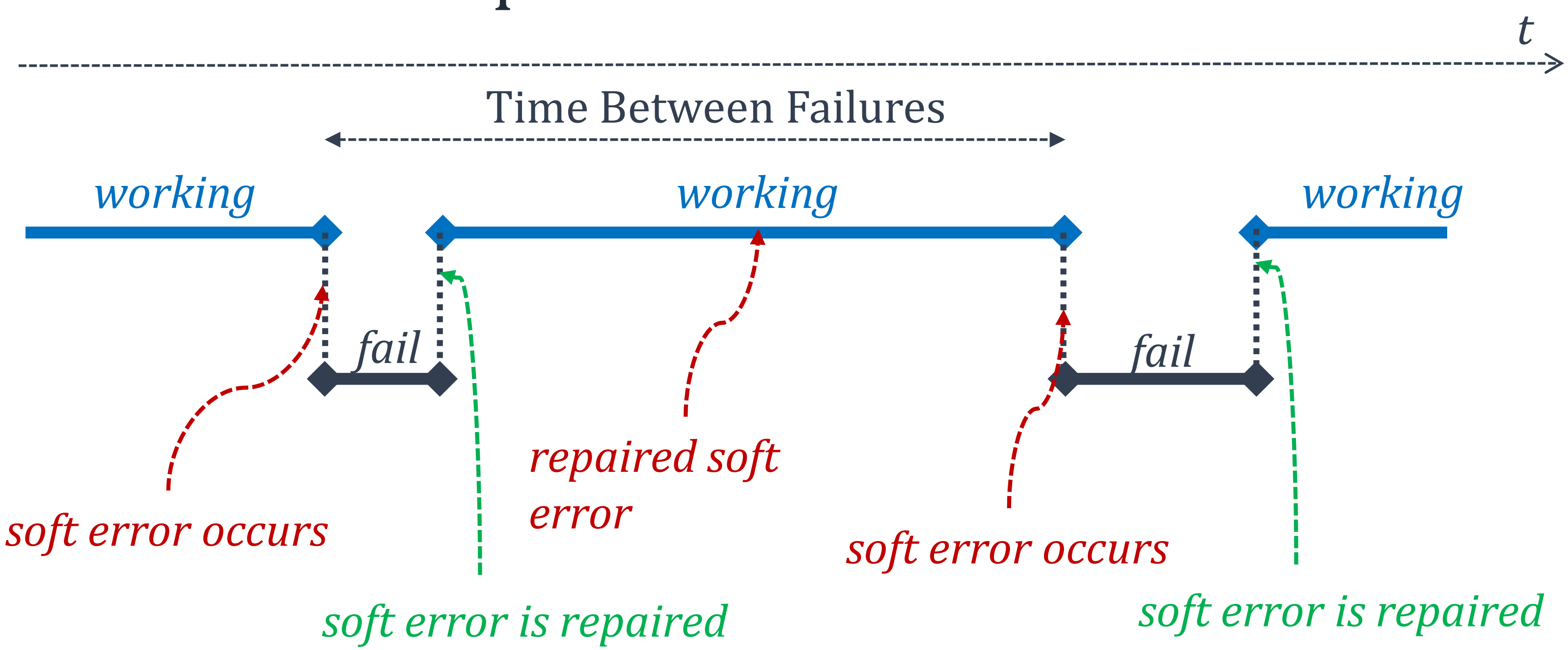
Reliability Assessment Methodology

- We proposed a reliability assessment method by using Markov-state model.
- The fault rate distribution is also proposed.
- To evaluate the efficiency of a fault-tolerance, we present a new parameter: Reliability Acceleration Factor.
- To assess the soft error resilient mechanism, we apply the method for it.

Mean Time Between Failure

Mean Time Between Failure is the average value of time between two consequent failures.



Given a reliability function R, MTBF is as follows:

$$MTBF = \lim_{s \to 0} R(s)$$

** in Laplace domain*

Fault Rate Model

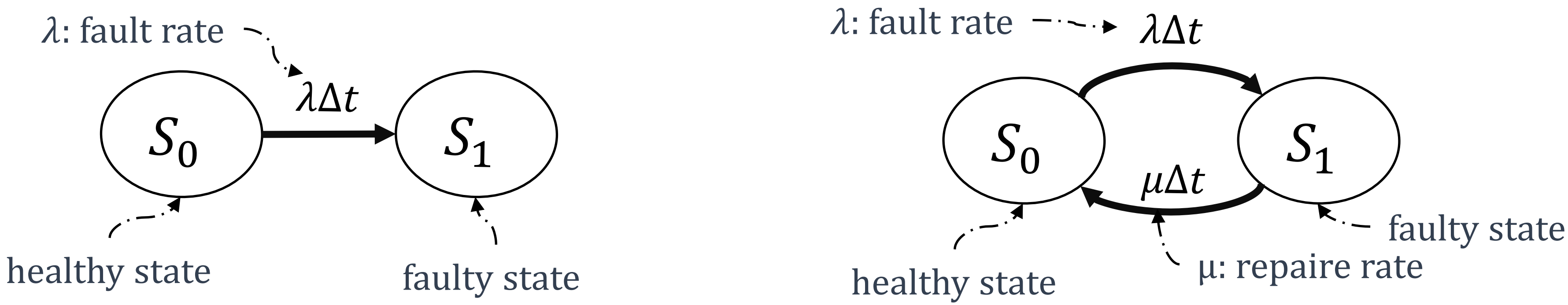
Fault rate of a system consisting of k modules:

$$\lambda_{system} = \sum_{i=1}^{k} f_i \times OR_i \times AR_i \times \lambda_{unit}$$

The design is assumed to be under "steady-state" which has a constant fault rate.

Parameter	**Description**
$unit$	A select module as a reference for calculation the system's fault rate.
OR_i	Operating time ratio of component i to $unit$
AR_i	Area cost ratio of component i to $unit$.
f_i	Changing rate caused by attaching the module i to the system.

Markov State Model (1)

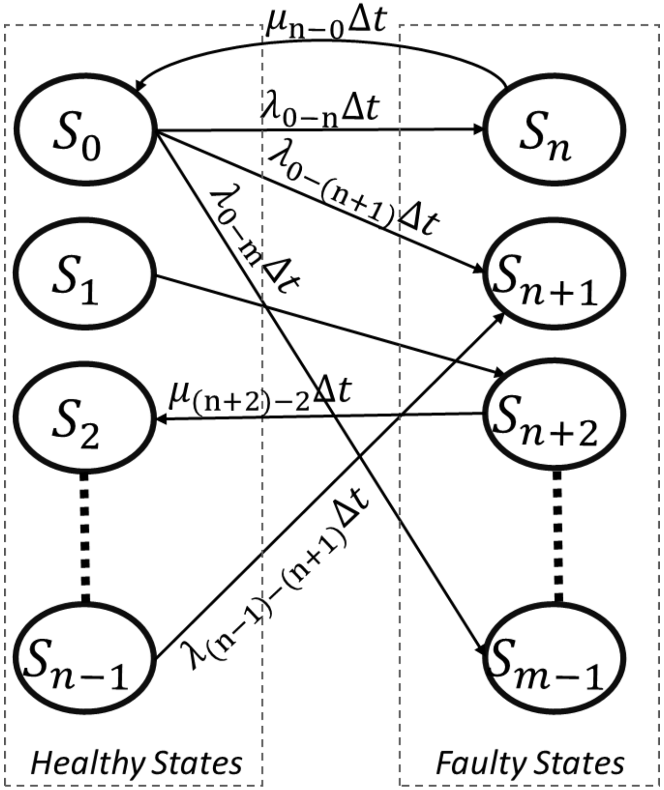


(a) non-repair system

(b) repairable system

- Each state S_i of the Markov state model represents a possible status of the system.
  - For example: S_0 is initial and healthy state, S_1 is faulty state.
- The transition from S_0 to S_1 is given by a fault rate λ ($\lambda = 1/MTBF$).
- When a repairable system failed, the repairable system can be recovered with a repair rate μ.

Markov State Model (2)



An example Markov state model

For a more complex system, its states can be separated into two sets:

$H \triangleq \{S_i \in S |$ the system works correctly$\}$
$F \triangleq \{S_i \in S |$ the system fails$\}$

The reliability function is defined the probability of healthy states (H with n states).

$$R(s) = P(H)$$

$$MTBF = \lim_{s \to 0}(P(H(s)) = \lim_{s \to 0} \sum_{i=0}^{n-1} S_i(s)$$

Note: Solving Markov state model can be seen in back-up slides

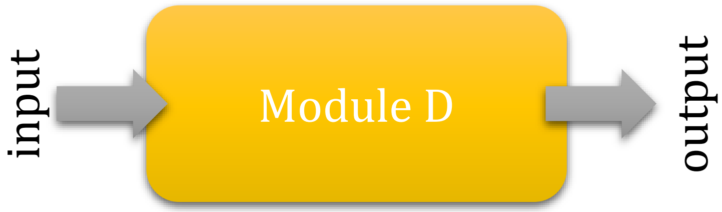
Reliability Acceleration Factor

- To obtained a numeric value representing the reliability of system, a new parameter: Reliability Acceleration Factor is used.

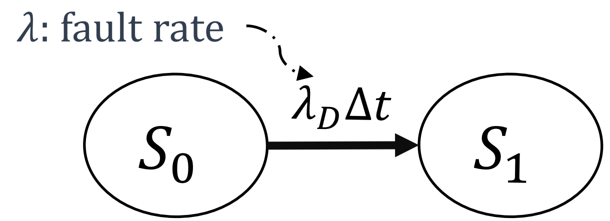
$$RAF = \frac{MTBF_{FT}}{MTBF_{original}}$$

- $MTBF_{original}$: Mean Time Between Failure of the original system.
- $MTBF_{FT}$: Mean Time Between Failure of the fault-tolerant system.
- Because $MTBF = 1/\lambda$, $RAF = 1/f$ (f is fault reduction rate in Fault Rate Model).

Modeling Non-Fault-Tolerant System



Original Module



Markov State model

A non-fault-tolerant system can be modeled as two states:

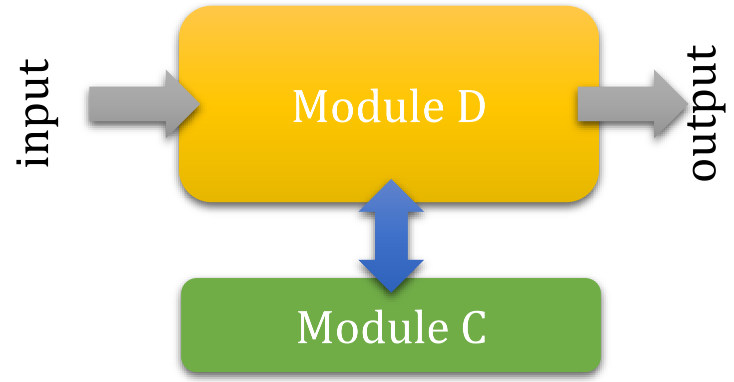
- S_0 is the initial state.
- S_1 the failure state.

MTBF of this system is given as follows:

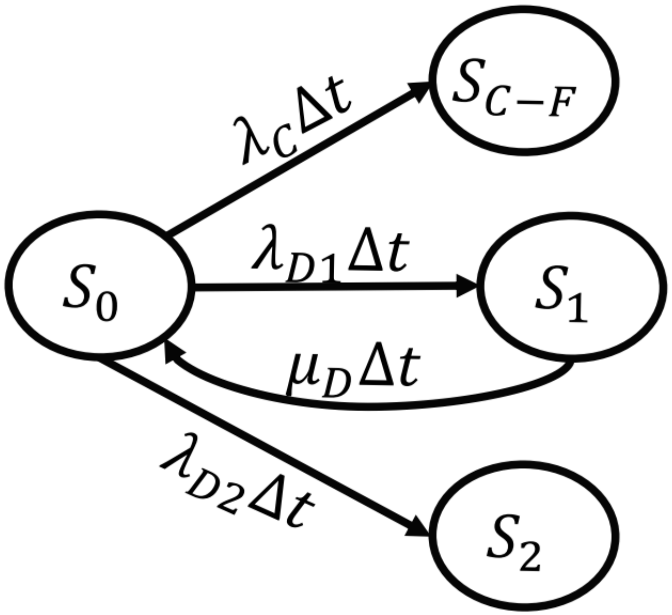
$$MTBF = \frac{1}{\lambda_D}$$

Modeling Fault-Tolerant System

- A non-fault-tolerant system can be modeled as three states:
- S_0 is the initial state.
- S_1 represents the part of fault rate which can be corrected by module C.
- S_2 represents the part of fault rate which cannot be corrected by module C.
- S_{C-F} is the state of module C fails.
- S_1 has fault rate λ_{D1}
- S_2 has fault rate λ_{D2}
- $\lambda_D = \lambda_{D1} + \lambda_{D2}$



Fault-Tolerant Module



Fault-Tolerant Markov-State Model

Modeling Fault-Tolerant System (2)

From the Markov model, MTBF of the Fault-Tolerant system is given as follows:

$$MTBF_{FT} = \frac{1}{\lambda_{D2} + \lambda_C}$$

In the fault rate model, the fault rate can be given as:

$$\lambda_{system} = \sum_{i=1}^{k} f_i \times OR_i \times AR_i \times \lambda_{unit}$$

Therefore, the fault rate of module D is as follows:

$$\lambda_{D2} = (OR_{D2} \times AR_{D2}) \times \lambda_{original} = f_D \times OR_D \times AR_D \times \lambda_{original}$$

The fault rate of module C:

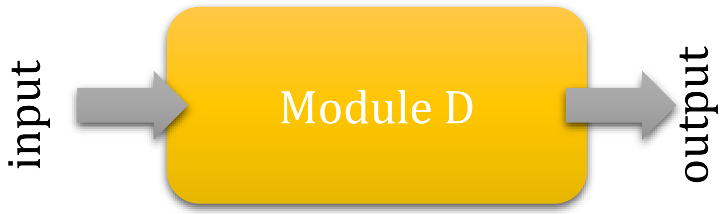
$$\lambda_c = (OR_c \times AR_c) \times \lambda_{original}$$

Modeling Fault-Tolerant System (3)

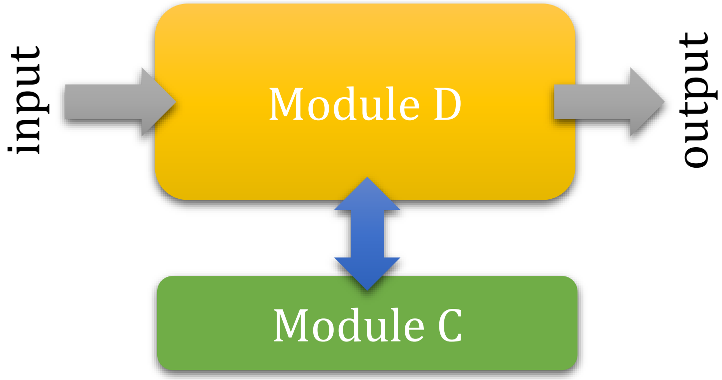
Finally, Reliability Acceleration Factor of the Fault-Tolerant system is as follows:

$$RAF = \frac{1}{(f_D \times OR_D \times AR_D) + (OR_C \times AR_C)}$$

- $f_D = \lambda_{D2}/\lambda_D$ is the reduction ratio of fault rate.
- OC_X is operation ratio of module X
- AC_X is area cost ratio of module X



Original Module



Fault-Tolerant Module

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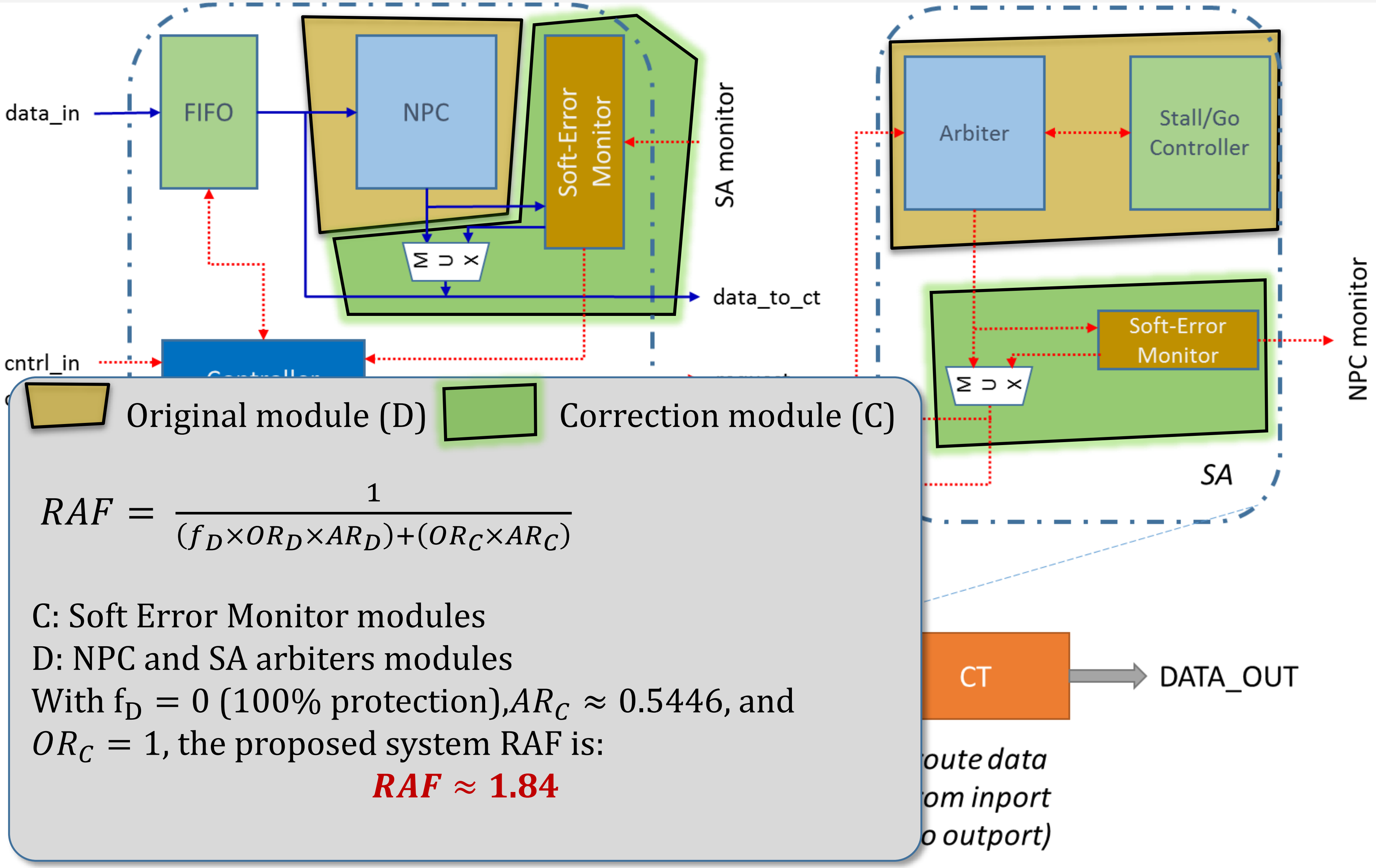
Evaluation Methodology

1. Analytical and Hardware Evaluation of the proposed soft error resilient system:
    - Calculate the Reliability Acceleration Factor value.
    - Verify the capacity of error correction.
2. Quantitative evaluation of the proposed system
    - Area cost.
    - Power consumption.
    - Performance:
        - Three benchmarks: Matrix-multiplication, Uniform and Transpose.
3. Comparison to some noticed soft error resilience methods
    - Reliability
    - Area overhead.
    - Latency

Evaluation Configuration

Architectures	LAFT-OASIS *[Akram 2014]*	TMR-OASIS *[*Dang 2015*]*	SER-3DR-NoC
Test-benches	Uniform, Transpose and Matrix-Multiplication		
Flit size	33		
Injection Rates	0%, 8.33%, 16.67%, 11.11%&6.67% and 33.33%		
Packet size	10 flits		
Routing	Switching: Wormhole-like Flow-control: Stop-Go Routing: Look-ahead routing algorithm		

Analytical Assessment for SER-3DR



Original module (D) Correction module (C)

$$RAF = \frac{1}{(f_D \times OR_D \times AR_D) + (OR_C \times AR_C)}$$

C: Soft Error Monitor modules

D: NPC and SA arbiters modules

With $f_D = 0$ (100% protection), $AR_C \approx 0.5446$, and $OR_C = 1$, the proposed system RAF is:

$$\boldsymbol{RAF \approx 1.84}$$

Reliability Comparison

Model	TMR for OASIS	Yu et al. [Yu 2013]	Prodromou et al. [Prodromou 2012]	SER-3DR
Mechanism	Majority Voting	Monitor	Monitor	Monitor
Area Overhead	204.33%	9%	3%	54.46%
AR_C	0.0433	0.09	0.03	0.5446
RAF	≈ 1.33	≈ 11.11	≈ 1 (only detection)	≈ 1.84
Delay	+0 cycle	+ 0 cycle (no fault) + 1 cycle (recovery)	+0	+ 1 cycle (redundancy) + 2 cycle (recovery)
Fault Coverage	100% hard faults and soft	7 faults	13 faults	100% soft errors

With the assume that the monitor-based technique can handle 100% faults, it provides the best reliability (in RAF). SER-3DR provides a medium value and is better than TMR by 38.35%.

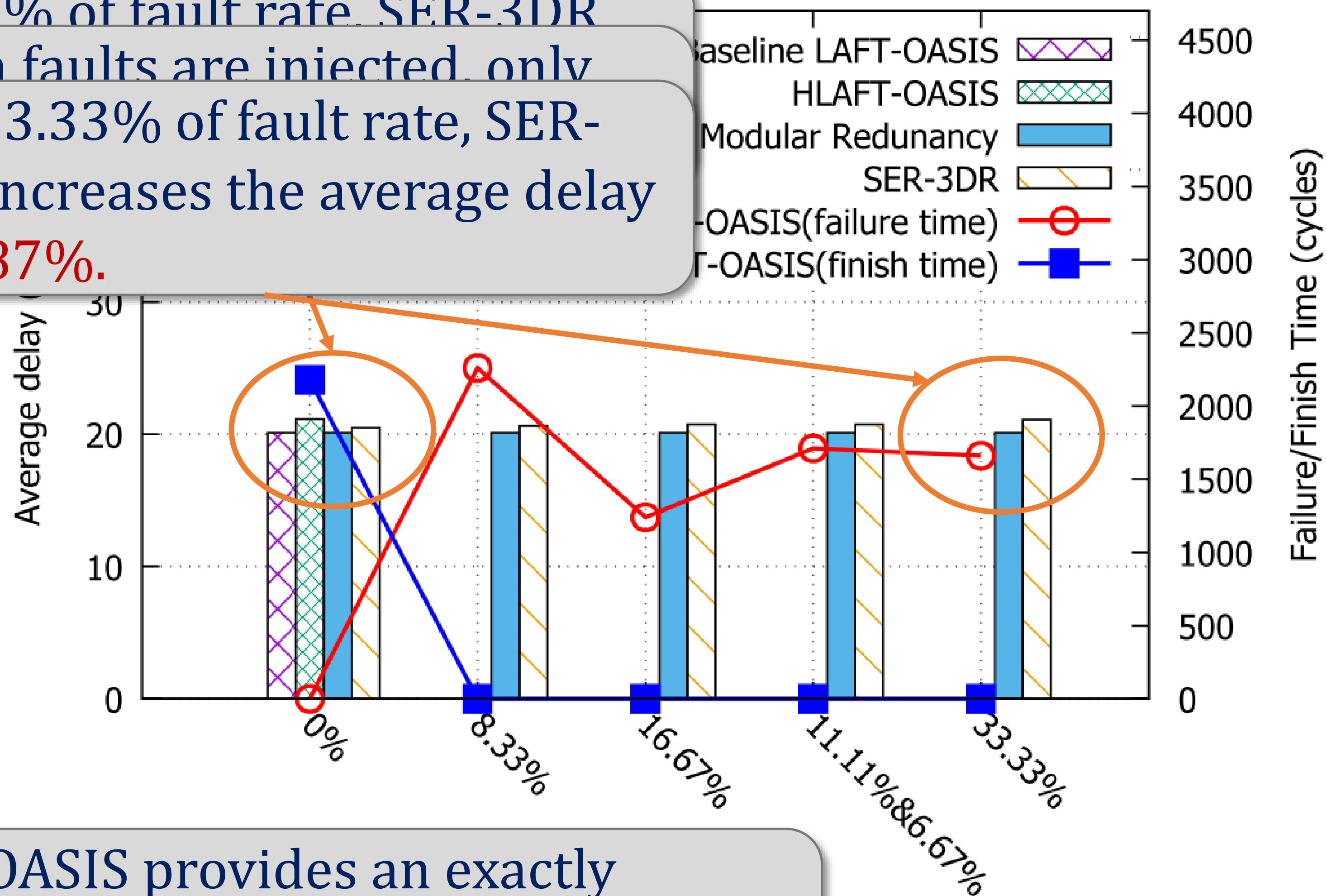
of faults (7 and 13).

Performance Evaluation (1)

At a 0% of fault rate, SER-3DR

When faults are injected, only

At a 33.33% of fault rate, SER-3DR increases the average delay by 4.87%.



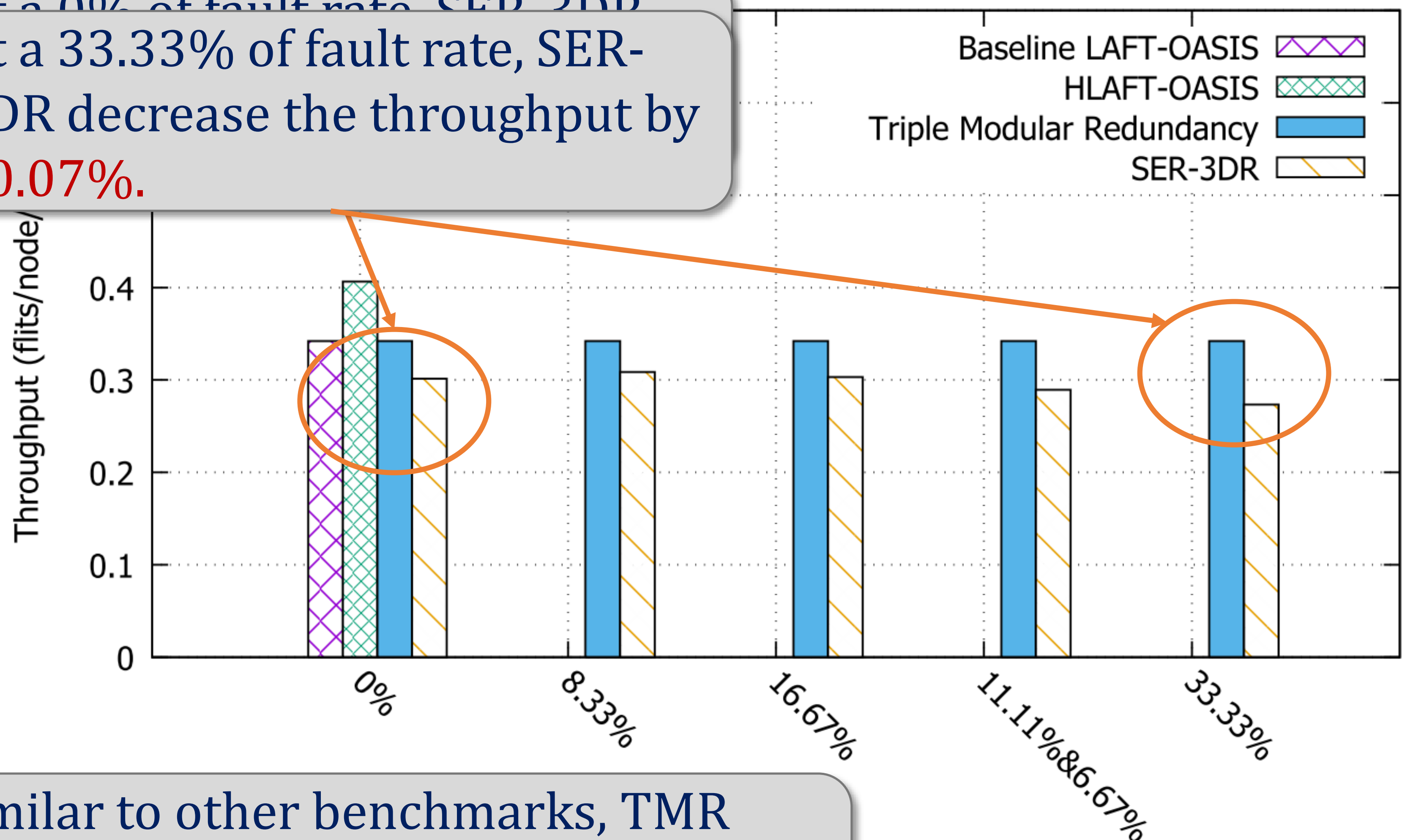
TMR-OASIS provides an exactly similar performance to the original system even under faults injection.

s; Network's size :4x4x4.

Performance Evaluation (2)

At a 0% of fault rate, SER-3DR

At a 33.33% of fault rate, SER-3DR decrease the throughput by 20.07%.



arks, Network's size : 4x4x4.

Similar to other benchmarks, TMR provides similar performance to the baseline model.

Hardware Evaluation

Design	Max Freq. (MHz)	Power consumption (mW)	Logic's area (μm^2)	#TSVs
LAFT OASIS	801.28	25.62	14,920	164
TMR-OASIS	763.36	30.31	21,664	164
SER-3DR	655.74	27.12	17,154	164

Comparison between the proposed model, baseline model and TMR model.

- TMR-OASIS costs 45.20% more area cost while the proposal (SER-3DR) requires 14.98% of additional logic area (30.22% less).
- The power consumption is slightly increased in our proposed system: 5.90% (10.49% less than TMR-OASIS).
- SER-3DR has the slowest maximum frequency: 655.74 MHz due to additional logic unit in the critical paths.

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Conclusion

- We proposed a method to improve the reliability of 3D-NoC router against soft errors.
- The proposed method is evaluated with reasonable performance degradation while having the ability to deal with extremely high error rates (33%).
- A reliability assessment method is proposed to help designer evaluate the efficiency of the design.
- In terms of reliability, the proposed method improves MTBF by 1.84 times with a small latency increase of 18.16% (in average).