Khanh N. Dang

Personal Information

Name	Khanh N. Dang
Position	Associate Professor
Affiliation	Department of Computer Science and Engineering The University of Aizu 965-8580 Tsuruga, Ikki-Machi, Aizu-Wakamatsu, Fukushima, Japan
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Research Interests

My research spans *VLSI design*, *thermal-awareness*, *fault-tolerance* and *neuromorphic computing*. In particular, I have a strong interest in building on the 3D Integrated Circuit based neuromorphic computing architecture that is highly-reliable and scalable enough to be safely and responsibly deployed in the real world.

Education

10/2014–09/2017	**Ph.D., Computer Science and Engineering** The University of Aizu, Japan
12/2011–04/2014	**M.Sc., Information Systems, and Technology** Paris-Sud University, France
09/2007–06/2011	**B.Sc., Electronics and Telecommunications** College of Technology, Vietnam National University, Hanoi, Vietnam

Professional Experience

04/2022–Current **The University of Aizu, Japan**
Position: Associate Professor

11/2017–03/2022 **VNU-UET, Vietnam National University, Hanoi, Vietnam**
Position: Lecturer

11/2020–03/2021 **The University of Aizu, Japan**
Position: Visiting Researcher

05/2019–09/2019 **The University of Aizu, Japan**
Position: Visiting Researcher

07/2011–09/2014 **SISLAB, Vietnam National University, Hanoi, Vietnam**
Position: Researcher

10/2010–04/2011 **Dolphin Vietnam IC Center, Vietnam**
Position: Intership

Publications

Book

1. A. B. Abdallah and K. N. Dang, *Neuromorphic computing principles and organization*. Springer, 2022

Book Chapters

1. K. N. Dang and A. B. Abdallah, "Architecture and design methodology for highly-reliable TSV-NoC systems," in *Horizons in Computer Science Research*. Nova Science Publishers, 2018, vol. 16, pp. 199–246
2. X. T. Tran, N. K. Dang, D. H. Bui, and A. Merigot, "Low cost inter-prediction architecture in H. 264/AVC encoders with an efficient data reuse strategy," in *Advances in Engineering Research*. Nova Science Publishers, 2021, vol. 40, ch. 6

Journal Publications

1. J. Wang, O. M. Ikechukwu, K. N. Dang, and A. B. Abdallah, "Spike-event X-ray image classification for 3D-NoC-based neuromorphic pneumonia detection," *Electronics*, vol. 11, no. 24, p. 4157, 2022
2. A. Ben Abdallah and K. N. Dang, "Toward robust cognitive 3D brain-inspired cross-paradigm system," *Frontiers in Neuroscience*, p. 795, 2021
3. D.-A. Nguyen, X.-T. Tran, K. N. Dang, and F. Iacopi, "A low-power, high-accuracy with fully on-chip ternary weight hardware architecture for deep spiking neural networks," *Microprocessors and Microsystems*, vol. 90, p. 104458, 2022
4. K. N. Dang, A. B. Ahmed, A. B. Abdallah, and X.-T. Tran, "Hotcluster: a thermal-aware defect recovery method for through-silicon-vias toward reliable 3-D ICs systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 4, pp. 799–812, 2021
5. K. N. Dang, N. A. V. Doan, and A. B. Abdallah, "Migspike: A migration based algorithms and architecture for scalable robust neuromorphic systems," *IEEE Transactions on Emerging Topics in Computing*, vol. 10, no. 2, pp. 602–617, 2021
6. O. M. Ikechukwu, K. N. Dang, and A. B. Abdallah, "On the design of a fault-tolerant scalable three dimensional NoC-based digital neuromorphic system with on-chip learning," *IEEE Access*, vol. 9, pp. 64 331–64 345, 2021
7. K. N. Dang, A. B. Ahmed, A. B. Abdallah, and X.-T. Tran, "A thermal-aware on-line fault tolerance method for TSV lifetime reliability in 3D-NoC systems," *IEEE Access*, vol. 8, pp. 166 642–166 657, 2020
8. K. N. Dang, M. C. Meyer, A. B. Ahmed, A. B. Abdallah, and X.-T. Tran, "A non-blocking non-degrading multiple defects link testing method for 3D-Networks-on-Chip," *IEEE Access*, vol. 8, pp. 59 571–59 589, 2020
9. K. N. Dang, A. B. Ahmed, A. B. Abdallah, and X.-T. Tran, "Tsv-oct: A scalable online multiple-tsv defects localization for real-time 3-d-ic systems," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, pp. 672–685, 2020
10. K. N. Dang, A. B. Ahmed, Y. Okuyama, and A. B. Abdallah, "Scalable design methodology and online algorithm for TSV-cluster defects recovery in highly reliable 3d-noc systems," *IEEE Transactions on Emerging Topics in Computing*, vol. 8, no. 3, pp. 577–590, 2020
11. K. N. Dang, M. Meyer, Y. Okuyama, and A. B. Abdallah, "A low-overhead soft–hard fault-tolerant architecture, design and management scheme for reliable high-performance many-core 3d-noc systems," *The Journal of Supercomputing*, vol. 73, pp. 2705–2729, 2017
12. K. N. Dang, A. B. Ahmed, X. T. Tran, Y. Okuyama, and A. B. Abdallah, "A comprehensive reliability assessment of fault-resilient network-on-chip using analytical model," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 11, pp. 3099–3112, 2017

Conferences

1. T. Fukuchi, M. I. Ogbodo, J. Wang, K. N. Dang, and A. Ben Abdallah, "Efficient pneumonia detection method and implementation in chest X-ray images based on a neuromorphic spiking neural network," in *Computational Collective Intelligence: 14th International Conference, ICCCI 2022, Hammamet, Tunisia, September 28–30, 2022, Proceedings*. Springer International Publishing Cham, 2022, pp. 311–321
2. M. I. Ogbodo, K. N. Dang, and A. B. Abdallah, "Study of a multi-modal neurorobotic prosthetic arm control system based on recurrent spiking neural network," in *The 4th ETLTC International Conference on ICT Integration in Technical Education (ETLTC2022*, 2022
3. O. M. Ikechukwu, K. N. Dang, and A. Ben Abdallah, "Energy-efficient spike-based scalable architecture for next-generation cognitive AI computing systems," in *Ubiquitous Networking: 7th International Symposium, UNet 2021, Virtual Event, May 19–22, 2021, Revised Selected Papers 7*. Springer International Publishing, 2021, pp. 225–238
4. D.-A. Nguyen, X.-T. Tran, K. N. Dang, and F. Iacopi, "A lightweight max-pooling method and architecture for deep spiking convolutional neural networks," in *2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. IEEE, 2020, pp. 209–212
5. K. N. Dang, A. B. Ahmed, F. Z. Rokhani, A. B. Abdallah, and X.-T. Tran, "A thermal distribution, lifetime reliability prediction and spare TSV insertion platform for stacking 3D-ICs," in *2020 International Conference on Advanced Technologies for Communications (ATC)*. IEEE, 2020, pp. 50–55
6. M. Ogbodo, K. Dang, F. Tomohide, and A. Abdallah, "Architecture and design of a spiking neuron processor core towards the design of a large-scale event-driven 3D-NoC-based neuromorphic processor," in *The ACM Chapter International Conference on Educational Technology, Language and Technical Communication (ETLTC), Jan. 27-31, 2020.*, 2020
7. M. Ogbodo, T. Vu, K. Dang, and A. Abdallah, "Light-weight spiking neuron processing core for large-scale 3D-NoC based spiking neural network processing systems," in *2020 IEEE international conference on big data and smart computing (BigComp)*. IEEE, 2020, pp. 133–139
8. K. N. Dang and A. B. Abdallah, "An efficient software-hardware design framework for spiking neural network systems," in *The International Conference on Internet of Things, Embedded Systems and Communications (IINTEC 2019)*, 2019
9. K. N. Dang, M. Meyer, A. B. Ahmed, A. B. Abdallah, and X.-T. Tran, "2D-PPC: A single-correction multiple-detection method for Through-Silicon-Via faults," in *2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2019)*, 2019
10. K. N. Dang, A. B. Ahmed, and X. T. Tran, "An on-communication multiple-TSV defects detection and localization for real-time 3D-ICs," in *2019 IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, 2019

11. K. N. Dang, A. B. Ahmed, B. A. Abderrazak, and X.-T. Tran, "TSV-IaS: Analytic analysis and low-cost non-preemptive on-line detection and correction method for TSV defects," in *Proc. IEEE Computer Society Annual Symp. VLSI (ISVLSI)*, 2019, pp. 501–506

12. K. N. Dang and X.-T. Tran, "Parity-based ECC and mechanism for detecting and correcting soft errors in on-chip communication," in *2018 IEEE 12th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*, 2018

13. S. Mie, Y. Okuyama, Y. Sato, Y. Chan, N. K. Dang, and B. A. Abderazek, "Real-time UAV attitude heading reference system using extended Kalman filter for programmable soc," in *2017 IEEE 11th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC)*. IEEE, 2017, pp. 136–142

14. A. B. Abdallah, K. N. Dang, and Y. Okuyama, "A low-overhead fault tolerant technique for TSV-based interconnects in 3D-IC systems," in *2017 18th International Conference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)*, 2017

15. K. N. Dang, M. Meyer, Y. Okuyama, and A. B. Abdallah, "Reliability assessment and quantitative evaluation of soft-error resilient 3D network-on-chip systems," in *2016 IEEE 25th Asian Test Symposium (ATS)*. IEEE, 2016, pp. 161–166

16. K. N. Dang, Y. Okuyama, and A. B. Abdallah, "Soft-error resilient Network-on-Chip for safety-critical applications," in *2016 International Conference on IC Design and Technology (ICICDT)*. IEEE, 2016, pp. 1–4

17. K. N. Dang, M. Meyer, Y. Okuyama, X.-T. Tran, and A. B. Abdallah, "A Soft-Error Resilient 3D Network-on-Chip Router," in *IEEE 7th International Conference on Awareness Science and Technology*, 2015

18. N.-M. Nguyen, E. Beigne, S. Lesecq, D.-H. Bui, N.-K. Dang, and X.-T. Tran, "H. 264/AVC hardware encoders and low-power features," in *2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*. IEEE, 2014, pp. 77–80

19. N.-K. Dang, X.-T. Tran, and A. Merirot, "An efficient hardware architecture for inter-prediction in H. 264/AVC encoders," in *17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems*. IEEE, 2014, pp. 294–297

20. H.-P. Phan, H. K. Nguyen, D.-H. Bui, N.-K. Dang, and X.-T. Tran, "System-on-chip testbed for validating the hardware design of H. 264/AVC encoder," in *Proceedings of the 2013 National Conference on Electronics and Communications (REV2013-KC01), Hanoi*, 2013

21. N.-K. Dang and X.-T. Tran, "A VLSI Implementation for Inter-Prediction Module in H. 264/AVC Encoders," in *Proceedings of the 2013 IEICE International Conference on Integrated Circuits, Devices, and Verification (ICDV 2013), Ho Chi Minh city, Vietnam*, 2013

22. N. K. Dang, T. V. Le Van, and X. T. Tran, "FPGA implementation of a low latency and high throughput network-on-chip router architecture," in *Proceedings of the 2011 International Conference on Integrated Circuits and Devices in Vietnam*, 2011

Patents

1. Khanh N. Dang, A. Ben Abdallah, "Program for generating migration flows for homogeneous computing systems and homogeneous computing devices", 2022-196416, Japan patent, (filed patent).
2. A. Ben Abdallah, Zhishang Wang, Khanh N. Dang, Masayuki Hisada, "EV Power Consumption Prediction Method and System for Power Management in Smart Grid",2020-194733, Japan patent, 2022 (filed patent).
3. A. Ben Abdallah, Huakun Huang, Khanh N. Dang, Jiangning Song, "AI Processor", 2020-194733, Japan patent, (patent pending).
4. A. Ben Abdallah, Khanh N. Dang, Masayuki Hisada, "Distance-aware Extended Parity Product Coding for multiple faults detection for on-chip links", 2020-171553, Japan patent, (patent pending).
5. A. Ben Abdallah, Khanh N. Dang, "A three-dimensional system on chip in which a TSV group including a plurality of TSVs provided to connect between layers", 2020-094220, JP2021190829A, Japan patent, (patent pending).
6. A. Ben Abdallah, Khanh N. Dang, Masayuki Hisada, "A TSV fault-tolerant router system for 3D-Networks-on-Chip", 2017-218953, JP2019092020A, Japan (patent pending).

Grants

1. "Hotspot aware Fault-Tolerant Architectures and Algorithms for TSV-based 3D Network-on-Chips", main PI, funded by National Foundation for Science and Technology Development (NAFOSTED) under No. 102.01-2018.312 (2019-2021).
2. "Soft Error Resilient Architecture and Algorithm for Network-on-Chip" : main PI, funded by VNU University of Engineering and Technology (VNU-UET) under project No. CN18.10 (2018-2019).
3. "Development of IoT Dual Band Transmitters for Agriculture (IOTA)", core member, funded by the Ministry of Science and Technology (World Bank project) (2018-2019).
4. "Reconfiguration Solution in Designing Network-on-Chip Architectures ", core member, funded by National Foundation for Science and Technology Development (NAFOSTED) under No. 102.01-2013.17 (2014-2016).
5. "Reconfiguration Solution in Designing Network-on-Chip Architectures ", core member, funded by National Foundation for Science and Technology Development (NAFOSTED) under No. 102.01-2013.17 (2014-2016).

Community Services

Organizing Commitee

1. **[IEEE MCSoC 2018]**: IEEE 12th International Symposium on Embedded Multicore/Many-Core Systems on Chip 2018. Role: Publication chair
2. **[IEEE MCSoC 2019]**: IEEE 13th International Symposium on Embedded Multicore/Many-Core Systems on Chip 2019. Role: TPC co-chair
3. **[IEEE APPCAS 2020]**: IEEE 16th Asia Pacific Conference on Circuits and Systems 2020. Role: TPC co-chair
4. **[IEEE MCSoC 2021]**: IEEE 14th International Symposium on Embedded Multicore/Many-Core Systems on Chip 2021. Role: TPC co-chair
5. **[IEEE APPCAS 2021]**: IEEE 17th Asia Pacific Conference on Circuits and Systems 2020. Role: Session co-chair
6. **[IEEE MCSoC 2022]**: IEEE 15th International Symposium on Embedded Multicore/Many-Core Systems on Chip 2022. Role: TPC co-chair
7. **[IEEE MCSoC 2023]**: IEEE 15th International Symposium on Embedded Multicore/Many-Core Systems on Chip 2022. Role: Publication chair

Program Committee

IEEE MCSoC 2018, IEEE MCSoC 2019, IEEE ICCE 2020, IEEE APCCAS 2020, IEEE MCSoC 2021, IEEE APCCAS 2021

Editor

1. **[JLPEA]**: Special Issue Journal of Low Power Electronics and Applications (ESCI/Scopus): "Advances in Embedded Artificial Intelligence and Internet-of-Things". Role: Special Issue Editor

Journal Reviews

ACM Journal on Emerging Technologies in Computing Systems, Applied Sciences, Elsevier Journal of Systems Architecture, Electronics, Frontiers in Computational Neuroscience, Frontiers in Neuroscience, IEEE Transactions on Circuits and Systems I : Regular Papers, IEEE Access, Journal of Supercomputing, Microprocessors and Microsystems, Microelectronics Journal

Invited Speaker

1. Technical presentation at The 1st IEEE South-East Asia Workshop on Circuits and Systems (SEACAS 2017)
2. Technical Presenter/Chapter representative at The 2nd IEEE South-East Asia Workshop on Circuits and Systems (SEACAS 2018)
3. Technical Presenter/Chapter representative at The 3nd IEEE South-East Asia Workshop on Circuits and Systems (SEACAS 2019)
4. Khanh N. Dang, "Fault-Tolerance Through-Silicon-Via For 3-D Integrated Circuits", Advanced Institute of Engineering and Technology, VNU-UET, VNU, Vietnam, 2021
5. Khanh N. Dang, "Robust Cognitive Brain-inspired Computing System: Architectures and Algorithms", 2022 4th International Conference on ICT Integration in Technical Education (ETLTC2022), Aizu-Wakamatsu, Japan, Jan 2022 (Plenary).

Honors & Awards

2015	Second Prize (the 2nd best) of Vietnamese Nhan Tai Dat Viet Award 2015. Awarded to the VENGME team.
2021	Best Student Paper Award at International Symposium on Ubiquitous Networking (UNet 2021) for paper: Ogbodo Mark Ikechukwu, Khanh N. Dang and Abderazek Ben. Abdallah, "Energy-efficient Spike-based Scalable Architecture for Next-generation Cognitive AI Computing Systems".

Languages

Vietnamese (native)

English (fluent)

References

[Available upon request]

[*CV compiled on February 7, 2023 for the website* https://u-aizu.ac.jp/~khanh/]

Aizuwakamatsu - Japan, February 7, 2023