(2) CV (Curriculum Vitae) (Last Update: June 21, 2021)

Name in full				Gender
DANG	NAM KHANH			M
FAMILY	First	Middle		
Date of Birth				Nationality
09	04	1989	32	Vietnamese
Day	Month	Year	Age	
Mailing address				
Office: Room 2.1, E4, Vietnam National University, Hanoi, 144 XuanThuy Rd., Cau Giay Distr. Hanoi, Vietnam Phone: +84-904-899-490 Fax:				
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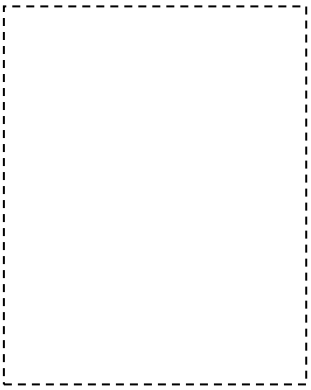

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Academic History (degree obtained, name of school) / Starting with admission to a university	
B.Sc. in Electronics & Telecommunications, VNU University of Engineering and Technology	From 09/2007 To 06/2011
M.Sc. in Information Systems & Technology, University of Paris-XI, France	From 12/2011 To 04/2014
Ph.D. in Computer Science and Engineering, The University of Aizu, Japan	From 10/2014 To 09/2017
	From Month/Year To Month/Year
	From Month/Year To Month/Year
	From Month/Year To Month/Year

Occupational History	From ~ To [Mth/Yr ~ Mth/Yr]	Institution / Position
	11/2010 – 04/2011	Dolphin Vietnam Center Ltd. / RTL Designer
	08/2011 – 09/2014	SISLAB, Vietnam National University Hanoi / Researcher
	05/2019-09/2019	The University of Aizu/ Visiting Researcher
	11/2020-03/2021	The University of Aizu/ Visiting Researcher
	11/2017 – now	VNU-UET, Vietnam National University Hanoi (VNU)/ Assistant Professor

Hobbies	Soccer, Chess	Condition of health (circle one)	(Excellent) Good Fair Poor

Marital status	Married (Unmarried)

Language ability	Grade your language ability (circle one for each language)
	English: Fluent (Advanced) Intermediate Beginner None
	Japanese: Fluent Advanced Intermediate (Beginner) None
	Specify other languages:

Affiliated academic societies	Institute of Electrical and Electronics Engineers (IEEE): Member IEEE Solid-State Circuits Society (SSCS): Member (Vietnam chapter) IEEE Circuits and Systems Society (CASS): Member (Vietnam chapter)
Official executive positions in the academic societies, Etc.	

(3) List of Publications and other Achievements

* Please indicate percentage of your contributions to each paper after your name.

* Please add other important metrics (impact factor, citations, etc.) for each paper (whenever they are available).

1. Original Papers

* Only papers already published or in press should be listed. Papers submitted but under review should be listed in "10. Other achievements".

① [Peer-Reviewed Journals]

On Web of Science Master Journal List / Scopus

1) Khanh N. Dang (55%), Akram Ben Ahmed, Abderazek Ben Abdallah, Xuan-Tu Tran, "HotCluster: A thermal-aware defect recovery method for Through-Silicon-Vias Towards Reliable 3-D ICs systems", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, (in press). (IF: 2.168, Scopus Q2).
2) Mark Ogbodo, Khanh N. Dang (15%), Abderazek Ben Abdallah, "On the Design of a Fault-tolerant Scalable Three Dimensional NoC-based Digital Neuromorphic System with On-chip Learning", IEEE Access, IEEE, Volume 9, pp 64331 - 64345, 2021 (IF: 3.745, Scopus Q1).
3) Khanh N. Dang (55%), Akram Ben Ahmed, Abderazek Ben Abdallah, Xuan-Tu Tran, "A thermal-aware on-line fault tolerance method for TSV lifetime reliability in 3D-NoC systems", IEEE Access, IEEE, Volume 8, pp 166642-166657, 2020. (IF: 3.745, Scopus Q1).
4) Khanh N. Dang (55%), Akram Ben Ahmed, Ben Abdallah Abderrazak and Xuan-Tu Tran, "TSV-OCT: A Scalable Online Multiple-TSV Defects Localization for Real-Time 3-D-IC Systems", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE, Volume 28, Issue 3, pp 672 - 685, 2020. (IF: 2.037, Scopus Q2).
5) Khanh N. Dang (55%), Michael Meyer, Akram Ben Ahmed, Abderazek Ben Abdallah, and Xuan-Tu Tran, "A non-blocking non-degrading multi-defect link test method for 3D-Networks-on-Chip", IEEE Access, IEEE, Volume 8, pp 59571 - 59589, 2020. (IF: 3.745, Scopus Q1).
6) Khanh N. Dang (55%), Akram Ben Ahmed, Yuichi Okuyama, Abderazek Ben Abdallah, "Scalable design methodology and online algorithm for TSV-cluster defects recovery in highly reliable 3D-NoC systems", IEEE Transactions on Emerging Topics in Computing (TETC), IEEE, Volume 8, Issue 3, pp 577-590, 2020. (IF: 6.043, Scopus Q1).
7) Khanh N. Dang (55%), Akram Ben Ahmed, Xuan-Tu Tran, Yuichi Okuyama, Abderazek Ben Abdallah, "A Comprehensive Reliability Assessment of Fault-Resilient Network-on-Chip Using Analytical Model", IEEE Transactions on Very Large Scale Integration Systems (TVLSI), IEEE, Volume 25, Issue 11, pp 3099-3112, 2017. (IF: 2.168, Scopus Q2).
8) Khanh N. Dang (55%), Michael Meyer, Yuichi Okuyama, Abderazek Ben Abdallah, "A Low-overhead Soft-Hard Fault Tolerant Architecture, Design and Management Scheme for Reliable High-performance Many-core 3D-NoC Systems", Journal of Supercomputing, Springer, Volume 73, Issue 6, pp 2705–2729, 2017. (IF: 2.469, Scopus Q2).

② [Peer-Reviewed Conference Proceedings]

1) Ogbodo Mark Ikechukwu, Khanh N. Dang (20%), and Abderazek Ben. Abdallah, "Energy-efficient Spike-based Scalable Architecture for Next-generation Cognitive AI Computing Systems", International Symposium on Ubiquitous Networking 2021 (UNET21), May 19 – May 22, 2021, Marakesh, Morocco. (accepted).
2) Duy-Anh Nguyen, Xuan-Tu Tran, Khanh N. Dang (15%), and Francesca Iacopi, "A lightweight Max-Pooling method and architecture for Deep Spiking Convolutional Neural Networks", 2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Dec. 8-10, 2020.
3) Khanh N. Dang (55%), Akram Ben Ahmed, Fakhrul Zaman Rokhani, Abderazek Ben Abdallah, and Xuan-Tu Tran, "A thermal distribution, lifetime reliability prediction and spare TSV insertion platform for stacking 3D NoCs", 2020 International Conference On Advanced Technologies For Communications (ATC), Nov. 8-10, 2020.
4) Ogbodo Mark Ikechukwu, Khanh N. Dang (15%), Tomohide Fukuchi, Abderazek Ben Abdallah, "Architecture and Design of a Spiking Neuron Processor Core Towards the Design of a Large-scale Event-Driven 3D-NoC-based Neuromorphic Processor", The ACM Chapter International Conference on Educational Technology, Language and Technical Communication (ETLTC), Jan. 27-31, 2020.
5) Mark Ogbodo, The Vu, Khanh N. Dang (20%), and Abderazek Abdallah, "Light-weight Spiking Neuron Processing Core for Large-scale 3D-NoC based Spiking Neural Network Processing Systems", 2020 IEEE International Conference on Big Data and Smart Computing (BigComp), Feb. 19-22, 2020.
6) Khanh N. Dang (55%), and Abderazek Ben Abdallah "An Efficient Software-Hardware Design Framework for Spiking Neural Network Systems", 2019 International Conference on Internet of Things, Embedded Systems and Communications (IINTEC), Dec. 20-22, 2019.
7) Khanh N. Dang (55%), Michael Meyer, Akram Ben Ahmed, Abderazek Ben Abdallah, and Xuan-Tu Tran, "2D-PPC: A single-correction multiple-detection method for Through-Silicon-Via Faults", 2019 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), Nov. 11-14, 2019.
8) Khanh N. Dang (55%), Akram Ben Ahmed, and Xuan-Tu Tran, " An on-communication multiple-TSV defects detection and localization for real-time 3D-ICs", 2019 IEEE 13th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Oct. 1-4, 2019.
9) Khanh N. Dang (55%), Akram Ben Ahmed, Ben Abdallah Abderrazak and Xuan-Tu Tran, "TSV-IaS: Analytic analysis and low-cost non-preemptive on-line detection and correction method for TSV defects", The IEEE Symposium on VLSI (ISVLSI) 2019, Jul. 15-17, 2019.
10) Khanh N. Dang (55%), and Xuan-Tu Tran, "Parity-based ECC and Mechanism for Detecting and Correcting Soft Errors in On-Chip Communication", 2018 IEEE 12th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Sep. 12-14, 2018.
11) Abderazek Ben Abdallah, Khanh N. Dang (35%), Yuichi Okuyama, "A Low-overhead Fault tolerant Technique for TSV-based Interconnects in 3D-IC Systems", The 18th International conference on Sciences and Techniques of Automatic control and computer engineering (STA), Dec. 21-23, 2017.

12) Shunsuke Mie, Yuichi Okuyama, Yusuke Sato, Ye Chan, Khanh N. Dang (10%), Ben Abdellash Abderazek, "Real-Time UAV Attitude Heading Reference System Using Extended Kalman Filter for Programmable SoC", 2017 IEEE 11th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC), Sep. 18-20, 2017.
13) Khanh N. Dang (55%), Michael Meyer, Yuichi Okuyama, Abderazek Ben Abdallah, "Reliability Assessment and Quantitative Evaluation of Soft-Error Resilient 3D NoC System", 25th IEEE Asian Test Symposium (ATS), Nov. 21-24, 2016,
14) Khanh N. Dang (55%), Yuichi Okuyama, Abderazek Ben Abdallah, "Soft-Error Resilient Network-on-Chip for Safety-Critical Applications", 2016 IEEE International Conference on Integrated Circuit Design and Technology (ICICDT), Jun. 27 – 29, 2016.
15) Khanh N. Dang (55%), Michael Meyer, Yuichi Okuyama, Abderazek Ben Abdallah, Xuan-Tu Tran, "Soft-Error Resilient 3D Network-on-Chip Router", IEEE 7th International Conference on Awareness Science and Technology (iCAST), Sep. 22-24, 2015,
16) Ngoc-Mai Nguyen, Edith Beigne, Suzanne Lesecq, Duy-Hieu Bui, Khanh N. Dang (10%), Xuan-Tu Tran, "H.264/AVC Hardware Encoders and Low-Power Features", 2014 IEEE Asia Pacific Conference on Circuits & Systems (APCCAS), Nov. 17-20, 2014.
17) Khanh N. Dang (55%), Xuan-Tu Tran, Alain Merigot, "An Efficient Hardware Architecture for Inter-Prediction in H.264/AVC Encoders", 17th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Apr. 23-25, 2014.
18) Hai-Phong Phan, Hung K. Nguyen, Duy-Hieu Bui, Khanh N. Dang (15%), Xuan-Tu Tran, " System-on-Chip Testbed for Validating the Hardware Design of H.264/AVC Encoder", National Conference on Electronics and Communications (REV2013-KC01), Hanoi, Dec., 2013.
19) Khanh N. Dang (55%), Van-Mien Nguyen, Xuan Tu Tran, "A VLSI Implementation for Inter-Prediction Module in H.264/AVC Encoders", 2013 International Conference on Integrated Circuits and Devices in Vietnam (ICDV), 2013,
20) Khanh N. Dang (55%), Thanh Vu Le Van, Xuan Tu Tran, "FPGA implementation of a low latency and high throughput network-on-chip router architecture", 2011 International Conference on Integrated Circuits and Devices in Vietnam (ICDV), 2011.

③ [Other Publications without Peer-Review System]

2. Books or Book Chapters

1) Book Chapter: Xuan-Tu Tran, Khanh N. Dang, and Alain Merigot, "Low Cost Inter-prediction Architecture in H.264/AVC Encoders with an Efficient Data Reuse Strategy", Advances in Engineering Research. Volume 40, Chapter 6. Nova Science Publishers, 2020. ISBN 978-1-53618-929-2.
2) Book Chapter: Khanh N. Dang and Abderazek Ben Abdallah, "Architecture and Design Methodology for Highly-Reliable TSV-NoC Systems", Invited Book Chapter, Horizons in Computer Science Research. Volume 16, Chapter 7. Nova Science Publishers, 2018. ISBN: 978-1-53613-327-1.

3. Invited Talks

1) Khanh N. Dang,"Fault-Tolerance Through-Silicon-Via For 3-D Integrated Circuits" Advanced Institute of Engineering and Technology, VNU-UET, VNU, Vietnam, 2021.
2) Khanh N. Dang, "TSV-OCT: A Scalable Online Multiple-TSV Defects Localization for Real-Time 3-D-IC Systems", The 3nd IEEE South-East Asia Workshop on Circuits and Systems (SEACAS), UPM, Malaysia, 2019.
3) Khanh N. Dang, "Toward Real-time Fault-tolerance Through-Silicon-Via based 3D Network-on-Chips", The 2nd IEEE South-East Asia Workshop on Circuits and Systems (SEACAS), Bandung, Indonesia, 2018.
4) Khanh N. Dang, "Fault-Tolerant Architectures and Algorithms for 3D-Network-on-Chips", The 1st IEEE South-East Asia Workshop on Circuits and Systems (SEACAS), Hanoi, Vietnam, 2017.

4. Teaching Experience

* Please indicate the starting and ending dates, and the language of instruction.

1) ELT3071: Real-time Embedded Systems, VNU-UET, Undergraduate, 2017 – 2019 (in Vietnamese).
2) INT3409: Robotics Programming, VNU-UET, Undergraduate, 2019 (in Vietnamese)
3) INT2212: Computer Architecture, VNU-UET, Undergraduate, 2020 (in Vietnamese)
4) ELT2401: Digital Electronics, VNU-UET, Undergraduate, 2018-2020 (in Vietnamese)
5) SYC04: Advanced Computer Organization, Uni. of Aizu, Graduate, invited lecturer in 2019 and 2021 (in English).

5. Awards or Prizes

1) Second Prize (the 2nd best) of Vietnamese Talents Award on in Information Technology, Health, Sciences and Technologies and the Environment, 2015. The Second Prize awarded to our VENGME H.264/AVC encoding chip in Grant 5 (No. QGĐA.10.02).

2) Best Student Paper Award at International Symposium on Ubiquitous Networking (UNet 2021) for paper: Ogbodo Mark Ikechukwu, Khanh N. Dang and Abderazek Ben. Abdallah, "Energy-efficient Spike-based Scalable Architecture for Next-generation Cognitive AI Computing Systems".

6. Patents

* Please indicate your contribution fraction of each intellectual property in percentage after your name.

① [Patent Applications]

1) Ben Abdallah, Huakun Huang, Khanh N. Dang (20%), Jiangning Song, "ＡＩプロセッサ (AI Processor)", 特願 2020-194733, Japan, 2020.
2) Ben Abdallah, Khanh N. Dang (40%), Masayuki Hisada, "Distance-aware Extended Parity Product Coding for multiple faults detection for on-chip links",特願 2020-171553, Japan , 2020.
3) Ben Abdallah, Khanh N. Dang (40%), "A three-dimensional system on chip in which a TSV group including a plurality of TSVs provided to connect between layers", 特願 2020-094220, Japan , 2020.
4) Ben Abdallah, Khanh N. Dang (30%), Masayuki Hisada, "A TSV fault-tolerant router system for 3D-Networks-on-Chip", 特願 2017-218953, JP2019092020A, Japan , 2020.

② [Patents Granted]

7. Received Funds/Grant

* Please indicate project achievements.

1) "Thermal-aware fault-tolerance Through-Silicon-Via based 3D interconnect", main PI, funded by National Foundation for Science and Technology Development (NAFOSTED) under No. 102.01-2018.312 (2019-2021). Project achievement: three publications in Web of Science Master Journal List.

2) "Soft Error Resilient Architecture and Algorithm for Network-on-Chip": main PI, funded by VNU-UET under project CN18.10 (2018-2019) Project achievement: one publications in IEEE conference, one publication in VNU journal.
3) "Development of IoT Dual Band Transmitters for Agriculture" (IOTA)", co-PI, funded by the Ministry of Science and Technology (World Bank project) (2018-2019)
4) "Reconfiguration Solution in Designing Network-on-Chip Architectures", co-PI, funded by National Foundation for Science and Technology Development (NAFOSTED) under No. 102.01-2013.17. (2014-2016). Project achievement: two publications in Web of Science Master Journal List.
5) "Investigation, Design, and Implementation of a Video Encoder for Next Generation Multimedia Equipment", member, funded by Vietnam National University, Hanoi (VNU) under No. QGĐA.10.02. (2010-2013). Project achievement: 1) H264. Encoding Chip in Global Foundry CMOS 13nm with 4mm×4mm die size, 100MHz, 1.2V, 32mW, QFP256; 2) Second Prize (the 2nd best) of Vietnamese Talents Award on in Information Technology, Health, Sciences and Technologies and the Environment, 2015.

8. Collaboration with Local Communities or Industry

* Please indicate project achievements.

9. Summary of Research Experiences/Achievements

1) H.264/AVC encoding chip design in SISLAB, Vietnam National University, Hanoi: This project was funded by Vietnam National University, Hanoi (VNU) under Project No. QGĐA.10.02. (2010-2013). Our group design a full hardware H.264/AVC encoding. I participate as a core member to design the inter-prediction part of the encoding process.

Achievements:

- Fabricated chip in Global Foundry CMOS 13nm with 4mm×4mm die size, 100MHz, 1.2V, 32mW, QFP256.
- Second Prize (the 2nd best) of Vietnamese Talents Award on in Information Technology, Health, Sciences and Technologies and the Environment, 2015.

1) Fault-tolerance design for 3D Network-on-Chip: I join the project as a Ph.D. student in Adaptive System Laboratory, The University of Aizu. The main objective is to design a comprehensive fault-tolerant design of 3D Network-on-Chip (3D-NoC) which support all type of defects: transient, intermittent and permanent. The 3D-NoC uses Through-Silicon-Vias as inter-layer interconnect.

Achievements:

- Three published journal papers (peer-reviewed journal papers 6,7, and 8). Four IEEE conference papers (peer-reviewed conference papers: 11, 13, 14, and 15).

2) Thermal-aware fault-tolerance 3D-ICs: This research was funded by NAFOSTED under No. 102.01-2018.312 and VNU-UET under CN 18.10.

The first phase of the research targets to use stastiscal analysis for detecting and localizing defective wires in Integrated Circuits. We apply the coding technique for inter-layer vias (TSV in 3D-ICs) and inter-router wires. The stastiscal error correction code method uses error correction codes in several cycles with adaptive mechanism for detecting and localizing faults.

The second phase of the system is to investigate the impact of high operating temperature on the system reliability focusing on TSV technology for 3D-ICs

Achievements:

- Four journal papers On Web of Science Master Journal List / Scopus (peer-reviewed journal papers 1,3, 4 and 5).
- Five IEEE conference papers (peer-reviewed conference papers: 3,7,8,9,10)

- Two Japanese patent applications (特願 2020-171553 and 特願 2020-094220)

3) **Neuromorphic Computing:** This is on-going project where we develop hardware for neuromorphic computing that mimics the behavior of biological brains. We developed LIF neuron with STDP learn and grouped them into clusters. Clusters of neurons are mapped into 3D-NoC. We also support full platform of deploying neuromorphic systems.
   Achievements:
   - One journal paper On Web of Science Master Journal List / Scopus (peer-reviewed journal paper 2).
   - Five IEEE conference papers (peer-reviewed conference papers: 1,2,4,5, and 6)
   - Two papers under major revision (IEEE TETC and Frontiers in Neuroscience)
   - One paper under review (Elsevier Microprocessors and Microsystems)
   - One Japanese patent application (特願 2020-194733)

10. Future Plans for Research and Education

[Research]

My research interests lie in the broad area of integrated circuits and computer architecture. In the near future, I plan to work on two main research topics: (1) **Neuromorphic Computing** and (2) **Machine Learning-based VLSI design**. My first topic is neuromorphic computing that targets to be performed on stand-alone embedded systems. Specifically, I target to design a completed platform from neuromorphic computing from specification, system model to hardware execution. The neuromorphic models and applications are first developed in software for debugging purposes. Then, I plan to support the mapping process from software to hardware system. The hardware system also supports on-chip learning for augmenting the performance in real-time. My second topic is Machine Learning-based VLSI design. In this topic, I develop a theoretical approach and practical approach for optimizing multiple objectives (for instance: reliability, temperature, area cost, performance) a large-scale VLSI system. I planned to apply machine learning techniques to optimize the system.

1) Architecture support for **Neuromorphic Computing**: Neuromorphic Computing (NC) is the emerging computing paradigm that mimics the operations of biological brains. The system is a set of neurons connected via weighted connections (synapses) and operated via spike operations. While NC can be simulated in software by a large-scale computing system or GPU, shifting to hardware architecture for NC allows us to have energy-efficiency accelerated execution. This allows NC to be performed in a wide range of applications: from Internet-of-Thing applications to high-performance computing (HPC) systems.

   Unlike Von Neumann's architecture, neuromorphic computing systems are not mature yet, especially for 3D-ICs architecture and fault-tolerance. While 3D-IC technology brings a smaller footprint and lower performance, large-scale and high operating temperature of neuromorphic computing confronts the reliability issues. Therefore, these problems need to be tackled in order to bring neuromorphic computing to be widely used.

   I consider the operation of neuromorphic computing need to satisfy three requirements: low power consumption, real-time, and dependability. The low power consumption of neuromorphic computing systems can be obtained by spike-based operations and extensive clock and power gating. Moreover, shifting to 3D-ICs allows the system to have a smaller footprint; therefore, it can shorten the wire lengths to deliver lower power consumption. Lower latencies due to the shorter distance of 3D-ICs is also an important benefit to ensure the real-timeliness of the system. Moreover, Network-on-Chip is the de facto communication paradigm for NC. Therefore, introducing 3D NoC could even enhance communication performance.

   On the other hand, by having a large-scale NC system with millions of neurons and billions of synapses, the accumulated fault probability could introduce more frequent faults during manufacture and operation. Having a high

operating temperature also leads to a shorter lifetime expectancy.

With my experiences in 3D-ICs and 3D-NoCs, I will characterize the NC applications to identify their constraints and requirements. After determining the bottlenecks and opportunities, I will focus on designing NC systems that provide the required capability. For example, using a machine-learning algorithm to optimize the communication cost. Here, we can decide which cluster a neuron belongs to and where a cluster is put within the 3D-NoCs.

Another direction I plan to pursue is to provide a large-scale fault-tolerant feature for NC systems. For example, my research on NC has explored using graph theory to remap the faulty neurons during operation. By using the max-flow min-cut theorem to find the maximum neuron that can be migrated from clusters to clusters. Applying genetic algorithms for optimizing the migration and communication of the recovery phase is also investigated. This can open a new approach to the self-correction NC system.

2) **Machine Learning-based VLSI design**: Designing and maintaining large-scale VLSI systems confronts multiple objectives. For example, the common optimization objectives are area cost, power consumption, latency and reliability.

As the complexity of the systems has evolved significantly to have millions or billion transistors, these multiple objectives optimization problems become more complicated. For example, new technologies such as sub-micron or 3D-ICs also introduce lower power consumption, smaller footprints but more fault sensitivity and higher operating temperature. In my previous research, I only consider reliability as the single objective of the design process; however, it might lead to high power consumption and a larger area.

In this topic, I consider that the VLSI systems should be approached comprehensively: from theoretical analyses to design phases and physical experiments. My research has been focused on using reliability theory to access the overall reliability of a system. I also designed several systems with fault detection, fault localization, and fault recovery. With my experience from the theory to the design phases, I will adapt to the new reliability issue of the new technology and architecture. I have investigated the usage of Genetic Algorithm in the reliability-aware design (see Conference paper 3). Instead using a simple grid search, I optimize the area cost by reducing the redundancies while maintaining similar reliability. In the future, multiple objective optimization (for example: GA platform such as NSGA-II) can be used and adapted into our system.

Another direction I plan to pursue is to optimize the operating temperature for a reliable system. Task mapping and task migration are considered in the process to reduce the operating temperature while the performance must be preserved. There are several objectives in the large scale VLSI system. I can also link this research topic to the NC research to optimize the NC platform, especially at a large scale.

[Education]

(a) Emphases to be placed regarding education

As a teacher and mentor, I aim to develop three main skills in the students: (1) the ability solve problems with critical thinking, (2) the ability to learn on their own and find new challenging problems, (3) the ability to think about the big picture and the details simultaneously, and (4) the ability to communicate at the correct level of abstraction. I think it is better to learn by doing, and the interaction improves the learning efficiency in the students. Therefore, I always design courses with project components, class presentations, and encourage discussions. I believe that showing enthusiasm and humor while teaching appeals the students' interests. I also think providing the fundamentals as well as intellectual challenges is important for students. Finally, I believe that being reflective about one's own teaching and paying attention to student feedback is crucial to improving the teaching experience.

Since my master studies, I have had the opportunities to get involved in teaching and mentoring students. In my master and phd studies, I served as teaching assistant in Digital Design, and Computer Architecture classes. After rejoined VNU University of

Engineering and Technology (VNU-UET), I have started to teach courses on my own and with my colleagues. I also start to mentor students since then. I have been teaching Real-time Embedded Systems (ELT3071) – an undergraduate level course in VNU-UET. Beside teaching fundamental topics, I have focused on project based learning where I predesign a system for the students. The students can design their own mini-games that allow them to understand the topics and the requirements for real-time systems. I also did teach the practical part of Robotics Programming (INT3409), which includes computer vision, machine learning and system control. Other courses are Digital Electronics (ELT2401) and Computer Architecture (INT2212). Both are undergraduate levels and focused on building the theoretical background for the students in computer engineering fields. In addition, I delivered two guest lectures for Prof. Abderazek Ben Abdallah in Advanced Computer Organization (SYC04) which I talked about designing 3D Network-on-Chip in VLSI technology and further applications.

I also experienced with mentoring students since I was master and Ph.D. students. I had an abundant opportunities to mentor junior students in the laboratory. I also mentored student on my own since I started working as an assistant professor at VNU-UET. One group of students I mentored did won the first prize of IEEE SEACAS Hackathon and participated the IEEE CASS student competition in ISCAS 2020. As I collaborated with Prof. Abderazek Ben Abdallah in the University of Aizu, I help mentor Mr. Mark Ogbodo who is a Ph.D. student. Mr. Mark Ogbodo successfully published several papers, won the best student paper award at UNET-2021.

(b) Concrete goals of educational activities

I am eager to teach courses on computer organization, architecture, microarchitecture, and hardware design at all levels. I am also interested in teaching similar courses on special topics in computer architecture. Moreover, I would like to help develop and teach course on architecture design for machine learning at the graduate level, which provides a deeper understanding of the machine learning algorithms with emphases on the applications and implementations on architecture. I also can teach introductory courses on operating system, distributed system, embedded system and programming languages.

I am also enthusiastic about mentoring students, especially at graduate levels and focused on computer architecture, microarchitecture and hardware design. Along with my current research topics, I am interested in mentoring students in hardware and system design for machine learning systems and fault-tolerance. For long-term activities, I would like to focus on hardware design for emerging computing systems. I want to nurture the enthusiasm of the students, encourage them to tackle difficult problems and exploring new research topics.

11. Other Achievements

Paper under-review:

1) Khanh N. Dang (55%), Nguyen Anh Vu Doan, Abderazek Ben Abdallah, "MigSpike: A Migration Based Algorithm and Architecture for Scalable Robust Neuromorphic Systems", IEEE Transactions on Emerging Topics in Computing (TETC), IEEE, (under major revision). (IF: 6.043, Scopus Q1).
2) Abderazek Ben Abdallah, Khanh N. Dang (45%), "Towards Robust Cognitive 3D Brain-inspired Cross-paradigm System", Frontiers in Neuroscience (under major revision). (IF: 3.707, Scopus Q2).
3) Duy-Anh Nguyen, Xuan-Tu Tran, Khanh N. Dang (15%), and Francesca Iacopi, "A Low-Power, High-Accuracy with Fully On-Chip Ternary Weight Hardware Architecture for Deep Spiking Neural Networks", Microprocessors and Microsystems, Elsevier, (under review), (IF: 1.161, Scopus Q3).

Book under-preparation:

1) "Neuromorphic Computing Principles and Organization", Abderazek Ben Abdallah, Khanh N. Dang, Springer.

Other Journals (peer-reviewed, local journals):

1) Khanh N. Dang, Akram Ben Ahmed, Ben Abdallah Abderrazak and Xuan-Tu Tran, "Thermal distribution and reliability prediction for 3D Networks-on-Chip", VNU Journal of Computer Science and Communication Engineering, Vietnam National University , Hanoi (VNU), Volume 36, No 1, pp 65-77, 2020.
2) Khanh N. Dang, Michael Meyer, Akram Ben Ahmed, Abderazek Ben Abdallah, and Xuan-Tu Tran, "2D Parity Product Code for TSV online fault correction and detection", REV Journal on Electronics and Communications (JEC), The Radio and Electronics Association of Vietnam (REV), pp. 11-21, Vol. 8, No. 1-2, Jan. - Jun., 2020.
3) Khanh N. Dang, and Xuan-Tu Tran, "An adaptive and high coding rate soft error correction method in Network-on-Chips", VNU Journal of Computer Science and Communication Engineering, Vietnam National University , Hanoi (VNU), Volume 35, No 1, pp 32-45, 2019.
4) Ngoc-Mai Nguyen, Edith Beigne, Duy-Hieu Bui, Khanh N. Dang, Suzanne Lesecq, Pascal Vivet, Xuan-Tu Tran, "An Overview of H.264 Hardware Encoder Architectures including Low-Power Features", REV Journal on Electronics and Communications (JEC), The Radio and Electronics Association of Vietnam (REV), pp. 8-17, Vol. 4, No. 1-2, Jan. - Jun., 2014.

Conferences Organizing

1) Organizing Committee Member: IEEE 14th International Symposium on Embedded Multicore/Manycore SoCs (MCSoC-2021)
2) TPC co-chair: IEEE 2020 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS-2020). APCCAS is a regional flagship conference of IEEE Circuit and System Society.
3) TPC co-chair: IEEE 13th International Symposium on Embedded Multicore/Manycore SoCs (MCSoC-2019)
4) Publication chair: IEEE 13th International Symposium on Embedded Multicore/Manycore SoCs (MCSoC-2018)

TPC member: MCSoC 2018, MCSoC 2019, ICCE 2020, APCCAS 2020, MCSoC 2021

Reviewer

- Journal
    1) ACM Journal on Emerging Technologies in Computing Systems
    2) Elsevier Journal of Systems Architecture
    3) IEEE Transactions on Circuits and Systems I : Regular Papers
    4) IEEE Access
    5) Journal of Supercomputing
    6) Microprocessors and Microsystems
- Conference
    1) IEEE MCSoC 2017, 2018, 2019
    2) IEEE ATC 2020
    3) IEEE APCCAS 2020
    4) IEEE ICCE 2020
    5) IEEE ISCAS 2021

Student mentoring:

1) IEEE SEACAS 2019 Hackathon, "Magic Spoon": First prize. The project is to develope a prototype of "Magic Spoon" which can compensate the vibration (shaking) of Parkinson patient's hand. Instead of using conventional PID, our students developed a single layer perceptron to control the servo motor. Database and Andriod app are also developed to provide the ability to diagnosis and proper treatment. The project is selected for 2019-2020 CASS Student Design Competition Finalists in IEEE ISCAS 2020.
2) 2019-2020 IEEE CASS Student Design Competition Finalists. "Application for Parkinson's Disease Detection" in IEEE ISCAS 2020.