

Task 5.2

Vending Machine:

- (1) Estimated clock period: 4.604ns
- (2) Worst case latency: Latency(cycles) = 0, Latency(ns) = 0.0
- (3) Number of FFs utilized: 33
- (4) Number of LUTs utilized: 155

Synthesis Summary(solution1) ×vending_machine.cpp

Synthesis Summary Report of 'vending_machine'

General Information

Date:Fri Dec 6 18:00:56 2024

Version: 2023.1 (Build 3854077 on May 4 2023)

Project: Ha_Do_2407698_E5

Solution:solution1 (Vivado IP Flow Target)

Product family:zynq

Target device:xc7z020-clg484-1

Timing Estimate

Target	Estimated	Uncertainty	
10.00 ns	4.604 ns	2.70 ns	

Performance & Resource Estimates ⓘ

ModulesLoops

Modules & Loops	Issue Type	Violation Type	Distance	Slack	Latency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM	
vending_machine				-	0	0.0		-	1	-	no	0	0	33	155	0

Debouncer:

- (1) Estimated clock period: 7.303ns
- (2) Worst case latency: Latency(cycles) = 0, Latency(ns) = 0.0
- (3) Number of FFs utilized: 69
- (4) Number of LUTs utilized: 302

debouncer.cpp

Synthesis Summary(solution1) x

Date: Fri Dec 6 19:39:07 2024

Version: 2023.1 (Build 3854077 on May 4 2023)

Project: debouncer

Solution: solution1 (Vivado IP Flow Target)

Product family: zynq

Target device: xc7z020-clg484-1

Timing Estimate

Target	Estimated	Uncertainty	
10.00 ns	7.303 ns	2.70 ns	

Performance & Resource Estimates ⓘ

Task 5.3

In general, working with FPGA programming in VHDL is challenging because it operates at a low level, requiring extensive coding to design and handle logical systems. However, it offers a deeper understanding of hardware programming and simulations

compared to C++, which operates at a higher abstraction level. In contrast, FPGA programming in C++ with High-Level Synthesis (HLS) is more accessible and user-friendly, especially for individuals without experience in hardware design or working with binary numbers. Nevertheless, this approach has drawbacks, as users might not gain a comprehensive understanding of how the hardware functions since the underlying processes are expressed in binary and abstracted away by HLS.

In the case of the vending machine project, the generated VHDL code in Vitis HLS is not particularly readable due to its length and complexity. However, it is still somewhat understandable because variables and signals are clearly declared based on their data types, and conditional statements such as if-else are used to manage the system's operations as expected.