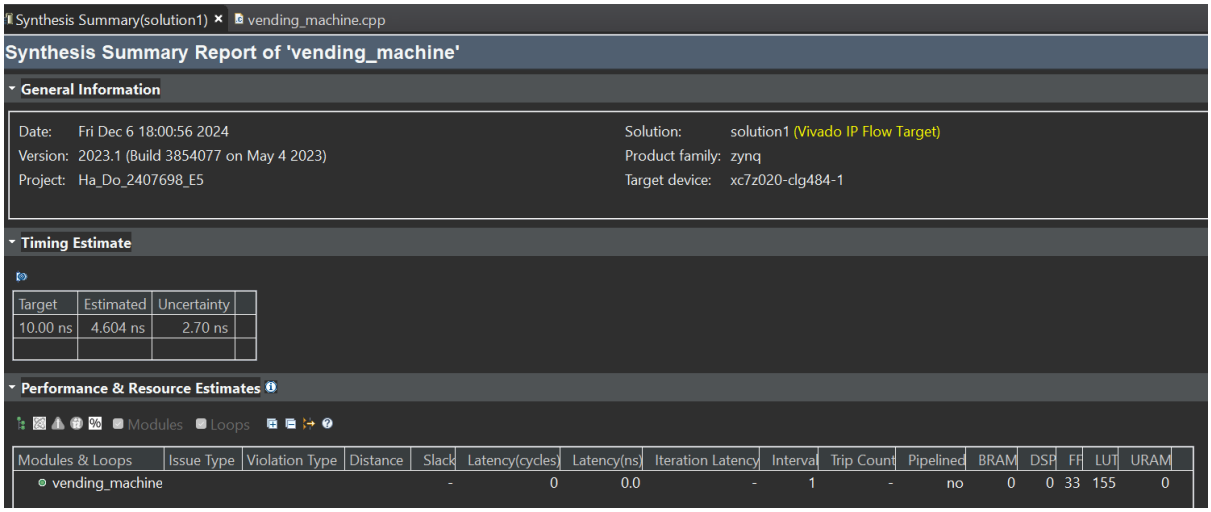
Task 5.2

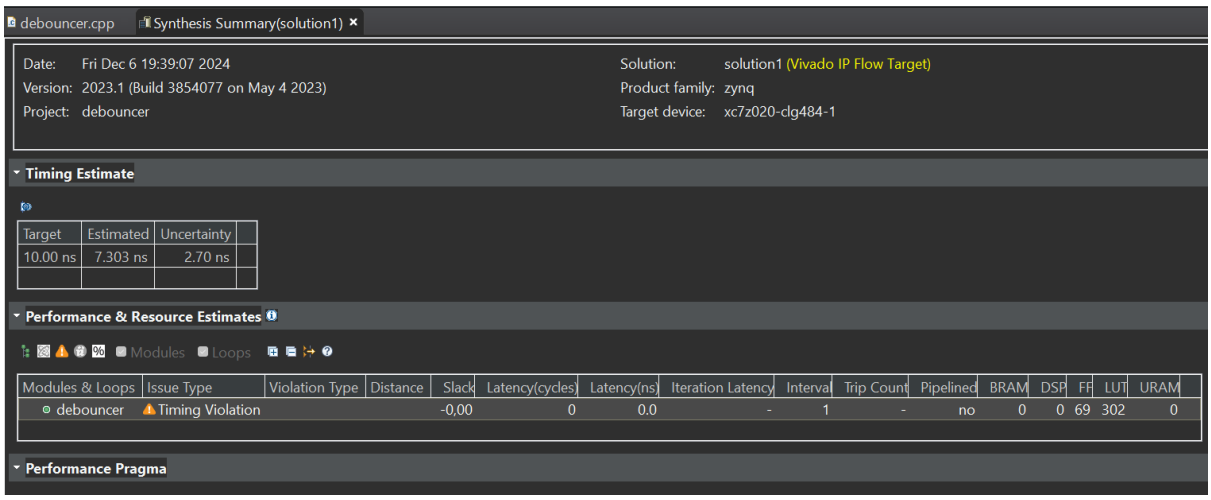
Vending Machine:

(1) Estimated clock period: 4.604ns
(2) Worst case latency: Latency(cycles) = 0, Latency(ns) = 0.0
(3) Number of FFs utilized: 33
(4) Number of LUTs utilized: 155



Debouncer:

(1) Estimated clock period: 7.303ns
(2) Worst case latency: Latency(cycles) = 0, Latency(ns) = 0.0
(3) Number of FFs utilized: 69
(4) Number of LUTs utilized: 302



Task 5.3

In general, working with FPGA programming in VHDL is challenging because it operates at a low level, requiring extensive coding to design and handle logical systems. However, it offers a deeper understanding of hardware programming and simulations

compared to C++, which operates at a higher abstraction level. In contrast, FPGA programming in C++ with High-Level Synthesis (HLS) is more accessible and user-friendly, especially for individuals without experience in hardware design or working with binary numbers. Nevertheless, this approach has drawbacks, as users might not gain a comprehensive understanding of how the hardware functions since the underlying processes are expressed in binary and abstracted away by HLS.

In the case of the vending machine project, the generated VHDL code in Vitis HLS is not particularly readable due to its length and complexity. However, it is still somewhat understandable because variables and signals are clearly declared based on their data types, and conditional statements such as if-else are used to manage the system's operations as expected.