Cohn Topology-based 1:8 Power Divider for S-Band Array Antenna Feeding Network

Achmad Munir[1†], Endon Bharata[1], Edwar[2]
[1]Radio Telecommunication and Microwave Laboratory, School of Electrical Engineering and Informatics
Institut Teknologi Bandung, Indonesia
[2]School of Electrical Engineering, Telkom University, Bandung, Indonesia
[†]munir@ieee.org

***Abstract*—In this paper, a design of 1:8 power divider is proposed for S-band array antenna feeding network. The proposed power divider which is designed based on Cohn topology is implemented on an RO4003C™ dielectric substrate which has the relative permittivity and the thickness of 3.55 and 1.524mm, respectively. Seven pairs of 1:2 power divider are used to construct the design of 1:8 power divider. Some parameters such as insertion, isolation and voltage standing wave ratio (VSWR) are used to analyze the performance of power divider in the frequency range of 2–4GHz. The result shows that the 1: 2 power divider has the values of insertion loss, isolation and VSWR of greater than 3.08dB, greater than 24dB, and less than 1.1, respectively. Meanwhile, the 1:8 power divider has the insertion value of greater than 9.26dB, isolation value of greater than 23dB, and VSWR value of less than 1.5. The characterization result has shown an adequate performance for S-band array antenna feeding network of radar system.**

***Keywords*—Array antenna; Cohn topology; feeding network; power divider; radar system.**

I. Introduction

In recent years, the commitment of government to being self-sufficient in fulfilling the needs of domestic defense equipment and its development including radar has stimulated the interest of academicians and researchers in conducting more in-depth research in related fields. This is indicated by the growth of several research centers focused on radar development as well as numerous radar-based components which high enough percentage of local content. One of the most commonly used components for radar system is power divider which is used for feeding the array antenna [1]–[2]. Unfortunately the power divider still needs to be ordered from abroad. This is the reason for the importance of proposing the design of power divider so that the dependence on such component can be gradually reduced, as well as to raise up the local content.

Basically a power divider or sometimes referred as power splitter is an equipment that has the capability to divide or split a signal power from a device to be spread out into some other devices. It has a 3-port T-network circuit which can be imagined as a 4-port hybrid T-network in which two series ports are terminated internally with a load without reflection [3]. Input power on parallel port of power divider will produce output power with equal amplitude and phase at 2 other output ports. For an ideal power divider, the return loss on each port is almost null, meanwhile the insertion loss of each output port or in other term called as the isolation is huge. Several techniques related to the design of a 3-port hybrid power divider module have been developed by researchers in which some of them have been reported in [4]–[12]. One of the most widely known design techniques is the Wilkinson method which proposed a power divider using stripline with 8 output ports [4]. It was reported that the proposed power divider performed well theoretically for the frequency range of 450-550MHz. However, at the center frequency of 500MHz the measured minimum isolation was 27dB although it was not constant for all output terminals.

Instead of employing Wilkinson method, in this paper, a 1:8 power divider is designed based on Cohn topology for S-band array antenna feeding network. The used of Cohn topology which consists of N-pairs multisection circuit is aimed to produce wide bandwidth response of power divider. It is developed from 7-pairs of 1:2 power divider workable in the frequency range of 2–4GHz. An RO4003C™ dielectric substrate with the relative permittivity of 3.55 and the thickness of 1.524mm is applied for the deployment. Prior investigation through simulation software, an overview of theoretical approach is presented especially for designing 1:2 power divider. Meanwhile, some essential parameters such as insertion, isolation and VSWR will be used to analyze its performance over the working frequency range. After result discussion, the conclusion is pointed out consecutively.

II. Overview of Power Divider

As illustrated in Fig. 1, the basic circuit of a symmetric 3-port power divider consists of N pairs of equal-length transmissions line and N bridging resistor split from port 1 to ports 2 and 3 [3]. The circuit is used to simplify the model of power divider applicable in the analysis of power dividing process. Due to the symmetrical circuit, the analysis method employs even mode and odd mode excitations of ports 2 and 3 with a Z_0 load connected to port 1. Furthermore, as the circuit can be imagined as a 4-port hybrid T-network, then the case of 4-port symmetrical structure discussed in [13] can be used to assist the analysis process. It is noted that the use of N-pairs multisection circuit is sometimes effective to improve the bandwidth response of power divider designed based on Wilkinson topology.

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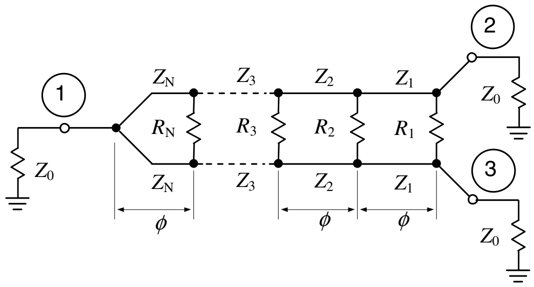

Fig. 1. Basic circuit of a symmetric 3-port power divider [3].

When the even mode excitation is used, the signal with equal-phase and amplitude is fed into ports 2 and 3. In such conditions, all pairs of junction points along the transmission line have no voltage difference, hence there is no power dissipated to the resistor. The output power at port 1 is the total power resultant of incoming power at ports 2 and 3 with the reflected power in port 1 due to the impedance mismatch. Since there is no current flow across from port 2 to port 3 or vice versa, the circuit in Fig. 1 can be replaced by a two-symmetrical circuit which is identic to port 1 on a $2Z_0$ load, as shown in Fig. 2.

Moreover, when the odd mode excitation is used, as in the even mode excitation, ports 2 and 3 are fed with the equal-amplitude signal but different phases of 180° each other along the transmission line. Under this condition, the resistor will have a voltage difference according to the value of resistance. However, since the circuit is symmetric, the midpoint of connecting resistor and connecting point on port 1 will have a zero potential (Z = 0). Therefore the circuit can be represented by a two-symmetrical circuit which is identic to port 1 on a zero potential as depicted in Fig. 3.

By using the case of 4-port symmetrical structure in [13] for the 3-port symmetrical circuit of power divider, the correlation of transmission coefficient for each port with the reflection coefficient for even mode and odd mode can be theoretically predicted as expressed in (1)–(4) [3]. It is assumed that the reflection coefficients of even mode and odd mode are Γ_e and Γ_o, respectively. Whilst the reflection and transmission coefficients for each port are Γ_1, Γ_2, Γ_3, T_{12}, T_{13}, and T_{23}.

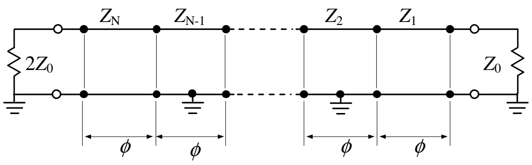

Fig. 2. A two-symmetrical circuit for even mode excitation [3].

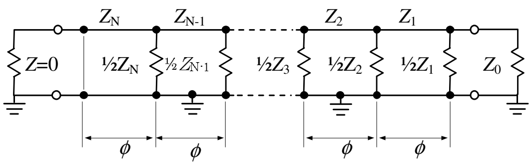

Fig. 3. A two-symmetrical circuit for odd mode excitation [3].

$$|\Gamma_1| = |\Gamma_e| \tag{1}$$

$$\Gamma_2 = \Gamma_3 = \tfrac{1}{2}\left(\Gamma_e + \Gamma_o\right) \tag{2}$$

$$T_{12} = T_{13} = \sqrt{\tfrac{1}{2}\left(1 - \Gamma_e^2\right)} \tag{3}$$

$$T_{23} = \tfrac{1}{2}\left(\Gamma_e - \Gamma_o\right) \tag{4}$$

III. Simulation Result and Discussion

A. 1:2 Power Divider

Based on theoretical approach explained above, the 1:2 power divider is implemented by use of Cohn topology. Fig. 4 shows the design of 1:2 power divider (N = 2) with the length of transmission line of $\lambda/4$. The wavelength (λ) is taken from the center frequency of S-band, i.e. 3GHz. By employing the normalized parameter of 3-port symmetrical circuit of power divider [3], the values of Z_1, Z_2, R_1 and R_2 can be determined. Then, by denormalizing them with the intrinsic impedance (Z_0) of 50_Ω, the values of Z_1, Z_2, R_1 and R_2 are obtained to be 60.99_Ω, 81.99_Ω, 241.02_Ω and 98.01_Ω, respectively. The 1:2 power divider is deployed on an RO4003C™ dielectric substrate with the relative permittivity of 3.55 and the thickness of 1.524mm.

By taking into account for the parameters of RO4003C™ dielectric substrate, the impedance Z_0, Z_1 and Z_2 can be realized using a microstrip line with the width, length and

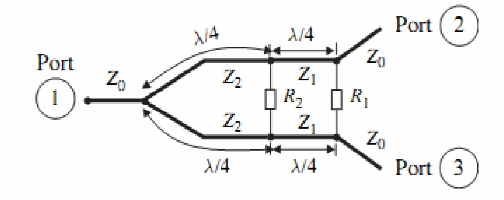

Fig. 4. Design of 1:2 power divider based on Cohn topology.

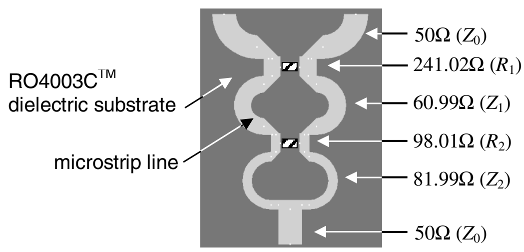

Fig. 5. Layout of a 1:2 power divider implemented using microstrip line.

TABLE I. Parameters of Microstrip Line.

Parameter	Characteristic Impedance		
	Z_0	Z_1	Z_2
Width (mm)	3.369	2.398	1.324
Length (mm)	59.6	60.5	61.9
Attenuation (dB/m)	1.92	1.93	2.07

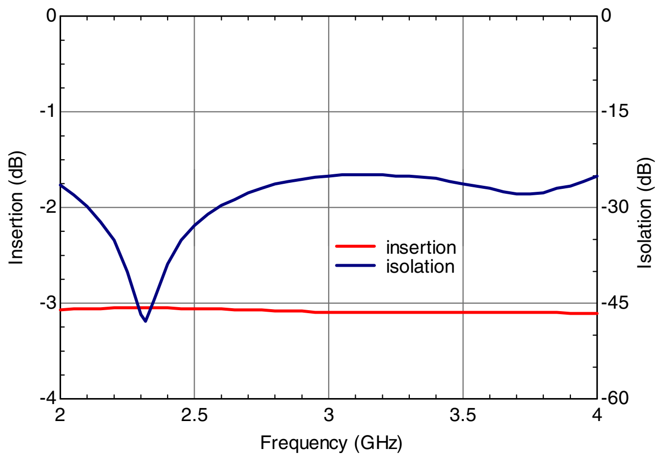

Fig. 6. Insertion of port 1 and isolation between ports 2 and 3 for proposed 1:2 power divider.

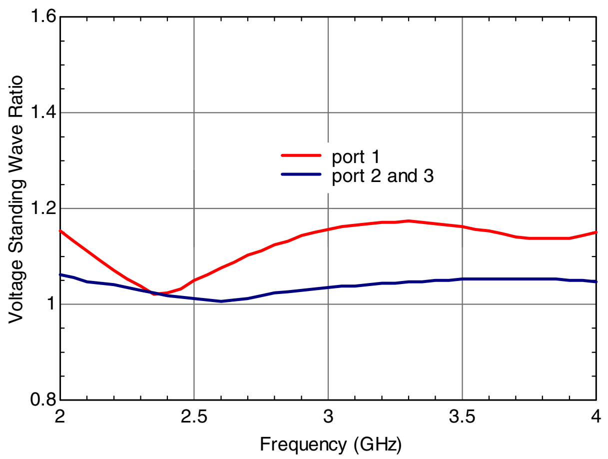

Fig. 7. VSWR of each port for proposed 1:2 power divider.

attenuation as tabulated in Table I. Fig. 5 illustrates the layout of a 1:2 power divider implemented using microstrip line on a 1.542mm thick RO4003C^{TM} dielectric substrate. The simulation result of insertion and isolation for the 1:2 power divider is plotted in Fig. 6, while Fig. 7 depicts the simulated VSWR of each port. The results shows that the proposed 1:2 power divider has good performance with insertion, isolation and VSWR values of greater than 3.08dB, greater than 24dB, and smaller than 1.1, respectively. These results have satisfied the required specification for desired application in which the minimum isolation is higher than 20dB.

B. 1:8 Power Divider

Next, to implement a 1:8 power divider, 7-pairs of 1:2 power divider are required to be constructed in such away as shown in Fig. 8. The layout of 1:8 power divider is deployed on a 1.542mm thick RO4003C^{TM} dielectric substrate with the dimension of 150mm $\times$ 95mm. It is noted that each 1:2 power divider is taken from the previous design based on Cohn topology, therefore the performance of 1:8 power divider mostly depends on the characteristic of 1:2 power divider. The performance of proposed 1:8 power divider is then analyzed through simulation software.

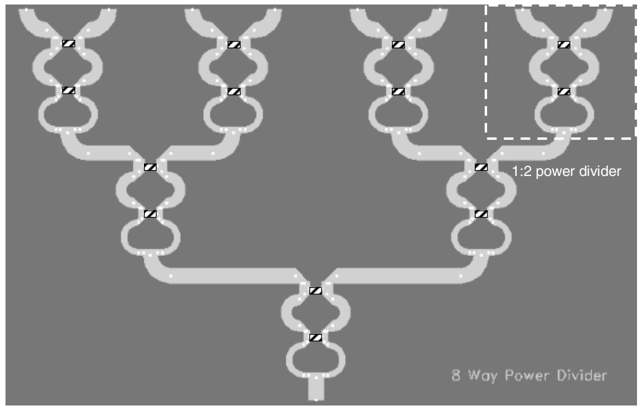

Fig. 8. Layout of a 1:8 power divider implemented using 7-pairs of 1:2 power divider.

The simulation results of insertion, isolation and VSWR values for 1:8 power divider are plotted in Figs. 9–10. From the results, although the performance of 1:8 power divider is less good than the 1:2 power divider, in general the designed 1:8 power divider has adequate performance which acceptable

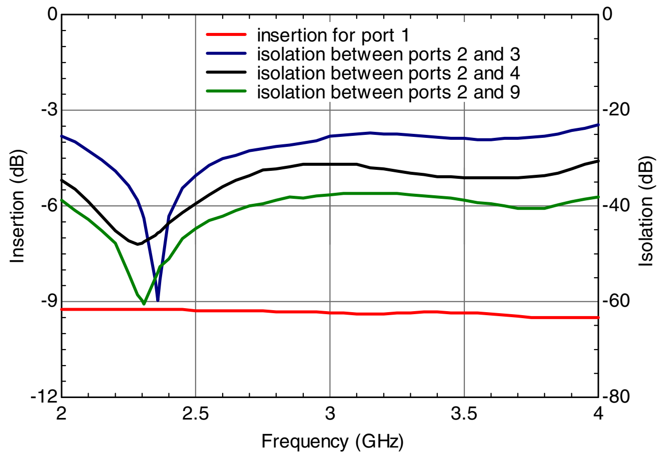

Fig. 9. Insertion of port 1 and isolation between ports 2 and 3 for proposed 1:2 power divider.

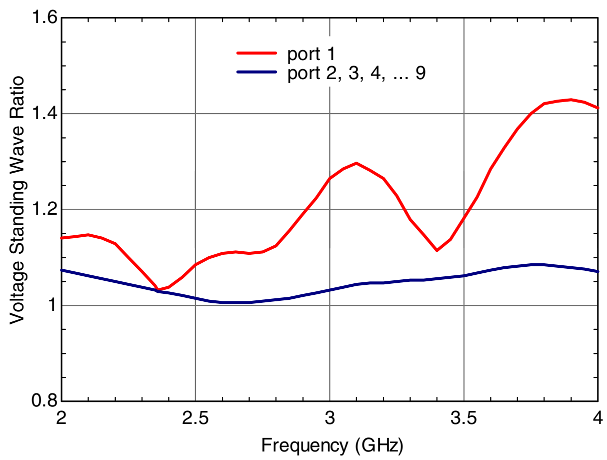

Fig. 10. VSWR of each port for proposed 1:2 power divider.

for S-band array antenna feeding network of radar system. The results show that the proposed 1:8 power divider has the insertion value of greater than 9.26dB, isolation value of greater than 23dB, and VSWR value of smaller than 1.5.

IV. Conclusion

The design of a 1:8 power divider for S-band array antenna feeding network has been demonstrated with the assist of simulation software. The performance of proposed power divider has been investigated through its parameters including insertion, isolation and VSWR. From the results, although there was slight differences in the performance between 1:2 power divider and 1:8 power divider, however in general the designed power dividers have satisfied and been acceptable for the desired application in radar system. In addition, further development of power divider to feed 16 elements of array antenna is still in progress where the performance is expected to be presented in the near future.

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