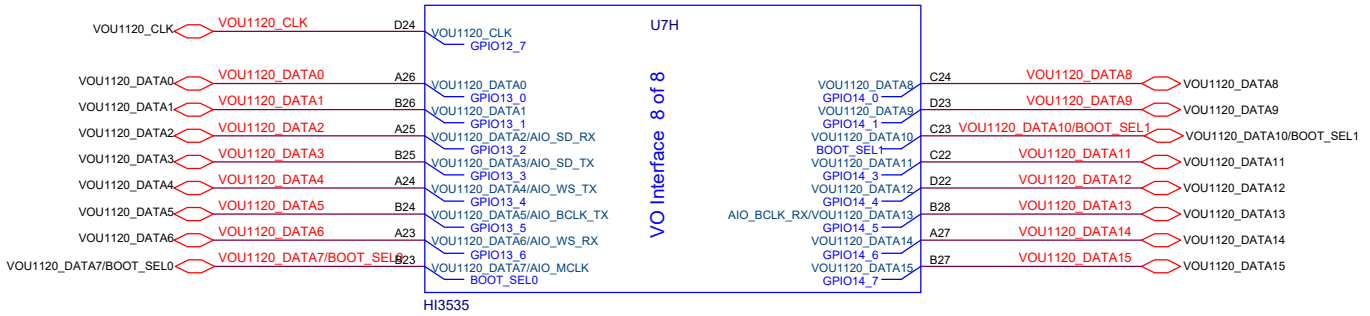
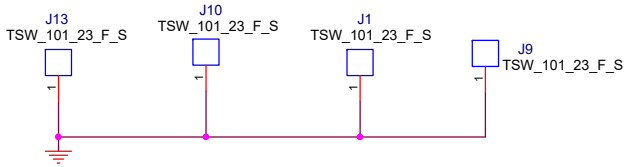
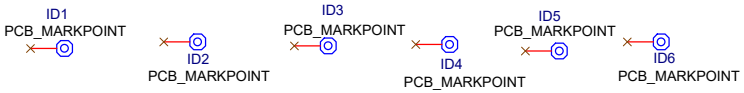
VO


U7H
VO Interface 8 of 8
HI3535
VOU1120_CLK
VOU1120_CLK
D24
VOU1120_CLK
GPIO12_7
VOU1120_DATA0
VOU1120_DATA0
A26
VOU1120_DATA0
GPIO13_0
VOU1120_DATA1
VOU1120_DATA1
B26
VOU1120_DATA1
GPIO13_1
VOU1120_DATA2
VOU1120_DATA2
A25
VOU1120_DATA2/AIO_SD_RX
GPIO13_2
VOU1120_DATA3
VOU1120_DATA3
B25
VOU1120_DATA3/AIO_SD_TX
GPIO13_3
VOU1120_DATA4
VOU1120_DATA4
A24
VOU1120_DATA4/AIO_WS_TX
GPIO13_4
VOU1120_DATA5
VOU1120_DATA5
B24
VOU1120_DATA5/AIO_BCLK_TX
GPIO13_5
VOU1120_DATA6
VOU1120_DATA6
A23
VOU1120_DATA6/AIO_WS_RX
GPIO13_6
VOU1120_DATA7/BOOT_SEL0
VOU1120_DATA7/BOOT_SEL0
B23
VOU1120_DATA7/AIO_MCLK
BOOT_SEL0
VOU1120_DATA8
GPIO14_0
C24
VOU1120_DATA8
VOU1120_DATA8
VOU1120_DATA9
GPIO14_1
D23
VOU1120_DATA9
VOU1120_DATA9
VOU1120_DATA10
BOOT_SEL1
C23
VOU1120_DATA10/BOOT_SEL1
VOU1120_DATA10/BOOT_SEL1
VOU1120_DATA11
GPIO14_3
C22
VOU1120_DATA11
VOU1120_DATA11
VOU1120_DATA12
GPIO14_4
D22
VOU1120_DATA12
VOU1120_DATA12
AIO_BCLK_RX/VOU1120_DATA13
GPIO14_5
B28
VOU1120_DATA13
VOU1120_DATA13
VOU1120_DATA14
GPIO14_6
A27
VOU1120_DATA14
VOU1120_DATA14
VOU1120_DATA15
GPIO14_7
B27
VOU1120_DATA15
VOU1120_DATA15

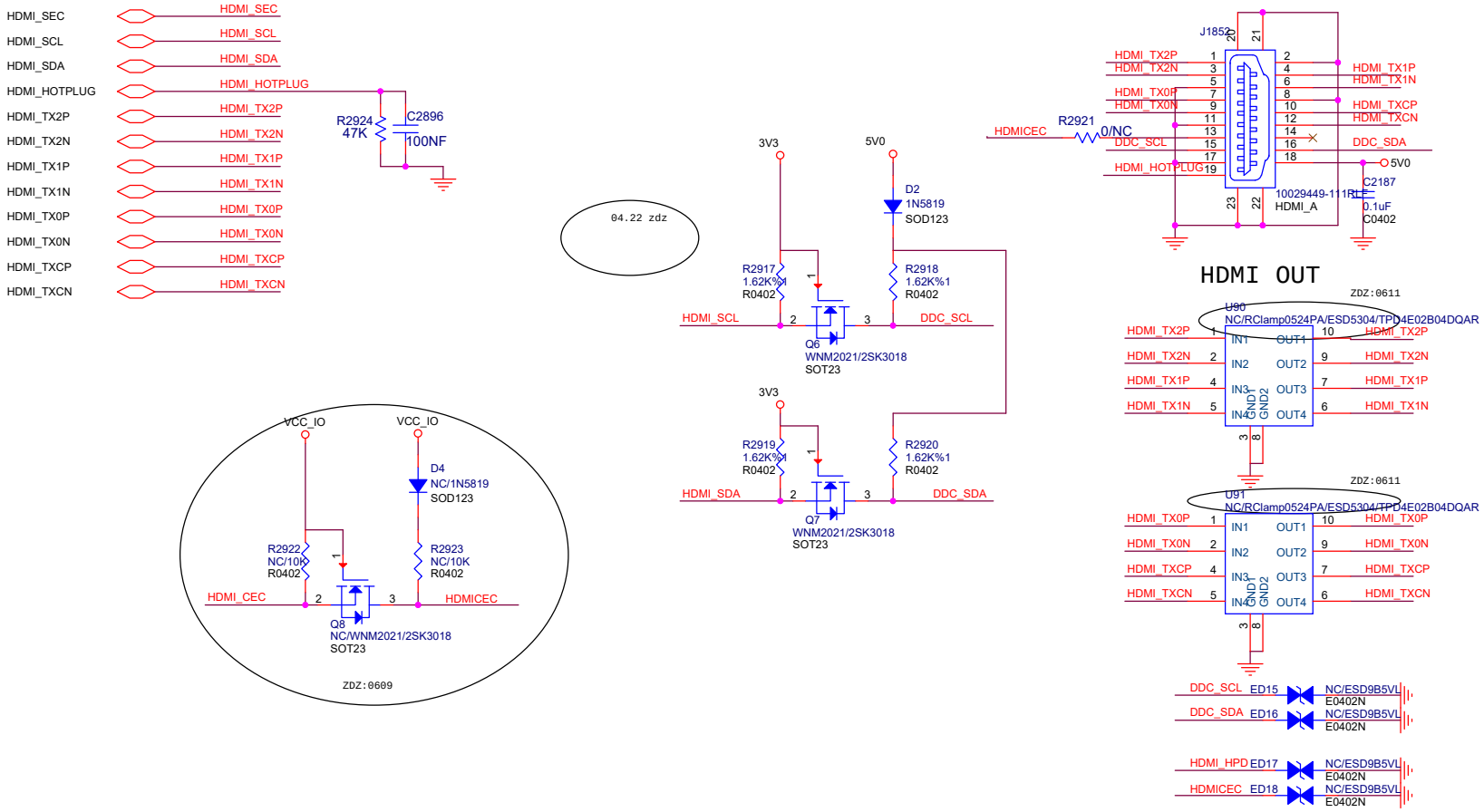

J13
TSW_101_23_F_S
J10
TSW_101_23_F_S
J1
TSW_101_23_F_S
J9
TSW_101_23_F_S
1
1
1
1


ID1
PCB_MARKPOINT
ID2
PCB_MARKPOINT
ID3
PCB_MARKPOINT
ID4
PCB_MARKPOINT
ID5
PCB_MARKPOINT
ID6
PCB_MARKPOINT

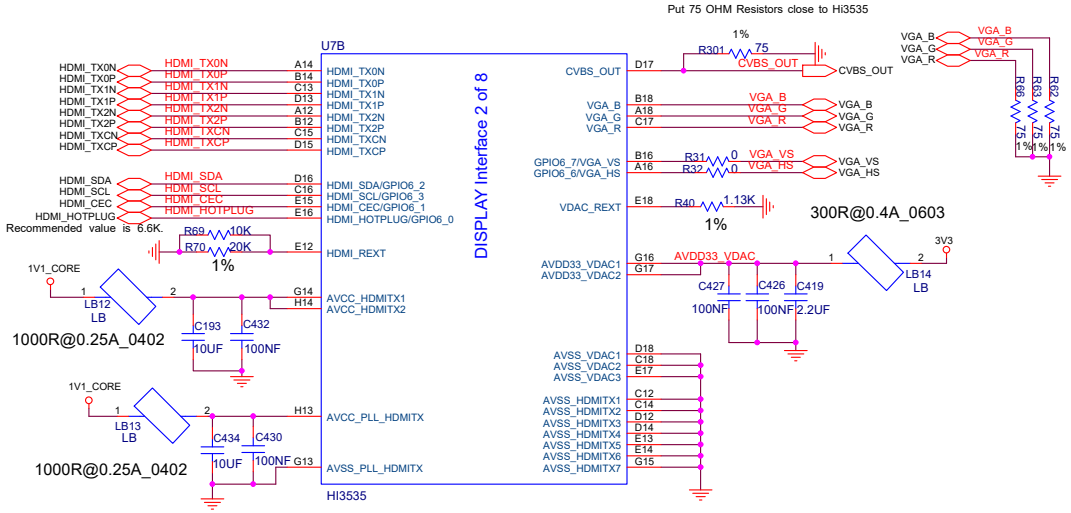
HDMI

The HDMI differential trace impedance is 100 OHM.

The HDMI trace length is less than 5 inch.



DISPLAY


Put 75 OHM Resistors close to Hi3535
U7B
DISPLAY Interface 2 of 8
HI3535
HDMI_TX0N
HDMI_TX0P
HDMI_TX1N
HDMI_TX1P
HDMI_TX2N
HDMI_TX2P
HDMI_TXCN
HDMI_TXCP
HDMI_SDA
HDMI_SCL
HDMI_CEC
HDMI_HOTPLUG
Recommended value is 6.6K.
R69 10K
R70 20K
1%
HDMI_REXT
1V1_CORE
LB12
LB
1000R@0.25A_0402
C193 10UF
C432 100NF
AVCC_HDMITX1
AVCC_HDMITX2
LB13
C434 10UF
C430 100NF
AVCC_PLL_HDMITX
AVSS_PLL_HDMITX
CVBS_OUT
R301 75
VGA_B
VGA_G
VGA_R
GPIO6_7/VGA_VS
GPIO6_6/VGA_HS
R31 0
R32 0
VGA_VS
VGA_HS
VDAC_REXT
R40 1.13K
300R@0.4A_0603
AVDD33_VDAC1
AVDD33_VDAC2
AVDD33_VDAC
C427 100NF
C426 100NF
C419 2.2UF
LB14
3V3
AVSS_VDAC1
AVSS_VDAC2
AVSS_VDAC3
AVSS_HDMITX1
AVSS_HDMITX2
AVSS_HDMITX3
AVSS_HDMITX4
AVSS_HDMITX5
AVSS_HDMITX6
AVSS_HDMITX7
R66 75
R63 75
R62 75

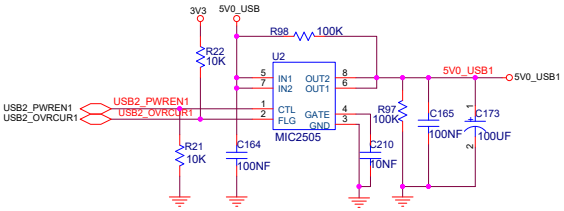
USB & SATA

The USB differential trace impedance is 90 OHM.

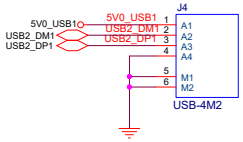
The USB trace length is less than 5 inch.

The SATA differential trace impedance is 100 OHM.

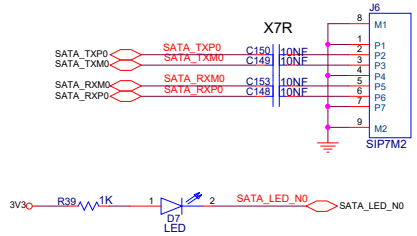
The SATA trace length is less than 5 inch.



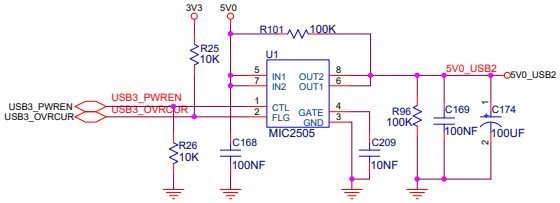
USB2.0 Port1

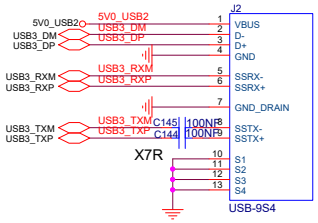


SATA3.0 Port0

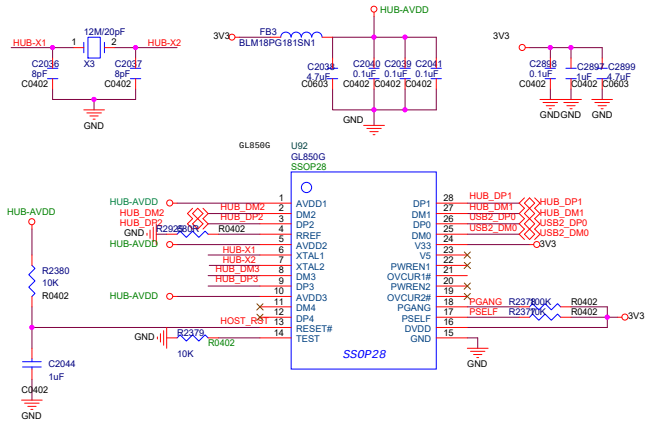


USB3.0

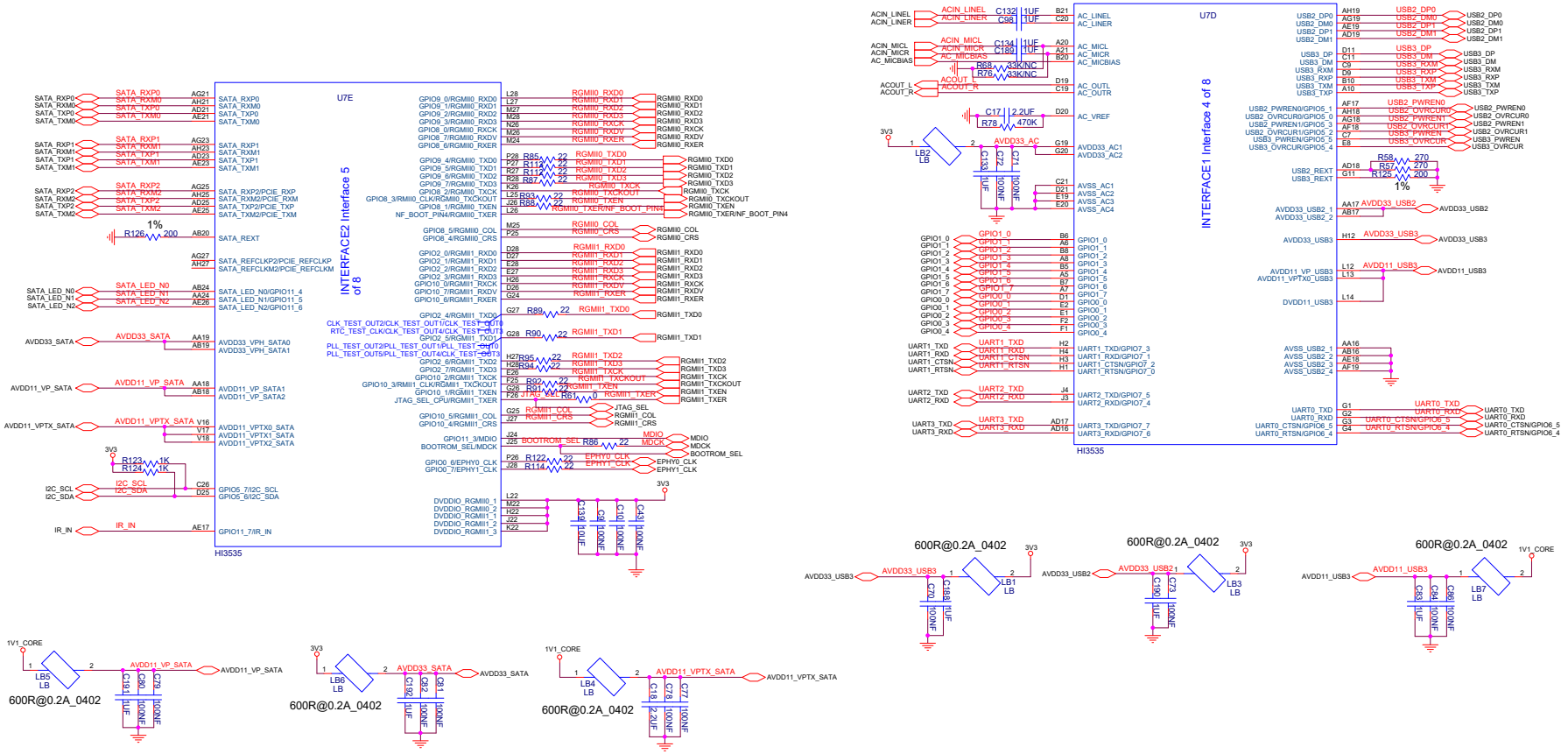




USB HUB



Interface


U7E
INTERFACE2 Interface 5 of 8
HI3535
U7D
INTERFACE1 Interface 4 of 8
HI3535
600R@0.2A_0402
LB1 LB
LB2 LB
LB3 LB
LB4 LB
LB5 LB
LB6 LB
LB7 LB

Power on setting pins

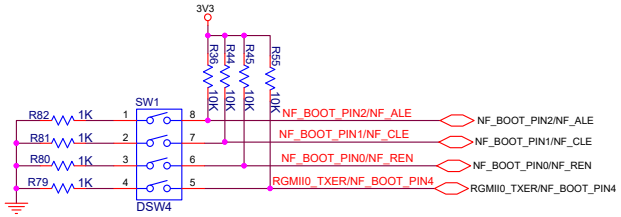
NF_BOOT_PIN[4:0]

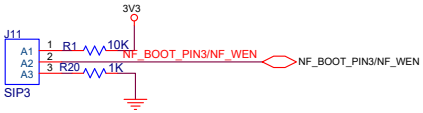
00011 2k page size,4bit ecc,64page/block,5addr

00100 4k page size,24bit ecc,256page/block,5addr
00101 2k page size,24bit ecc,64page/block,5addr
00111 8k page size,24bit ecc,256page/block,5addr

01000 4k page size,4bit ecc,128page/block,5addr
01001 4k page size,4bit ecc,64page/block,5addr
01010 2k page size,4bit ecc,64page/block,4addr
01011 4k page size,24bit ecc,128page/block,5addr
01101 8k page size,24bit ecc,128page/block,5addr

10000 8k page size,24bit ecc,64page/block,5addr
10001 4k page size,24bit ecc,64page/block,5addr
10101 2k page size,4bit ecc,128page/block,5addr
10110 2k page size,8bit ecc,128page/block,5addr
11001 2k page size,24bit ecc,128page/block,5addr
11010 2k page size,8bit ecc,64page/block,5addr
11110 4k page size,8bit ecc,64page/block,5addr
11111 4k page size,8bit ecc,128page/block,5addr

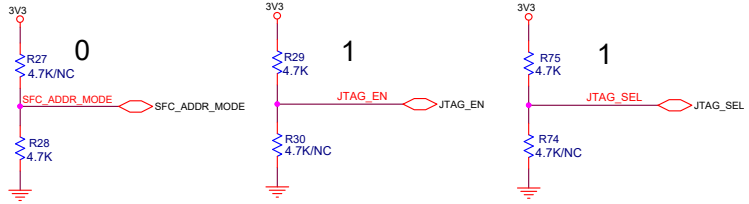




	SFC_ADDR_MODE
0	3 Byte mode
1	4 Byte mode

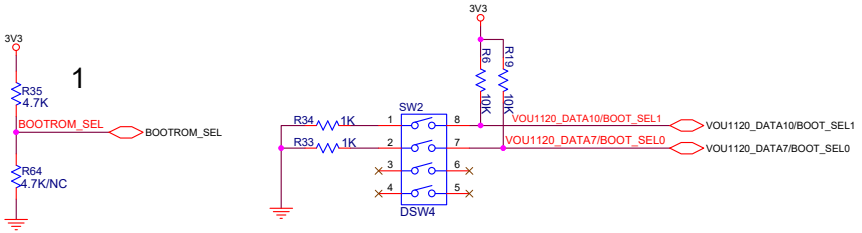
	JTAG_EN
0	Disable JTAG
1	Enable JTAG

	JTAG_SEL
0	Other
1	CPU

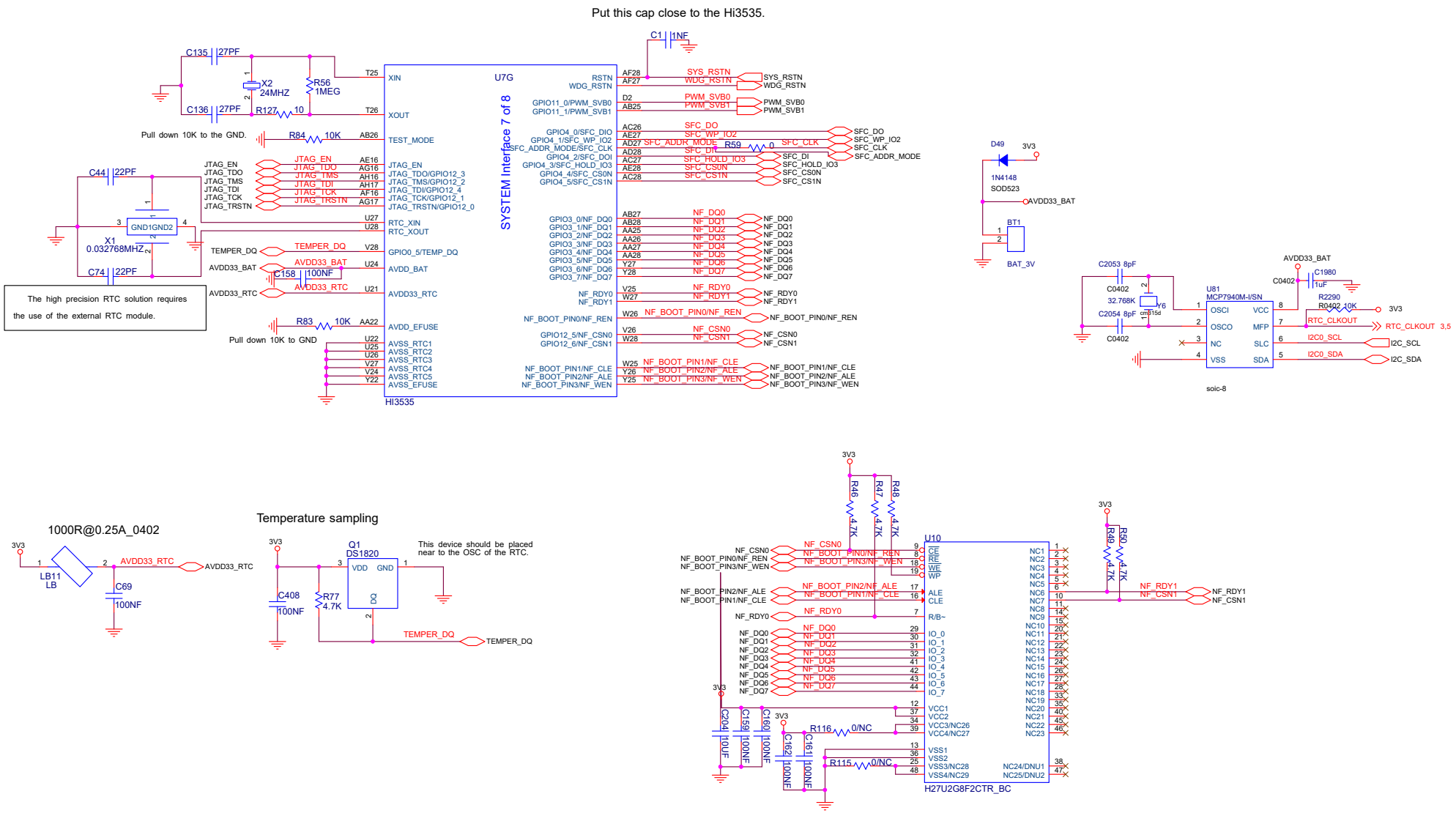


	BOOTROM_SEL
0	Boot from BOOT_SEL
1	Boot from Bootrom

	BOOT_SEL[1:0]
00	SPI FLASH
01	DDR
10	NAND FLASH
11	Reserve

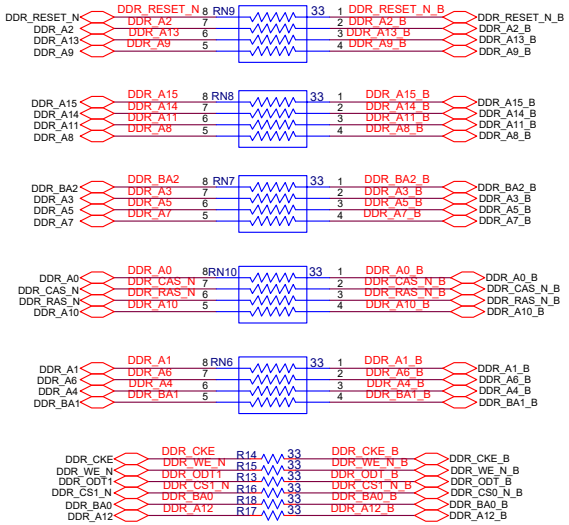


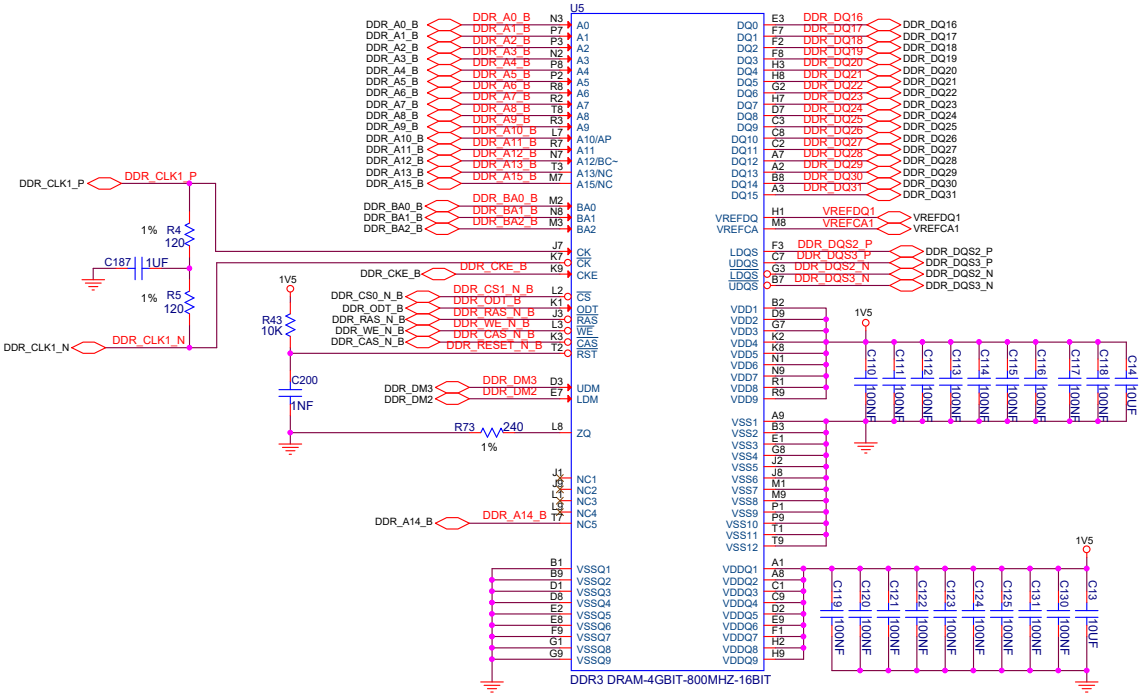
SYSTEM & FLASH

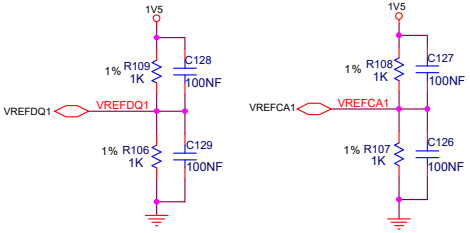


DDR3_B

The routing design of the DDR must be
the same as that for the Hi3535 demo board.

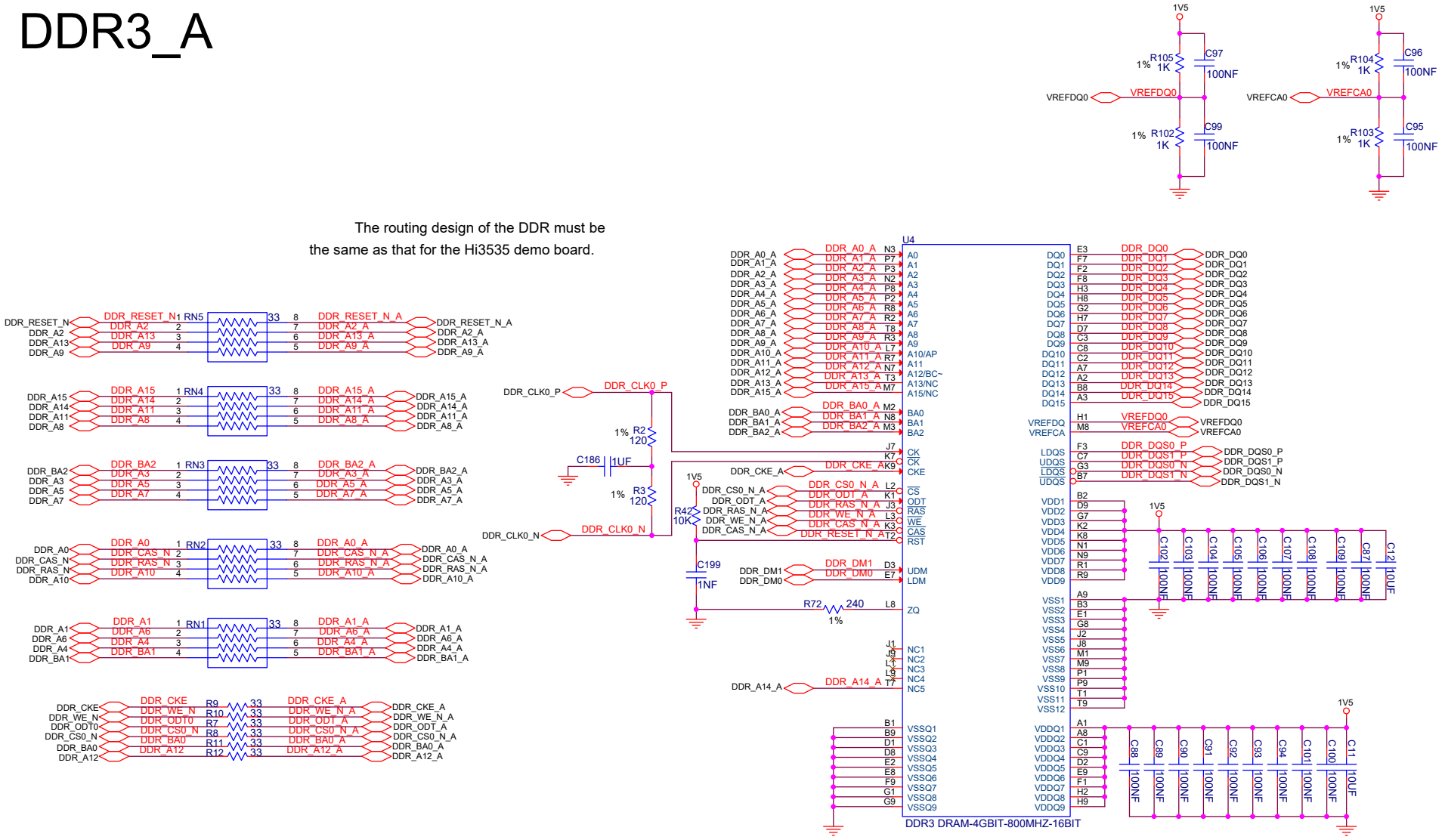




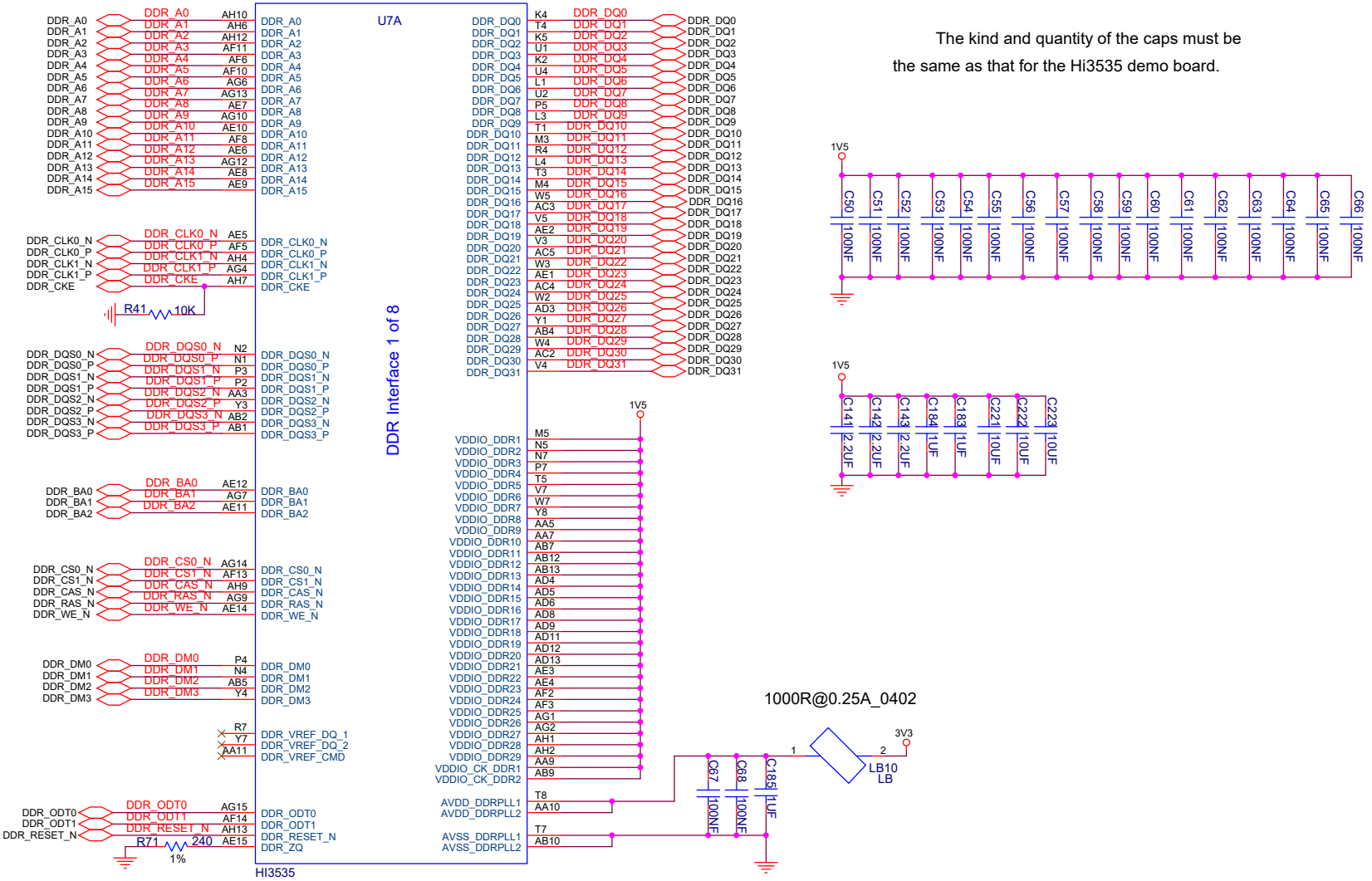


DDR3_A

The routing design of the DDR must be the same as that for the Hi3535 demo board.

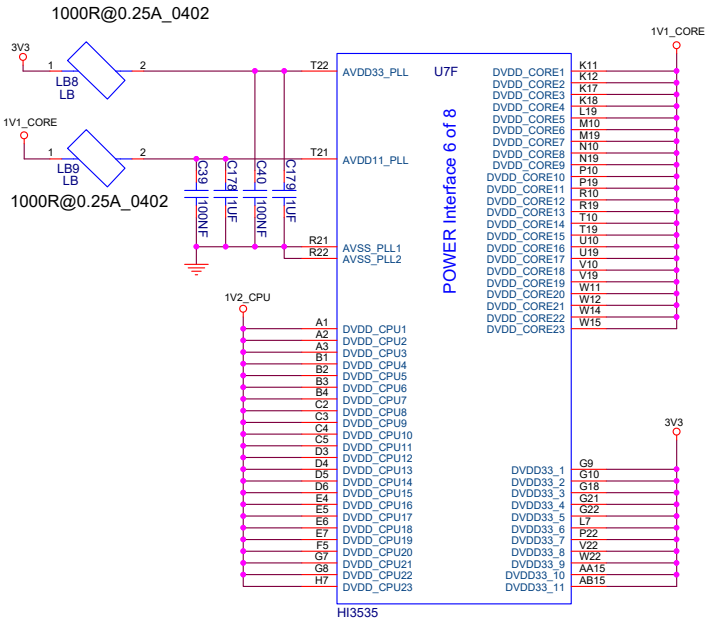


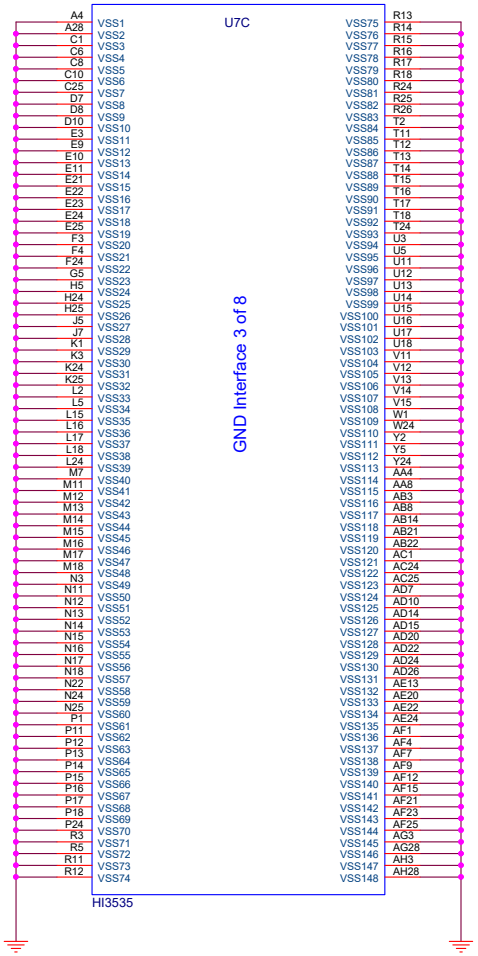
HI3535 DDR3



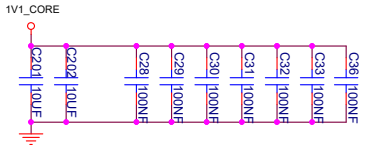
The kind and quantity of the caps must be the same as that for the Hi3535 demo board.

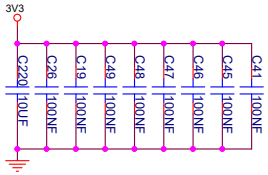
POWER & VSS

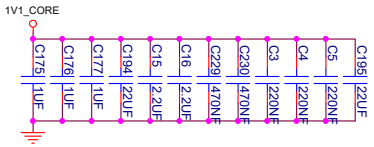


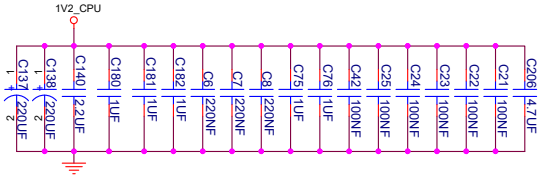


The kind and quantity of the caps must be the same as that for the Hi3535 demo board.

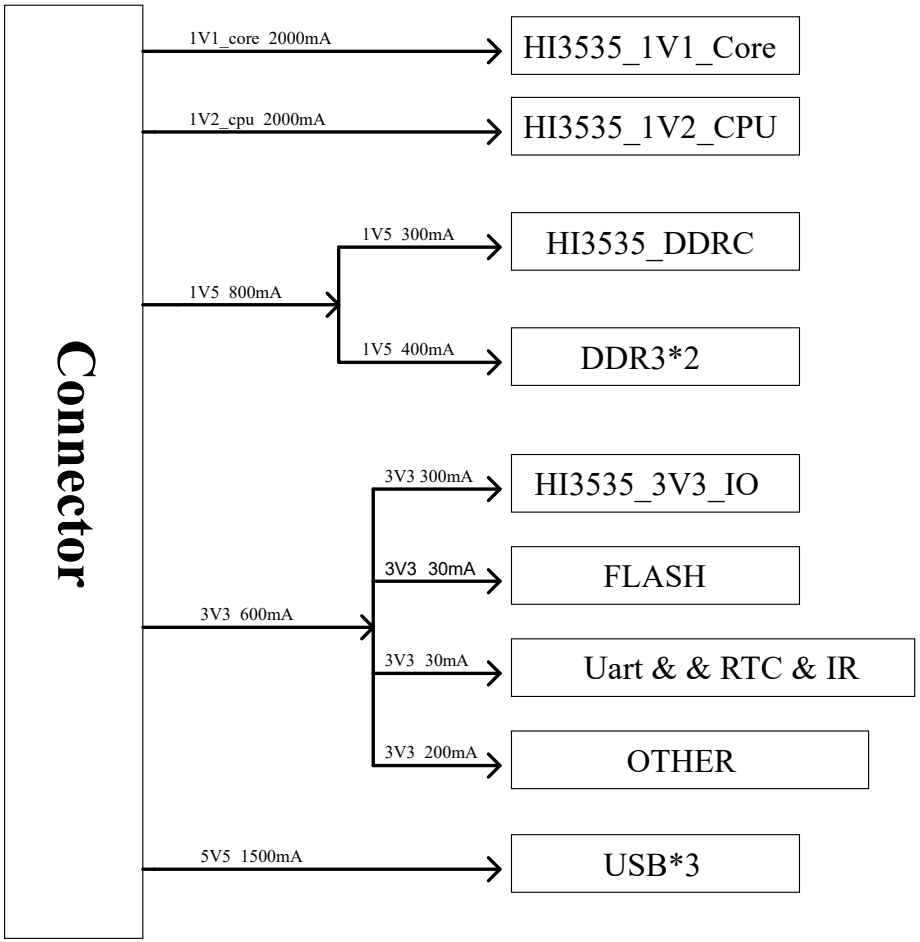




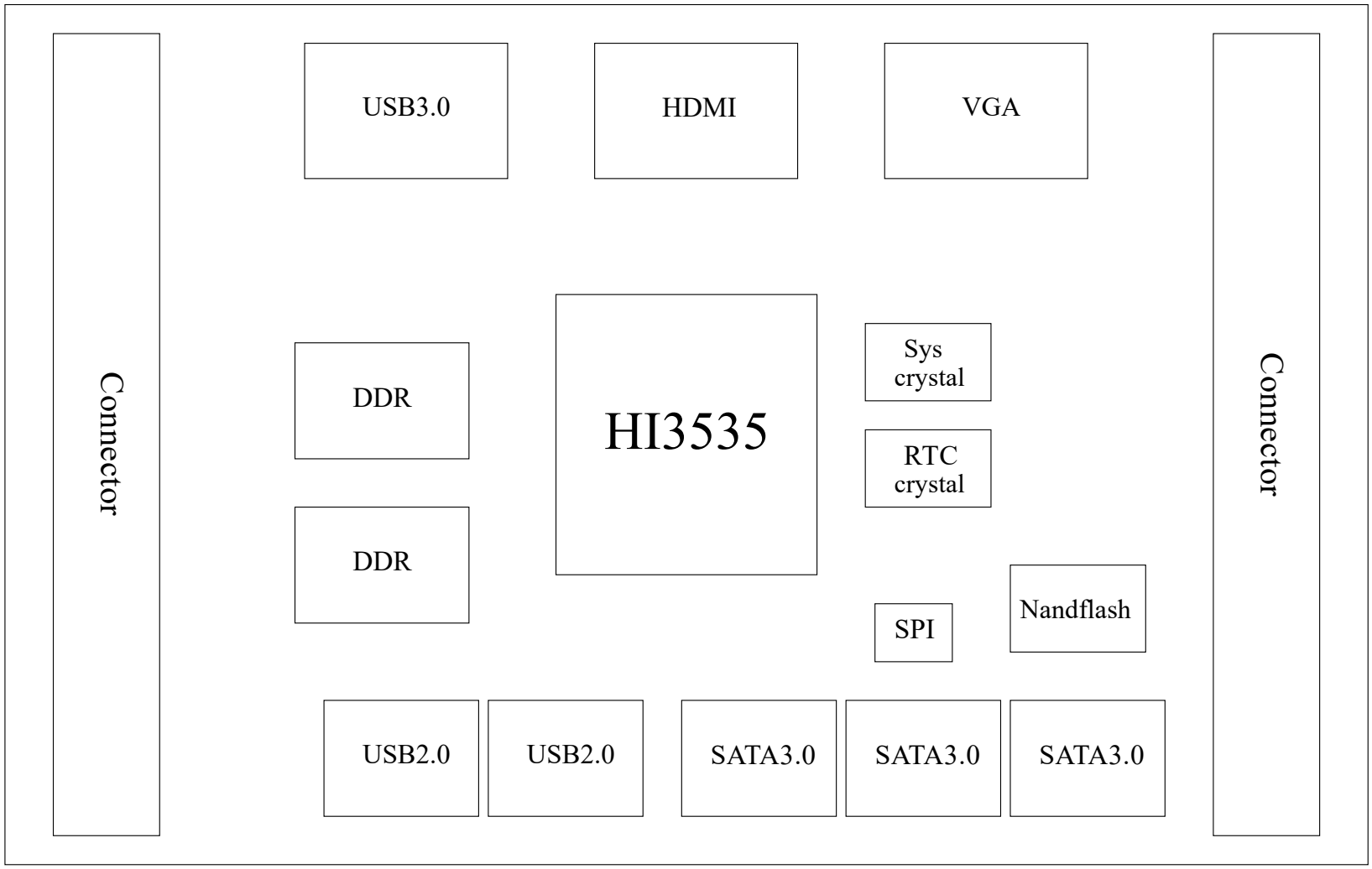




POWER TREE


Connector
1V1_core 2000mA
HI3535_1V1_Core
1V2_cpu 2000mA
HI3535_1V2_CPU
1V5 800mA
1V5 300mA
HI3535_DDRC
1V5 400mA
DDR3*2
3V3 600mA
3V3 300mA
HI3535_3V3_IO
3V3 30mA
FLASH
3V3 30mA
Uart & & RTC & IR
3V3 200mA
OTHER
5V5 1500mA
USB*3

BLOCK DIAGRAM



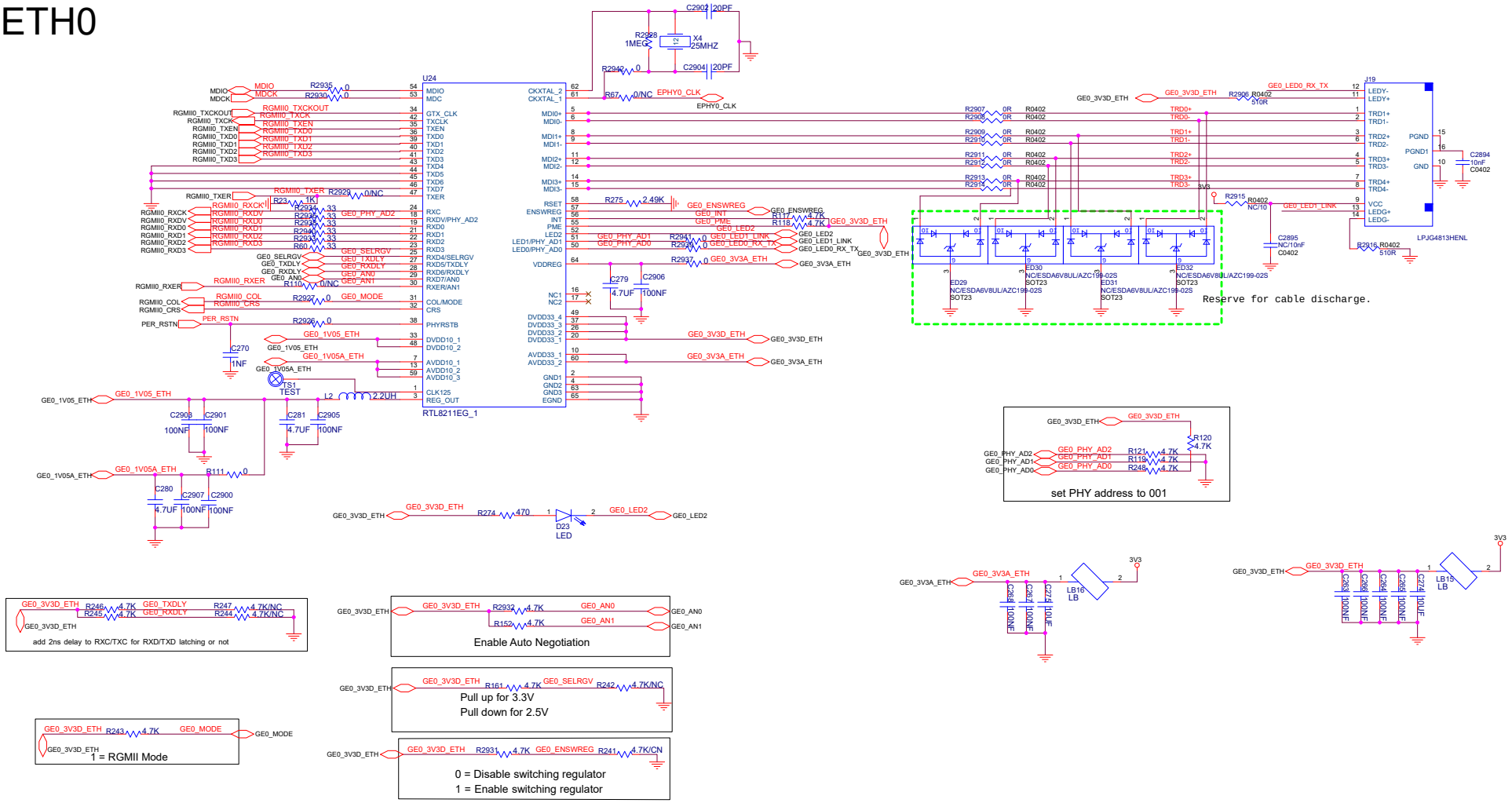
CHANGE LIST

2013.07.10 Ver.A schematic

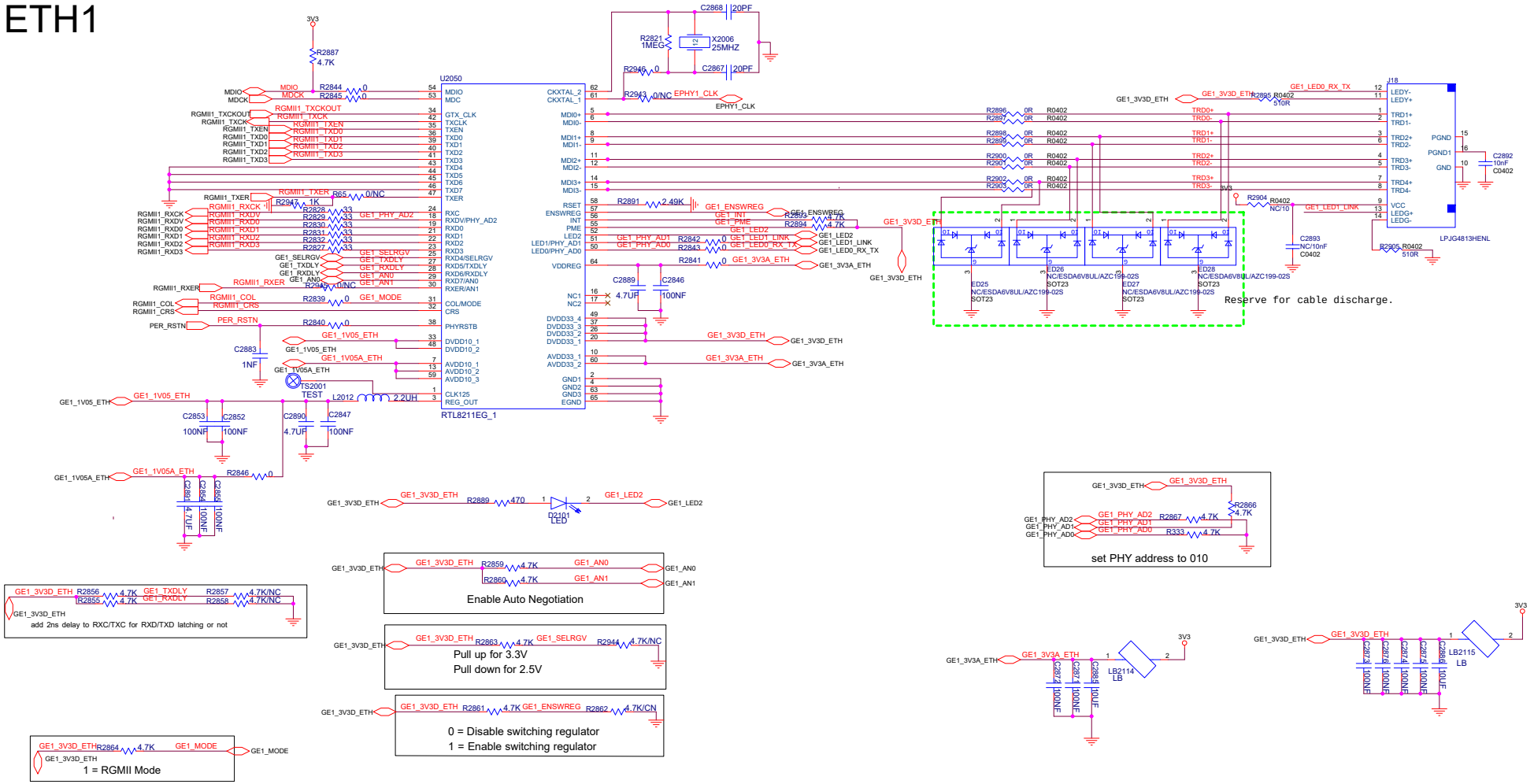
2013.09.27 Change C144 C145 form 10nF to 100nF

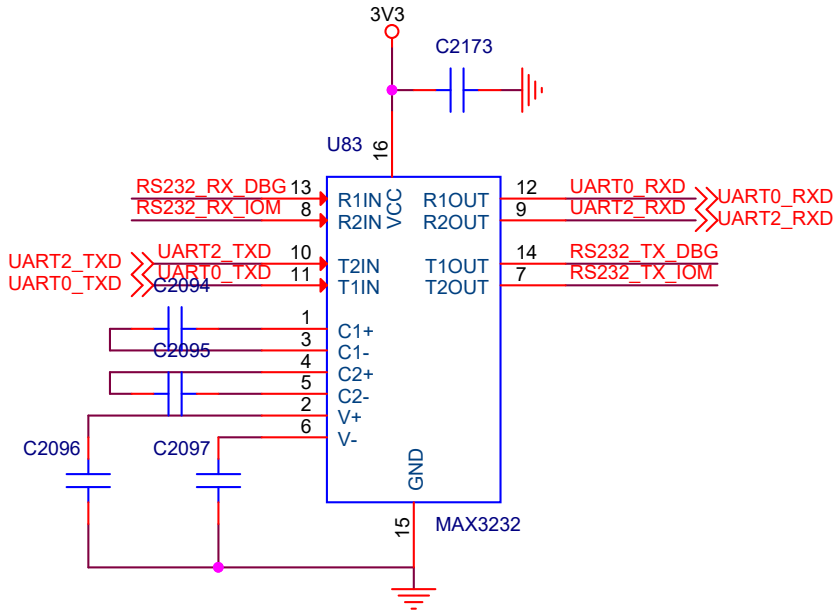
Hi3535DMEB VER.A

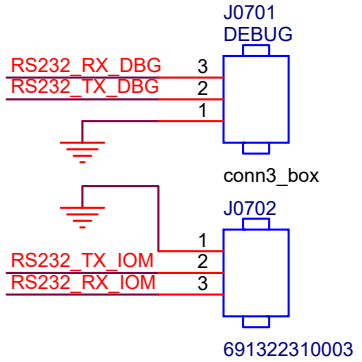
ETH0


U24
RTL8211EG_1
MDIO
MDCK
RGMII0_TXCKOUT
RGMII0_TXCK
RGMII0_TXEN
RGMII0_TXD0
RGMII0_TXD1
RGMII0_TXD2
RGMII0_TXD3
RGMII0_TXER
RGMII0_RXCK
RGMII0_RXDV
RGMII0_RXD0
RGMII0_RXD1
RGMII0_RXD2
RGMII0_RXD3
RGMII0_RXER
RGMII0_COL
RGMII0_CRS
PER_RSTN
GE0_SELRGV
GE0_TXDLY
GE0_RXDLY
GE0_AN0
GE0_AN1
GE0_MODE
GE0_PHY_AD2
GE0_ENSWREG
GE0_INT
GE0_PME
GE0_LED2
GE0_LED1_LINK
GE0_LED0_RX_TX
GE0_1V05_ETH
GE0_1V05A_ETH
GE0_3V3D_ETH
GE0_3V3A_ETH
EPHY0_CLK
TS1
TEST
D23
LED
J19
LPJG4813HENL
ED29
ED30
ED31
ED32
NC/ESDA6V8UL/AZC199-02S
SOT23
Reserve for cable discharge.
set PHY address to 001
add 2ns delay to RXC/TXC for RXD/TXD latching or not
Enable Auto Negotiation
Pull up for 3.3V
Pull down for 2.5V
1 = RGMII Mode
0 = Disable switching regulator
1 = Enable switching regulator

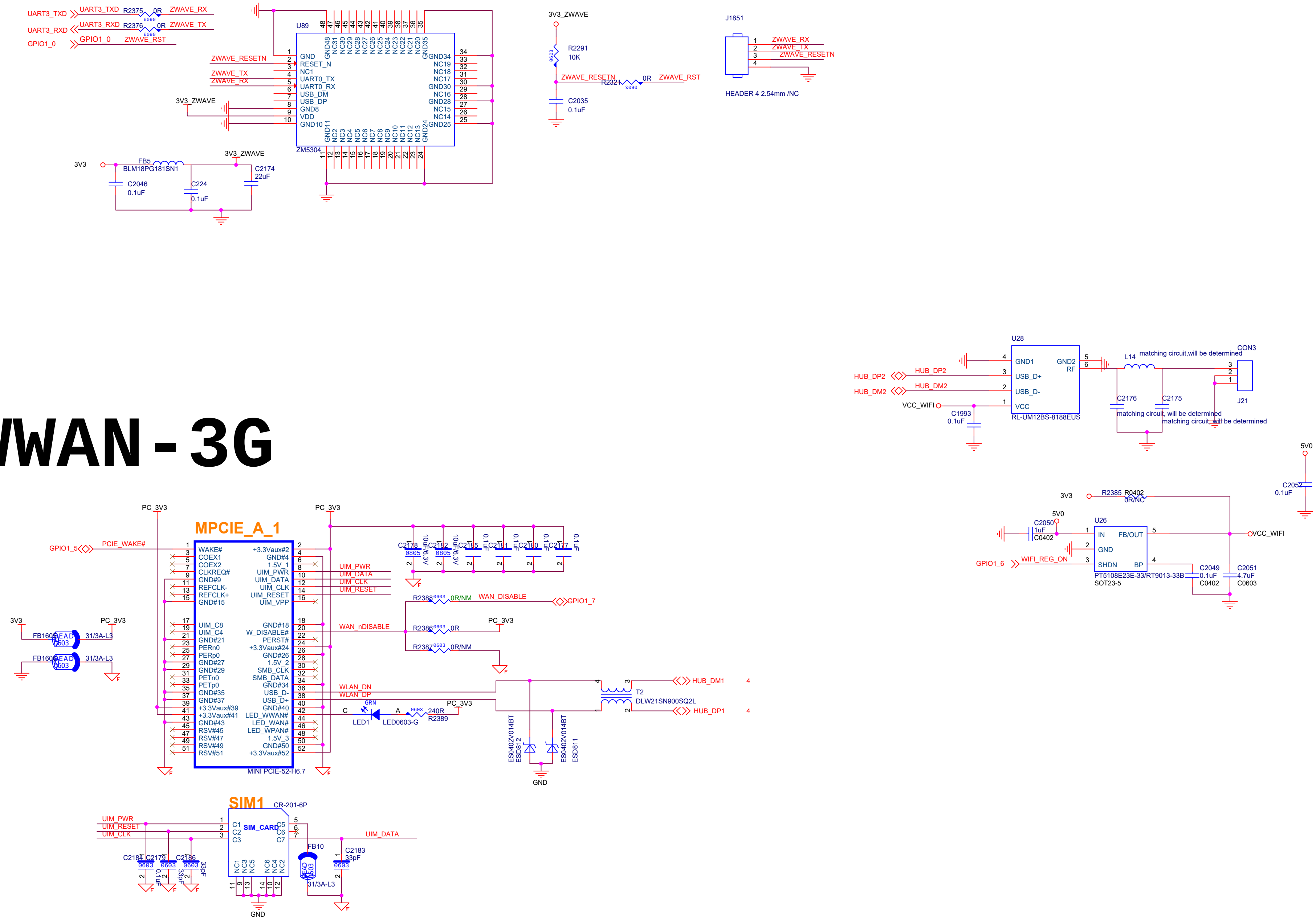
ETH1


U2050
RTL8211EG_1
Reserve for cable discharge.
set PHY address to 010
Enable Auto Negotiation
Pull up for 3.3V
Pull down for 2.5V
0 = Disable switching regulator
1 = Enable switching regulator
1 = RGMII Mode
add 2ns delay to RXC/TXC for RXD/TXD latching or not
LPJG4813HENL
LB2114
LB2115


3V3
C2173
U83
16
RS232_RX_DBG
RS232_RX_IOM
13
8
R1IN
R2IN
VCC
R1OUT
R2OUT
12
9
UART0_RXD
UART2_RXD
UART0_RXD
UART2_RXD
UART2_TXD
UART0_TXD
C2094
10
11
T2IN
T1IN
T1OUT
T2OUT
14
7
RS232_TX_DBG
RS232_TX_IOM
1
3
4
5
2
6
C1+
C1-
C2+
C2-
V+
V-
C2095
C2096
C2097
GND
15
MAX3232


J0701
DEBUG
RS232_RX_DBG
RS232_TX_DBG
3
2
1
conn3_box
J0702
1
RS232_TX_IOM
RS232_RX_IOM
2
3
691322310003

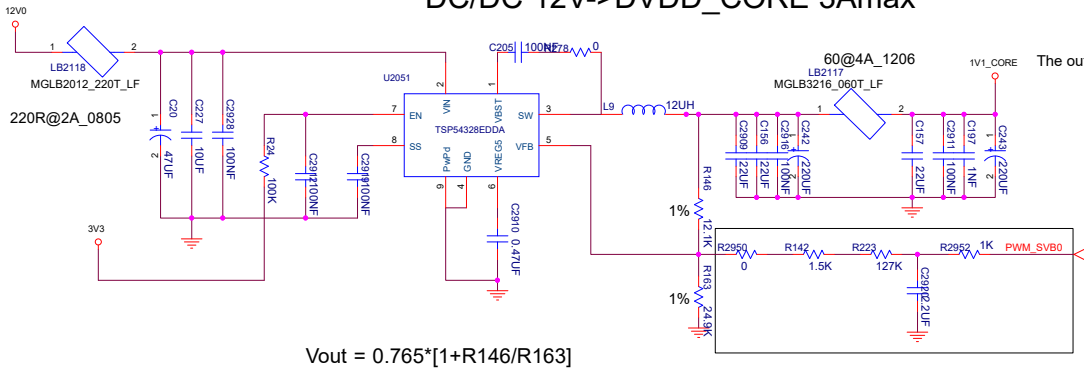
WWAN-3G



UART3_TXD
UART3_RXD
GPIO1_0
R2375 0R
R2376 0R
ZWAVE_RX
ZWAVE_TX
ZWAVE_RST
U89
ZM5304
GND
RESET_N
NC1
UART0_TX
UART0_RX
USB_DM
USB_DP
GND8
VDD
GND10
GND34
GND30
GND28
GND25
ZWAVE_RESETN
3V3_ZWAVE
3V3
FB5
BLM18PG181SN1
C2046
0.1uF
C224
0.1uF
C2174
22uF
R2291
10K
R2921
0R
C2035
0.1uF
J1851
ZWAVE_RX
ZWAVE_TX
ZWAVE_RESETN
HEADER 4 2.54mm /NC
U28
GND1
USB_D+
USB_D-
VCC
GND2
RF
RL-UM12BS-8188EUS
HUB_DP2
HUB_DM2
VCC_WIFI
C1993
0.1uF
L14
matching circuit,will be determined
C2176
C2175
matching circuit, will be determined
CON3
J21
5V0
C2052
0.1uF
3V3
R2385 R0402
0R/NC
U26
IN
GND
SHDN
FB/OUT
BP
C2050
1uF
C0402
GPIO1_6
WIFI_REG_ON
PT5108E23E-33/RT9013-33B
SOT23-5
C2049
0.1uF
C0402
C2051
4.7uF
C0603
VCC_WIFI
PC_3V3
MPCIE_A_1
GPIO1_5
PCIE_WAKE#
WAKE#
COEX1
COEX2
CLKREQ#
GND#9
REFCLK-
REFCLK+
GND#15
UIM_C8
UIM_C4
GND#21
PERn0
PERp0
GND#27
GND#29
PETn0
PETp0
GND#35
GND#37
+3.3Vaux#39
+3.3Vaux#41
GND#43
RSV#45
RSV#47
RSV#49
RSV#51
+3.3Vaux#2
GND#4
1.5V_1
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
UIM_VPP
GND#18
W_DISABLE#
PERST#
+3.3Vaux#24
GND#26
1.5V_2
SMB_CLK
SMB_DATA
GND#34
USB_D-
USB_D+
GND#40
LED_WWAN#
LED_WAN#
LED_WPAN#
1.5V_3
GND#50
+3.3Vaux#52
MINI PCIE-52-H6.7
UIM_PWR
UIM_DATA
UIM_CLK
UIM_RESET
WAN_nDISABLE
WLAN_DN
WLAN_DP
C2178
C2182
C2185
C2181
C2180
C2177
10uF/6.3V
0.1uF
R2388 0R/NM
WAN_DISABLE
GPIO1_7
R2386 0R
R2387 0R/NM
LED1
GRN
LED0603-G
240R
R2389
T2
DLW21SN900SQ2L
HUB_DM1
HUB_DP1
ES0402V014BT
ESD812
ESD811
GND
FB1600
31/3A-L3
SIM1
CR-201-6P
SIM_CARD
UIM_PWR
UIM_RESET
UIM_CLK
UIM_DATA
C2184
C2179
C2186
33pF
C2183
33pF
FB10
31/3A-L3
GND

Power Supply

DC/DC 12V->DVDD_CORE 3Amax



The output Voltage is controlled by the SVB circuit.

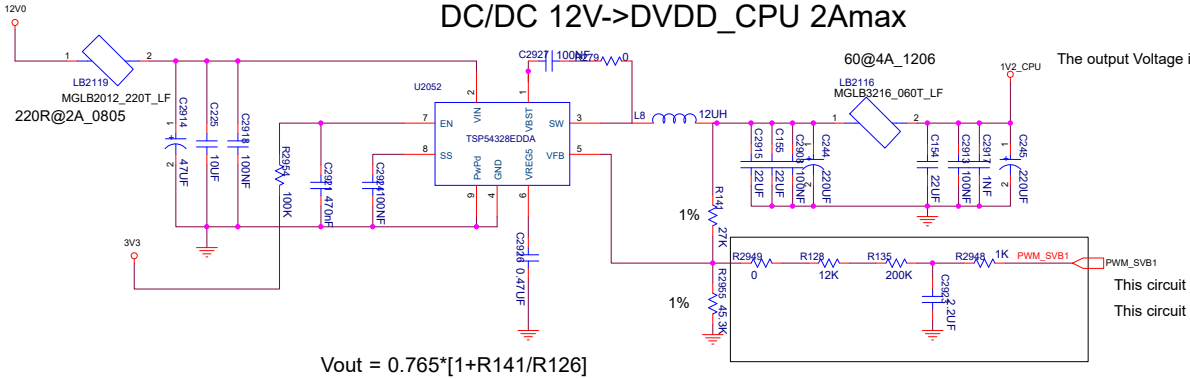
PWM_SVB0

This circuit should be palced near to the DC-DC.

This circuit is left for the SVB.

Vout = 0.765*[1+R146/R163]

DC/DC 12V->DVDD_CPU 2Amax



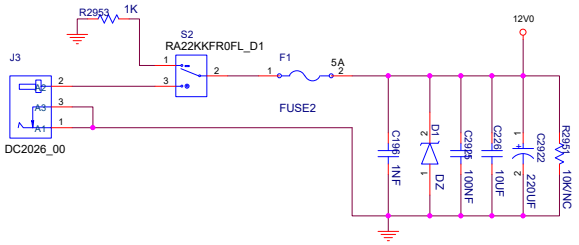
The output Voltage is controlled by the SVB circuit.

PWM_SVB1

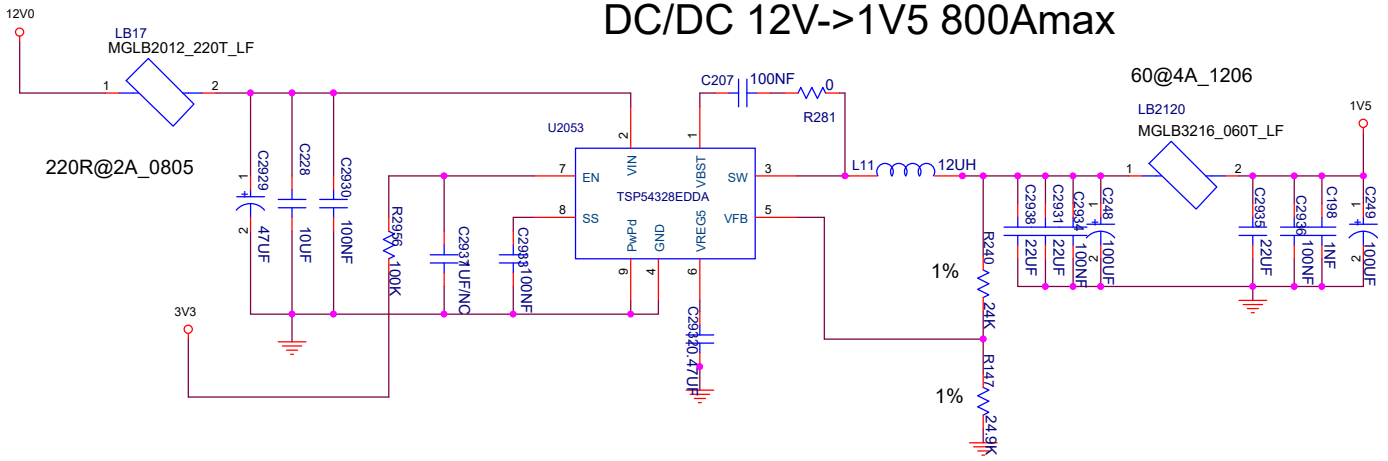
This circuit should be palced near to the DC-DC.

This circuit is left for the SVB.

Vout = 0.765*[1+R141/R126]

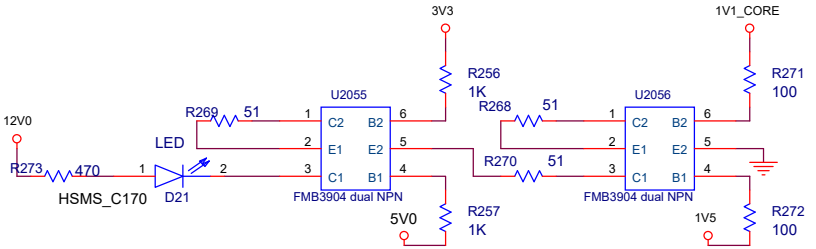


Power Supply



Vout = 0.765*[1+R240/R147]

Power Indicator LED



Power Supply

12V -> 5V - 2A and 3.3V - 2A