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Professor Pawan Hanumolu

ECE 483 Final Project- Implementation of an LDO

Choice of Resistors for Feedback

The resistors R_{b1} and R_{b2} were chosen for feedback to obtain the desired feedback voltage $V_{feedback}$. The resistors were implemented by using diode-type NMOS devices. This was done primarily to gain control of the resistance (hence β) and decrease the area occupied which would otherwise be occupied by resistors with much larger area. The resistance R_{b2} was implemented by using two NMOS devices with identical dimensions to have better control of β.

Implementation of Error Amplifiers to obtain optimal DC loop Gain and Phase Margin

A-dual stage telescopic amplifier is used with 4 PMOS devices and 4 NMOS (along with another NMOS biasing transistor) devices to maximize the loop gain. The output swing of this amplifier is limited because of the number of devices that are used and hence it is harder to bias the devices in saturation; however, the design choice does not lay much emphasis on the output swing of the error amplifier. It is easier to achieve stability because they only have one dominant pole. However, with folded telescopic cascade, the output swing is much better and are still easy to stabilize. They also have good DC gain and higher gain bandwidth. However, the static power consumption is worse than the amplifier of choice. The input referred noise and offset tends to be poor. A capacitor C_c is connected between the output node and the drain of NMOS with the V_{ref} biasing. This capacitor helps in achieving quicker transient response and Power Supply Rejection(PSR) which is better than the standard miller compensation that is used. This also helps in pushing the RHP zero to a high frequency in order to stabilize the system. It also helps in pushing the second pole to higher frequencies. The transistors are biased using NMOS and PMOS transistors which are driven by low current of $50\mu A$. The reference voltage is set based on the desired output from the LDO. Due to the poor choice (much lower in value) of the C_c capacitance, the phase margin criteria were not met for all the load currents used. The gain obtained was very high, but this high gain came with some caveats in the sense that the transient response was slightly poor than expected. The high frequency PSR was poorer because of the low C_c capacitance and PSR is sensitive to the load current that is used. The gain is very large because of the dual stage and the effective gain is $(g_m r_{ds})^2$ which is very beneficial in high gain applications.

Choice of Current Source

The current source I_d is used to bias the error amplifier adequately. The current used is relatively small in order to lower the power consumption and keep the overdrive voltage to lower values for most of the transistors. There is a current source I_L that is used at the output instead of the resistor in order to gain better control of the load current.

Pass Device

The pass device is implemented using a PMOS device with a very high width and a consequently a very high $\frac{W}{L}$ ratio. This is the variable resistor which determines the value of dropout voltage and helps in determining the load current as well as minimizing the quiescent current. High value of the $\frac{W}{L}$ ratio is very beneficial as it decreases the resistance and gives a high current at the output.

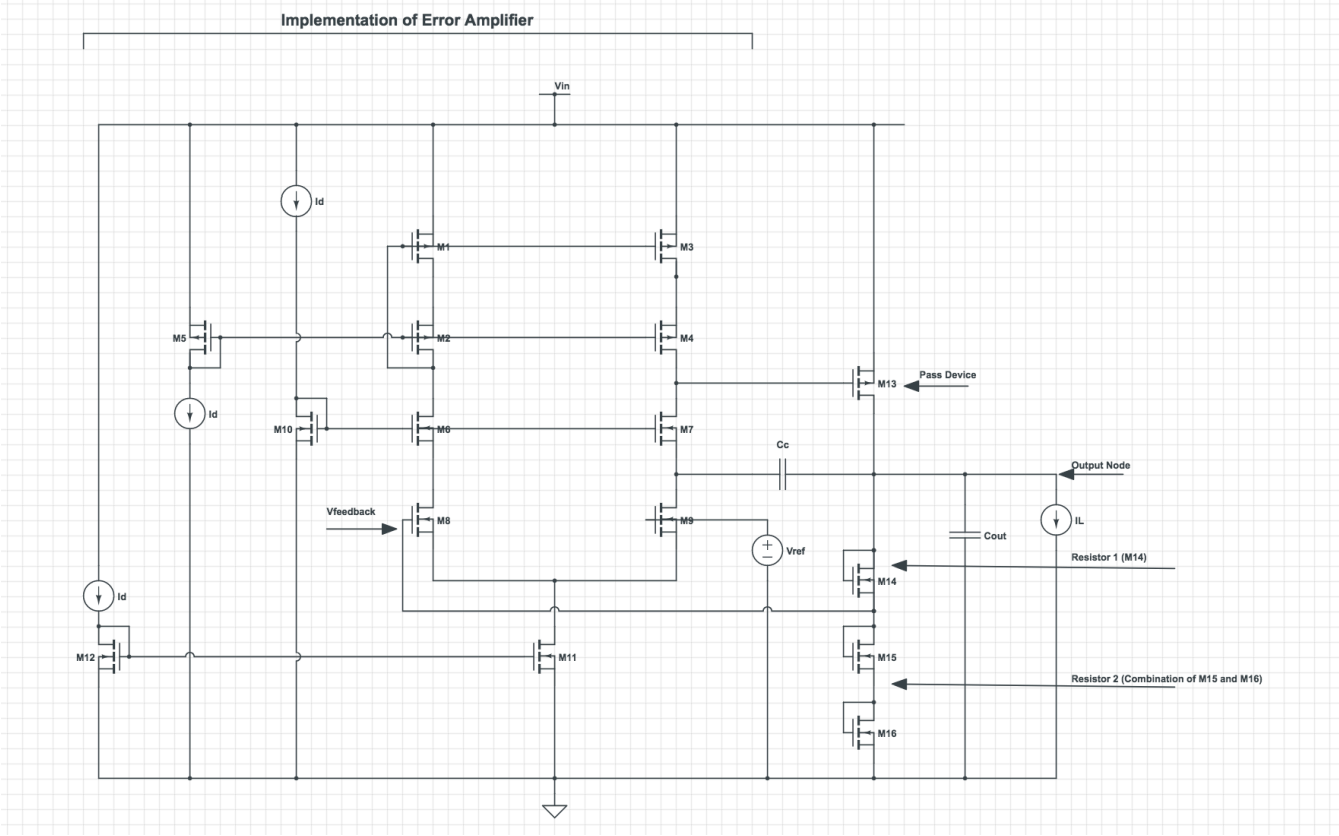


Figure 1. The diagramatic representation of the LDO

Table 1. The device sizes, g_m and Δs parameters of MOS devices

MOS Device(s)/Region	Width (μm)	Length (μm)	$g_m(mho)$	Δs
M1-M3/SAT	237.6	0.315	$5.12 * 10^{-4}$	0.130
M2-M4/SAT	237.6	0.315	$5.14 * 10^{-4}$	0.130
M6-M7/SAT	42.57	0.450	$7.34 * 10^{-4}$	0.091
M8-M9/SAT	8.51	0.450	$4.99 * 10^{-4}$	0.134
M11/SAT	12.77	0.450	$8.61 * 10^{-4}$	0.156
M5/Sub-thresh.	26.40	0.315	$2.05 * 10^{-4}$	0.488
M10/Sub-thresh.	0.946	0.450	$1.94 * 10^{-4}$	0.516
M12/Sub-thresh.	8.51	0.450	$6.52 * 10^{-4}$	0.153
M13/SAT	685.53	0.360	0.054	0.922
M14/Sub-thresh.	86.40	0.630	$0.743 * 10^{-4}$	0.075
M15-M16/Sub-thresh.	108.00	0.360	$0.738 * 10^{-4}$	0.076

Table 3. The parameters of the capacitors, voltage sources and current sources

Parameter	Type	Value
C_C	Capacitor	$2pF$
C_{OUT}	Capacitor	$40pF$
V_{REF}	Voltage source	$765mV$
V_{IN}	Voltage source	$1.8V(or\ as\ specified)$
I_L	Current source	$1 - 25\ mA(as\ specified)$
I_d	Current source	$50\mu A$

Table 2. The performance summary of the LDO device

Design Parameter	Simulated Performance	Specification
Input Voltage (V_{IN})	1.8V	1.6-2.0V
Output Voltage (V_{OUT})	1.304-1.305 V	1.0V-1.3V
Total Capacitance	$42pF$	$\leq 500pF$
Output Voltage Error	0.75-1.16%	$\leq 3\%$
Load Current	1mA-25mA	1mA-25mA
DC Load Regulation	14.29-189 $\mu V/mA$	$\leq 100\mu V/mA$
DC Line Regulation	$0.8 - 5.57\mu V/V$	$\leq 2mV/V$
Quiescent Current ($I_L = 1mA/25mA$)	$169.893 - 169.912\mu A$	Minimum
Current Efficiency ($I_L = 1mA/25mA$)	85.48-99.33%	-
PSR: $\left(\frac{V_{IN}}{V_{OUT}}\right) = \frac{1.8V}{1.3V}, I_L = 25mA(@1kHz/1MHz)$	-70.11/-31.93 dB/dB	-40dB/-20dB
PSR: $\left(\frac{V_{IN}}{V_{OUT}}\right) = \frac{1.65V}{1.4V}, I_L = 25mA(@1kHz/1MHz)$		-40dB/-20dB
Worst-case PSR	-31.93dB	-
DC loop gain: $\left(\frac{V_{IN}}{V_{OUT}}\right) = \frac{1.8V}{1.3V}$ ($I_L = 1mA/25mA$)	101.8/74.78	-
DC loop gain: $\left(\frac{V_{IN}}{V_{OUT}}\right) = \frac{1.6V}{1.4V}$ ($I_L = 1mA/25mA$)		-
Worst-case DC loop gain	74.78	-
Loop-gain UGF ($I_L = 1mA/25mA$)	33.88/55.88 MHz	-
Loop-gain PM ($I_L = 1mA/25mA$)	20.85/24.67 dB	-
Loop-gain GM ($I_L = 1mA/25mA$)	47.42°/ 77.70°	-
Transient Response ($I_L = 1mA/25mA$)	7.35%	Undershoot $\leq$ 5%
Transient Response ($I_L = 1mA/25mA$)	None found	Overshoot $\leq$ 5%
Output ($I_L = 1mA/25mA$) Noise	0.00	-

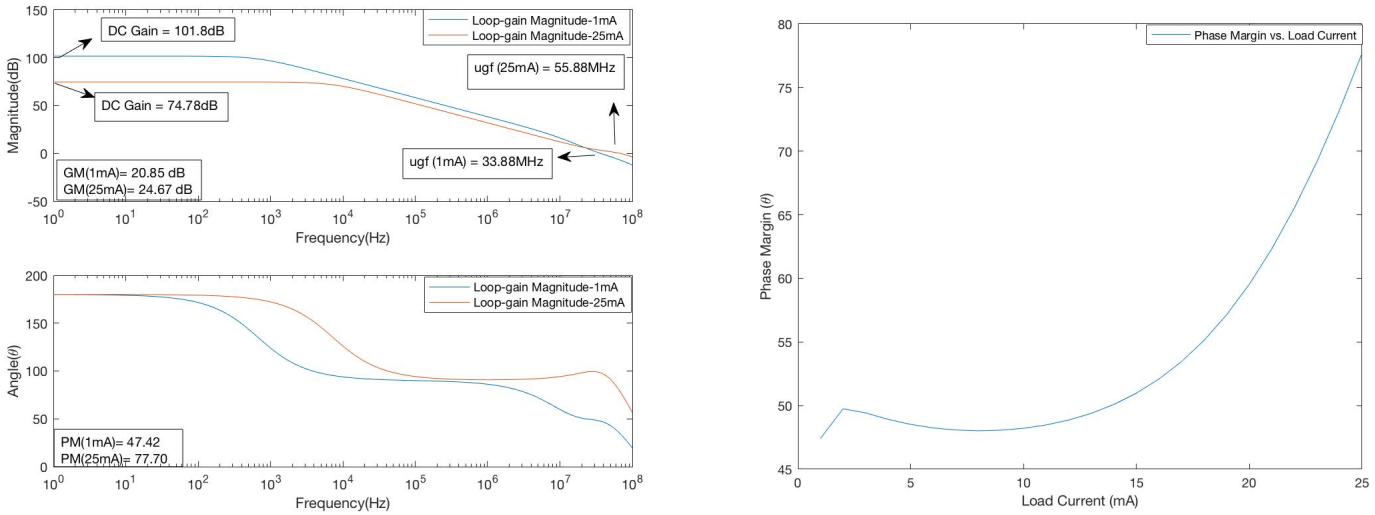


Figure 2. (a) The plot for Loop-gain AC response and (b) phase margin vs. load current

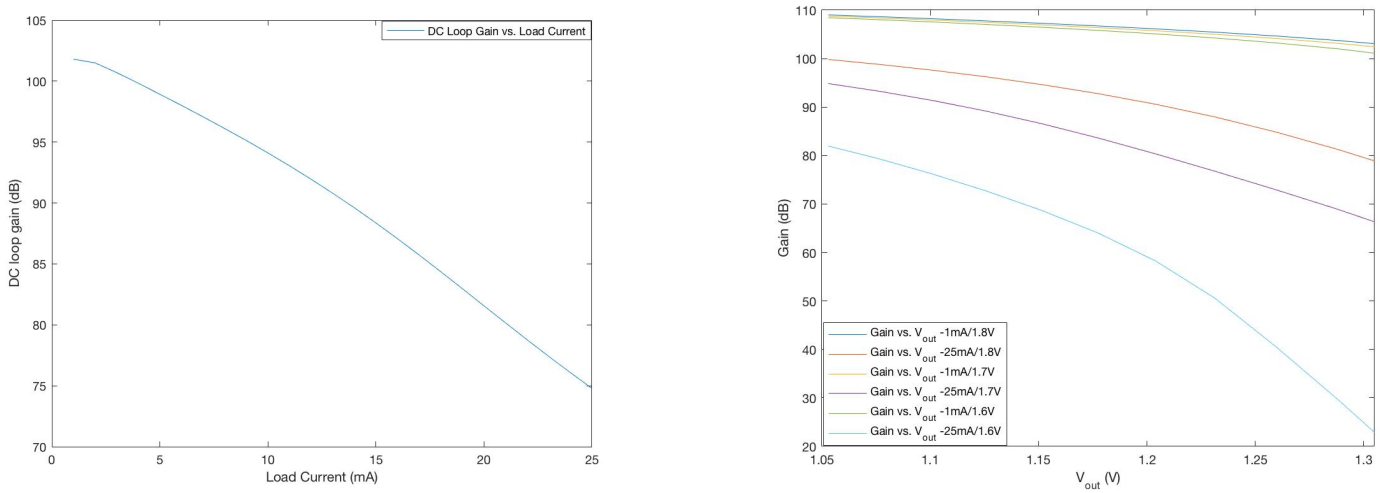


Figure 3. The plot for (a) DC loop gain vs. Load Current and (b) DC loop gain as a function of output voltage

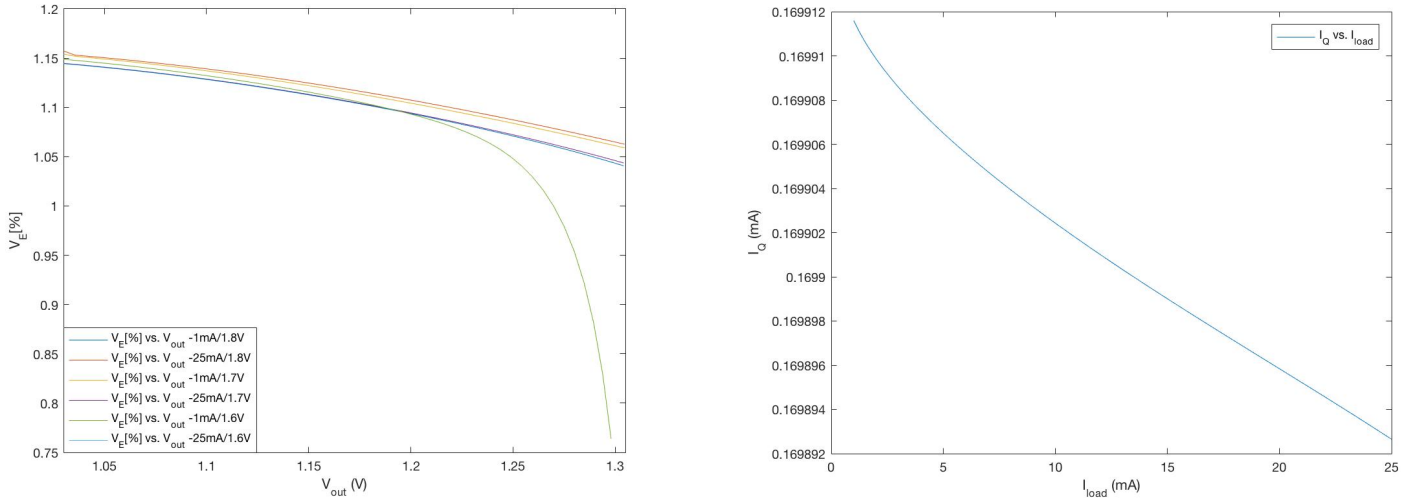
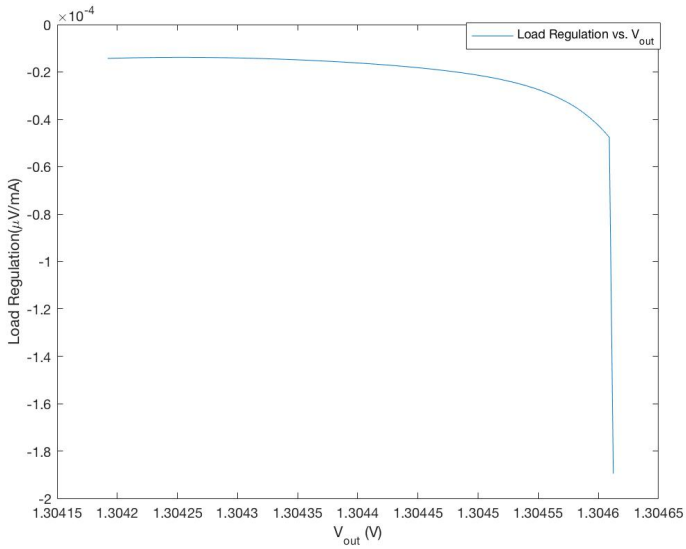


Figure 4. The plot for (a) error voltage as a function of output voltage and (b) Quiescent current as a function of load current



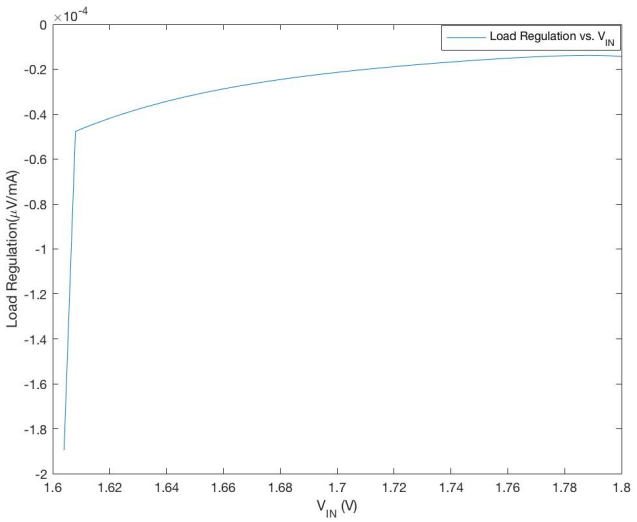
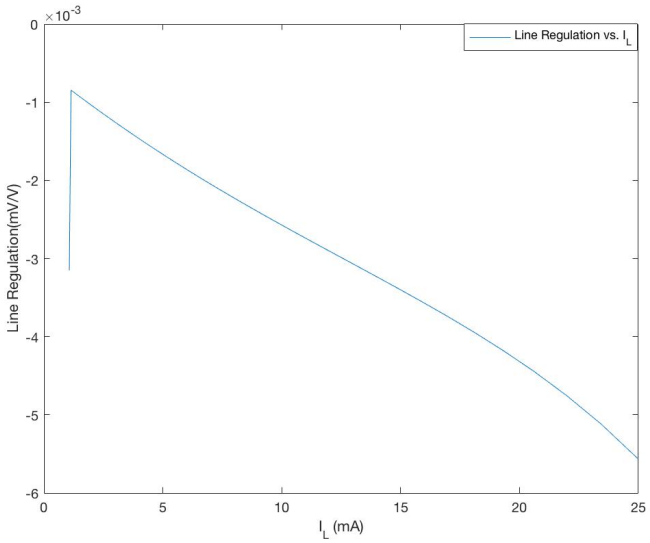


Figure 5. The plot for (a) Load regulation as a function of output voltage and (b) Load regulation as a function of input voltage



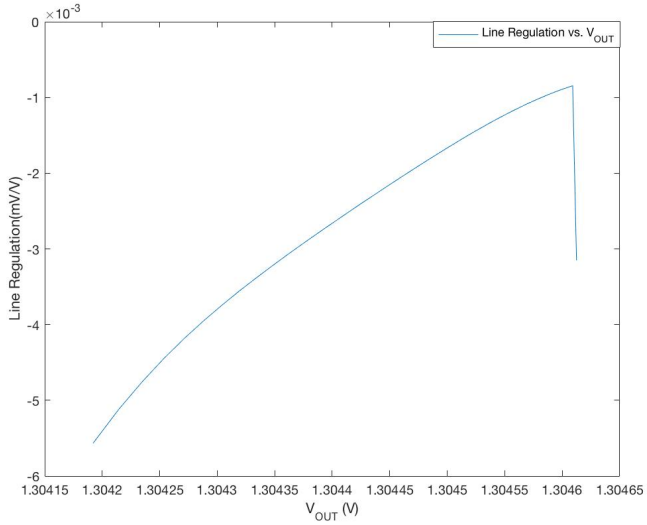


Figure 6. The plot for (a) Line regulation as a function of Load current and (b) Line regulation as a function of output voltage

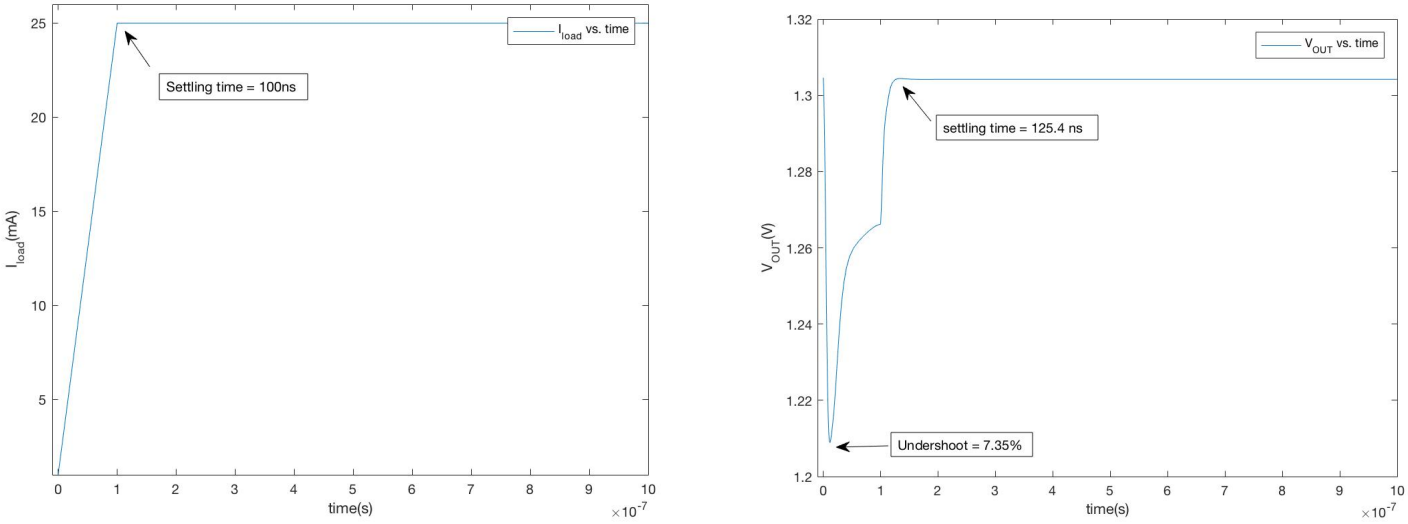


Figure 7. The plot for (a) The current transient response and (b) output voltage transient response

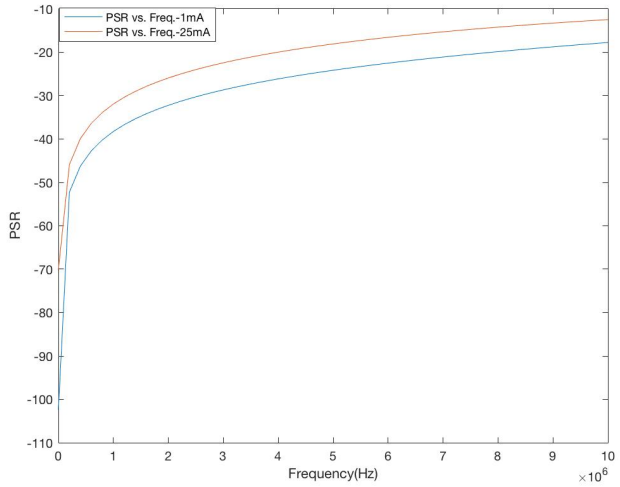


Figure 8. The plot for PSR as a function of Frequency for $\frac{V_{IN}}{V_{OUT}} = \frac{1.8V}{1.3V}$