Sequential logic-2

EEE 241: Digital Logic Design

Department of Electrical and Computer Engineering

Lecture Contents

- Review
- Flip Flops
- SR Flip Flop
- D Flip Flop
- Jk Flip Flop
- T Flip Flop

Reference Readings and Acknowledgements

- Chapter 5: Digital Design with Introduction to Verilog HDL M. Morris Mano, Michael D. Ciletti, 5th Edition

Flip-Flops

- A trigger
  - The state of a latch or flip-flop is switched by a change of the control input
- Level triggered – latches
- Edge triggered – flip-flops

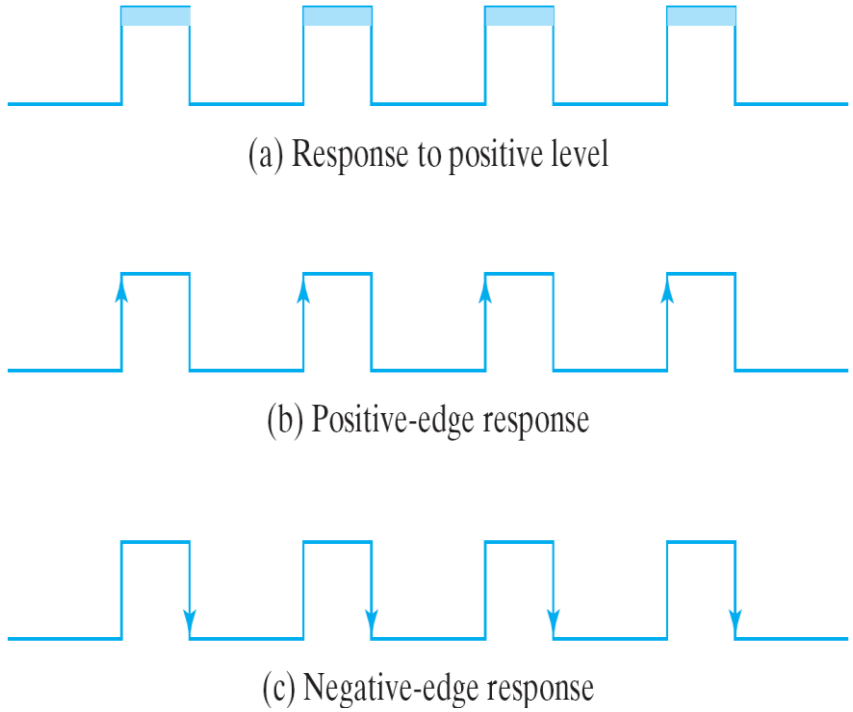
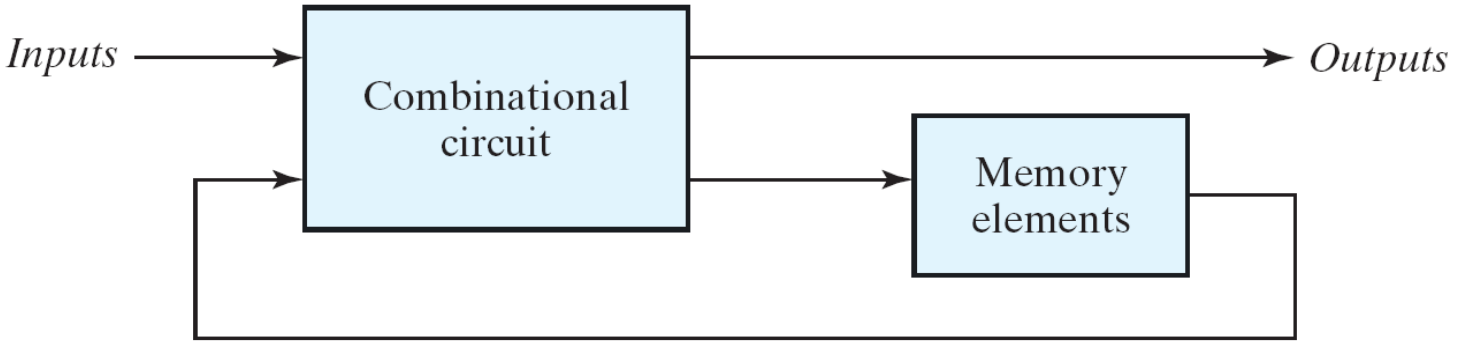


Fig. 5.8

Clock response in latch and flip-flop



- If level-triggered flip-flops are used
  - the feedback path may cause instability problem
- Edge-triggered flip-flops
  - the state transition happens only at the edge
  - eliminate the multiple-transition problem

Edge-triggered D flip-flop

- Master-slave D flip-flop
  - two separate flip-flops
  - a master flip-flop (positive-level triggered)
  - a slave flip-flop (negative-level triggered)

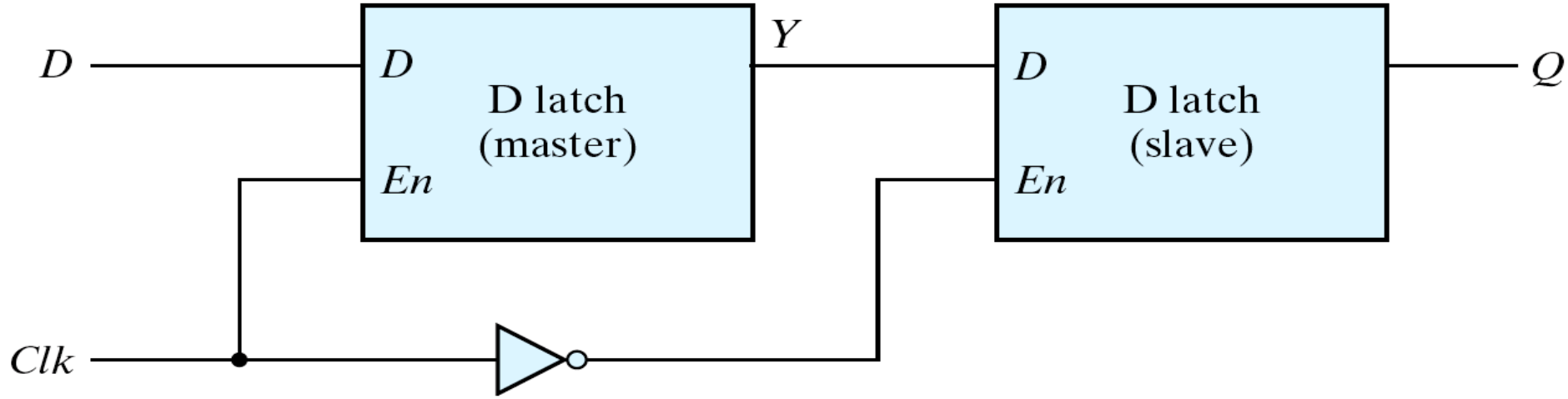
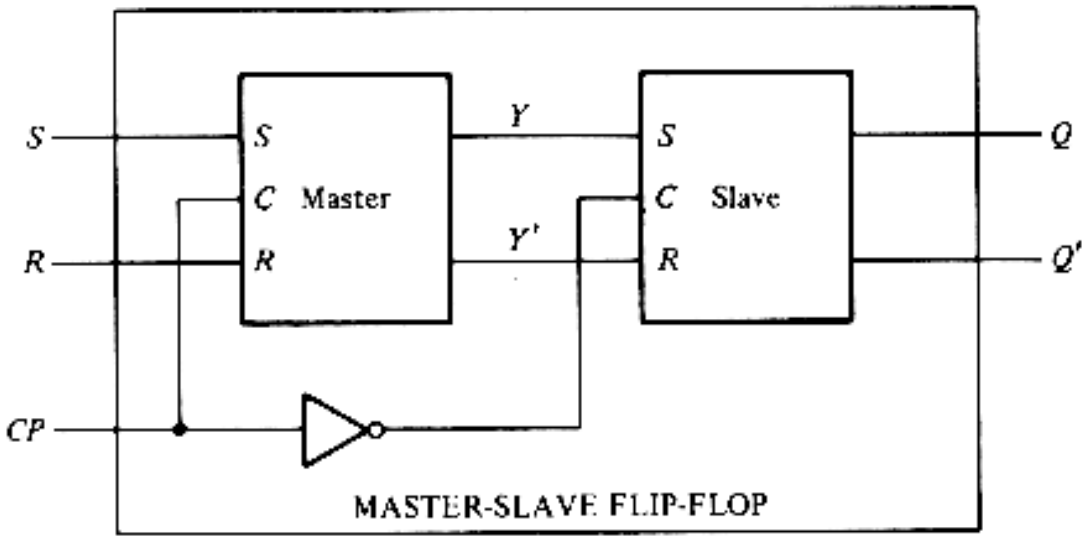
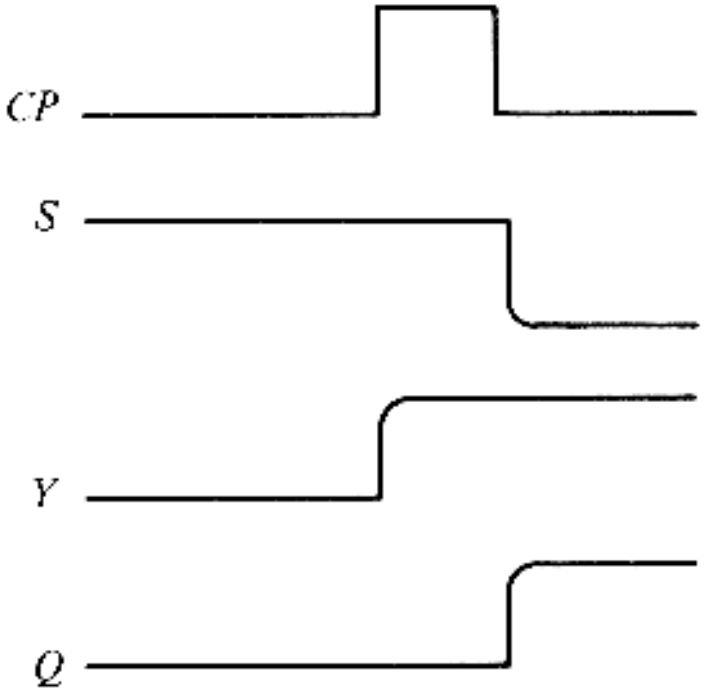


Fig. 5.9
Master-slave *D* flip-flop





- CP = 1: (S,R) ⇒ (Y,Y'); (Q,Q') holds
- CP = 0: (Y,Y') holds; (Y,Y') ⇒ (Q,Q')
- (S,R) could not affect (Q,Q') directly
- the state changes coincide with the negative-edge transition of CP

- Edge-triggered flip-flops
  - the state changes during a clock-pulse transition
- A D-type positive-edge-triggered flip-flop

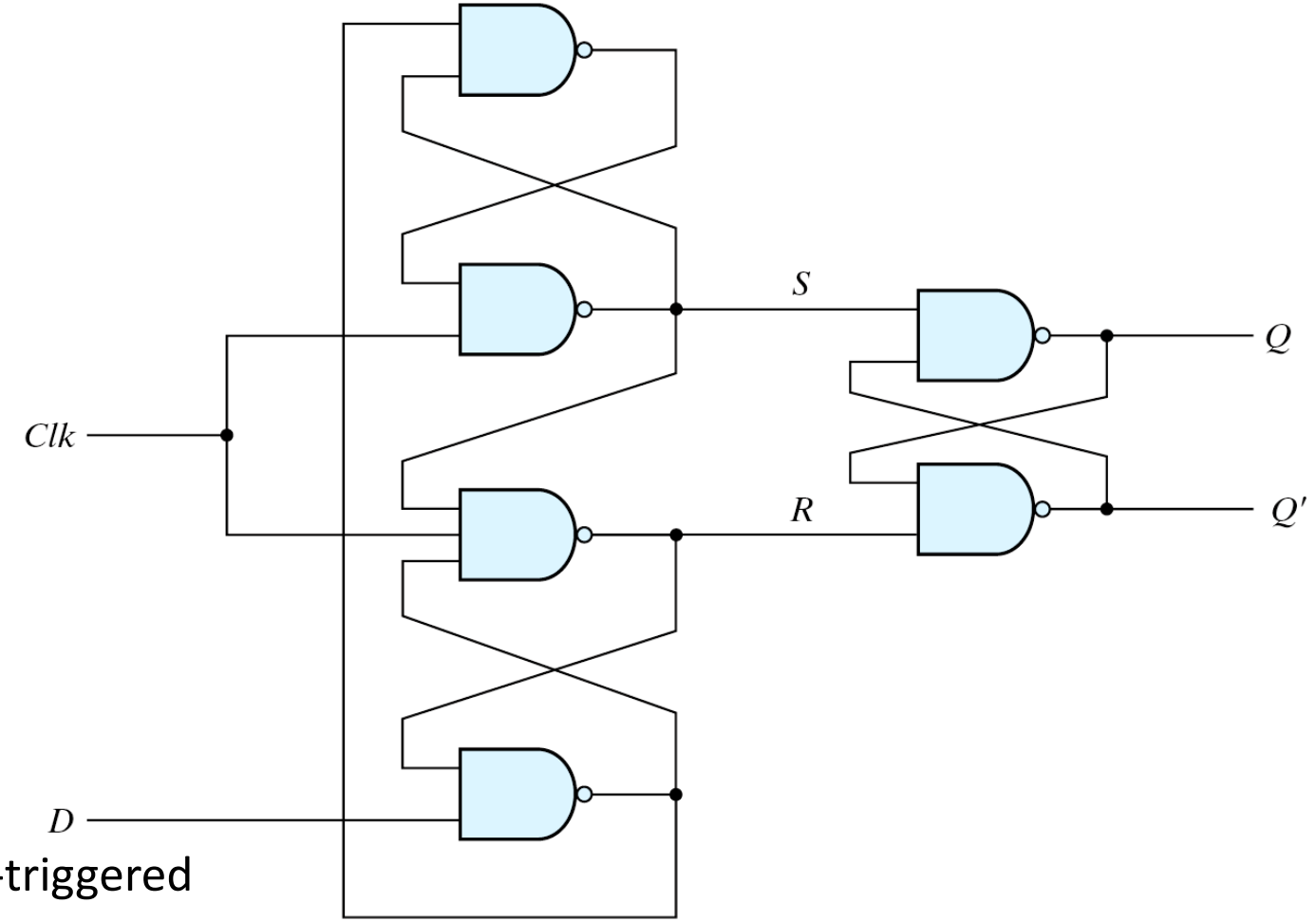


Fig. 5.10
D-type positive-edge-triggered flip-flop

- three basic flip-flops
- (S,R) = (0,1): Q = 1
- (S,R) = (1,0): Q = 0
- (S,R) = (1,1): no operation
- (S,R) = (0,0): should be avoided

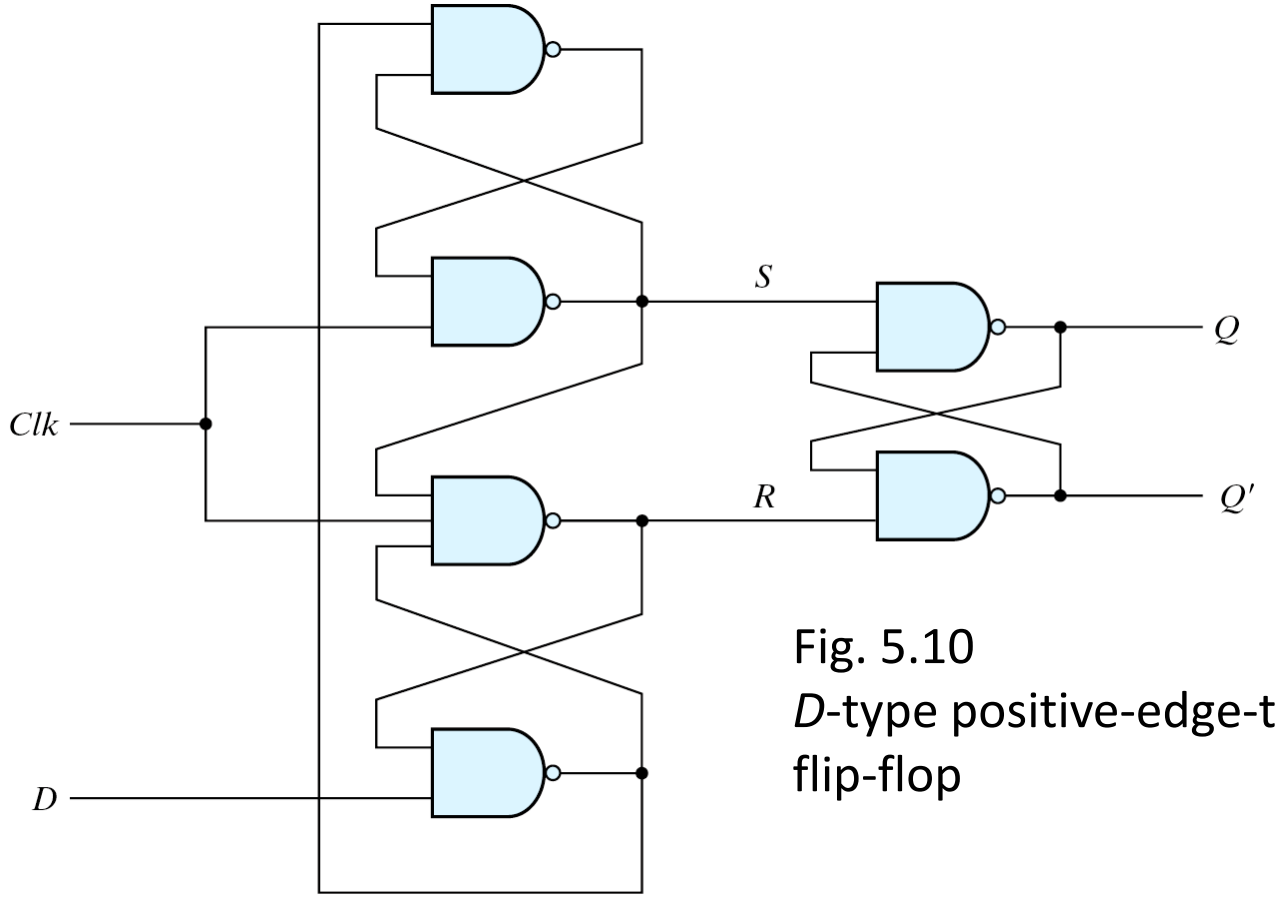
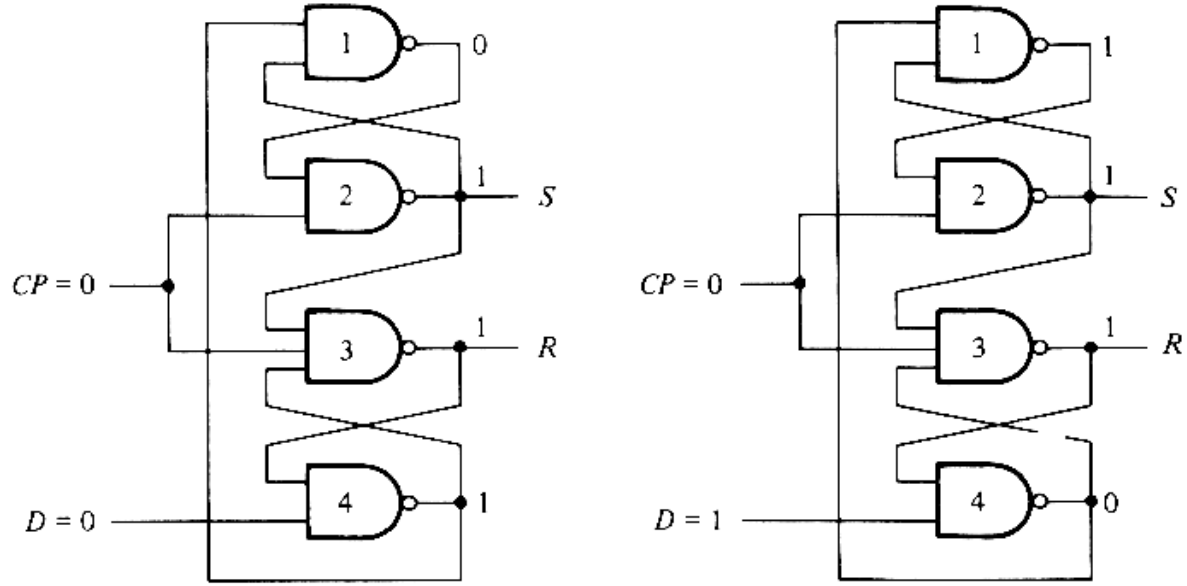
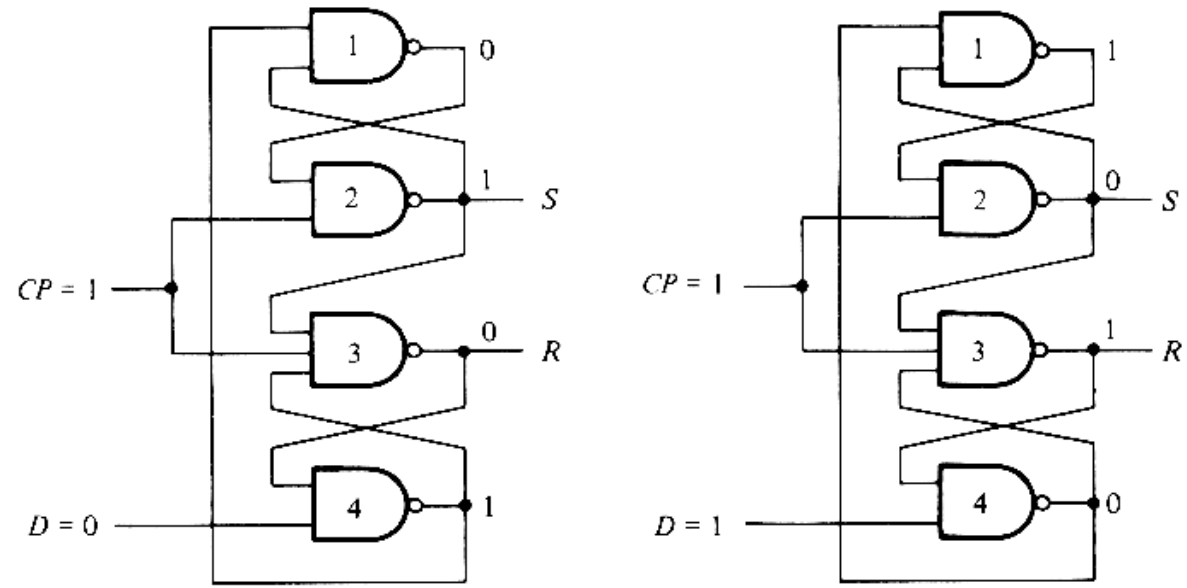


Fig. 5.10
D-type positive-edge-triggered flip-flop

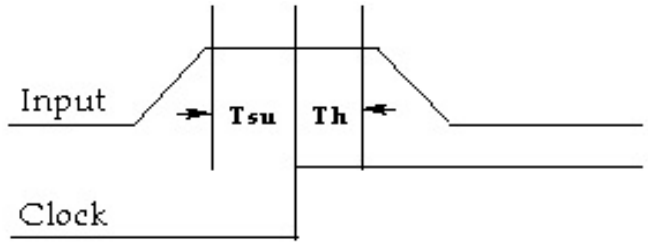


(a) With $CP = 0$



(b) With $CP = 1$

- The setup time
  - D input must be maintained at a constant value prior to the application of the positive CP pulse
- The hold time
  - D input must not changes after the application of the positive CP pulse



- The propagation delay time
  - The interval between the trigger edge and the stabilization of the output to a new state

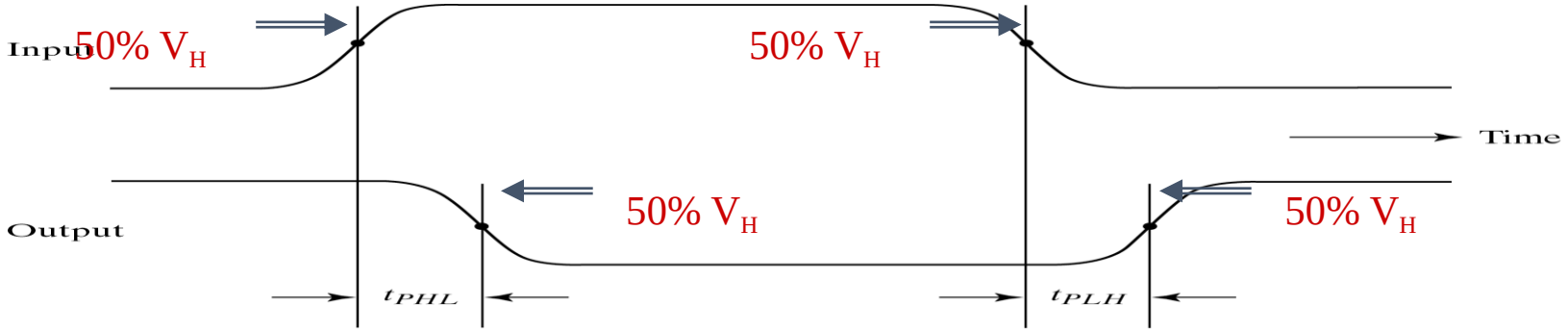
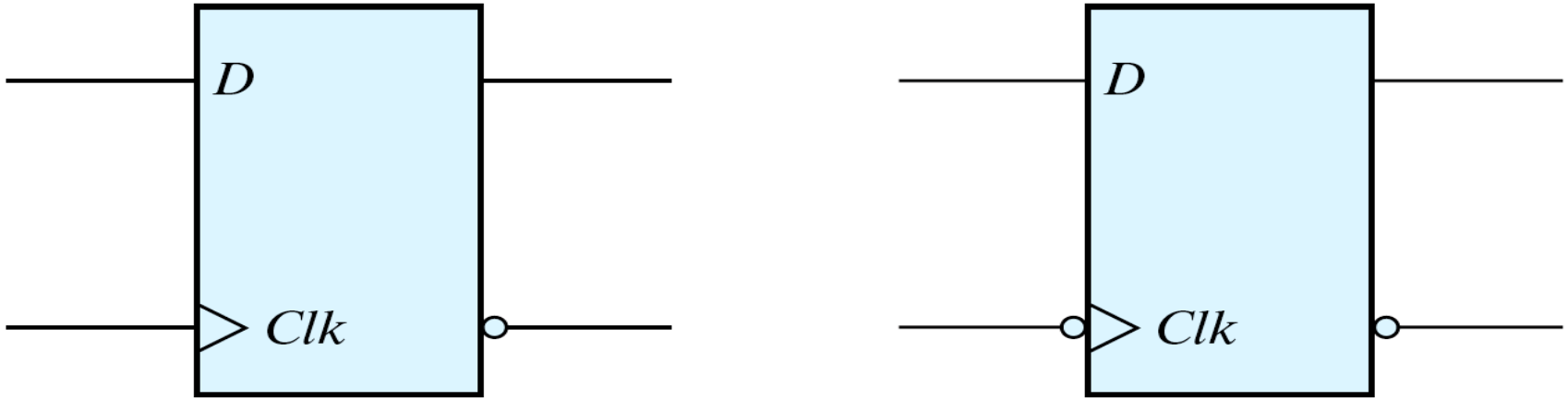


Fig. 10-4 Measurement of Propagation Delay

- Summary
  - CP=0: (S,R) = (1,1), no state change
  - CP=↑: state change once
  - CP=1: state holds

Other Flip-Flops

- The edge-triggered D flip-flops
  - The most economical and efficient
  - Positive-edge and negative-edge

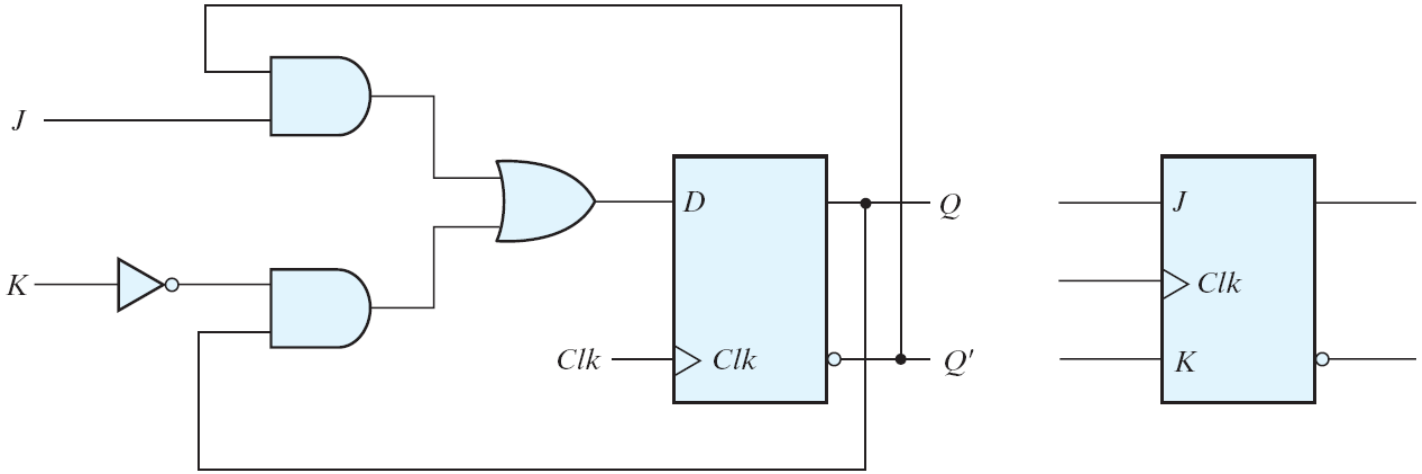


(a) Positive-edge (a) Negative-edge

Fig. 5.11
Graphic symbols for edge-triggered *D* flip-flop

Fig. 5.12
JK flip-flop

- JK flip-flop
  - D=JQ'+K'Q
    - J=0, K=0: D=Q, no change
    - J=0, K=1: D=0 , Q =0
    - J=1, K=0: D=1 , Q =1
    - J=1, K=1: D=Q’ , Q =Q'

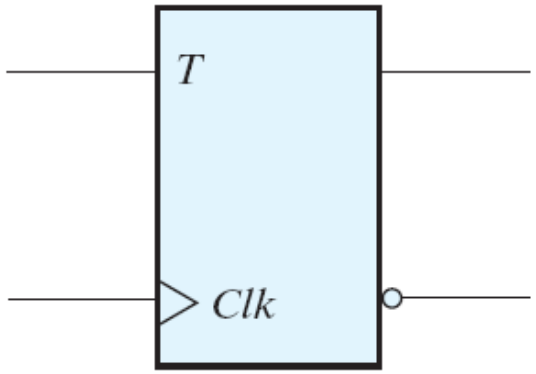


(a) Circuit diagram (b) Graphic symbol

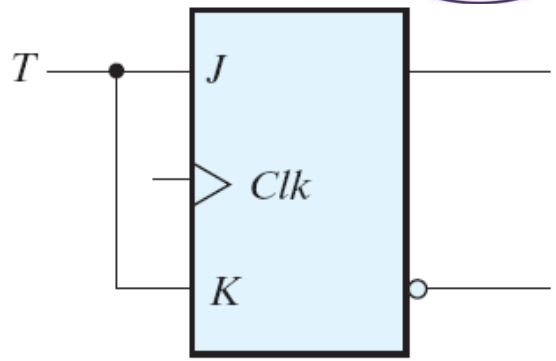
Fig. 5.13
T flip-flop

- T flip-flop

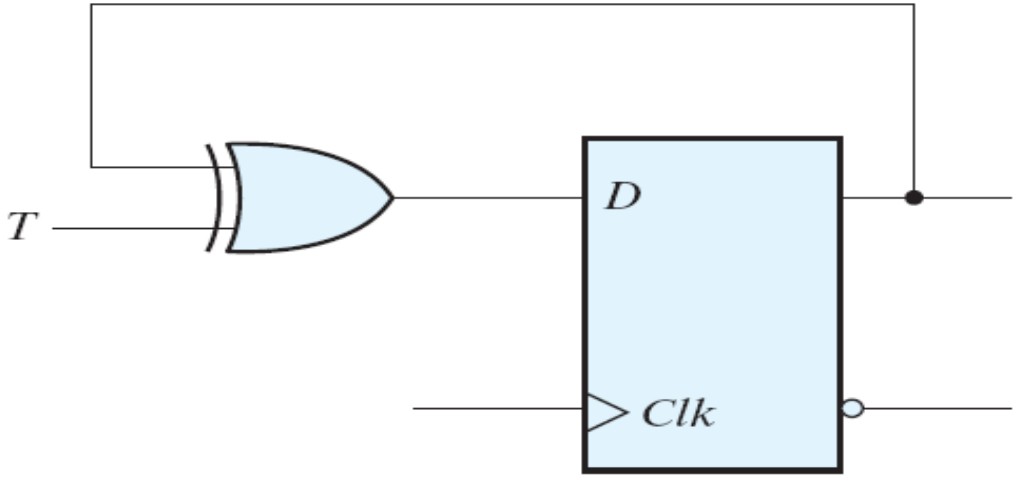
- D = T⊕Q = TQ'+T'Q
  - T=0: D=Q, no change
  - T=1: D=Q’ , Q=Q'



(c) Graphic symbol



(a) From *JK* flip-flop



(b) From *D* flip-flop

- Characteristic tables

Table 5.1
Flip-Flop Characteristic Tables

JK Flip-Flop

J	K	Q(t + 1)	
0	0	$Q(t)$	No change
0	1	0	Reset
1	0	1	Set
1	1	$Q'(t)$	Complement

D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

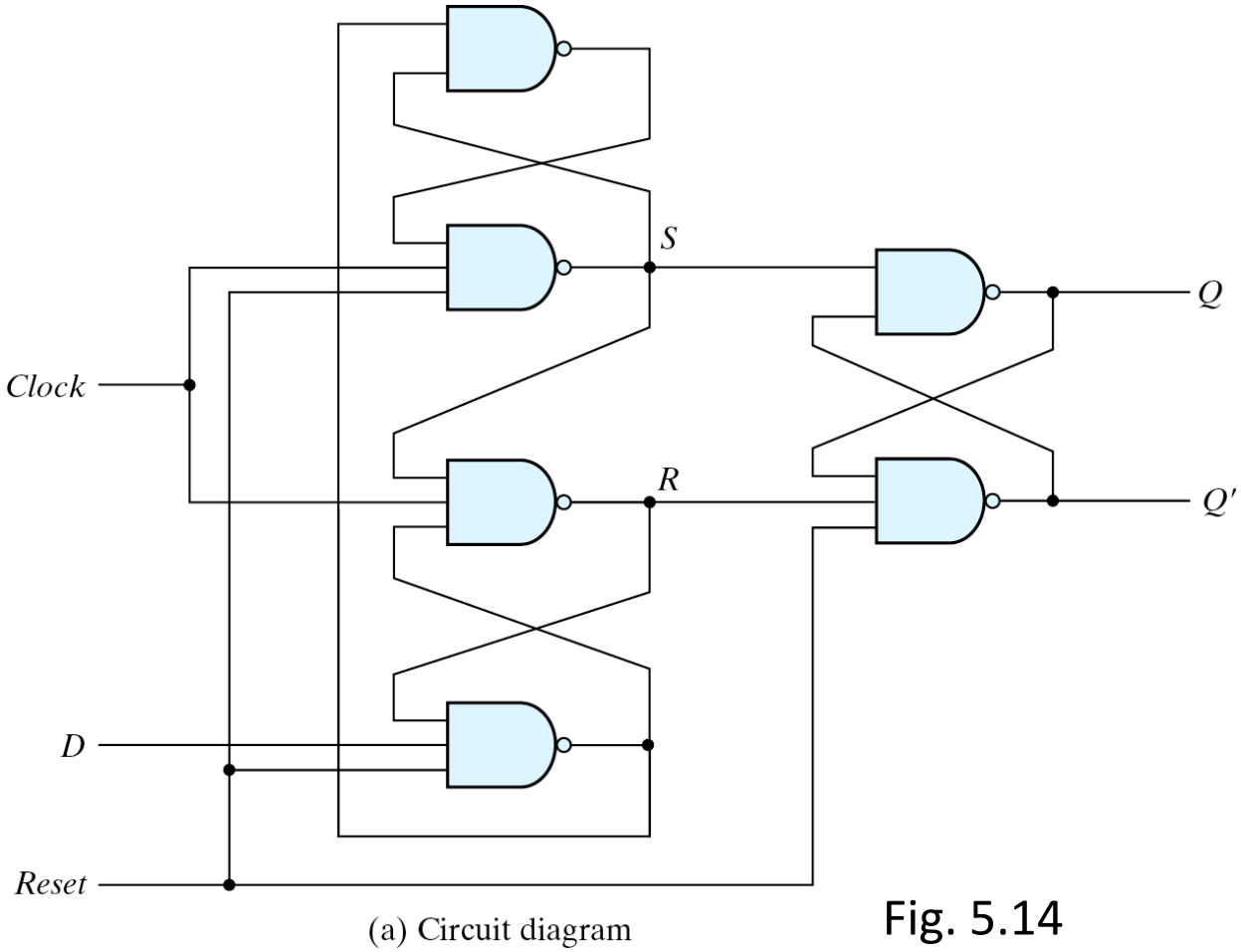
T Flip-Flop

T	Q(t + 1)	
0	$Q(t)$	No change
1	$Q'(t)$	Complement

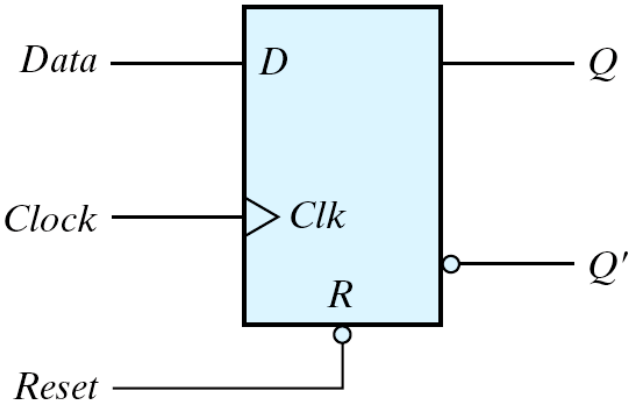
- Characteristic equations
  - D flip-flop
    - $Q(t+1) = D$
  - JK flip-flop
    - $Q(t+1) = JQ'+K'Q$
  - T flop-flop
    - $Q(t+1) = T \oplus Q$

Direct inputs

- asynchronous set and/or asynchronous reset



(a) Circuit diagram



(b) Graphic symbol

R	Clk	D	Q	Q′
0	X	X	0	1
1	↑	0	0	1
1	↑	1	1	0

(b) Function table

Fig. 5.14
D flip-flop with asynchronous reset