ECGR 4101/5101 - Leafure 11
Embedded System app of the day bost loader 1
Now cole Plash Dused to "bast system Now cole Plash PAM Flash PAM Flash
9 Firm wave
Chapter 6
Vin Analogy Vin Analogy Vin Analogy State of the State Vin Analogy Vin Analogy Pevesas Vvef- Pevesas
Specially could be uptoo 18 bits
Setro(hardvere)
· Vref + & Vref - are set (wired)
· Identity ports for input (wire)
· Vrof+ & Vref- are set (wired) · Identify ports) for input (wire) · Ensure signal floats (no-pull-upor pull-down Rs)
Mcontroller provides: 2) Hold circuitry -> takes shapshot 2) AD Conversion > digital representation
2) A/D Conversion > digital representation

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Lecture 11

Guessing Game number between 0 &100

Guess 1 = 50 L

2= 25L

3= 12L

4= 62

5= 31

6 = 1 H

7 = 2 !!!!!

How much time for our somewhite ? Conversion? tD = A/D Cour start delay time tspl= Somple

tSAM = Successive conversion // most

tCONV = tD+tSPL+tSAM <

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LECTURE 11

$$N = \frac{(V_{in}-V_{ref})(2^{N}-1)}{(V_{ref}+-V_{ref}-)} + \frac{1}{2} int$$

Vref+

N= bits most ADC Vin= Input analog signal
Vreft = highest voltage Via could be
Vvef -= lowest voltage Vir could be

Vin = SV Vreft = 10V Vrof - = -10V N=12

what is n? N= 307/10 max. n could be is ZN-1

= 4095 min in could be is o

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CHAPTER 6 / CONVERTING BETWEEN THE ANALOG AND DIGITAL DOMAINS

