Fachgebiet Technische Informatik	Dependability and Fault Tolerance WS 2018/2019	Brandenburgische Technische Universität Cottbus - Senftenberg

Task 1: Investigation of fault effects in digital CMOS circuits

Introduction

Digital circuits can be subject to various fault effects. These may be caused by impurities or parametric variations during the production. Additionally, faults can occur when the circuit is already in operation. The aim of this task is to perform electrical simulations of different faults in a CMOS circuit in order to gain an understanding of the complexity of their causes and their impact on the circuit's functionality. Figure 1 shows the circuit of a two-input NAND gate, which is supposed to be examined in more detail using the OrCAD tool suit which includes the PSpice circuit simulator.

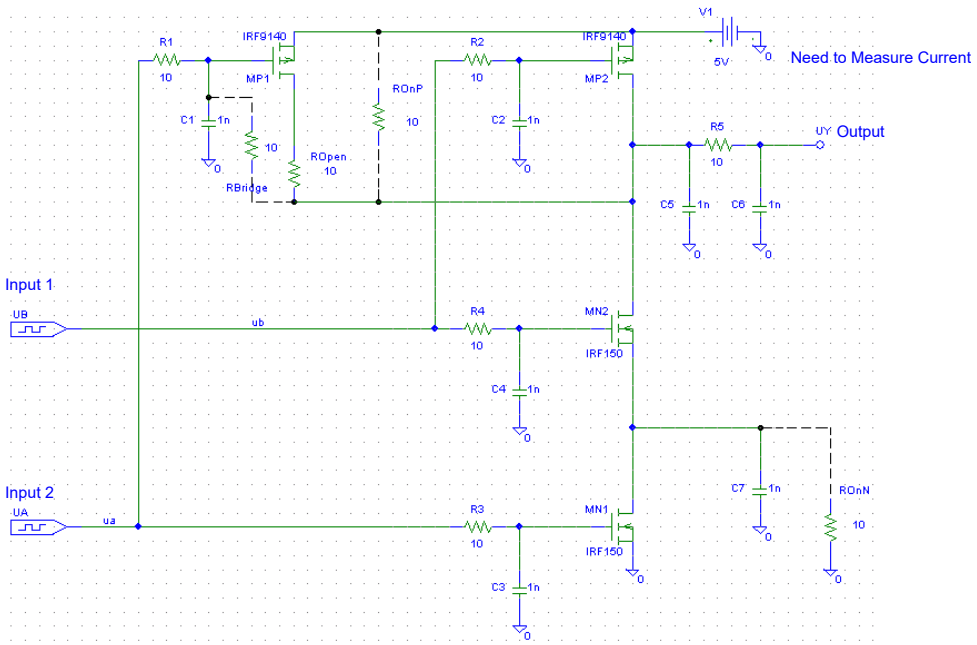


Figure 1: CMOS circuit of a two-input NAND gate

Task 1.1

An OrCAD project with the initial NAND circuit can be found in the given ZIP file. Copy the project to "C:/Laboratory/ZuFT/Task1" on your lab PC, open it in OrCAD and perform a simulation of the defect-free circuit. The signal curves for the inputs of the NAND gate are shown in Figure 2(a). Document the simulation results in the chart in Figure 2(b)!

Task 1.2

Examine the behavior of the circuit from figure 1 for various faults. These can be introduced into the circuit by additional wires and resistors (dashed lines in Figure 1) or by altering already existing resistances. The circuit has to be modified individually for each fault! Log the results into the chart in Figure 3(a), 3(b), 4(a) and 4(b) and note down the quiescent currents (I_{DDQ}) for the input vector 00!

(a) Defect-free circuit — Input vector =00, And measure I(ddq) — Input vector Voltage [VUA:2.4988mV& VUB : 2.4988 mV] — I_{DDQ} = -5.6256 uA

(b) Bridging Fault ($R_{Bridge} = 10\Omega$) — Input vector Voltage [VUA: 123.089mV] — I_{DDQ} = -241.306mA

When to measure other fault I need to make 0 ohm for other fault

(c) Stuck-Open ($R_{Open} = 100k\Omega$) — I_{DDQ} = -5.6256 uA

(d) Stuck-On-P ($R_{OnP} = 10\Omega$) — I_{DDQ} = -5.6256 uA

(e) Stuck-On-N ($R_{OnN} = 10\Omega$) — I_{DDQ} = -11.251 uA

Task 1.3

(a) How does the circuit behavior change if the value of the respective fault resistance is increased/decreased? Determine the resistance value at which the function of the circuit is still just given! The following conditions must be met: maximum voltage of logical $0 = 1V$, minimum voltage of logical $1 = 4V$, maximum switching delay $= 25\mu s$

Fault	Circuit behavior	Function still given at
Bridging Fault	When the resistance is increased then it is observed that the faulty circuit is going to behave like as fault free circuit.	R(Bridge) = 200 ohm
Stuck-Open	When the resistance is decreased then it is observed that the faulty circuit is going to behave like as fault free circuit.	R(Stuck-Open) = 20 Kohm
Stuck-On-P	When the resistance is decreased the it is observed that the circuit is going to behave like faulty circuit and output voltage is given a floating value due to less voltage drop in the resistance ROnP.	R(Stuck-On-P) = 1 ohm
Stuck-On-N	When the resistance is increased then it is observed that the faulty circuit is going to behave like as fault free circuit. Otherwise it try to behave faulty due to short circuit and voltage drop in register ROnN.	R(Stuck-On-N) = 30 ohm

(b) The quiescent current of a fault-free circuit may well vary by around ±50%. Which fault can be detected by measuring the quiescent current (I_{DDQ} test)? Which input vectors can be applied for the detection?

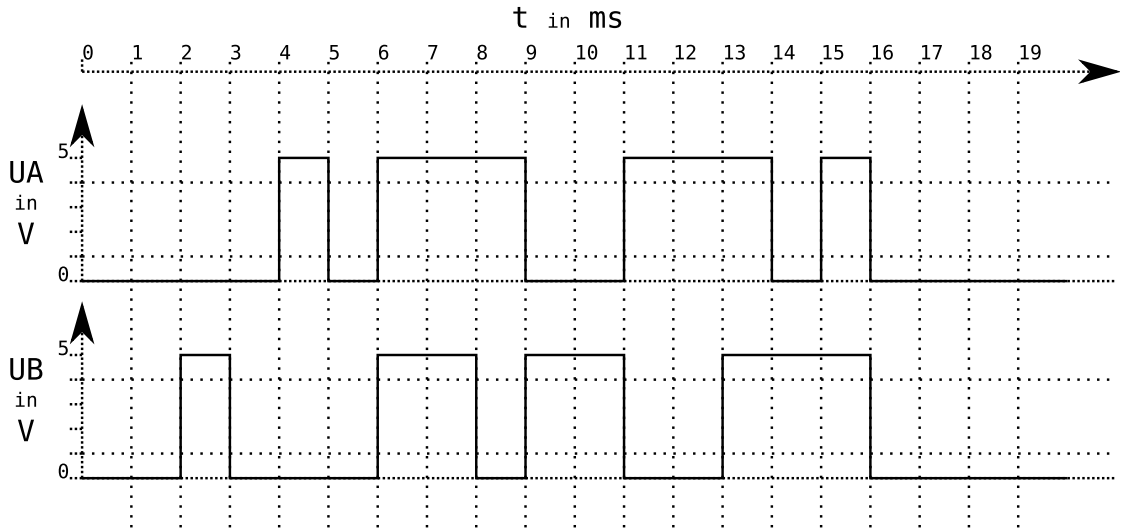
Fault	Detectable by I_{DDQ} test?	Input vector(s)
Bridging Fault	1st, Iq = 111.221mA, then value decreased for 2nd, Iq = 131.797uA, 3rd, Iq =22.158 uA , but still the current flow is more than 1.50%	1st, Va,Vb=(0,1) 2nd Va,Vb=(1,0) 3rd, Va,Vb=(1,1)
Stuck-Open	1st Iq = 882.857 nA current flow decreased 2nd Iq=11.072 uA current flow which is more than 1.50%	1st, Va,Vb=(0,1) 2nd, Va,Vb=(1,0)
Stuck-On-P	1st Iq = 11.251 uA current flow increase 2nd Iq = 484.701 mA current flow increase	1st Va,Vb = (1,0) 2nd Va,Va=(1,1)
Stuck-On-N	Iq = 182.223 mA current flow which is much more than 1.50% and it is maintained through out all the time	1st, 2nd, 3rd, Va,Vb = (0,1) otherwise, Va,Vb=(0,0), (1,0) & (1,1)

(c) Which faults can be detected by observing the circuit's output signal (U_Y)? Write down suitable input vectors or, if required, a sequence of input vectors. Again, the high logic level should be at least $4V$ and the low logic level at most $1V$ to be able to determine the binary value clearly.

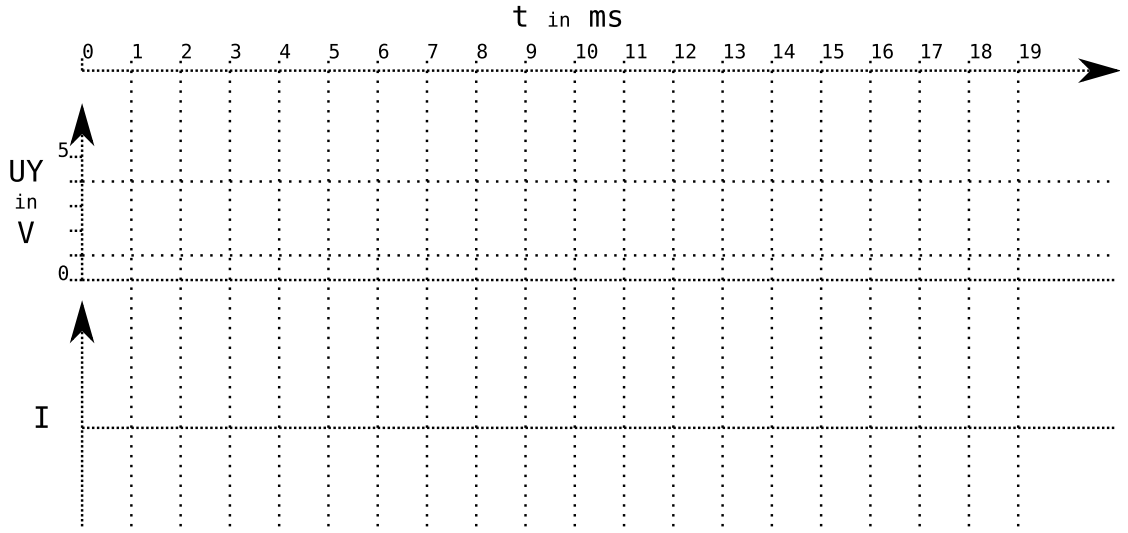
Fault	Input vector or sequence
Bridging Fault	Va,Vb = (0,1) then output signal Uy varies from 5v to 2.2825v.
Stuck-Open	Va,Vb=sequence (1,1) to (0,1) then output signal Uy varies and don't reach the logic '1' voltage level at time 14ms to 15ms
Stuck-On-P	This is not possible by measuring with output voltage Uy.
Stuck-On-N	Va,Vb = (0,1) then output signal Uy varies from 5v to 3.1394v.

(d) Which input vector (or sequence) allows for the detection of the most of the simulated faults if I_{DDQ} and U_Y are observed?

Most of the cases, the detection of the fault can be done with input vector (or sequence) Va,Vb = (0,1) except Stuck-On-P.

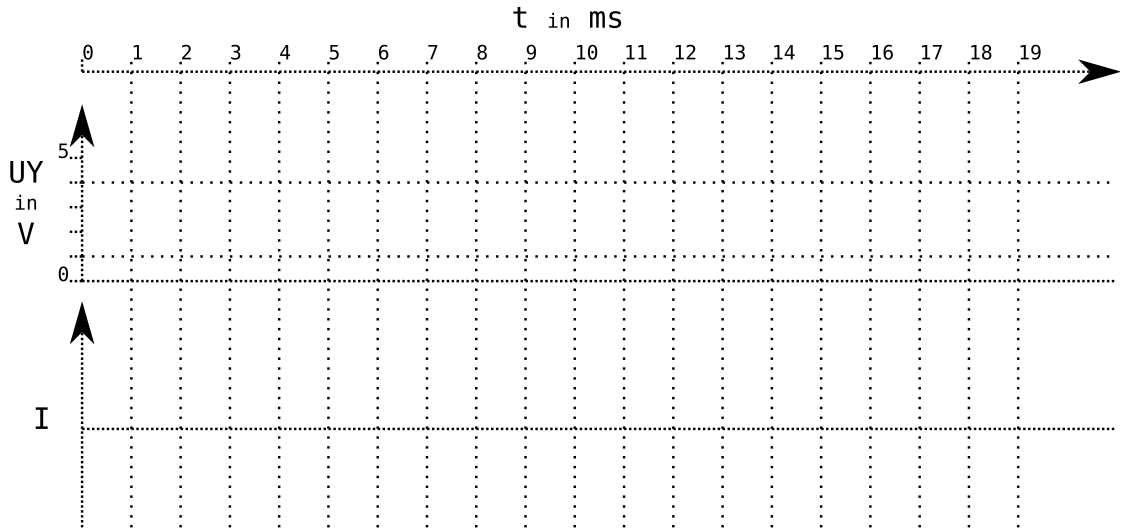


(a)

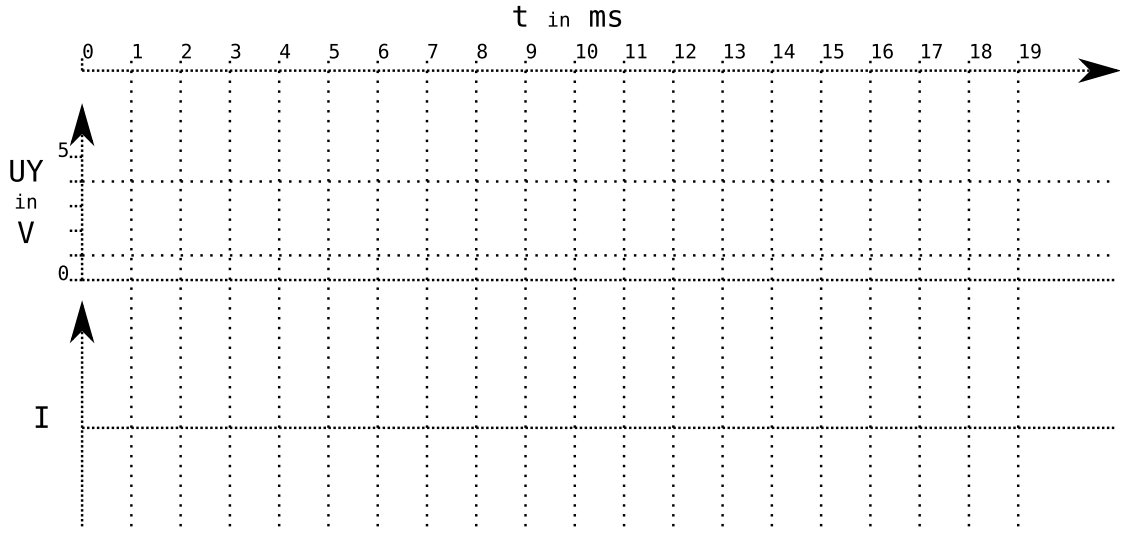


(b)

Figure 2: Curves of the input signals (a) and behavior of the faultless circuit (b)

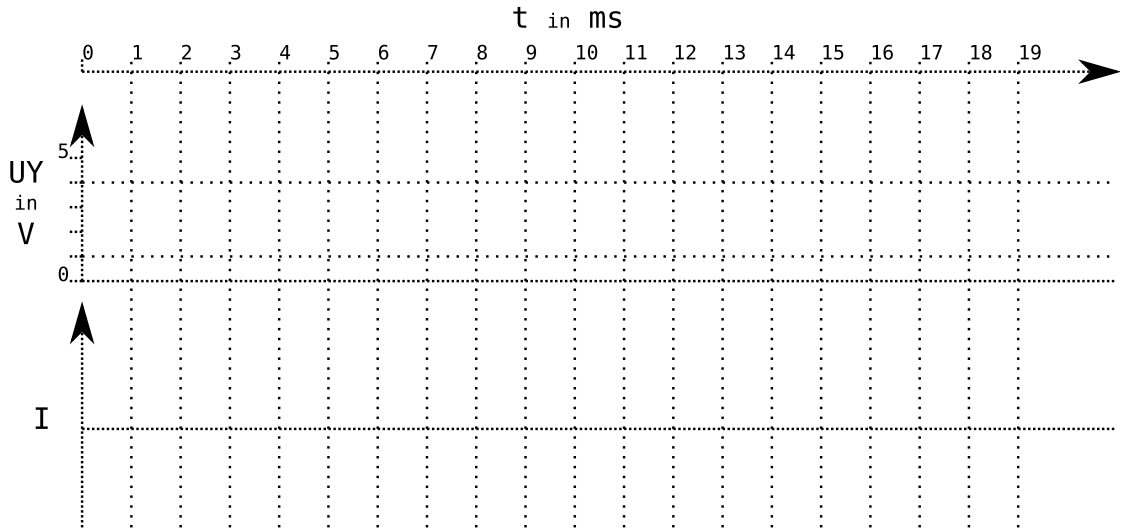


(a)

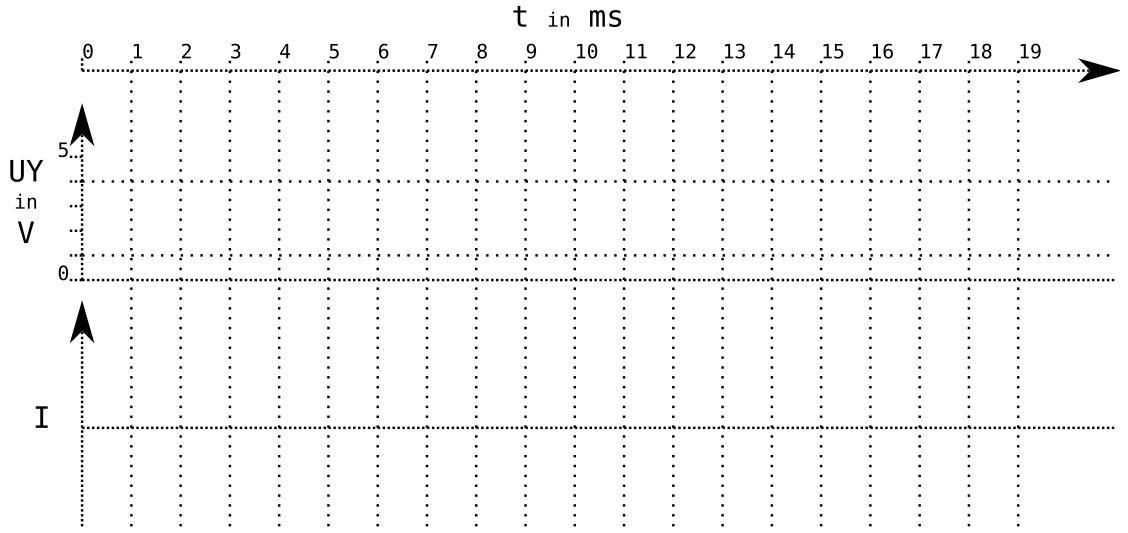


(b)

Figure 3: Behavior of the circuit with a Bridging Fault (a) or a Stuck-Open Fault (b)



(a)



(b)

Figure 4: Behavior of the circuit with a Stuck-On-P Fault (a) or a Stuck-On-N Fault (b)