ECGR 4101/5101 Lecture7 uprocessor architecture Program week RAM (Konholler) notoution Memory Protection Flash ( in controller) Vuits Memory (data) hemory Manage-RAM (ma Po Revesor RX62N-> \* Datapath = 32 bits, 100 MHZ VS Z.6 GHz Intel \* FPV - Floating Point Unit Cost - more silicon \* Memory - RAM 96 K Bytes - Flash (ROM) SIZKBycks - Data Flash (non-volatile) 32k Byles \*Diagnostic Data \* Calibration Data - Address space = 232

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\* Clock - built in

\* Reset

\* DMA - Direct memory access

\* Timers / counters

\* Sevial ports

\* Communication

\* A/D g D/A Converters

Operations +, -, \*, :

\*\* Carry (

\*\* hegative

\*\* positive

\*\* Zero

\*\* Over flow

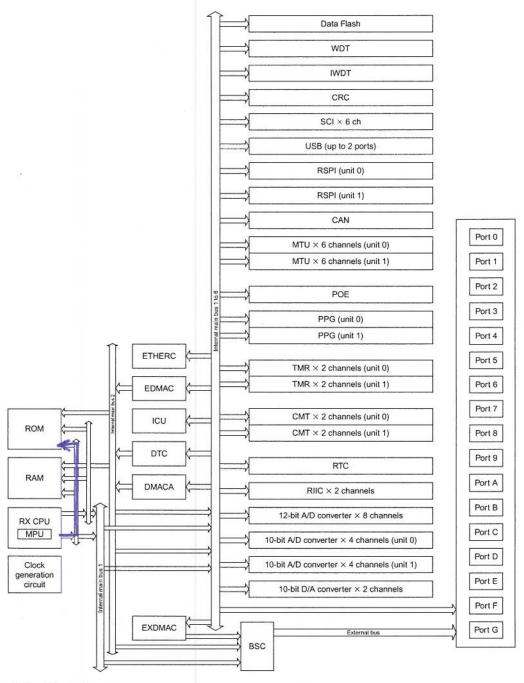
Status word

\*\* Interrupt level

\*\* Tuterrupt enable

2

#### 40 EMBEDDED SYSTEMS USING THE RENESAS RX62N MICROCONTROLLER



**Figure 3.5** Block diagram. Source: *Hardware Manual, Renesas 32-Bit Microcomputer, RX Family/RX600 Series,* Renesas Electronics America, Inc., 2010, Figure 1.2, page 1–12.

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Lecture 7

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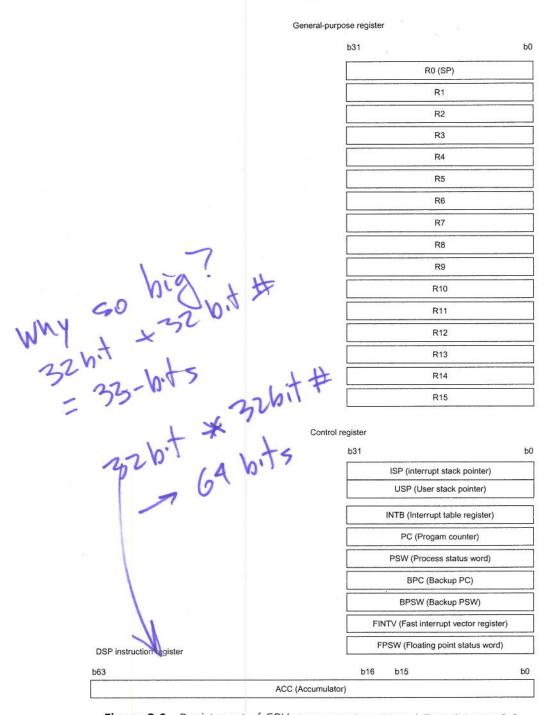


Figure 3.6 Register set of CPU. Source: Hardware Manual, Figure 2.1, page 2–2.



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### 1. Integer:

		b7	bC
Signed byte (8-bit) Integer			
		b7	b0
Unsigned byte (8-bit) Integer			
	b15		b0
Signed word (16-bit) Integer			
	b15		b0
Unsigned word (16-bit) Integer			
b31			b0
Signed longword (32-bit) Integer			
b31		THE RESERVED TO SERVED TO	bC
Unsigned longword (32-bit) Integer			

Figure 3.10 Integer. Source: Hardware Manual, Figure 2.2, page 2-14.

### 2. Floating-Point:

The IEEE standard defines four different types of precision for floating point operations. They are single precision, double precision, single-extended precision, and double-extended precision. Most of the floating-point hardware follows IEEE 754 standard's single and double precision for floating point computations. RX family supports single precision floating-point computation. There are in total eight operations that can be done with such floating-point operands: FADD, FCMP, FDIV, FMUL, FSUB, FTOI, ITOF, and ROUND.

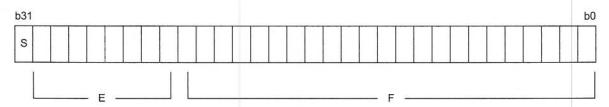


Figure 3.11 Floating point. Source: Hardware Manual, Figure 2.3, page 2-14.

Single-precision floating-point

S: Sign (1 bit)

E: Exponent (8 bits)

F: Mantissa (23 bits)

Value = 
$$(-1)^S \times (1 + F \times 2^{-23}) \times 2^{(E-127)}$$

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Figure 3.15 Data arrangement in registers. Source: Hardware Manual, Figure 2.6, page 2–21.

Data type Address			Little endian								Big endian							
	b7							b0		b7							b0	
Address L	7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
Address L	MSB							LSB		MSB							LSB	
Address M Address M + 1	MSB							LSB		MSB							LSB	
Address N Address N + 1 Address N + 2								LSB		MSB								
Address N + 3	MSB																LSB	
	Address L  Address M  Address M + 1  Address N  Address N + 1  Address N + 2	Address L 7  Address L MSB  Address M	Address L	Address L	Address L	Address L	Address L	Address L	b7	Address L	b7	b7	b7	b7	b7	b7	b7	

Figure 3.16 Data arrangement in memory. Source: Hardware Manual, Figure 2.7, page 2–21.

#### 3.2.6 Bus Specification

In total, there are five different types of buses in RX62N microcontroller board. The following section lists various bus specifications. It describes whether the bus operates in synchronization with a clock or not.

#### 1. CPU bus:

## Instruction bus:

It is connected to the CPU and to the on-chip memory such as on-chip RAM and on-chip ROM. It operates in synchronization with the system clock (ICLK).