ECGR 4101/5101

Ledure &

Embedded app of the day Stone Coton

Oven Controller ->

(1) × (1+F×2-23) × 2(E4127) Value

Where S= sign (+ or -, meaning Oor 1)

E = Exponent 8 bits

F: Manlissa 23 bit actual value

range 0 to 2²⁴1 range 0 to 2²³-1
0 to 8,388,607

15,0 1111 = 15.510 [[1]] =

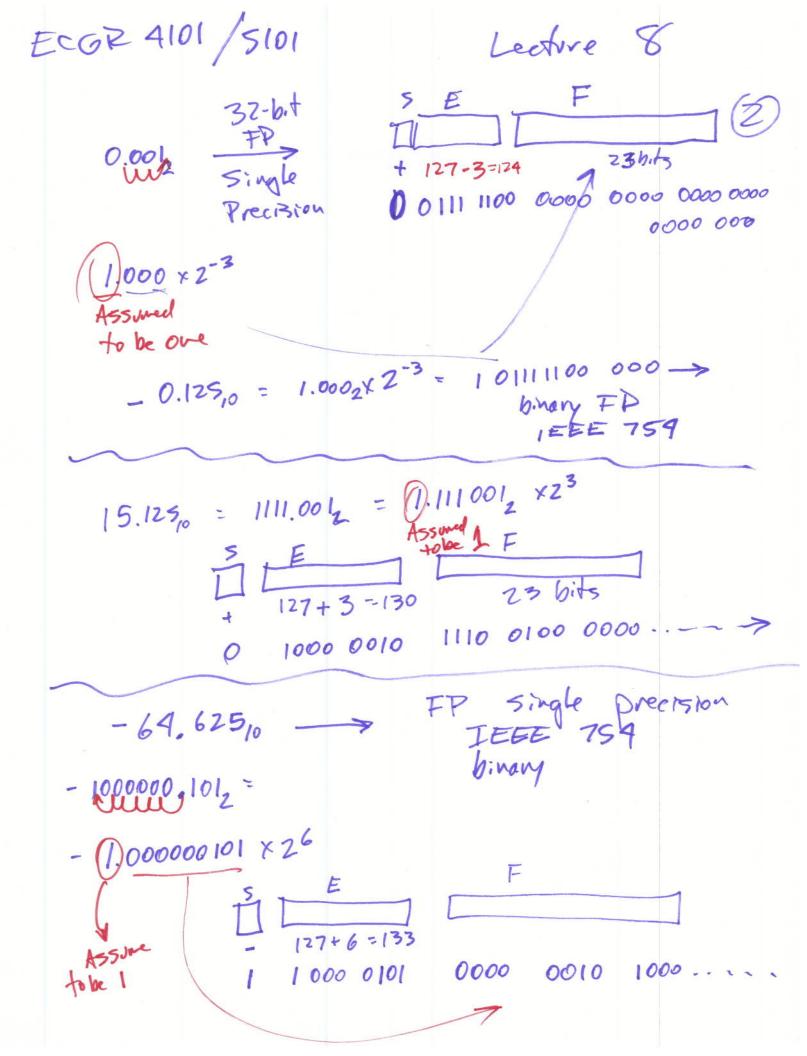
15.2510 1111.01 =

15.125 1111.001 =

0.125,0 0.001 =

0.0012 = 1.0002 x 2 3

1111,0012 = 1.1110012 × 23



ECGR 4101/5101 Lecture 8 Clodes External Bus Clock -> 100 MHZ BCLK SDRAM Clock SORAL SOCK -> SOMHZ Seral Clock -> Set this AD Clock -> Set this 5,1 Pipe line Laundry Wash dry Sort washer dryer told Total Time = 6T wash dry fold wash (try fold wash dry fold AT ST 6T 7T 8T 9T 10

Switch (x) {
Case 3:

break;

Case 4:

is true the highest % of the true first

ECGR 4101/5101

Lecture 8

CHAPTER 3 / ORGANIZATION AND ARCHITECTURE . . .



	Single-chip mode*2		On-chip ROM enabled extended mode		On-chip ROM disabled extended mode
0000 0000h	On-chip RAM	0000 0000h	On-chip RAM	0000 0000h	On-chip RAM
0001 8000h	Reserved area"	0001 8000h	Reserved area 1	0001 8000h	Reserved area"
0000 8000h	Perpheral I/O registers	0008 0000h	Perpheral I/O registers	0008 0000h	Perpheral I/O registers
0010 0000h	On-chip ROM (data flash)	0010 0000h	On-chip ROM (data flash)	0010 0000h	
0010 8000h	Reserved area*1	0010 8000h	Reserved area ⁻¹		
07F 8000h	FCU-RAM ³	007F 8000h	FCU-RAM ³		3
07F A000h	Reserved area ^{'1}	007F A000h	Reserved area ¹¹		16
07F C000h	Perpheral I/O registers	007F C000h	Perpheral I/O registers		Reserved area
07F C500h	Reserved area ^{*1}	007F C500h	Reserved area		Reserved area
07F FC00h	Perpheral I/O registers	007F FC00h	Perpheral I/O registers		
080 0000h	Reserved area ^{"1}	0080 0000h	Reserved area ^{*1}		
0F8 0000h	On-chip ROM (program ROM) (write only)	00F8 0000h	On-chip ROM (program ROM) (write only)		
100 0000h		0100 0000h		0100 0000h	
£		0800 0000h	External address space (CS area)	0800 0000h	External address space (CS area)
			External address space (SDRAM)	0.000.000.000	External address space (SDRAM)
	□ Reserved area 1 □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □ □	1000 0000h		1000 0000h	9
				- 1	
	reserved area	*	ະ Reserved area້¹ ≈	*	Reserved area ^{*1}
EFF E000h	On-chip ROM (FCU firmware) ³	EEEE E000b	On-chip ROM (FCU firmware) ³	~	Reserved area ^{*1}
EFF E000h	On-chip ROM (FCU firmware) ³ (read only)	EEEE E000b	On-chip ROM (FCU firmware) ³ (read only)	FF00 0000h	⊱ Reserved area ' ≃
F00 0000h	On-chip ROM (FCU firmware) ³ (read only) Reserved area ¹ On-chip ROM (user boot)	FEFF E000h	On-chip ROM (FCU firmware) ³ (read only) Reserved area ¹ On-chip ROM (user boot)		
	On-chip ROM (FCU firmware) ² (read only) Reserved area ² On-chip ROM (user boot) (read only)	FEFF E000h FF00 0000h	On-chip ROM (FCU firmware) ³ (read only) Reserved area ³ On-chip ROM (user boot) (read only)		Reserved area **
F00 0000h F00 C000h	On-chip ROM (FCU firmware) ³ (read only) Reserved area ¹ On-chip ROM (user boot)	FEFF E000h FF00 0000h FF7F C000h FF80 0000h	On-chip ROM (FCU firmware) ³ (read only) Reserved area ¹ On-chip ROM (user boot)		0.000.000.000.000

- 1. Reserved areas should not be accessed, since the correct operation of LSI is not guaranteed if they are accessed.
 2. The address space in boot mode and user boot mode is the same as the address space in single-chip mode.
 3. For details on the FCU, see section 37, ROM (Flash Memory for Code Storage) and section 38, Data Flash (Flash Memory for Data Storage) in the Hardware Manual.

Figure 3.31 Memory map in each operating mode. Source: Hardware Manual, Figure 4.1, page 4–1.