Assignment 3 – Amplifier Design

Section 1: Design and investigate the DC, AC and transient responses of a single-stage Op-amp by simulation and analysis.

a) Calculate the aspect ratios of all transistors (i.e. M1, M2, M3, M4, Mo, and Mbias) in the design. Make sure to represent these as a whole number of λ_m. Show your calculations and final values

[10/100]

To determine value of I_o

From $\frac{dQ}{dt} = I_o = C_L \frac{dV_0}{dt}$

Hence $I_o = SR \times C_L$

To satisfy the provide slew rate (SR = $v/\mu sec$) for a known load capacitance (C_L)

$$I_o = 5\ v/\mu sec \times 20\ pF$$
$$= 0.1\ mA$$

To determine aspect ratio of M1, M2

From $GB = \frac{g_{m1,2}}{2\pi C_L}$ and $g_m = \frac{dI_{Dsat}}{dV_{GS}}$

Hence $\left(\frac{W}{L}\right)_{M1} = \frac{(g_{m1,2})^2}{2I_{D1}K_{n1}}$

To satisfy the setting of gain-bandwidth product *GB* of 1 MHz at unity gain (0 dB)

$$GB = gain \times bandwidth$$
$$= 1 \times 1\ MHz = 1\ M$$

$$g_{m1,2} = GB \times 2\pi \times C_L$$
$$= 1M \times 2\pi \times 20pF = 125.7\ \mu$$

$$I_{D1} = I_o/2$$

$$\left(\frac{W}{L}\right)_{M1} = \frac{(g_{m1,2})^2}{2I_{D1}K_n} = \frac{(125.7\ \mu)^2}{2 \times \left(\frac{0.1\ m}{2}\right) \times 96.4\ \mu} = 1.64$$

From $\left(\frac{W}{L}\right)_{M1} = 2$, given $W_{M1} = 4\lambda_m$ (4.8 µm) and $L_{M1} = 2\lambda_m$ (2.4 µm).

For matched devices, ratio of M1 and M2 are the same.
Hence W_{M2} = 4λm (4.8 µm) and L_{M2} = 2λm (2.4 µm).

To determine aspect ratio of M3, M4

To ensure M1 is saturated,

$$V_{DSM1} \geq V_{GSM1} - V_{Tn1}$$
$$V_{x1} \geq V_{in1(max)} - V_{Tn}$$
$$\geq 4.5\ V - 0.79\ V = 3.71\ V$$

where $V_{in1(max)}$ is the maximum input voltage or ICMR (+) and V_{Tn} is the threshold voltage of M1.

The minimum value of V_{x1} is 3.71 V.

From V_{x1} = 3.71 V, so V_{GSM3} = 3.71 V − 5 V = − 1.29 V.

$$\left(\frac{W}{L}\right)_{M3} = \frac{2I_{D3}}{K_p\left(V_{GSM3} - V_{Tp}\right)^2}$$
$$= \frac{0.1\ mA}{29.4\ \mu \times \left(-1.29\ V - (-0.91V)\right)^2}$$
$$= 23.56$$

From $\left(\frac{W}{L}\right)_{M3} = 24$, given W_{M3} = 96λm (115.2 µm) and L_{M3} = 4λm (24.8 µm).

For matched devices, ratio of M3 and M4 are the same.
Hence W_{M4} = 96λm (115.2 µm) and L_{M4} = 4λm (24.8 µm).

To determine aspect ratio of M_o, M_{bias}

To ensure M1 is saturated,

$$V_{\mathrm{GSM1}} \geq V_{\mathrm{in1(min)}} - V_{\mathrm{DSMo}}$$

where $V_{in1(min)}$ is the minimum input voltage or ICMR (-).

From $\frac{I_o}{2} = \frac{\left(\frac{W}{L}\right)_{M1}}{2} K_n (V_{GSM1} - V_{Tn})^2$

0.1 mA = 2 × 96.4 µ/V² × $(V_{GSM1} - 0.79\ V)^2$

V_{GSM1} = 1.51 V

From $V_{\mathrm{GSM1}} \geq V_{\mathrm{in1(min)}} - V_{\mathrm{DSMo}}$

$1.51\ \mathrm{V} \geq 0.5\ \mathrm{V} - V_{\mathrm{DSMo}}$

$V_{\mathrm{DSMo}} = -1.01\ \mathrm{V}$

To ensure Mo is saturated, $V_{DSMo} = V_{GSMo} - V_{Tn}$.

From $I_{Mo} = \frac{\left(\frac{W}{L}\right)_{Mo}}{2} K_n (V_{GSMo} - V_{Tn})^2$

$I_{Mo} = \frac{\left(\frac{W}{L}\right)_{Mo}}{2} K_n (V_{DSMo})^2$

$$0.1\ \mathrm{mA} = \frac{\left(\frac{W}{L}\right)_{Mo}}{2} \times 96.4\ \mu\mathrm{V}^2 \times (-1.01\ V)^2$$

$$\left(\frac{W}{L}\right)_{Mo} = 2.03$$

From $\left(\frac{W}{L}\right)_{M0} = 2.5$, given W_{Mo} = 5λm (6.0 µm) and L_{Mo} = 2λm (2.4 µm).

For matched devices, ratio of Mo and Mbias are the same.

Hence W_{Mbias} = 5λm (6.0 µm) and L_{Mbias} = 2λm (2.4µm).

b) Show the corresponding simulation results for your amplifier DC, AC (i.e. Bode and phase plots) and transient (i.e. slew rate, rise/fall edge) responses

[10/100]

Figure 1 represents circuit schematic of a single-stage differential CMOS Op-amp with aspect ratio of M1 and M2 are 4 λ_m /2 λ_m, the aspect ratio of M3 and M4 are 48 λ_m /2 λ_m, and the aspect ratio of M_o and M_{bias} are 5 λ_m /2 λ_m.

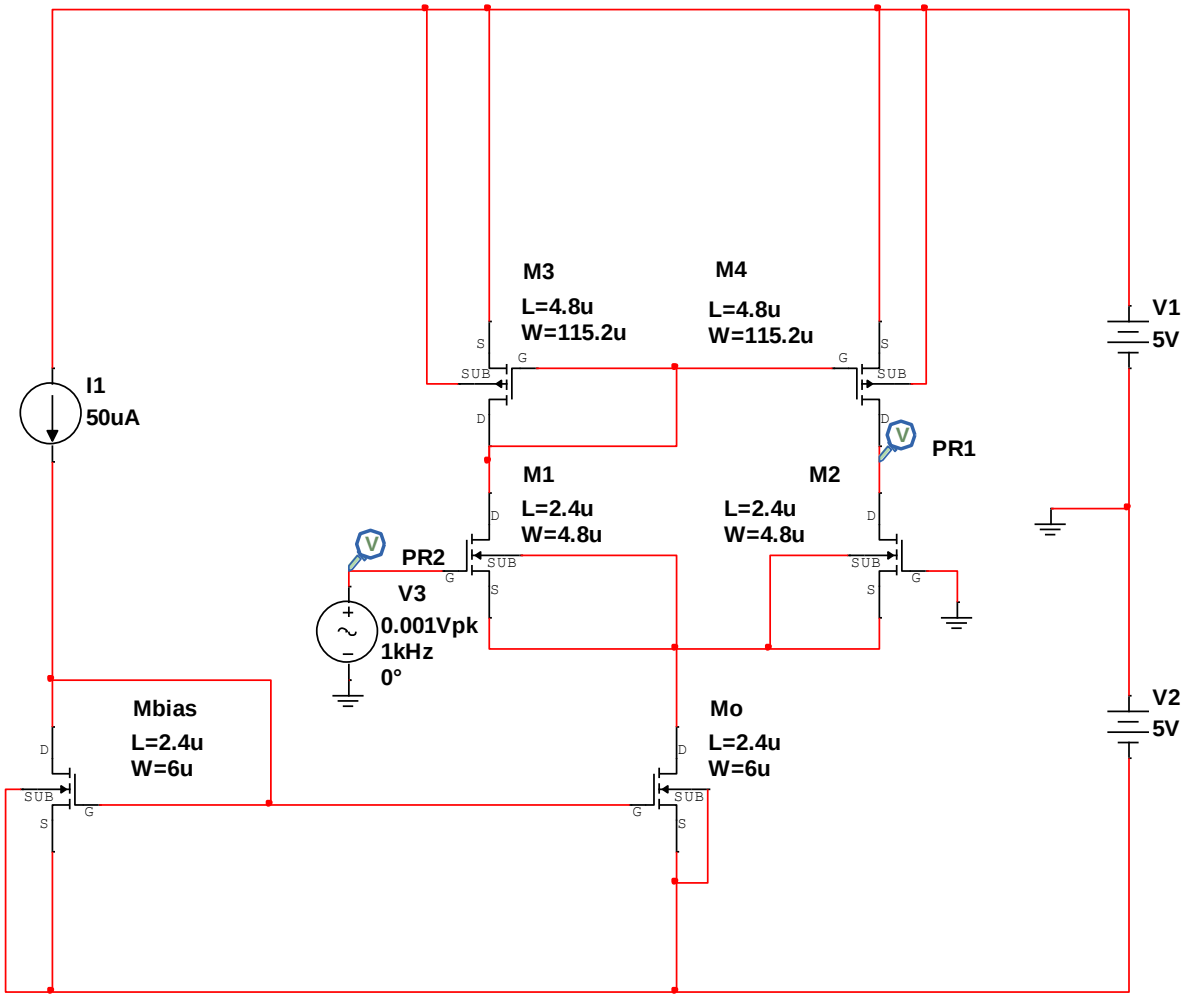


Figure 1 Circuit design of a single-stage differential CMOS Op-amp (Design no.1).

Figure 2 represents transient responses of single stage op-amp (design no.1), the rise time of Vout is 294.8 µs and the fall time of Vout is 106.4 µs. The amplitude of input signal is 999.2 µV - (-999.2 µV) = 2 mV while the amplitude of Vout is 3.9765 V - 3.6388 = 0.3 V. The slope of output signal is (3.9427 - 3.6726)V/(2.1471-1.8523)ms = 0.001 V/µs.

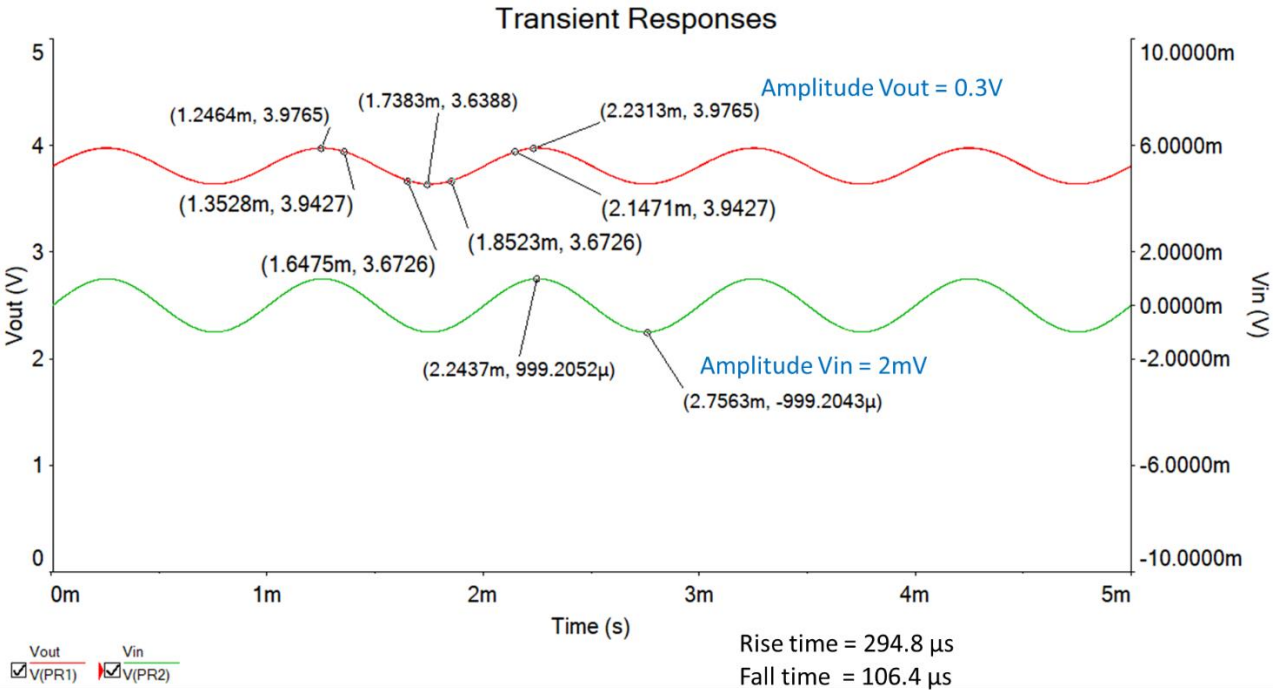


Figure 2 Transient responses (design no.1)

Figure 3 represents DC transfer characteristic of single stage op-amp (design no.1), the slope of the graph is 575. Figure 4 illustrates AC sweep of single stage op-amp (design no.1), at 1MHz, the magnitude is 52.8 dB (~440) and the phase margin is 26°. While frequency at 822 MHz, the magnitude of output is 0dB (gain = 1).

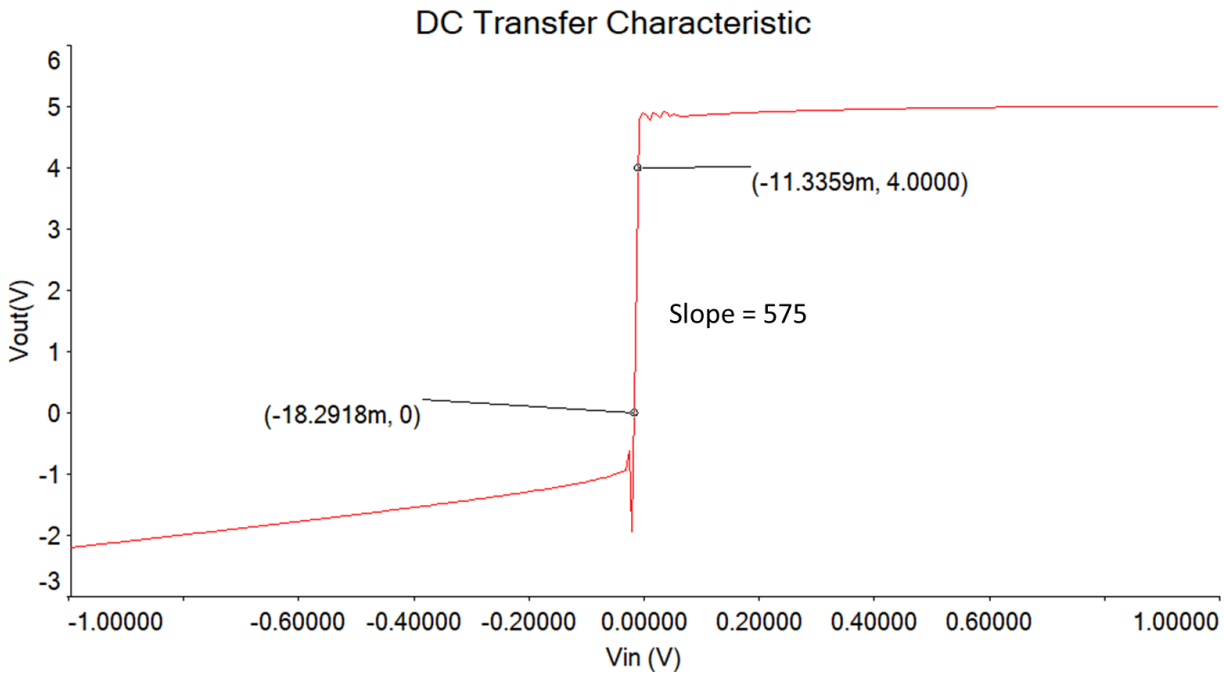


Figure 3 DC transfer characteristics (design no.1)

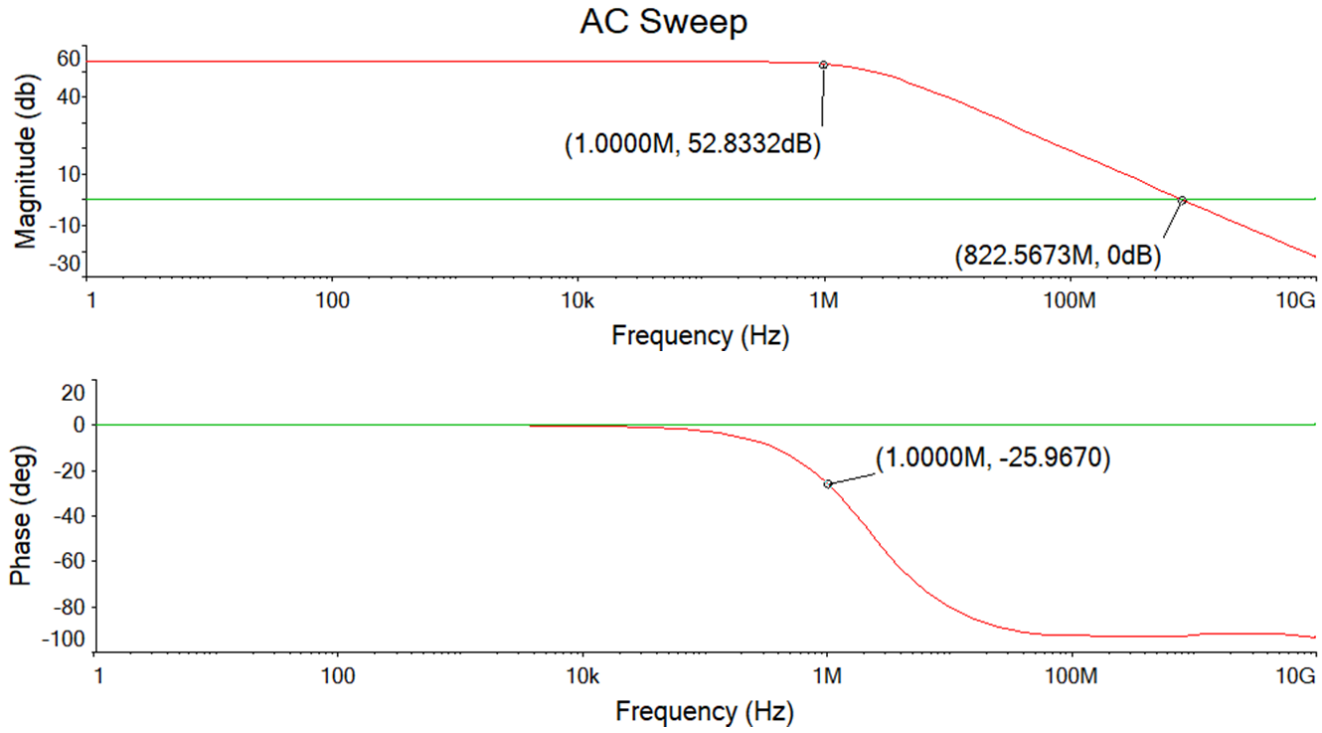


Figure 4 AC sweep (design no.1)

c) Analyse the responses obtained in b), and extract/examine the key parameters from the characteristics including gain, gain-bandwidth and phase-margin etc. Compare and comment on the outputs obtained from the simulations to those provided in the specifications

[10/100]

From the DC transfer characteristic of the single-stage op-amp (Figure 3), the slope of the graph is 575, which corresponds to the gain of the circuit. Comparing this to the expected Av of greater than 100 ($\geqslant$ 40 dB), this circuit meets expectations. However, at a frequency of 1MHz, the magnitude is 52.8 dB (approximately 440), and the phase margin is 26°, which means that the gain-bandwidth product of 1MHz is satisfactory, although the phase margin falls short of the expected 60°. At unity gain, this circuit can operate at 822MHz, which exceeds the expected frequency of 1MHz. Hence, there is a need to improve the phase margin for 1d.

d) Further optimise your design and show how the gain and gain-bandwidth may be improved using this design architecture.

[10/100]

Increasing the width of the transistors increases the bandwidth, but at the same time, it can introduce parasitic capacitance, which can degrade the phase margin. On the other hand, increasing the length reduces the bandwidth but can improve the phase margin by reducing the effect of parasitic capacitance.

In design no.2, the aspect ratio of M1, M2 (1/2) are the same but the width and length are different, the new WM1, WM2 = 4λm (4.8 µm) and LM1, LM2= 8λm (9.6 µm). Figure 5 represents transient response of new design, the rise time of Vout is 293.6 µs and the fall time of Vout is 296.1 µs. In this design both rise and fall time has nearly same value as matched devices. The amplitude of input signal is 999.2 µV - (-999.2 µV) = 2 mV while the amplitude of Vout is 4.2450 V - 3.3798 V = 0.87 V. The amplitude of Vout is 2.5 times previous amplitude. The slope of output signal is (3.9427 - 3.6726) V/ (2.1471-1.8523) ms = 0.002 V/µs which means the skew rate is increased.

Figure 6 illustrates DC transfer graph of improved design width and length; the slope is increased to 985. Figure 7 shows AC sweep of new circuit values which the gain-bandwidth is increased to 57.5 dB at 1MHz, while the phase is also increased to 63° more than the expected of 60°. The frequency at unity gain is decreased to 646.7 MHz which is more than setting value.

Normally, when the aspect ratio is same, the gain should not change due to equation $g_m \approx \sqrt{2I_D\beta}$ and $A_v = -\sqrt{\frac{2}{I_D}}\left(\frac{\sqrt{\beta_1}+\sqrt{\beta_2}}{\lambda_1+\lambda_2}\right)$ but when the length is changed, the length modulation is changed too, that explain why when we double both width and length of transistors, the gain is changed.

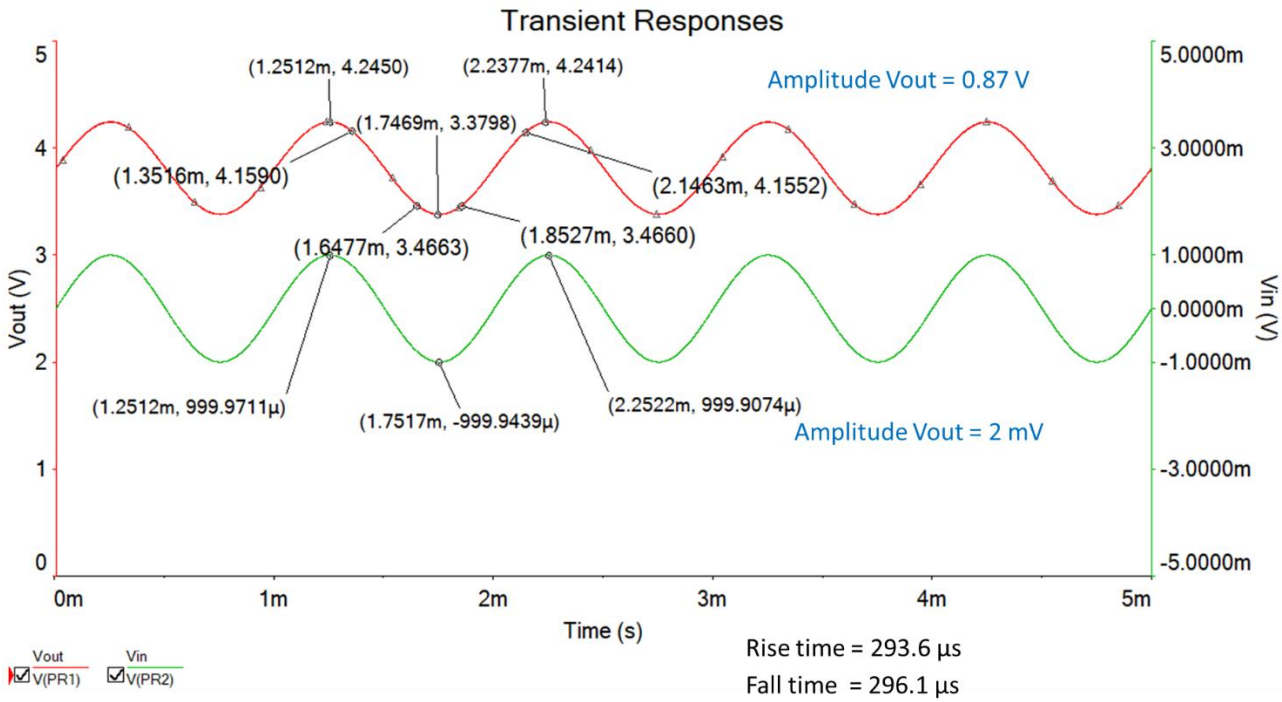


Figure 5 Transient responses (design no.2)

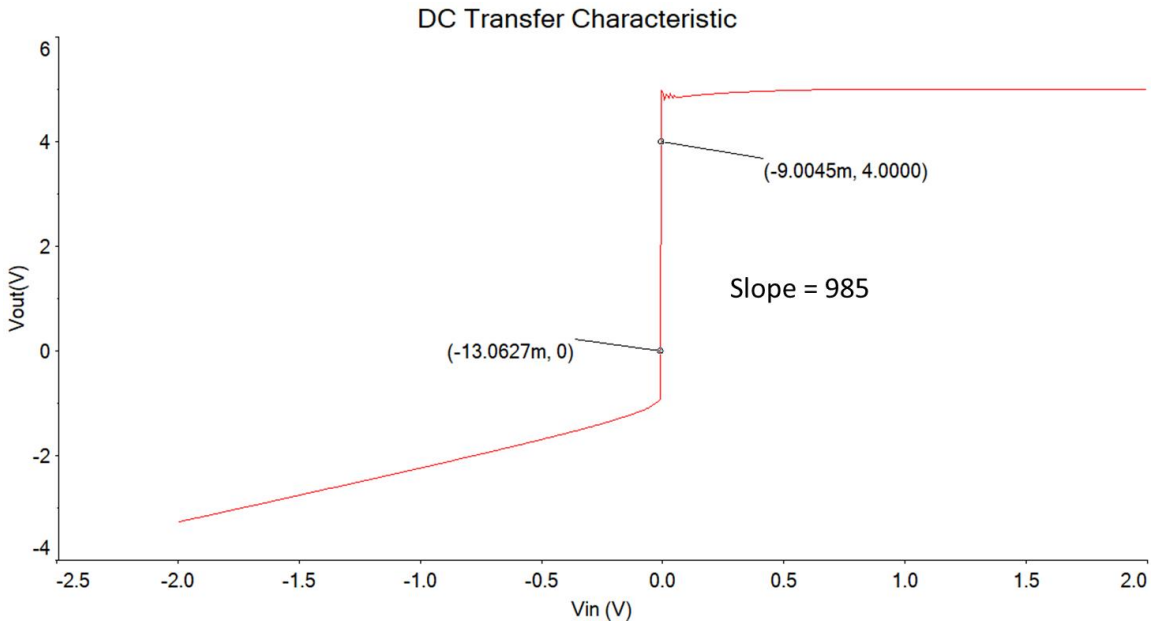


Figure 6 DC transfer characteristics (design no.2)

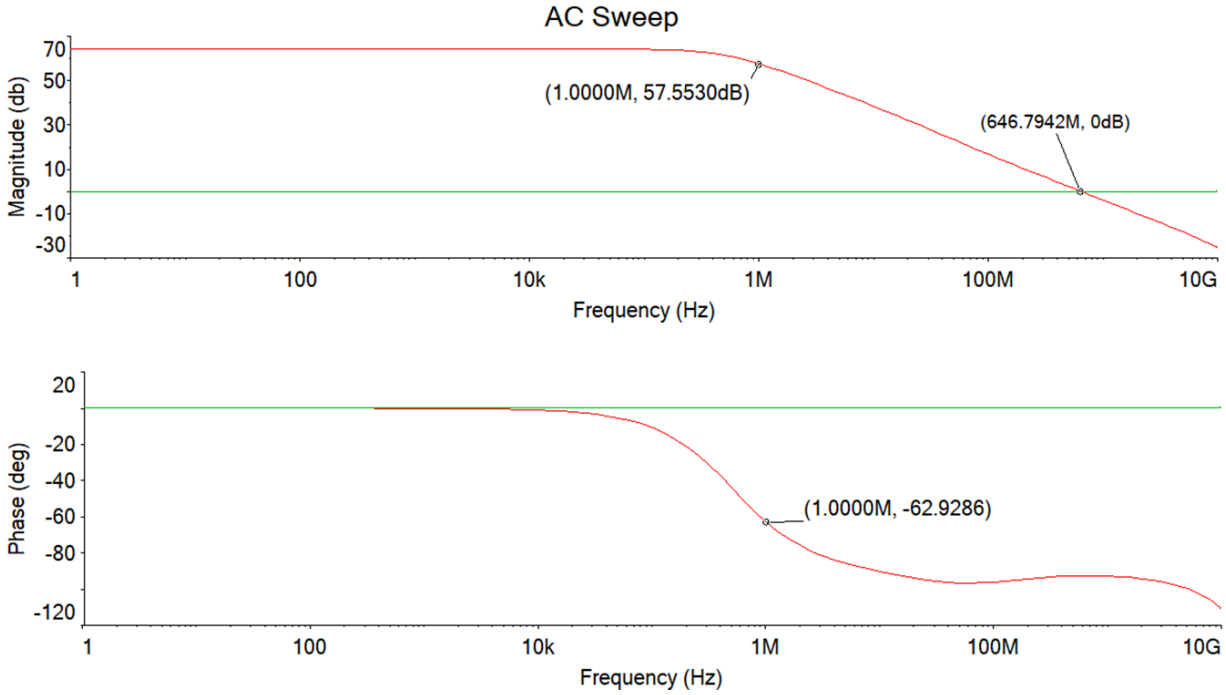


Figure 7 AC sweep (design no.2)

In design no.3, the aspect ratio of M1, M2 (1/2) are the same but the width and length are different, the new WM1, WM2 = 6λm (7.2 μm) and LM1, LM2= 12λm (14.4μm). Figure 8 represents transient response of design no.3, the rise time of Vout is 293.5 μs and the fall time of Vout is 294 μs. In this design both rise and fall time has nearly same value as matched devices. The amplitude of input signal is 999.9 μV - (-999.7 μV) = 2 mV while the amplitude of Vout is 4.2450 V - 3.3798 = 1.1 V. The amplitude of Vout is increased compared to previous design. The slope of output signal is (4.2430 - 3.3736) V/ (2.1470-1.8535) ms = 0.003 V/μs which means the skew rate is increased.

Figure 9 illustrates DC transfer graph of improved design; the slope is increased to 953 nearly the same gain. Figure 10 shows AC sweep of new circuit values which the gain-bandwidth is increased to 57.4 dB at 1MHz, while the phase is also increased to 78° indicating more stability in the design circuit. The bandwidth at unity gain is decreased to 560 MHz but it is still acceptable.

To summarize, a single-stage CMOS op-amp is its limited gain and bandwidth compared to multi-stage designs. Single-stage op-amps typically have lower gain and bandwidth due to the constraints of a single amplification stage, which may restrict their applicability in high-performance applications requiring higher gain or wider bandwidth. Additionally, single-stage op-amps may exhibit higher levels of distortion and noise compared to multi-stage designs, impacting their overall performance in precision analogue circuits.

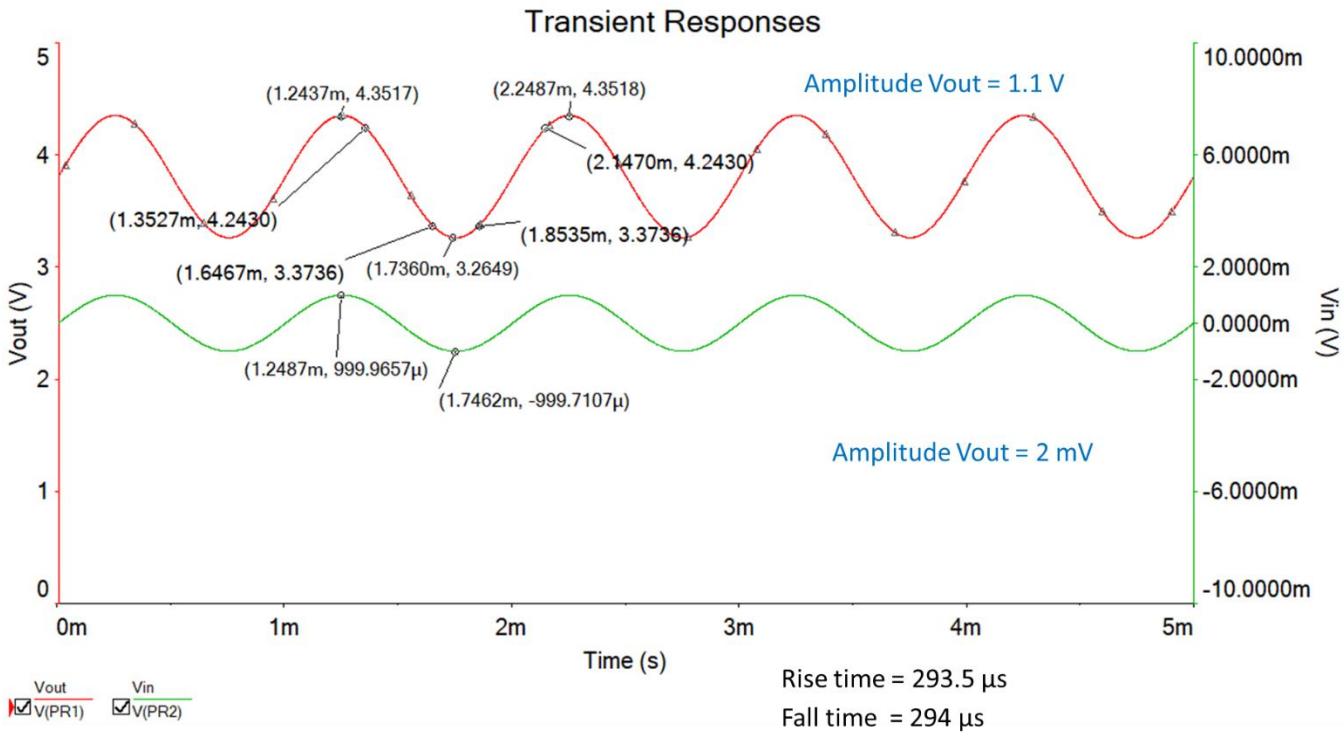


Figure 8 Transient responses (design no.3)

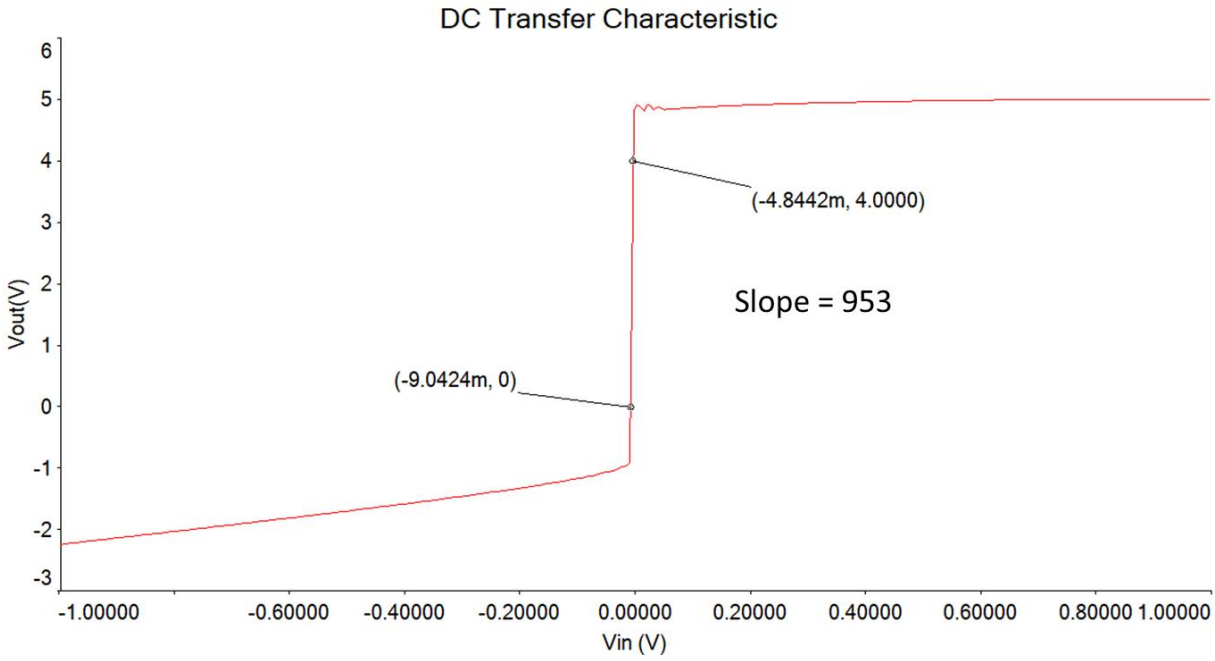


Figure 9 DC transfer characteristics (design no.3)

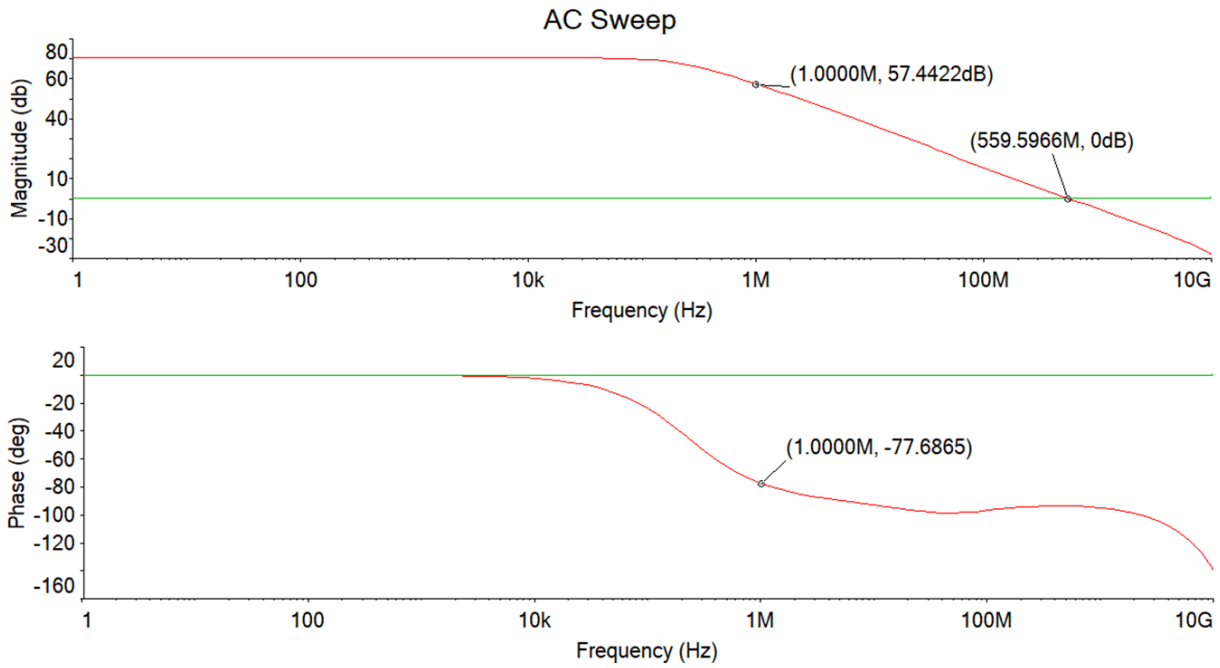


Figure 10 AC sweep (design no.3)

Section2: Design and investigate the DC, AC and transient responses of a two-stage Op-amp with compensating capacitor by simulation and analysis

a) Calculate the aspect ratios of all transistors (i.e. M1, M2, M3, M4, Mo, and Mbias) in the design. Make sure to represent these as a whole number of λ_m. Show your calculations and final values

[10/100]

To determine value of I_o

From $I_o = SR \times C_C$

To satisfy the provide slew rate (SR = $v/\mu sec$) for a known compensating capacitance (C_c)

$$I_o = 5\ v/\mu sec \times 5\ pF$$
$$= 25\ \mu A$$

To determine aspect ratio of M1, M2

From $GB = \frac{g_{m1,2}}{2\pi C_L}$ and $g_m = \frac{dI_{Dsat}}{dV_{GS}}$

Hence $\left(\frac{W}{L}\right)_{M1} = \frac{(g_{m1,2})^2}{2I_{D1}K_{n1}}$

To satisfy the setting of gain-bandwidth product *GB* of 1 MHz at unity gain (0 dB)

$$GB = gain \times bandwidth$$
$$= 1 \times 5\ MHz = 5\ M$$

$$g_{m1,2} = GB \times 2\pi \times C_L$$
$$= 5\ M \times 2\pi \times 5\ pF = 1.57\ m$$

$$I_{D1} = I_o/2$$

$$\left(\frac{W}{L}\right)_{M1} = \frac{(g_{m1,2})^2}{2I_{D1}K_n} = \frac{(1.57\ m)^2}{2 \times \left(\frac{25\ \mu}{2}\right) \times 96.4\ \mu} = 10.24$$

From $\left(\frac{W}{L}\right)_{M1} = 11$, given W_{M1} = 22λ_m (26.4 µm) and L_{M1} = 2λ_m (2.4 µm).

For matched devices, ratio of M1 and M2 are the same.
Hence W_{M2} = 22λm (26.4 µm) and L_{M2} = 2λm (2.4 µm).

To determine aspect ratio of M3, M4

To ensure M1 is saturated,

$$V_{DSM1} \geq V_{GSM1} - V_{Tn1}$$
$$V_{x1} \geq V_{in1(max)} - V_{Tn}$$
$$\geq 4.5\ \text{V} - 0.79\ \text{V} = 3.71\ \text{V}$$

where $V_{in1(max)}$ is the maximum input voltage or ICMR (+) and V_{Tn} is the threshold voltage of M1.

The minimum value of V_{x1} is 3.71 V.

From V_{x1} = 3.71 V, so V_{GSM3} = 3.71 V − 5 V = − 1.29 V.

$$\left(\frac{W}{L}\right)_{M3} = \frac{2I_{D3}}{K_p\left(V_{DD} - \text{ICMR}\,(+) - V_{Tp} + V_{Tn}\right)^2}$$
$$= \frac{25\ \mu A}{29.4\ \mu\ \times\ (5\ V - 4.5\ V - (-0.91\ V) + 0.79)^2}$$
$$= 0.18$$

From $\left(\frac{W}{L}\right)_{M3} = \frac{1}{5}$, given W_{M3} = 2λm (2.4 µm) and L_{M3} = 5λm (6 µm).

For matched devices, ratio of M3 and M4 are the same.
Hence W_{M4} = 2λm (2.4 µm) and L_{M4} = 5λm (6 µm).

To determine aspect ratio of M_o, M_{bias}

To ensure M1 is saturated,

$$V_{\text{in1(min)}} \geq V_{\text{GSM1}} + V_{\text{DSMo(sat)}}$$

where $V_{in1(min)}$ is the minimum input voltage or ICMR (-).

From $\frac{I_o}{2} = \frac{\left(\frac{W}{L}\right)_{M1}}{2} K_n (V_{GSM1} - V_{Tn})^2$

25 µA = 11 × 96.4 µ/V² × $(V_{GSM1} - 0.79\ V)^2$

V_{GSM1} = 0.94 V

From $V_{DSMo(sat)} \geq V_{in1(min)} - V_{GSM1}$

$1.51\ V \geq 0.5\ V - 0.94\ V$

$V_{DSMo} = -0.44\ V$

To ensure Mo is saturated, $V_{DSMo} = V_{GSMo} - V_{Tn}$.

From $I_{Mo} = \left(\frac{W}{L}\right)_{Mo} {}^{K_n}/_2\ (V_{GSMo} - V_{Tn})^2$

$I_{Mo} = \left(\frac{W}{L}\right)_{Mo} {}^{K_n}/_2\ (V_{DSMo})^2$

$25\ \mu A = \left(\frac{W}{L}\right)_{Mo} \times {}^{96.4\ \mu/V^2}/_2 \times (-0.44\ V)^2$

$\left(\frac{W}{L}\right)_{Mo} = 2.63$

From $\left(\frac{W}{L}\right)_{Mo} = 3$, given W_{Mo} = 12λ_m (14.4 µm) and L_{Mo} = 4λ_m (4.8µm).

For matched devices, ratio of Mo and Mbias are the same.
Hence W_{Mbias} = 12λ_m (14.4 µm) and L_{Mbias} = 4λ_m (4.8µm).

To determine aspect ratio of M_{op} for the required phase margin, we assume

$$g_{mMop} \geq 10 g_{m1}$$

and when M3 and M4 are matched, V_{GS} and V_{DS} are the same as M_{op}. In this case, the different in these devices are their aspect ratios and current flow, which is given as the expression below,

$$\frac{\left(\frac{W}{L}\right)_{Mop}}{\left(\frac{W}{L}\right)_{M4}} = \frac{I_{DMop}}{I_{DM4}}$$

$$\frac{\left(\frac{W}{L}\right)_{Mop}}{\left(\frac{W}{L}\right)_{M4}} = \frac{g_{mMop}}{g_{mM4}}$$

From $g_{mM4} = \sqrt{2I_{DM4}K_p\left(\frac{W}{L}\right)_{M4}}$

$$\left(\frac{W}{L}\right)_{Mop} = \frac{g_{mMop}}{\sqrt{2I_{DM4}K_p\left(\frac{W}{L}\right)_{M4}}} \times \left(\frac{W}{L}\right)_{M4}$$

$$\left(\frac{W}{L}\right)_{Mop} = \frac{g_{mMop}}{\sqrt{2I_{DM4}K_p}} \times \sqrt{\left(\frac{W}{L}\right)_{M4}}$$

$$\left(\frac{W}{L}\right)_{Mop} = \frac{10g_{m1}}{\sqrt{2\,{I_o}/{2}\,K_p}} \times \sqrt{\left(\frac{W}{L}\right)_{M4}}$$

$$\left(\frac{W}{L}\right)_{Mop} = \frac{1.57\,m}{\sqrt{25\mu A\,\times 29.4\,\mu A/V^2}} \times \sqrt{0.2}$$

$$\left(\frac{W}{L}\right)_{Mop} = 25.9$$

From $\left(\frac{W}{L}\right)_{Mop} = 26$, given W_{Mop} = 52λ_m (62.4 µm) and L_{Mop} = 2λ_m (2.4µm).

To determine aspect ratio of M_{on},

$$I_{DMop} = \frac{\left(\frac{W}{L}\right)_{Mop}}{\left(\frac{W}{L}\right)_{M4}} \times\ I_{DM4}$$

From $I_{DM4} = {I_o}/{2} = 12.5\,\mu A$, $I_{DMop} = \frac{26}{0.2} \times\ 12.5\,\mu A = 1.625\,mA$

If the devices are matched, V_{GS} and V_{DS} of M_o and M_{on} are the same, such that

$$\left(\frac{W}{L}\right)_{Mon} = \frac{I_{DMon}}{I_{DMo}} \times \left(\frac{W}{L}\right)_{Mo}$$

And $I_{DMon} = I_{DMop}$,

$$\left(\frac{W}{L}\right)_{Mon} = \frac{1.625\ mA}{25\ \mu A} \times\ 3 = 195$$

From $\left(\frac{W}{L}\right)_{Mon} = 195$, given W_{Mon} = 390λ_m (468 µm) and L_{Mon} = 2λ_m (2.4µm).

b) Show the corresponding simulation results for your amplifier DC, AC (i.e. Bode and phase plots) and transient (i.e. slew rate, rise/fall edge) responses

[10/100]

Figure 11 represents circuit schematic of a two-stage differential CMOS Op-amp with aspect ratio of M1 and M2 are 2 λ_m /22 λ_m, the aspect ratio of M3 and M4 are 2 λ_m /10 λ_m, the aspect ratio of M_o and M_{bias} are 30 λ_m /90 λ_m, the aspect ratio of M_{op} is 2λ_m /52 λ_m, and he aspect ratio of M_{on} is 2λ_m /390 λ_m.

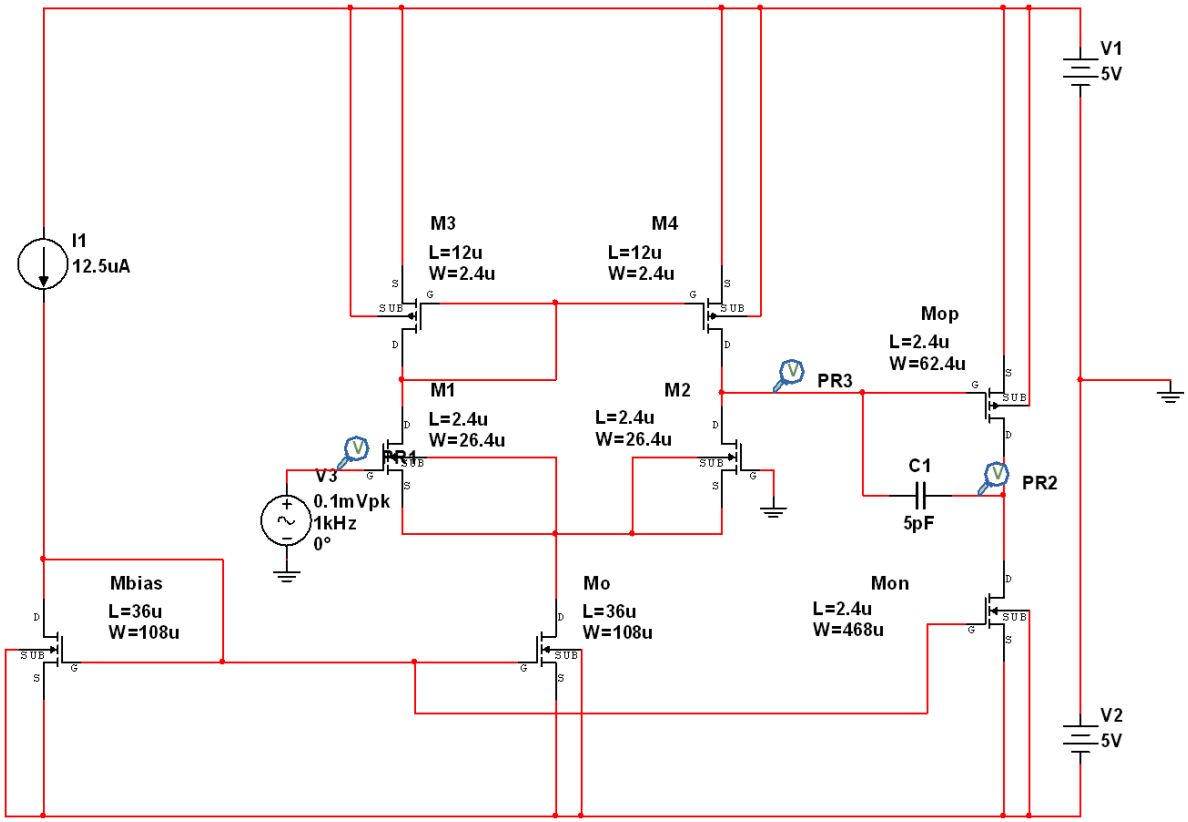


Figure 11 Circuit design of a two-stage differential CMOS Op-amp (Design no.1).

Figure 12 represents transient responses of a two-stage differential CMOS Op-amp. The rise time of Vout is 289.2 µs and the fall time of Vout is 304.3µs. The amplitude of input signal is 99.8 µV - (-99.8 µV) = 0.2 mV while the amplitude of Vout is 3.8757 V - 3.7647 V = 110 mV. The amplitude of Vat1 (first stage output) is 2.3140 V - 2.2425 V = 70 mV The slope of output signal is (3.8647 - 3.7758) V/ (2.6789-2.3897) ms = $3.1*10^{-4}$ V/µs .

Figure 13 represents DC transfer characteristic of a two-stage op-amp (design no.1), the slope of the graph is 1762 (green line). Figure 14 illustrates AC sweep of a two-stage op-amp (design no.1), at 5MHz, the magnitude is -8.3 dB (0.4) and the phase margin is 60°. While frequency at 1.97 MHz, the magnitude of output is 0dB (gain = 1).

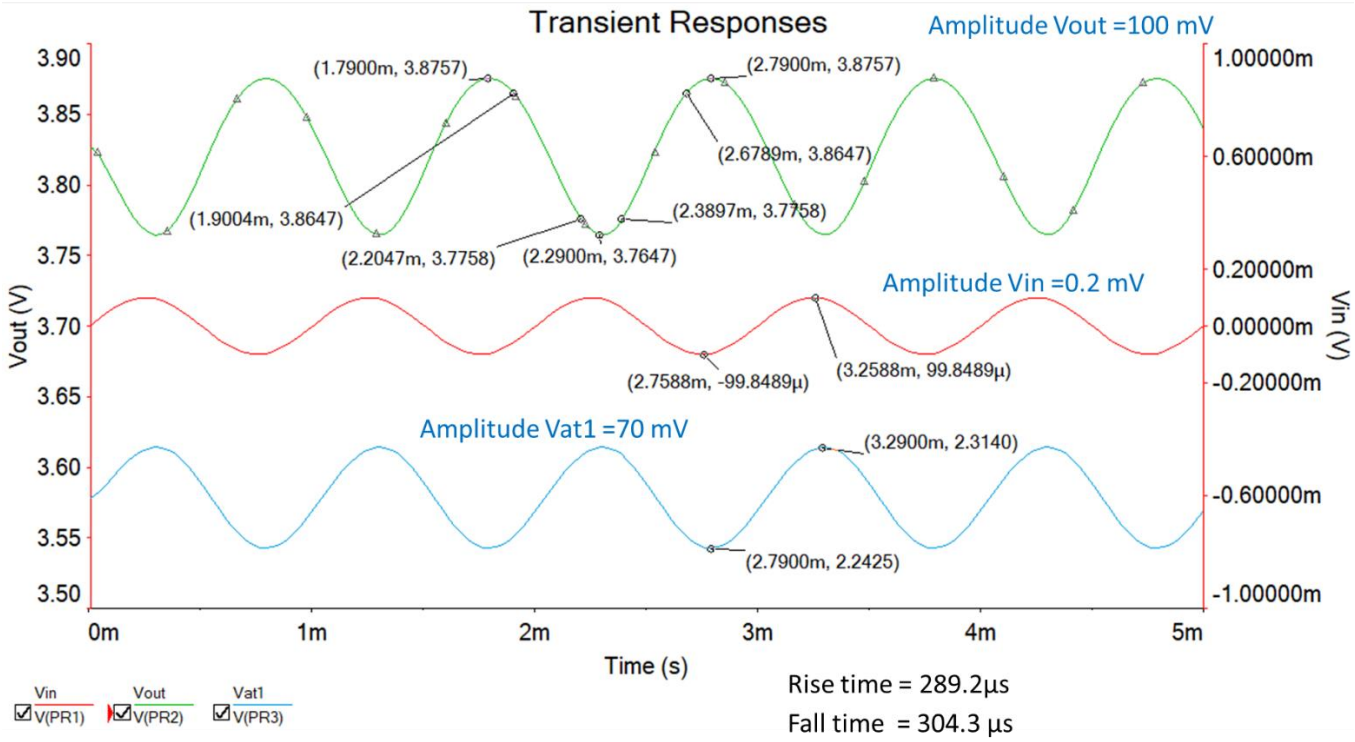


Figure 12 Transient responses (design no.1)

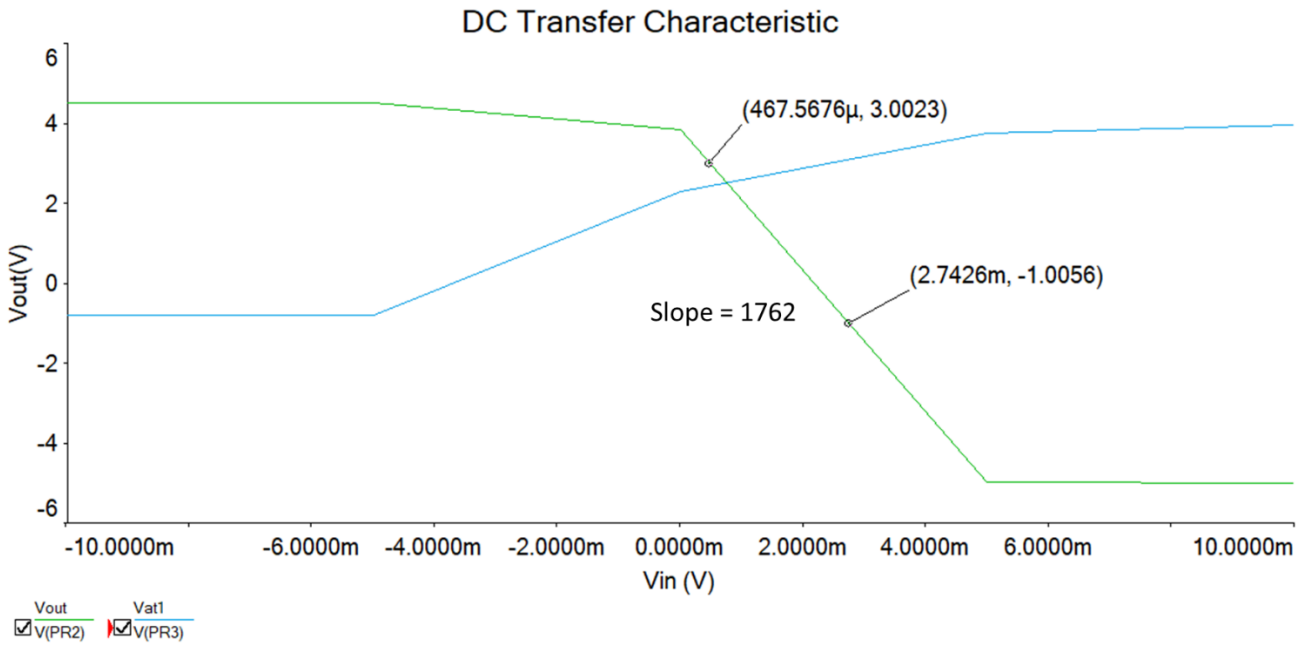


Figure 13 DC transfer characteristics (design no.1)

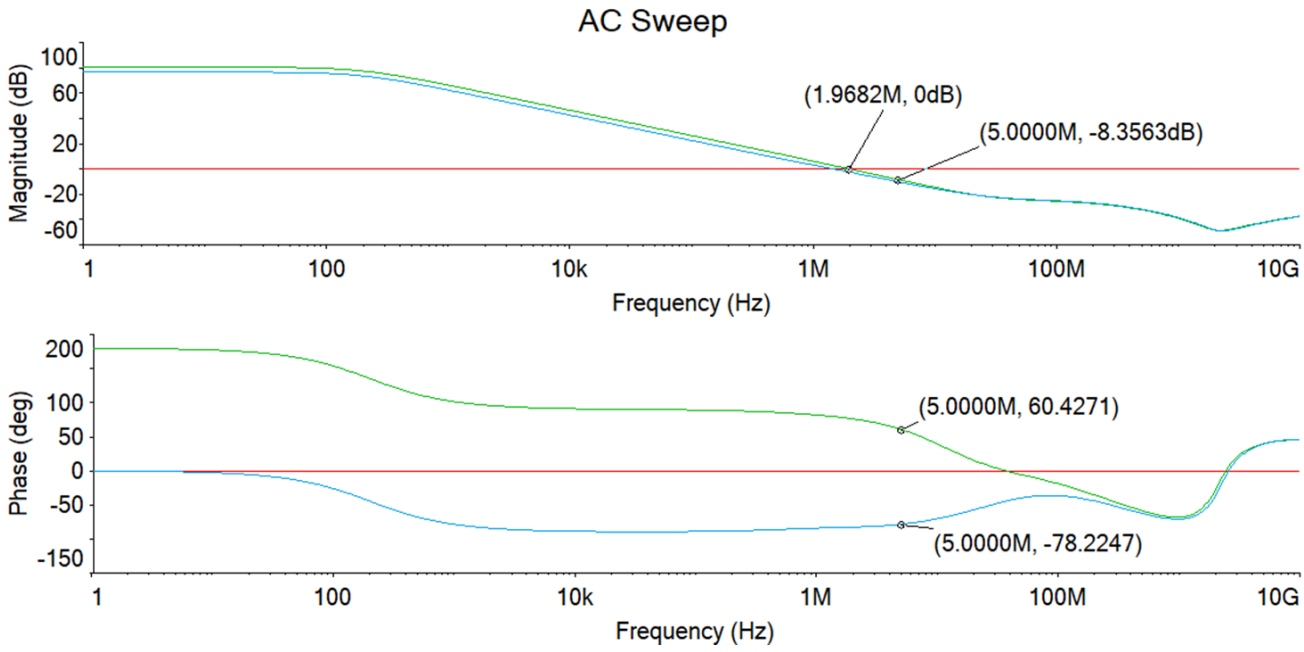


Figure 14 AC sweep (design no.1)

c) Analyse the responses obtained in b), and extract/examine the key parameters from the characteristics including gain, gain-bandwidth and phase-margin etc. Compare and comment on the outputs obtained from the simulations to those provided in the specifications

[10/100]

From the DC transfer characteristic of a two-stage op-amp (Figure 13), the slope of the graph is 1762, which corresponds to the gain of the circuit. Comparing this to the expected Av of greater than 1000 ($\geqslant$ 60 dB), this circuit meets expectations. However, at a frequency of 5MHz, the magnitude is -8.3 dB (approximately 0.4), and the phase margin is 60°, which means that the phase margin is satisfactory, although the gain-bandwidth product of 5MHz falls short of the expected. At unity gain, this circuit can operate at 1.97 MHz, which fails the expected frequency of 5MHz. Hence, there is a need to improve the gain-bandwidth product of 5MHz for 2d.

d) Further optimise your design and show how the gain and gain-bandwidth may be improved using this design architecture.

[10/100]

To improve the gain-bandwidth product (GBW) of a two-stage op-amp involves optimizing various aspects of its design and circuit configuration. Increasing the transconductance (gm) of transistors in the amplifier stages can enhance the gain bandwidth product. This can be achieved by increasing the width (W) of the transistors, which boosts their transconductance. However, increasing width also increases parasitic capacitance, so a balance must be struck.

The second design of two-stage op-amp changes only width and length of Mo and Mbias to $W_{Mo} = W_{Mbias} = 150\lambda_m$ (180 µm) and $L_{Mo} = L_{Mbias} = 50\lambda_m$ (60µm). Ratio is 3 as initial design.

From the DC transfer characteristic in Figure 15, the slope is same as previous (~1760), so the gain is the same. From AC sweep in Figure 16, at 5MHz, the magnitude is -7.8 dB (0.4) and the phase margin is 61°. While frequency at 2.05 MHz, the magnitude of output is 0dB (unity gain). It shows that when scale up both width and length size of Mo and Mbias, the gain-bandwidth is improved but it is still not as expectation.

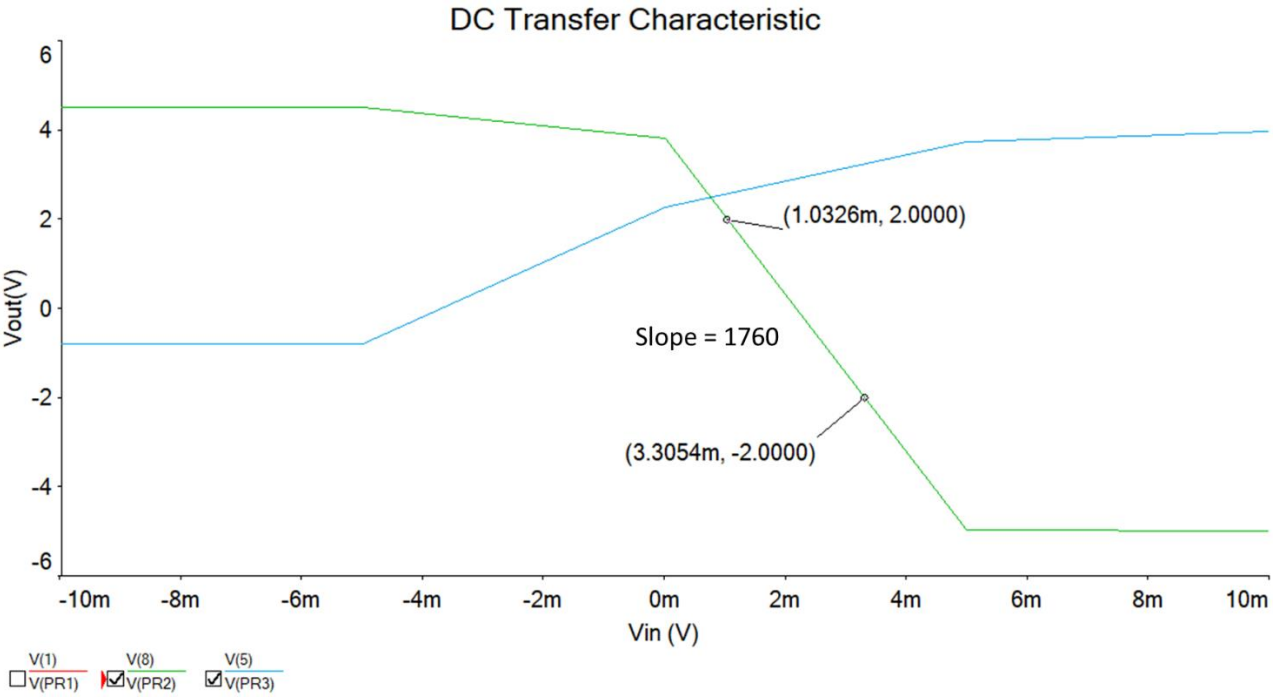


Figure 15 DC transfer characteristics (design no.2)

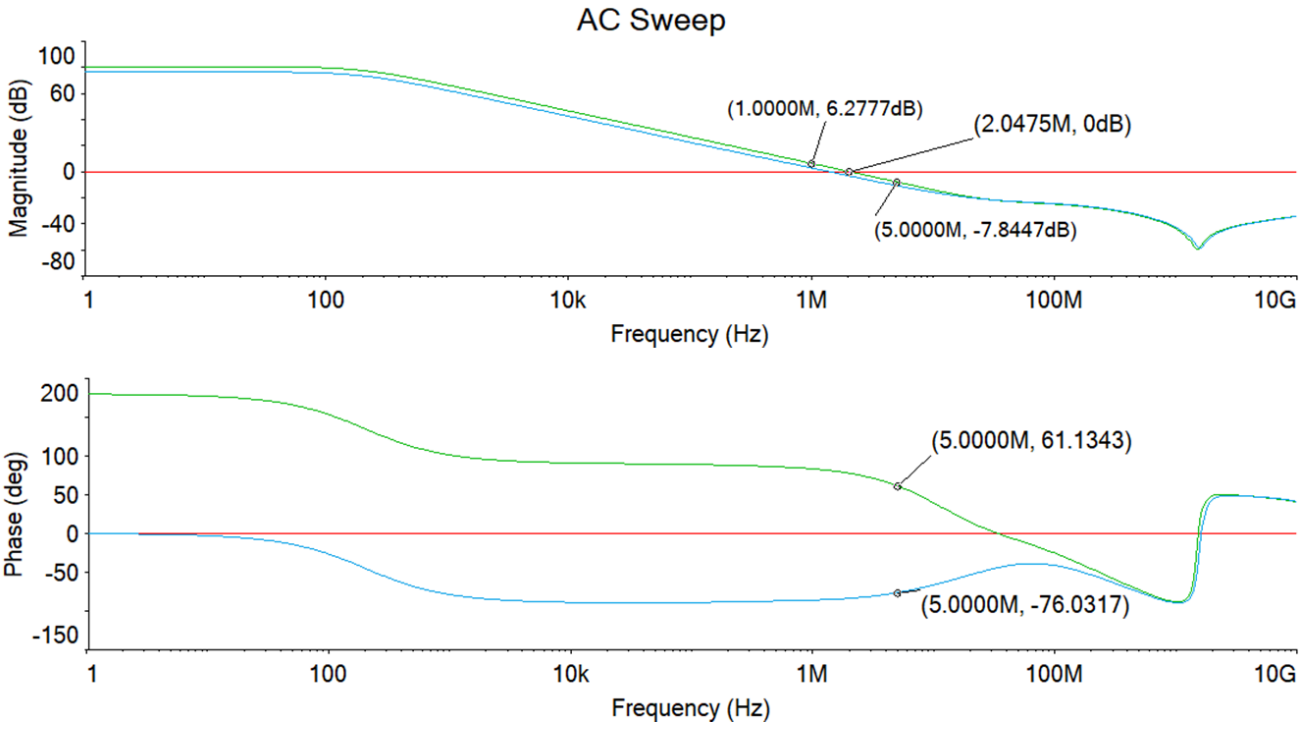


Figure 16 AC sweep (design no.2)

The third design will recalculate some aspect ratio of devices to increase gm of transistors. The updated aspect ratio of M1 and M2 will be 18.75, which $W_{M1} = W_{M2} = 75\lambda_m$ (90 µm) and $L_{M1} = L_{M2} = 4\lambda_m$ (4.8 µm).

Then aspect ratio of Mo and Mbias will change to $W_{Mo} = W_{Mbias} = 200\lambda_m$ (240 µm) and $L_{Mo} = L_{Mbias} = 50\lambda_m$ (60µm). Ratio is updated to 4. Because of for matched design, V_{GS} and V_{DS} of M_o and M_{on} are the same. The aspect ratio of M_{on} is updated to $W_{Mon} = 520\lambda_m$ (624 µm) and $L_{Mon} = 2\lambda_m$ (2.4µm). Ratio of M_{on} is 260.

Figure 17 represents transient response of design no.3, the rise time of Vout is 274 µs and the fall time of Vout is 308.4µs. The amplitude of input signal is 99.8 µV - (-99.8 µV) = 0.2 mV while the amplitude of Vout is 3.9827 V - 3.4351 V = 550 mV. The amplitude of Vout is increased compared to initial design of 2-stage op-amp.

From the DC transfer characteristic in Figure 18, the slope is 1900, so the gain is increased. Gain is increased because the design increased gm of transistors M1 and M2. Figure 19 shows AC sweep of new circuit values which the gain-bandwidth is increased to 2.56 dB at unity gain, while the phase is 58° at 5 MHz. The bandwidth is better compared to two previous designs but cannot meets the requirement.

One disadvantage of a two-stage CMOS op-amp is its increased complexity compared to single-stage designs, leading to higher manufacturing costs and larger chip area requirements. Additionally, two-stage op-amps may suffer from limited bandwidth and increased susceptibility to noise due to the cascaded nature of their amplification stages. Furthermore, the presence of multiple stages can introduce more opportunities for non-linearities and distortion, potentially compromising overall performance.

A two-stage CMOS op-amp without feedback faces stability problems and is highly sensitive to variations in process, temperature, and supply voltage. The absence of feedback means that the op-amp's gain is solely determined by the intrinsic characteristics of its amplifier stages, leading to inconsistencies in performance and compromised stability, particularly at higher frequencies. Consequently, these op-amps lack the ability to accurately control gain or tailor their response to specific requirements, limiting their suitability for various practical applications.

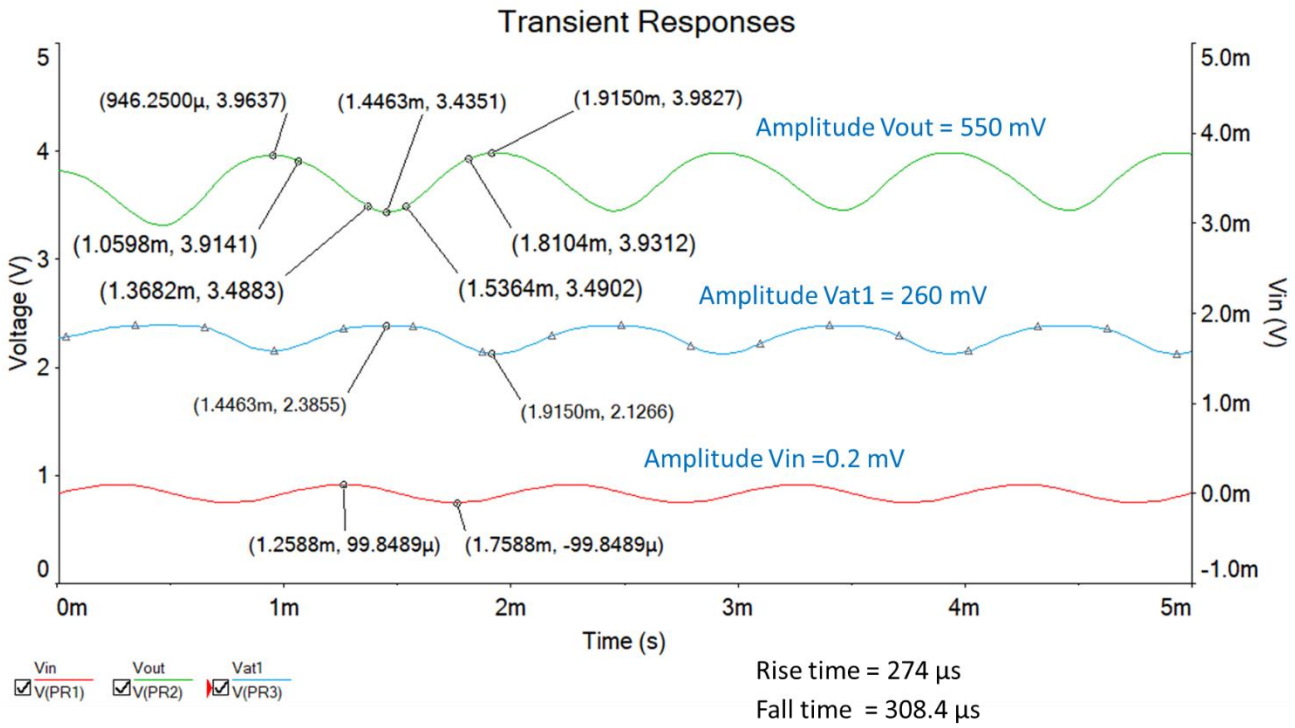


Figure 17 Transient responses (design no.3)

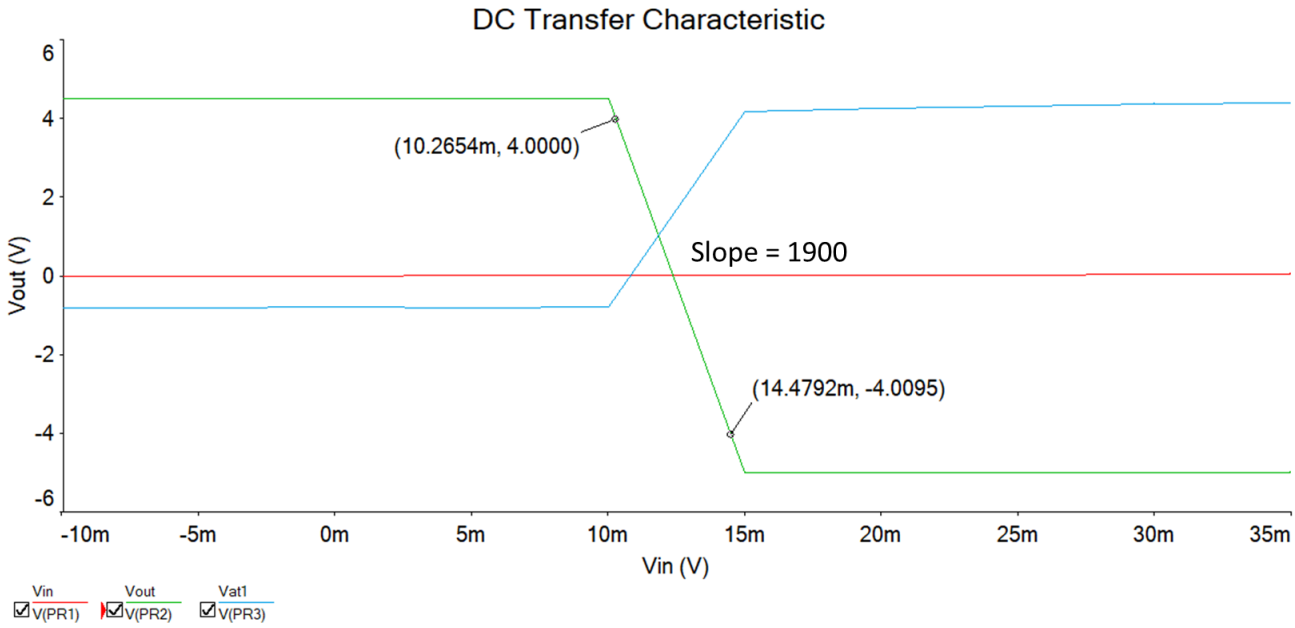


Figure 18 DC transfer characteristics (design no.3)

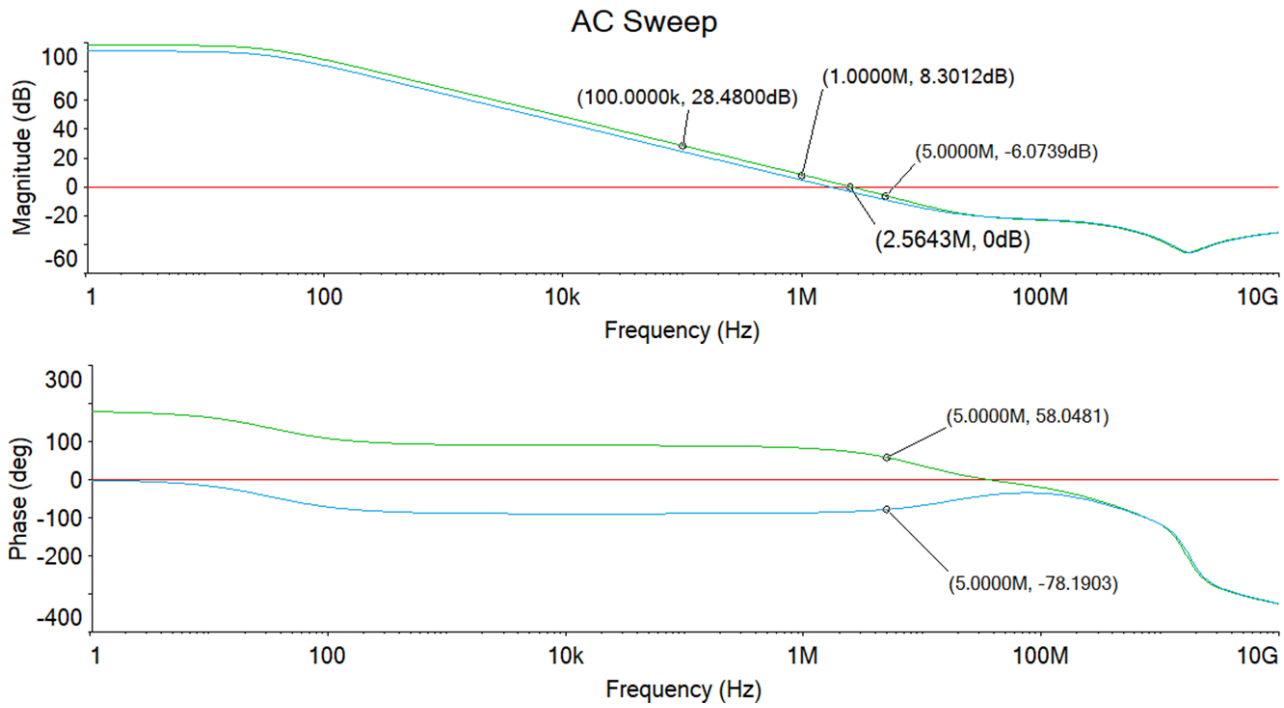


Figure 19 AC sweep (design no.3)

Section 3: Investigate amplifier circuits with closed-loop gain.

a) Briefly explain how negative feedback is used to control gain in operational amplifiers.

[5/100]

Negative feedback is utilized in operational amplifiers to regulate gain by continuously comparing the output voltage with the desired voltage and adjusting the amplification accordingly. In an op-amp circuit with negative feedback, a portion of the output voltage is fed back to the inverting input terminal, creating a closed-loop configuration. When the output deviates from the desired value, this feedback voltage drives the input towards the desired value, effectively reducing the voltage difference between the input terminals. As a result, the op-amp adjusts its output to maintain equilibrium, effectively controlling the gain. By adjusting the feedback network's parameters, such as resistor values, the degree of feedback can be tailored, allowing precise control over the op-amp's gain. This mechanism ensures that the op-amp operates in a stable, linear manner, with the gain determined by the ratio of feedback to input resistance. Negative feedback thus provides a straightforward and effective means of controlling gain in operational amplifiers.

b) Modify the circuit from section 1 to build and simulate the circuit design on *Multisim*, which uses negative feedback to create gains between -0.1 and -1000 and obtain the corresponding DC, AC (i.e. Bode and phase) plots. Explain your circuit and discuss the results. (You probably want to use 'parameter sweeps' to automate this – See *MultiSim* guidance for details.)

[5/100]

Figure 20 shows circuit diagram that modify from section 1. The closed loop gain is calculated as $-\frac{R_2}{R_1}$. From Figure 21 (transient responses), it can observe that output signal is 180 phase shifts compared to input signal as it is inverter circuit. Figure 22 shows that the gain is 0.2. Figure 23 represents different gain from using negative feedback, when R1 = 1M Ω and 5M Ω and R2 = 100 Ω, the gain goes up to more than -1000 (40dB). When R1 is 10k Ω and R2 = 100 Ω, the gain is -0.1 (-20dB).

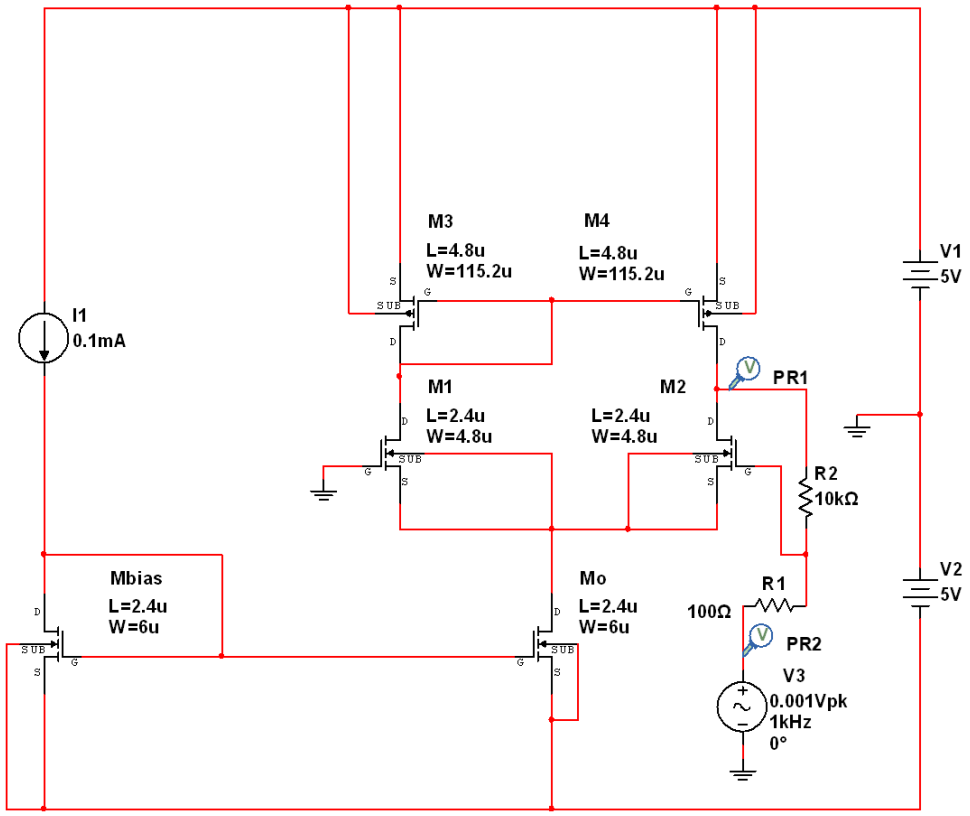


Figure 20 Schematic of inverting operational amplifier (single-stage op-amp)

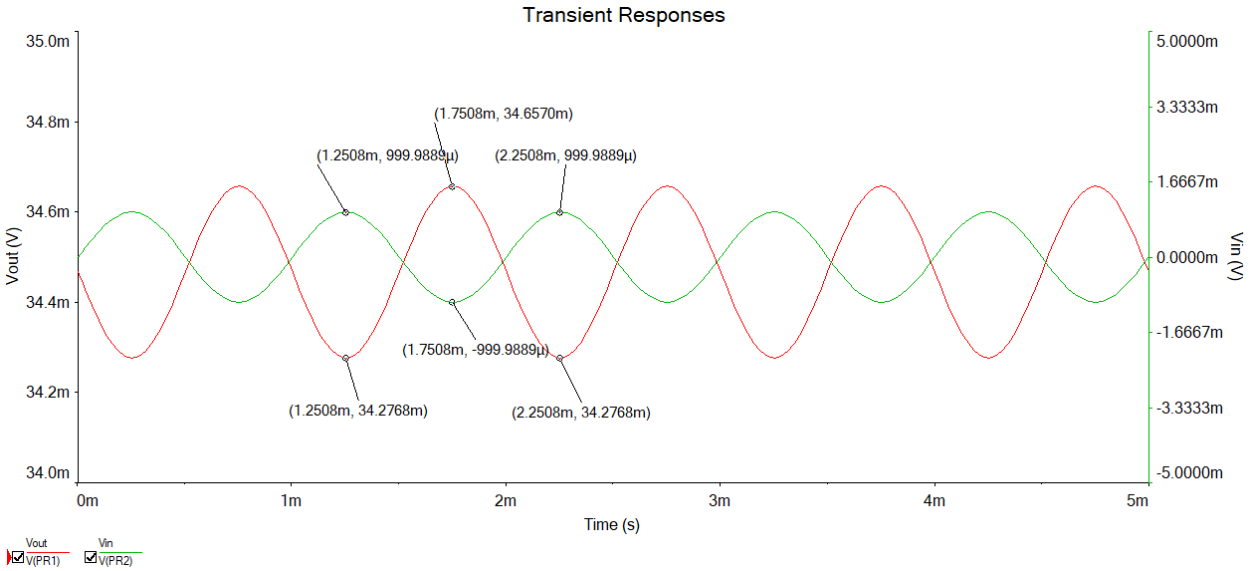


Figure 21 Transient responses of inverter op-amp (single-stage)

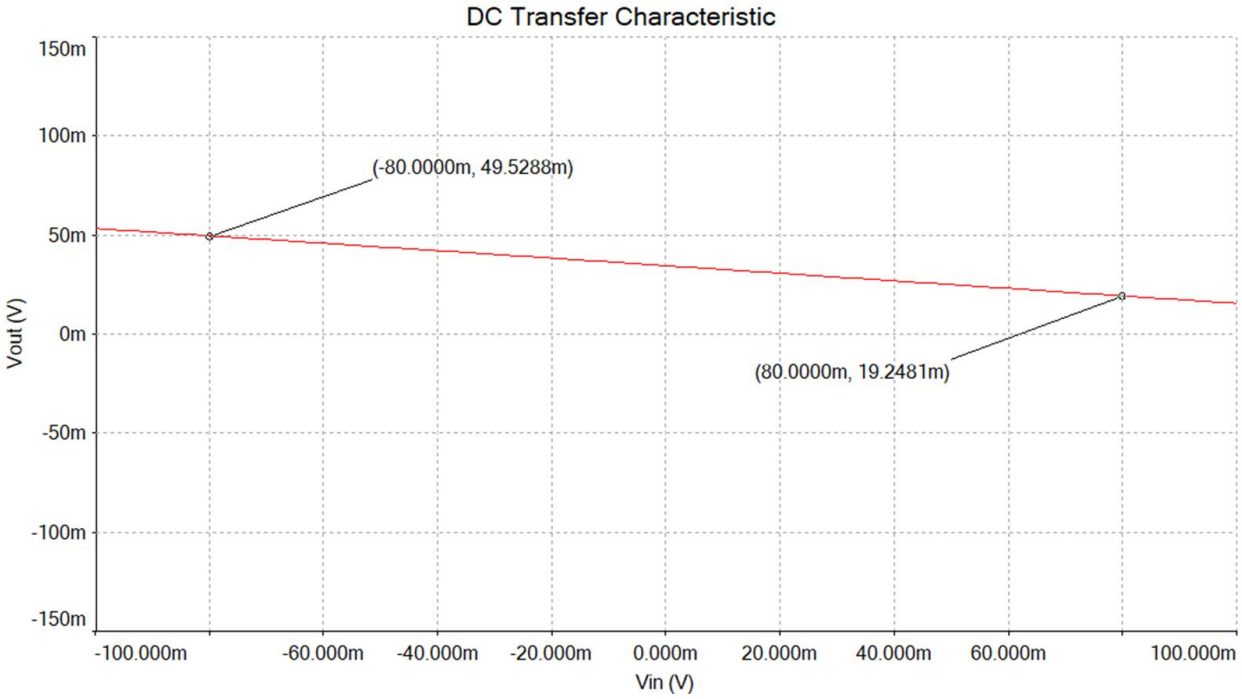


Figure 22 DC transfer characteristics of inverter op-amp (single-stage)

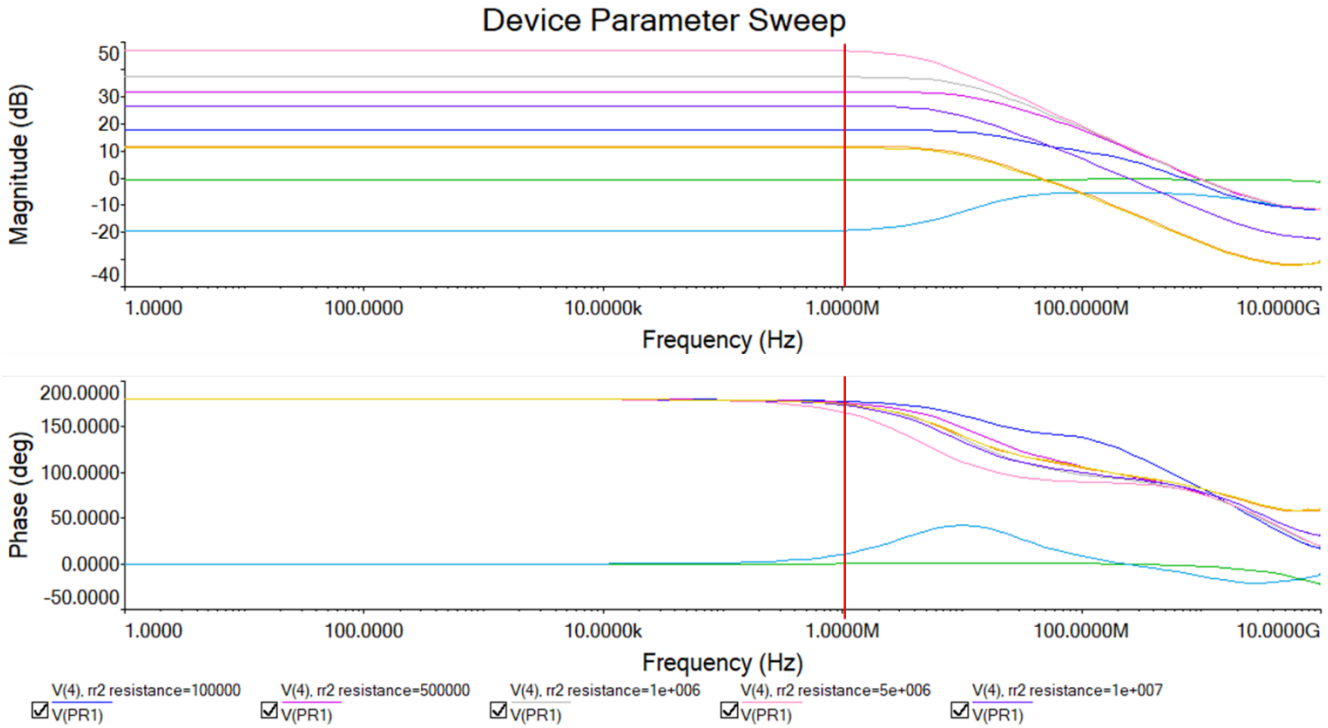


Figure 23 Device parameter sweep (AC sweep)

c) Modify the circuit from section 2 to build and simulate the circuit design on Multisim, which uses negative feedback to create gains between -0.1 and -1000 and obtain the corresponding DC, AC (i.e. Bode and phase) plots. Explain your circuit and discuss the results. Compare with the results from section 3b.

[5/100]

In the same theory of single-stage op-amp, Figure 24 shows circuit diagram that modify from section 2. The closed loop gain is calculated as $-\frac{R_2}{R_1}$. From Figure 25 (transient responses), it can observe that output signal is 180 phase shifts compared to input signal as it is inverter circuit. Figure 26 shows that the slope is 2000, so the gain is 2000. Figure 27 represents different gain from using negative feedback, when R1 = 80k Ω and 100k Ω and R2 = 100 Ω, the gain goes up to more than -1000 (40dB). When R1 is 20k Ω to 40k Ω and R2 = 100 Ω, the gain is -0.1 (-20dB).

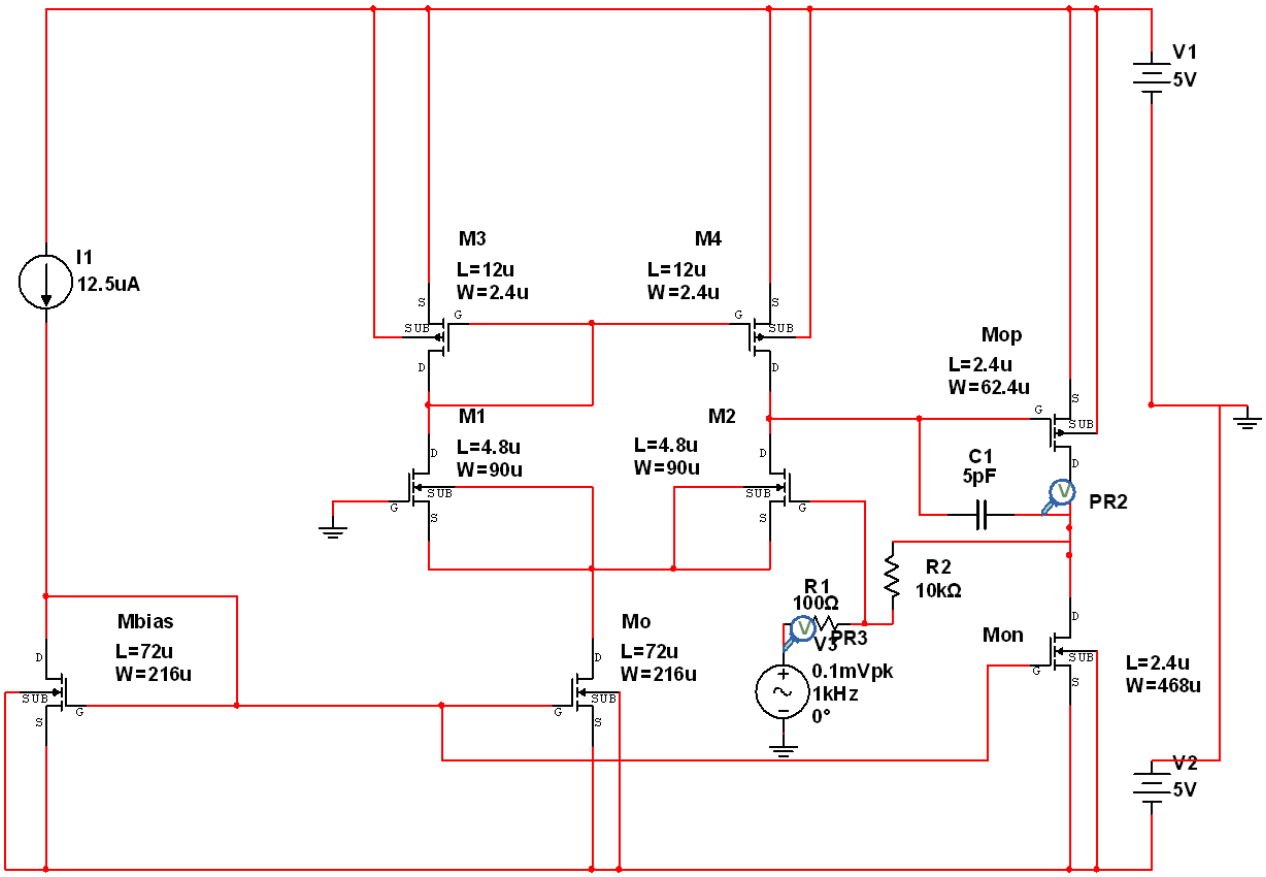


Figure 24 Schematic of inverting operational amplifier (2-stage op-amp)

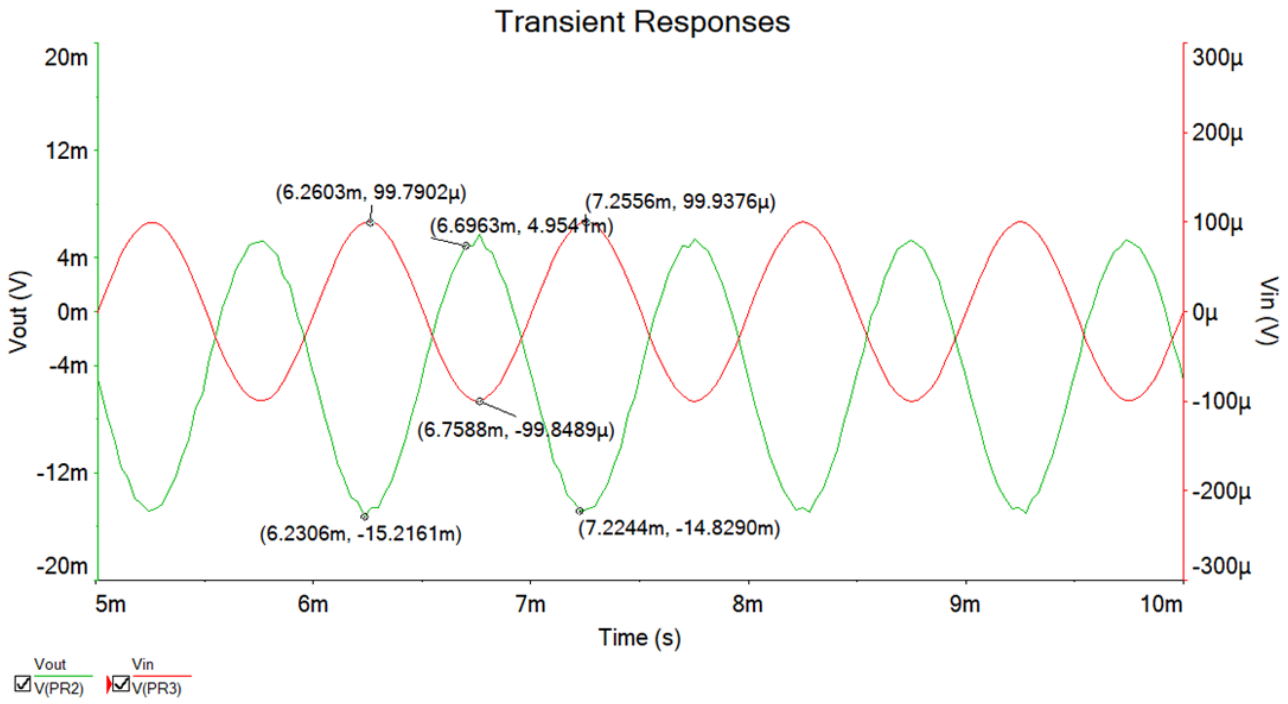


Figure 25 Transient responses of inverter op-amp (2-stage op-amp)

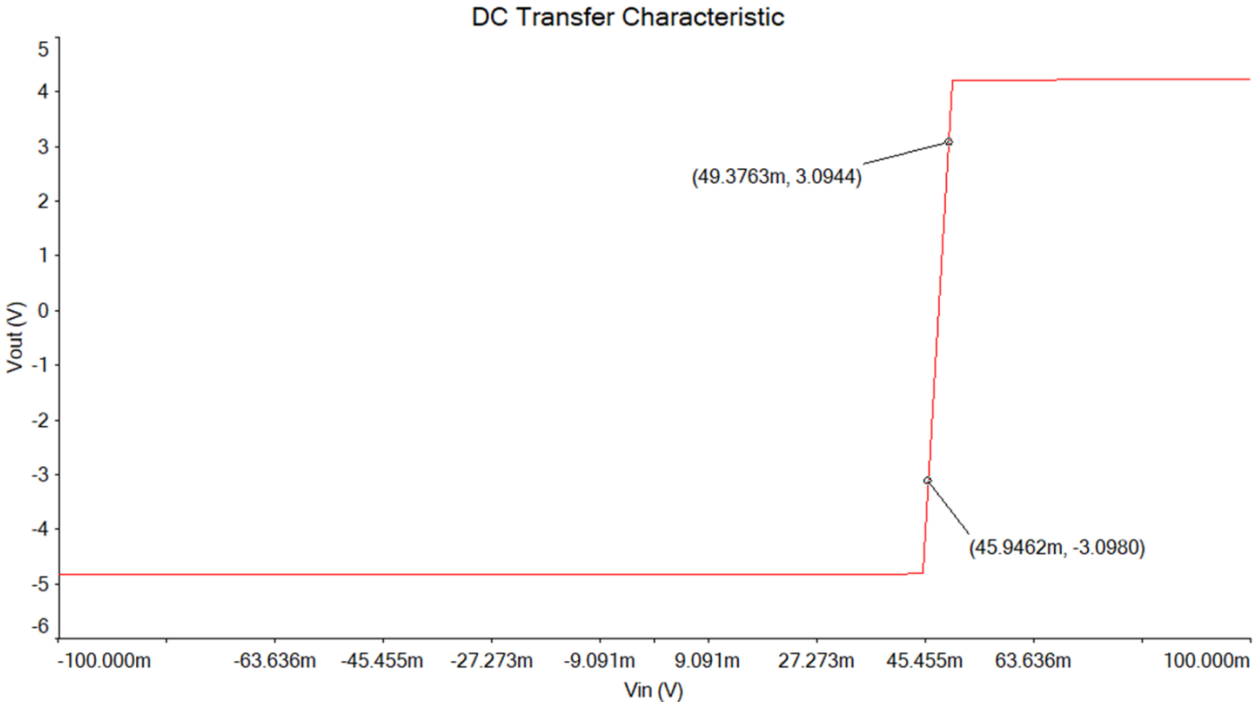


Figure 26 DC transfer characteristics of inverter op-amp (2-stage op-amp)

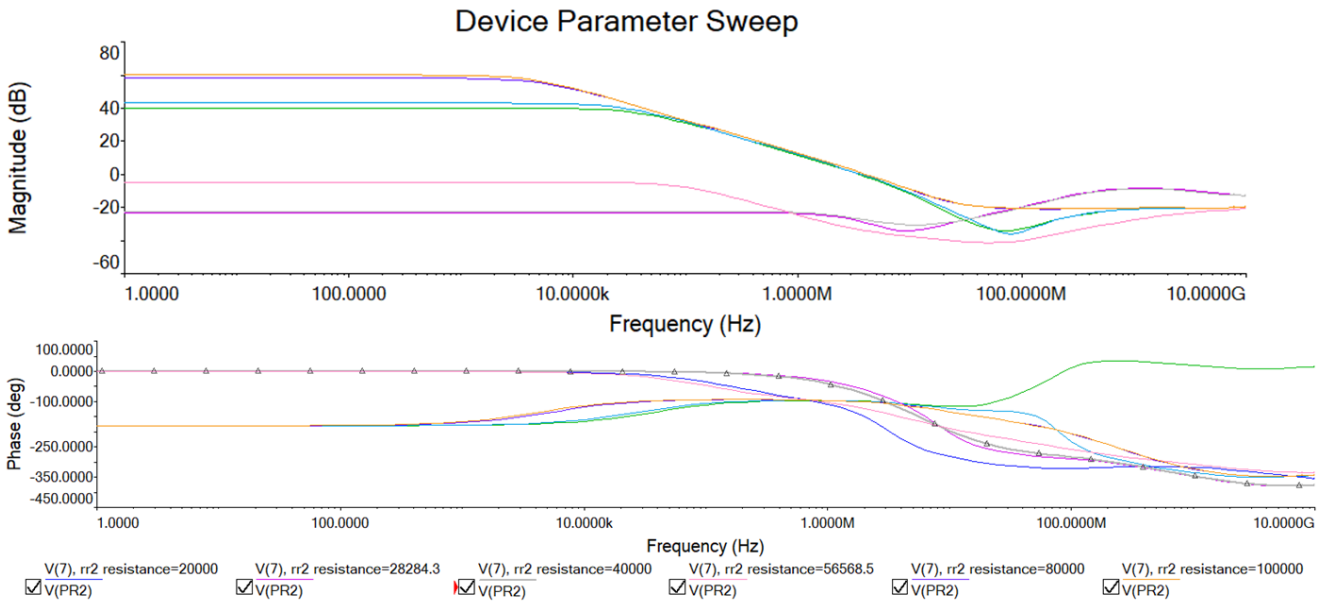
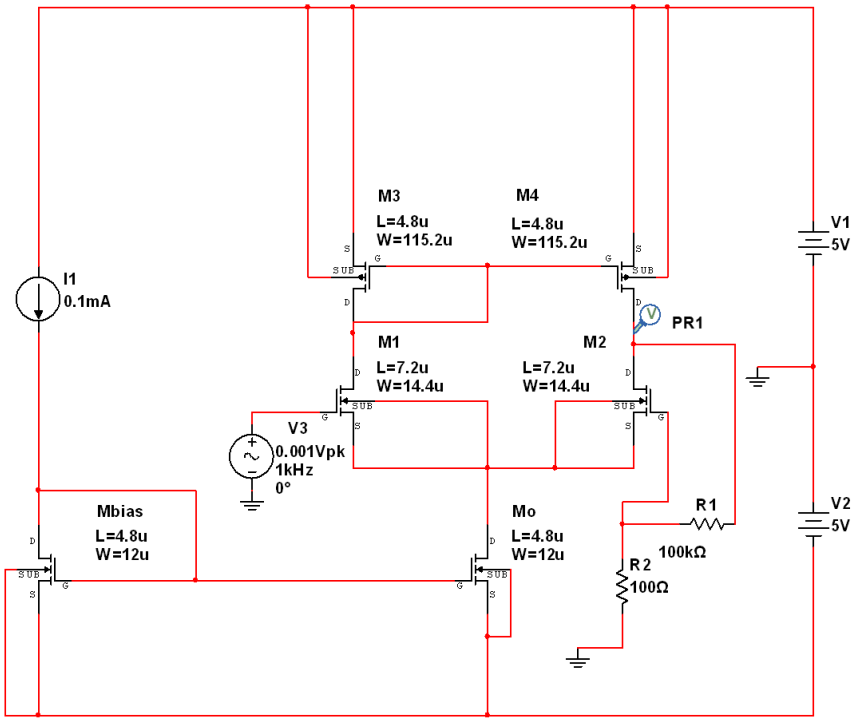


Figure 27 Device parameter sweep (AC sweep for 2-stage op-amp)

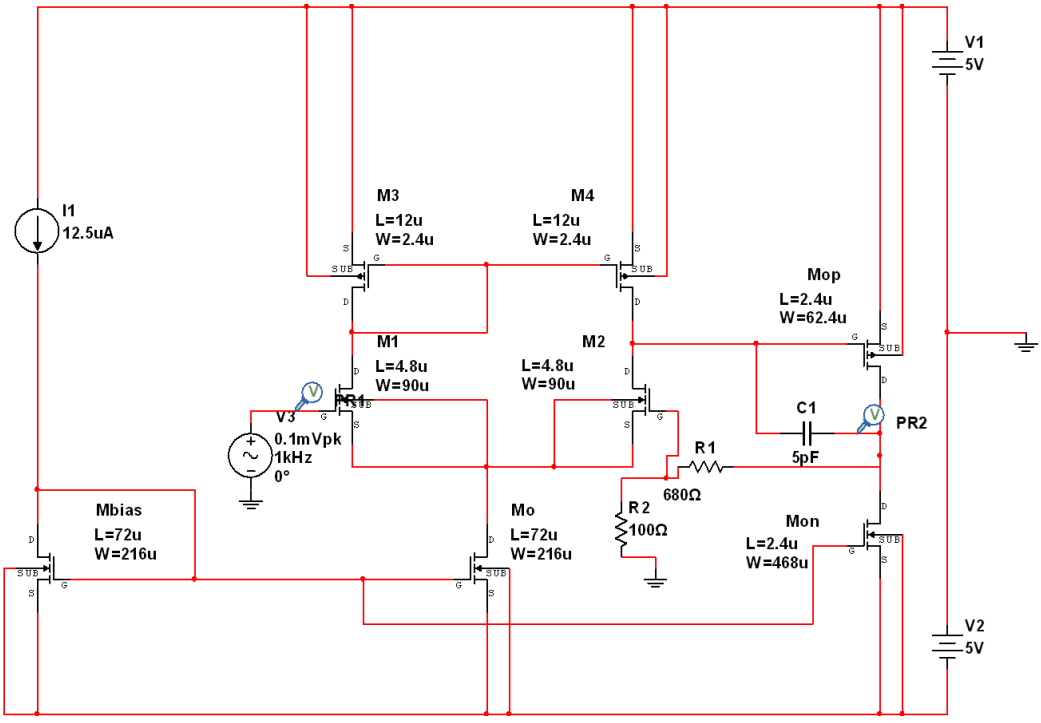
d) Modify the circuit from sections 1 and 2 to build and simulate the circuit design on **Multisim**, which uses negative feedback to create noninverting gains between +0.1 and +1000 and obtain the corresponding DC, AC (i.e. Bode and phase plots). Explain your circuit and discuss the results. Compare this with the results from sections 3b and 3c

[5/100]

In the non-inverting operational amplifier configuration, the input voltage signal (VIN) is directly connected to the non-inverting (+) input terminal. This arrangement results in a positive gain for the amplifier's output, unlike the "Inverting Amplifier" circuit where the output gain is negative. The closed loop gain is $1 + \frac{R_2}{R_1}$. Figure 28 represents circuit diagram of single-stage op-amp modified from section 1 (Figure 28a) and two-stage op-amp modified from section 2 (Figure 28b). For single stage non-inverter circuit, Figure 29 shows there is no phase shifting between input and output signal, the calculated gain is 11. Figure 30 shows the slope at 11.5, so the gain is 11.5 which correlate to ratio of input and output magnitudes from Figure 29. Figure 31 illustrates that when R1 = 1M Ω , 5M Ω and 10M Ω R2 = 100 Ω, the gain goes up to more than 1000 (40dB). When R1 is 10k Ω and R2 = 100 Ω, the gain is 0 (~1dB).



(a)



(b)

Figure 28 Schematic of non-inverting operational amplifier ((a) single-stage (b) 2-stage)

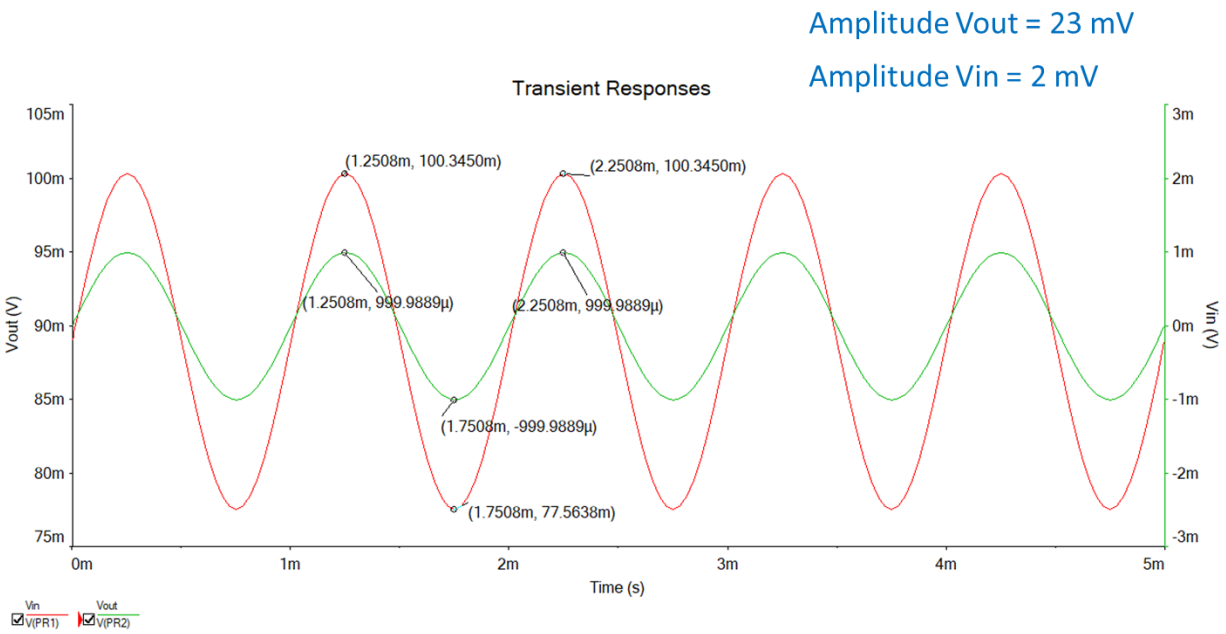


Figure 29 Transient responses of non-inverter op-amp (single-stage op-amp)

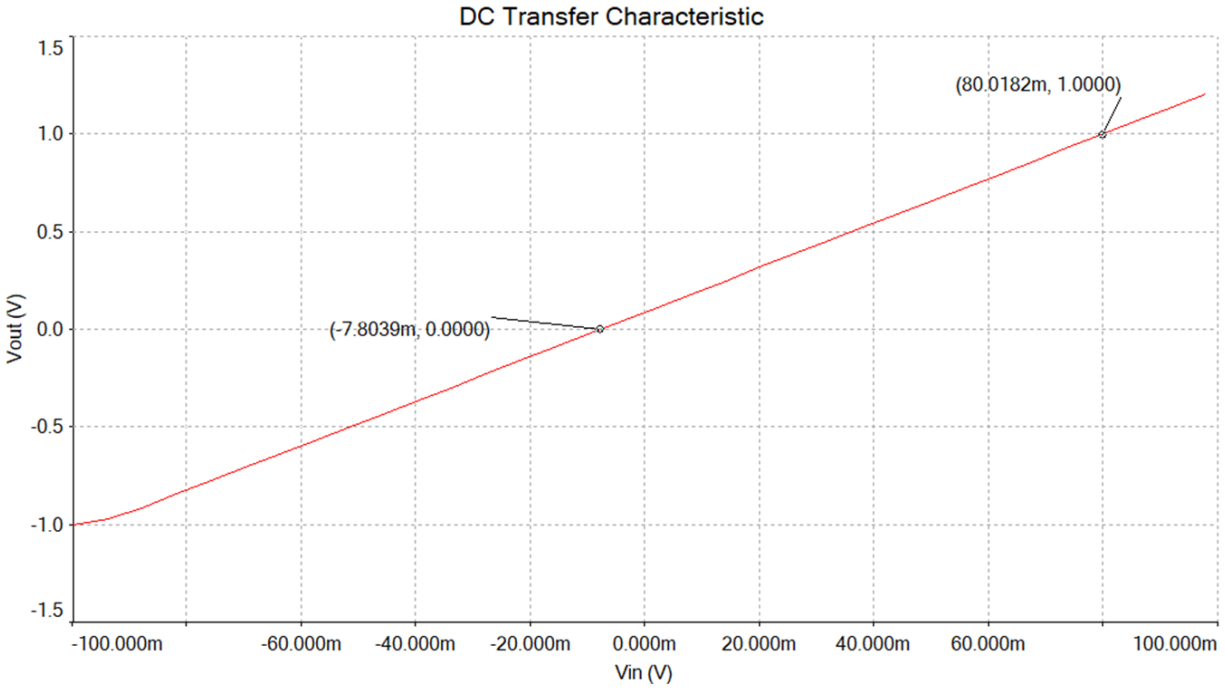


Figure 30 DC transfer characteristics of non-inverter op-amp (single-stage op-amp)

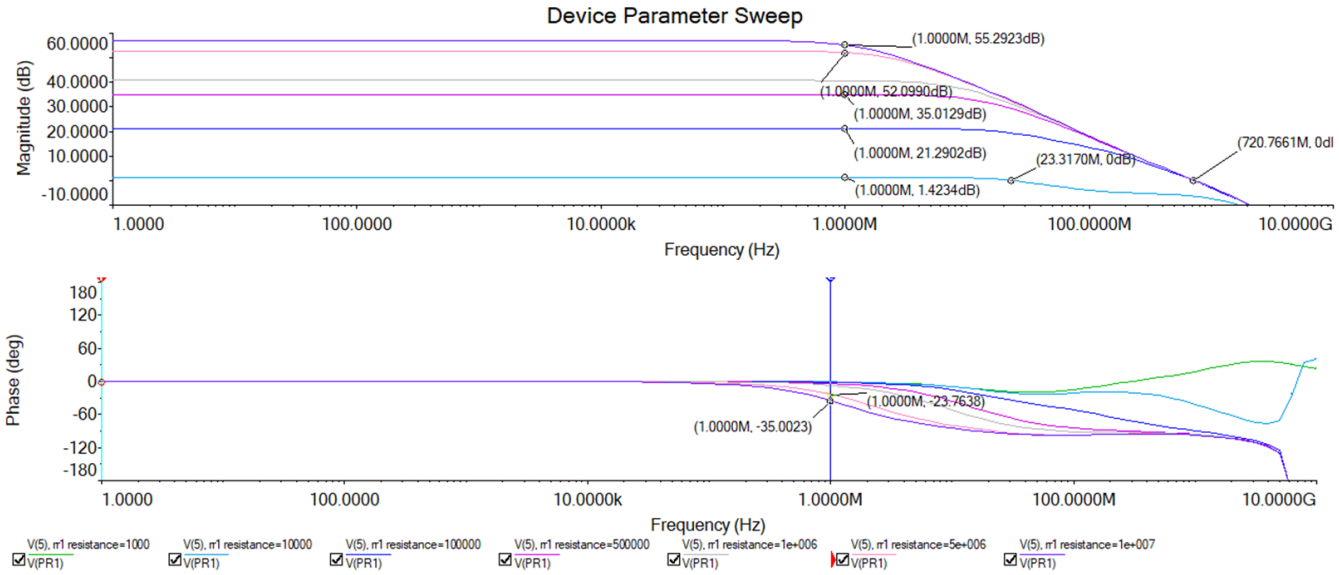


Figure 31 Device parameter sweep (AC sweep for single-stage non-inverter op-amp)

For two-stage non-inverter circuit, Figure 32 shows there is no phase shifting between input and output signal, the calculated gain is 7.5. Figure 33 shows the slope at 5. Figure 34 illustrates that when R1 = 750k Ω and 1M Ω R2 = 100 Ω, the gain goes up to more than 1000 (40dB). When R1 is 250k Ω and R2 = 100 Ω, the gain is 0.3 (-10dB).

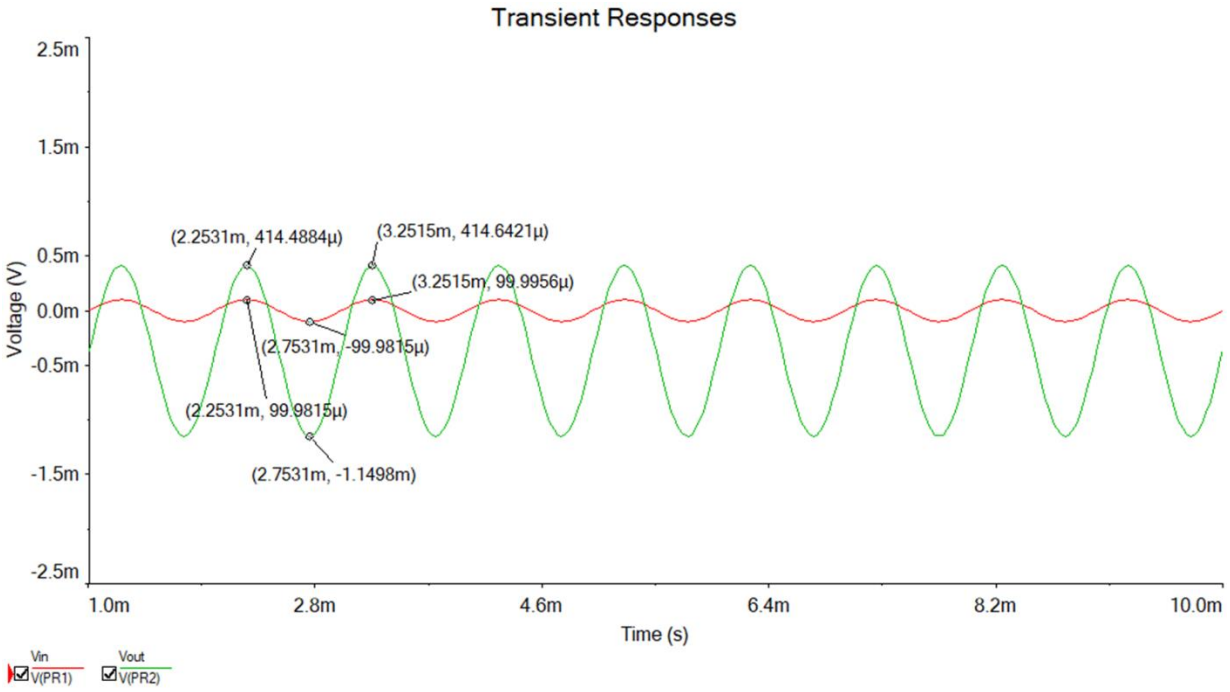


Figure 32 Transient responses of non-inverter op-amp (two-stage op-amp)

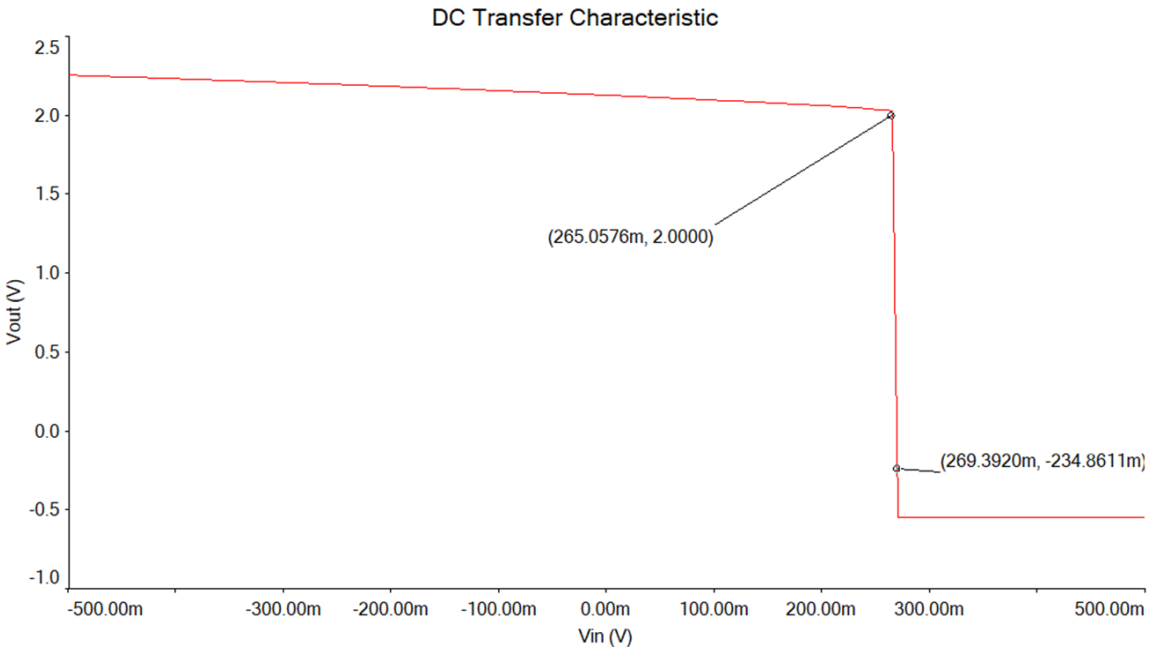


Figure 33 DC transfer characteristics of non-inverter op-amp (two-stage op-amp)

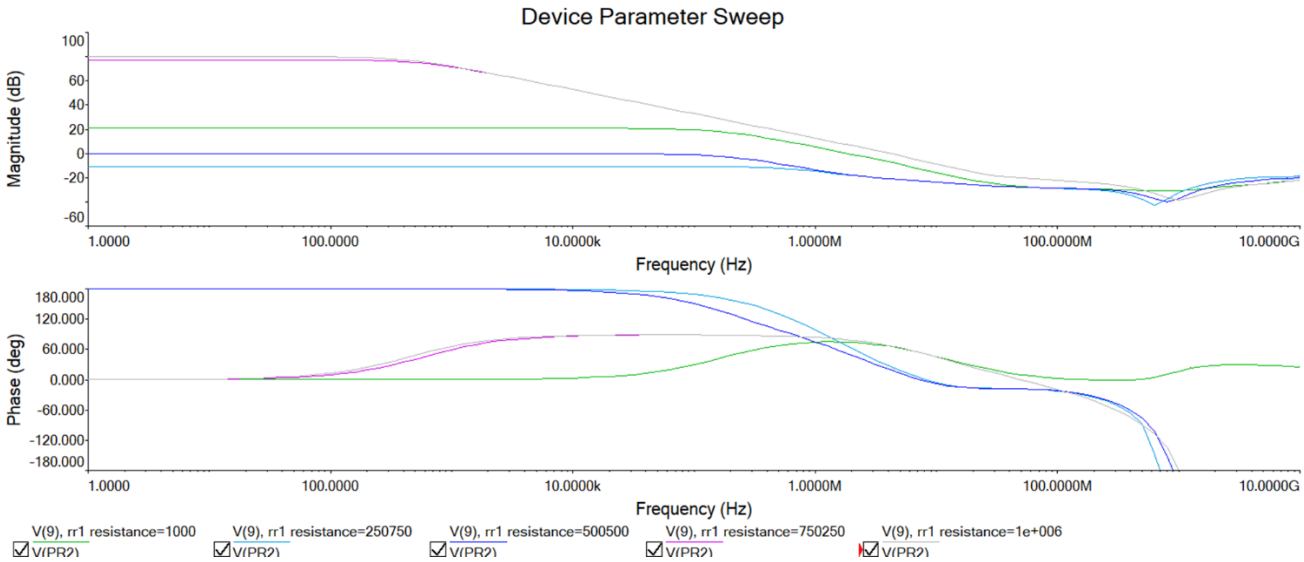


Figure 34 Device parameter sweep (AC sweep for two-stage non-inverter op-amp)