ELEC372/472: Integrated Circuit Design Assignment 3

Objectives:

- To understand the fundamental concepts underlying the behaviour of an operational amplifier (Op-amp) as covered in ELEC372/472 in the context of design.
- To design a single-stage Op-amp using a **1.2 µm CMOS technology** with specified input and output conditions. This requires initially calculating the aspect ratios of all transistors in the design, followed by simulating the design on *MultiSim*, and verifying key findings to those in the specification.
- To design and simulate a two-stage Op-amp by introducing a common-source stage and a compensation capacitor to the above design. The aspect ratios will need to be recalculated, and the design simulated on *MultiSim*, with key outputs verified to those in the specifications.

For guidance, a 15-credit module unit is meant to occupy 150 hours in total (including both private study and contact hours). You should aim to spend about 3-4 hours per week at the terminals. The remainder of the time will be taken up with background reading and research.

KEEP A LOG BOOK OF YOUR PROGRESS.

EFFECTIVE TIME MANAGEMENT IS A KEY SKILL THAT APPLIES TO ALL PROFESSIONS AND WORKING SITUATIONS.
SO IF YOU GET STUCK, ASK – DO NOT WASTE TIME – STAY FOCUSED

Any queries on the assignment, email:

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Introduction

Operational amplifiers (Op-amps) are key building blocks used in digital and analogue systems to increase the current, voltage or power of an input signal. The simplest single-stage Op-amp circuit design is shown in Fig.1, comprising of a:

a. **Differential pair** (*n*MOSTs: **M1** and **M2**). A differential amplifier amplifies analogue and digital signals and offers an output in response to the differential inputs (V_{in1} and V_{in2}). The tail of the differential pair is biased by a DC supply current source i.e. I_o represented by M_o, M_{bias} and I_{bias}, which ensures that the circuit always operates in ***saturation***. Typically, the aspect ratios of M1 and M2, and M_o and M_{bias} are the same respectively.

b. **Current mirror** (*p*MOSTs: **M3** and **M4**). A current mirror copies a current through one active device by controlling the current in another active device regardless of loading. In the circuit, M3 is always *saturated* i.e. its drain and gate terminals are tied (or $V_{DS} = V_{GS} - V_T$). As M3 and M4 have a common gate i.e. V_{GS} are identical, then the current through M3 and M4 would be the same if the dimensions are identical i.e. the current in the two transistors are mirrored.

If the aspect ratios of M1 and M2, and, M3 and M4 are the same respectively, then the same current will flow in the left and right branches (i.e. $I_o/2$), with the sum of these currents equal to I_o. Note for accurate operation of the Op-amp, all transistors need to operate in ***saturation*** (i.e. on-resistance remains high and mostly constant thus resulting in high gain).

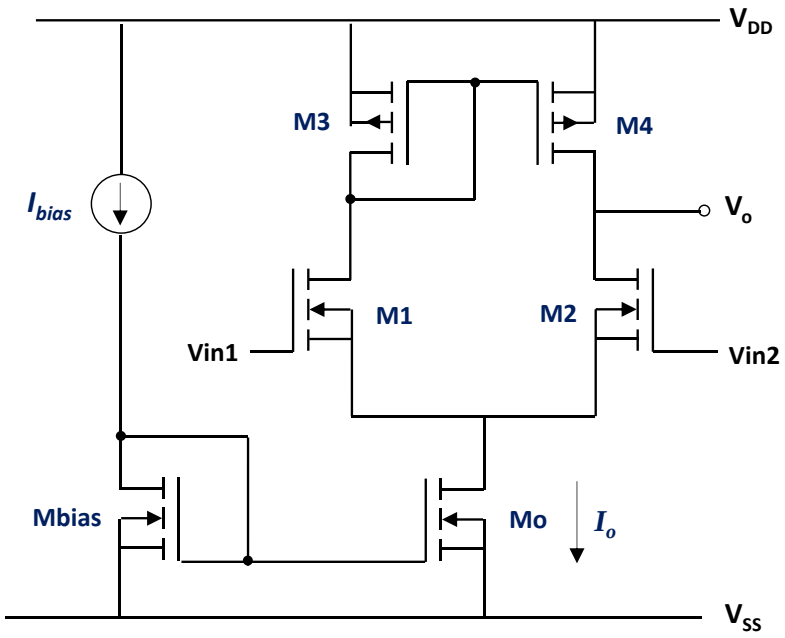


Fig. 1: Circuit design of a single-stage differential CMOS Op-amp.

Typically, the gain obtained from an Op-amp designed using a CMOS technology tends to be lower compared to that developed using bipolar technology. The gain of the CMOS Op-amp can be improved by adding an amplifiers stage such as the common-source stage shown in Fig. 2. Here, the output from the first differential amplifier stage is connected to the second common-source amplifier stage, comprising of a *p*MOST, $\mathbf{M_{op}}$. The *n*MOST, $\mathbf{M_{on}}$ is also added and connected to point X. The stability of such an amplifier can also be enhanced by introducing a compensation capacitor (C_c), which is connected between the outputs of the differential and common-source amplifier stages. The value of C_C depends on the required phase margin and is typically smaller than C_L. For example, for a phase margin of 60°, we can assume, $C_C \geq 0.22\ C_L$.

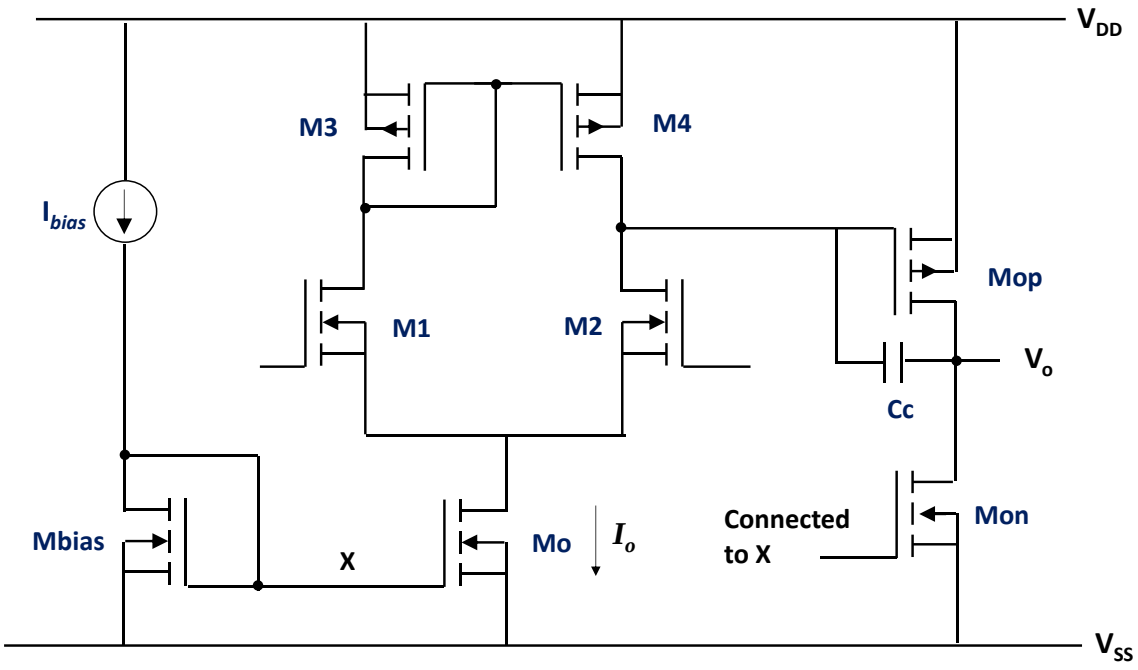


Fig. 2: Circuit design of a two-stage CMOS Op-amp consisting of a differential stage, common-source stage and compensation capacitor.

The design and simulations of the Op-amp (both single and two stages) will utilise the **1.2 µm CMOS technology** on *Multisim*. With such long channels, we can assume the channel modulation, λ is negligibly small, and thus utilise the standard saturation drain current model. The respective SPICE and design parameters are as specified in Table 1 in *Appendix A1*, and the design procedures are provided in *Appendix A2*.

Section 1 – Design and investigate the DC, AC and transient responses of a single-stage Op-amp by simulation and analysis

Design and simulate the single-stage Op-amp in Fig.1 with a voltage gain, A_v of greater 100 (≥ 40 dB), gain-bandwidth product *GB* of 1 MHz and phase margin of 60^o (at unity gain or 0 dB).

a) Calculate the aspect ratios of all transistors (i.e. M1, M2, M3, M4, M_o, and M_{bias}) in the design. Make sure to represent these as a whole number of λ_m.

b) Build and simulate the circuit design on *Multisim*, and obtain the corresponding DC, AC (i.e. Bode and phase plots) and transient (i.e. slew rate, rise/fall edge) responses.

c) Analyse the responses obtained in b), and extract/examine the key parameters from the characteristics including gain, gain-bandwidth and phase-margin etc. Compare and comment on the outputs obtained from the simulations to those provided in the specifications.

d) Further, optimise your design, and show how the gain and gain-bandwidth may be improved using this design architecture.

Section 2 – Design and investigate the DC, AC and transient responses of a two-stage Op-amp with compensating capacitor by simulation and analysis

Design and simulate the two-stage stage Op-amp in Fig. 2, consisting of an additional common source stage and a compensating capacitor, to operate with a gain, A_v of greater than 1000 (≥ 60 dB), gain-bandwidth, *GB* of 5 MHz, and phase margin of greater than 60^o.

a) Calculate the aspect ratios of all transistors (i.e. M1, M2, M3, M4, M_o, M_{bias}, M_{op}, and M_{on}) in the design. Make sure to represent these as whole multiple of λ_m.

b) Build and simulate the circuit design on *Multisim*, and obtain the corresponding DC, AC (i.e. Bode and phase plots) and transient (i.e. slew rate, rise/fall edge) responses.

c) Analyse the responses obtained in b), and extract/examine the key parameters from the characteristics including gain, gain-bandwidth and phase-margin etc. Compare and comment on the outputs obtained from the simulations to those provided in the specifications.

d) Further, optimise your design, and show how the gain and gain-bandwidth may be improved using this design architecture. Comment on the significance of the compensating capacitor.

Section 3 – Investigate amplifier circuits with closed loop gain

In Sections 1 and 2 we investigated the open loop gain of an operational amplifier. In practical applications, operational amplifiers are rarely used as open-loop circuits but is negative feedback to control the gain of the circuit.

a) Briefly explain how negative feedback is used to control gain in operational amplifiers.

b) Modify the circuit from section 1 to build and simulate the circuit design on *Multisim*, which uses negative feedback to create gains between -0.1 and -1000, and thus obtain the corresponding DC, AC (i.e. Bode and phase) plots. Explain your circuit and discuss the results. (You probably want to use 'parameter sweeps' to automate this – See *MultiSim* guidance for details).

c) Modify the circuit from section 2 to build and simulate the circuit design on *Multisim*, which uses negative feedback to create gains between -0.1 and -1000 and thus obtain the corresponding DC, AC (i.e. Bode and phase) plots. Explain your circuit and discuss the results. Compare with the results from section 3b.

d) Modify the circuit from sections 1 and 2 to build and simulate the circuit design on *Multisim*, which uses negative feedback to create non-inverting gains between +0.1 and +1000 and obtain the corresponding DC, AC (i.e. Bode and phase plots). Explain your circuit and discuss the results. Compare with the results from sections 3b and 3c.

Appendix A1: Input/output specifications

Table 1 provides the input parameters and design specifications to be utilised in the design of the Op-amp following the procedures in Appendix A2.

Parameter	Definition	Value
λ_m (µm)	CMOS Technology (minimum feature size)	1.2
V_{DD} / V_{SS} (V)	Supply rails	± 5
V_{Tp} (V)	Threshold voltage of *p*MOST	– 0.91
V_{Tn} (V)	Threshold voltage of *n*MOST	0.79
K_p (A/V^2)	Transconductance parameter of *p*MOST	2.94×10^{-5}
K_n (A/V^2)	Transconductance parameter of *n*MOST	9.64×10^{-5}
C_L (pF)	Load capacitance	20
C_C (pF)	Compensation capacitance	5
SR (V/µsec)	Slew rate	5
ICMR(+) (V)	Maximum input voltage	4.5
ICMR(–) (V)	Minimum input voltage	0.5
P_{diss} (mW)	Power dissipation	≤ 1

Table 1: SPICE and Design Parameters.

Appendix A2: Design procedure of a single-stage Op-Amp

The design procedure for the **single-stage Op-Amp** is provided below:

1. Determine the **value of I_o** to satisfy the provided *slew rate* (*SR*) for a known *load capacitance* (C_L) and *power dissipation* (P_d). In Fig. 1, consider a load capacitor (C_L) connected at the output, charging through M4. The charging current can be given as,

$$\frac{dQ}{dt} = I_o = C_L \frac{dV_o}{dt}$$

Or,

$$\frac{I_o}{C_L} = \frac{dV_o}{dt}$$

Thus, the rate of change in the output voltage V_o or the *slew rate, SR* (i.e. maximum rate of change of voltage at the output) is given as,

$$SR = \frac{dV_o}{dt} = \frac{I_o}{C_L}$$

Or,

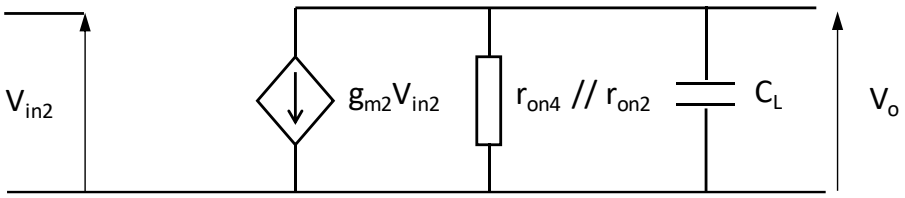
$$I_o = SR \times C_L$$

Here I_o is the DC current needed to bias the circuit i.e. flowing through M_o. Note, the current flowing through the left and right branches of the differential amplifier in Fig.1 is given as $\left({}^{I_o}/_{2}\right)$ respectively, if the aspect ratios of M1 and M2, and, M3 and M4 are matched respectively.

The power dissipation can also be determined as:

$$P_d = (V_{DD} + |V_{SS}|)\, I_o$$

2. Determine the **aspect ratios of M1 and M2** to satisfy the required *gain-bandwidth product*. Consider the small-signal circuit of one half of differential amplifier circuit e.g. right-hand side in Fig. 1 as shown below.



Here, r_{on2} and r_{on4} are the on-resistances of M2 and M4 connected in parallel and C_L is the load capacitance. The voltage gain is given as,

$$\frac{v_o}{v_{in2}} = -\frac{g_{m1,2}\,(r_{on2}//r_{o4})}{1 + 2\pi C_L\,(r_{on2}//r_{o4})}$$

This is a single-pole system with DC gain, A_v and pole, P_1 given as,

$$A_v = -g_{m1,2}\,(r_{on2}//r_{o4})$$

$$P_1 = -\frac{1}{(r_{on2}//r_{o4})C_L}$$

The gain-bandwidth product is given as,

$$GB = A_v \times P_1$$

Or alternatively substituting the above expressions results in,

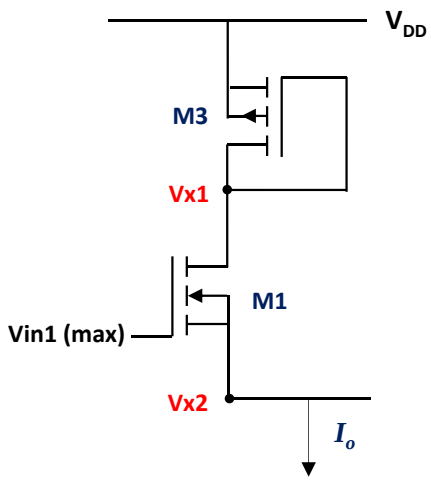
$$GB = \frac{g_{m1,2}}{2\pi C_L}$$

Using this expression, the value of $g_{m1,2}$ can be determined for the required GB and C_L provided. Following on this, the aspect ratio of M1 (and M2) can be calculated using the expression below,

$$\left(\frac{W}{L}\right)_{M1} = \frac{{g_{m1,2}}^2}{2\,I_{D1}K_{n1}}$$

Note: $g_m = {dI_{Dsat}}/{dV_{GS}}$ and using the saturation drain current expression, the above equation can be derived.

3. Determine the **aspect ratios of M3 and M4** to satisfy the *maximum input voltage, ICMR*(+). Consider one half of the differential circuit i.e. left-hand side in Fig. 1 as shown on the side. To ensure **M1 is saturated,** we require,



$$V_{DSM1} \geq V_{GSM1} - V_{Tn1}$$

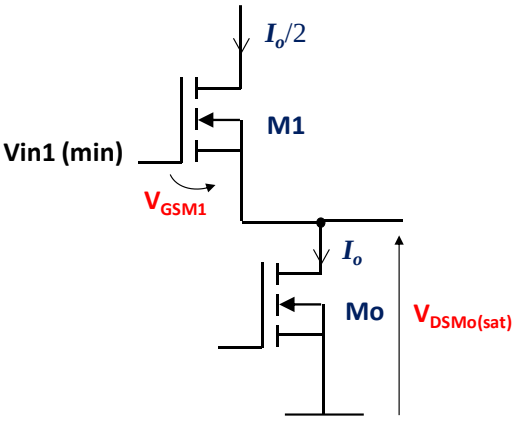
Or,

$$(V_{x1} - V_{x2}) \geq (V_{in1(max)} - V_{x2}) - V_{Tn1}$$

$$V_{x1} \geq V_{in1(max)} - V_{Tn}$$

Where $V_{in1(max)}$ is the *maximum input voltage* or *ICMR*(+) and V_{Tn} is the threshold voltage of M1. This allows the value of V_{x1} (or the drain voltage of M3) to be determined. Subsequently, the value of V_{DSM3} (or V_{GSM3}) of M3 can be calculated. Following on this, using the appropriate current expression, the aspect ratio of M3 (and M4) can be determined. Note, the value of the current flowing in half of this branch is $I_o/2$.

4. Determine the **aspect ratio of M_o and M_{bias}** to satisfy the *lower input voltage, ICMR*(–) or $V_{in1(min)}$. Consider the part of the circuit shown on the side where V_{DSMo} is the drain-source voltage of M_o in saturation and V_{GSM1} is the gate-source voltage of M1 given as,



$$V_{GSM1} = V_{in1(min)} - V_{DSMo}$$

Using appropriate drain current expression and aspect ratio for M1 obtained in part 2) above, initially determine the value for V_{GSM1}. Note the current through M1 is $I_o/2$. Subsequently, work out the value of V_{DSMo} using the above expression, assuming the given minimum input voltage. Note this could be a negative voltage value. Following on this, using the appropriate drain expression for M_o, work out its aspect ratio, assuming $V_{DSMo} = V_{GSMo} - V_T$.

5. Simulate your design. If required, iterate the process so as to optimise the design and attain the required gain and gain bandwidth.

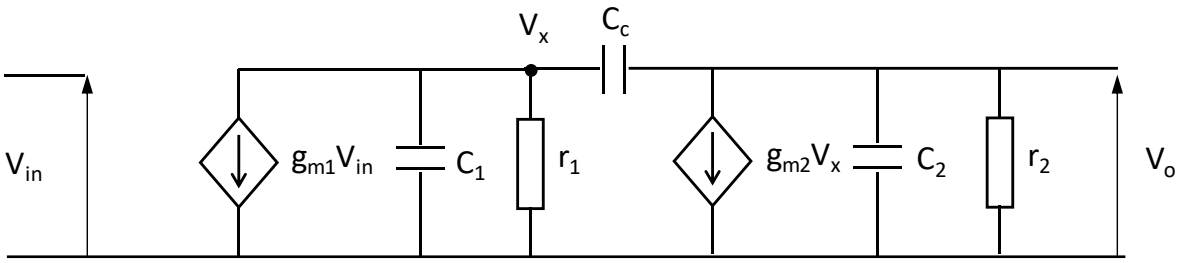
Appendix A3: Design procedure of a two-stage Op-Amp

The design procedure for the **two-stage Op-Amp** is provided below:

1. Determine the **value of I_o** to satisfy the *slew rate* (*SR*) for a known value of *compensating capacitance* (C_c) as given by expression below.

$$I_o = SR \times C_c$$

2. Determine the **aspect ratios of M1 and M2** to satisfy the required *gain-bandwidth product*. The small-signal circuit of the two-stage amplifier is shown below. For simplicity, we can consider each amplifier stage separately, such that $g_{m1}V_{in}$, C_1 and r_1 relates to the 1st stage amplifier, whilst $g_{m2}V_x$, C_2 and r_2 relates to the 2nd stage amplifier. Here, V_x is the output from the first stage into the second stage amplifier.



The DC gain of the two-stage amplifier can be given as,

$$A_v = g_{m1}r_1 \times g_{m2}r_2$$

Note this is a two-pole system with respective poles given as,

$$P_1 = \frac{1}{g_{m2}r_1r_2C_c} \qquad \text{and} \qquad P_2 = -\frac{g_{m2}}{C_2}$$

The gain-bandwidth product is given as,

$$GB = A_v \times P_1$$

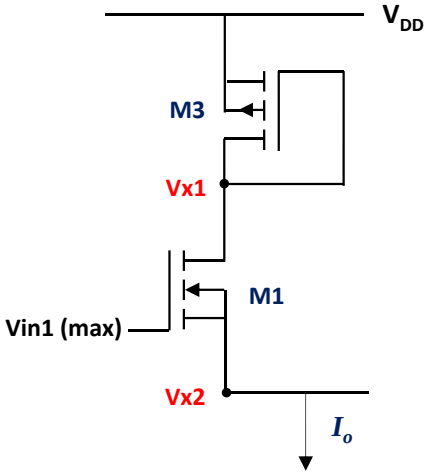
Substituting the above expressions, we find,

$$GB = \frac{g_{m1}}{2\pi C_c}$$

Using this expression, the value of g_{m1} can be determined assuming the respective values of *GB* and C_c provided. Following on this, the aspect ratio of M1 (and M2) can be calculated using the expression below:

$$\left(\frac{W}{L}\right)_{M1} = \frac{{g_{m1}}^2}{2\, I_{D1} K_n}$$

3. Determine the **aspect ratios of M3 and M4** to satisfy the *maximum input voltage*, *ICMR*(+) or $V_{in1(max)}$. Consider half of the differential circuit as shown in the circuit. To ensure **M1** operates in saturation, we require,



$$V_{DSM1} \geq V_{GSM1} - V_{Tn1}$$

Or $$V_{in1(max)} \leq (V_{x1} + V_{Tn1})_{min}$$

Here $V_{in1(max)}$ is the *maximum input voltage ICMR*(+). $V_{x1(min)}$ needs to be determined, which can be done by determining the current in **M3**. Note M3 is operating in saturation since its gate is tied to its drain, such that,

$$V_{x1(min)} = V_{DD} - V_{GSM3}$$

Using the drain current expression, we can express V_{GSM3} as below,

$$V_{GSM3} = \sqrt{\frac{2I_{DsatM3}}{K_p\left(\frac{W}{L}\right)_{M3}}} + V_{Tp3}$$

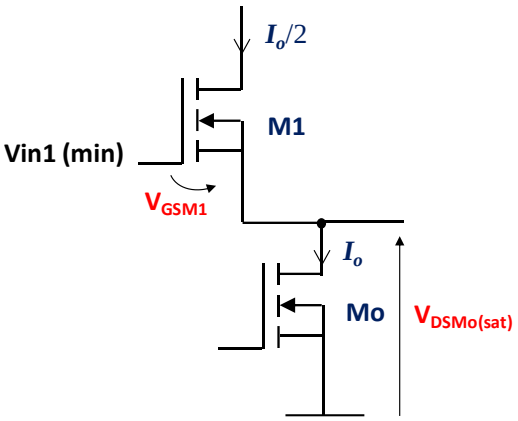
And substituting this to the equation above, we find,

$$V_{x1(min)} = V_{DD} - \left[\sqrt{\frac{2I_{DM3}}{K_p\left(\frac{W}{L}\right)_{M3}}} + V_{Tp3}\right]$$

Substituting this expression above and rearranging, we obtain expression below, which can used to determine the aspect ratio of M3.

$$\left(\frac{W}{L}\right)_{M3} = \frac{2I_{DM3}}{K_p\left(V_{DD} - ICMR(+) - V_{Tp3} + V_{Tn1min}\right)^2}$$

4. Determine the **aspect ratio of M_o and M_{bias}** to satisfy the *lower input voltage*, *ICMR*(−) or $V_{in1(min)}$. Consider the part of the circuit shown on the side where V_{DSMo} is the drain-source voltage of **M_o** in saturation and V_{GSM1} is the gate-source voltage of **M1**. To ensure that Mo remains in saturation, we need to maintain a $V_{DSMo(sat)}$ value such that,



$$V_{in1(min)} \geq V_{GSM1} + V_{DSMo(sat)}$$

Note,

$$V_{GSM1} = \sqrt{\frac{2I_{DsatM1}}{K_n\left(\frac{W}{L}\right)_{M1}}} + V_{TnM1}$$

Substituting this in the above expression, we can find the expression for $V_{DSMo(sat)}$ as given below, and subsequently its corresponding value can be calculated. Note this could be a negative voltage value.

$$V_{DSMo(sat)} \geq V_{in1(min)} - \sqrt{\frac{2I_{DsatM1}}{K_n\left(\frac{W}{L}\right)_{M1}}} - V_{TnM1}$$

And using the current expression below, the aspect ratio of **M_o** can be determined. Here I_{DsatMo} is equal to I_o in the circuit diagram.

$$I_{DsatMo} = \frac{K_n}{2}\left(\frac{W}{L}\right)_{Mo}(V_{DSMo})^2$$

5. Determine the **aspect ratio of M_{op}** for the required *phase margin*, such that we can assume that,

$$g_{m\text{Mop}} \geq 10\, g_{m1}$$

And if **M3** and **M4** are matched correctly, then we can assume the corresponding V_{GS} and V_{DS} are the same to that of **M_{op}**. In this case, the difference in these devices are their respective aspect ratios, which subsequently determines the current flowing through them. Thus, we can represent the ratios as given in the expression below,

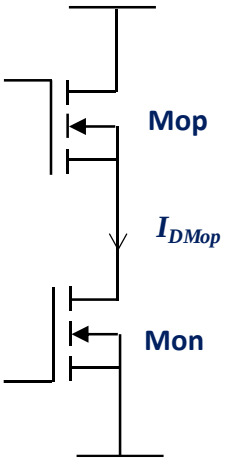
$$\frac{(W/L)_{Mop}}{(W/L)_{M4}} = \frac{I_{DMop}}{I_{DM4}}$$

Or,

$$\frac{(W/L)_{Mop}}{(W/L)_{M4}} = \frac{g_{mMop}}{g_{mM4}}$$

Using this expression, the aspect ratio of **M_{op}** can be calculated.

6. Determine the **aspect ratio of M_{on}**. Consider part of the circuit as shown, the same current, I_{DMop} is flowing in M_{op} and M_{on}. Using the same expression above, we can find the value of the current, I_{DMop} such that,



$$I_{DMop} = \frac{(W/L)_{Mop}}{(W/L)_{M4}} I_{DM4}$$

Similarly, if the devices are matched appropriately then the V_{DS} and V_{GS} of **M_o** and **M_{on}** are the same, such that,

$$\frac{(W/L)_{Mon}}{(W/L)_{Mo}} = \frac{I_{DMon}}{I_{DMo}}$$

Thus, the aspect ratio of **M_{on}** can be determined.

7. Iterate and optimise the design, if needed, to attain the required gain and gain bandwidth from the simulations.