

Assignment 2 – Analogue Design

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By submitting this work electronically, I confirm that I have acted honestly, ethically and professionally in conduct leading to assessment for the programme of study.

I confirm that I have not copied material from another source nor committed plagiarism nor fabricated, falsified or embellished data when completing the attached piece of work. I confirm that I have not copied material from another source, nor colluded with any other student in the preparation and production of this work.

Section 1: Design and simulation of a CMOS Inverter

- a) Set the p-MOST with the width (in microns) equal to the number assigned to you (see the list on Canvas). The n-MOST should have a width of 4.8 μm .
Paste screenshots of the transient and DC simulations below and discuss overshoot, undershoot, rise- and fall times.

[5/100]

As referenced, the fall-time is defined as the time taken for an n-channel MOSFET in a CMOS inverter to pull down the output voltage from 90% to 10% of the supply voltage. The voltages are calculated as follow:

90% of the supply voltage: 4.5 V

10% of the supply voltage: 0.5 V

From $\beta_p = \mu_p * W_p / L_p$ and $\beta_n = \mu_n * W_n / L_n$

n-MOST have a width of 4.8 μm and a length of 2.4 μm so $\beta_n = 0.19 \text{ mA/V}^2$.

p-MOST have a width of 9.6 μm and a length of 2.4 μm so $\beta_p = 0.12 \text{ mA/V}^2$.

Because of β_p is less than β_n so the rise time, which is controlled by the depletion load (pull-up) transistor would be slower than the fall time, which is controlled by the enhancement (pull-down) n-MOST as shown in Figure 1 that the rise time of transient analysis is 479.0 ps which is slower than the fall time (which is 340.5 ps).



In comparison to the theoretical assumptions discussed in the lecture, certain factors are considered during fall time analysis. These factors include neglecting the current in the p-channel device and assuming that the n-MOS driver transistor is initially saturated before transitioning to an unsaturated state. However, in transient simulation, there is observable p-MOS current, as evidenced by the observed overshoot. The overshoot is calculated as $(5.3080 - 5.0000) / 5.0000 * 100 = 6.16\%$. Similarly, during transient analysis at rise time, n-MOS current is observed, indicating the presence of undershoot at 1.92%.

Figure 2 represents DC transfer characteristic with a width of p-MOST = 9.6 μm and a width of n-MOST = 4.8 μm . For the switching threshold voltage, there is a shift from VDD/2 (which is 2.5 V) to the left at Vin = 2.1790 V.

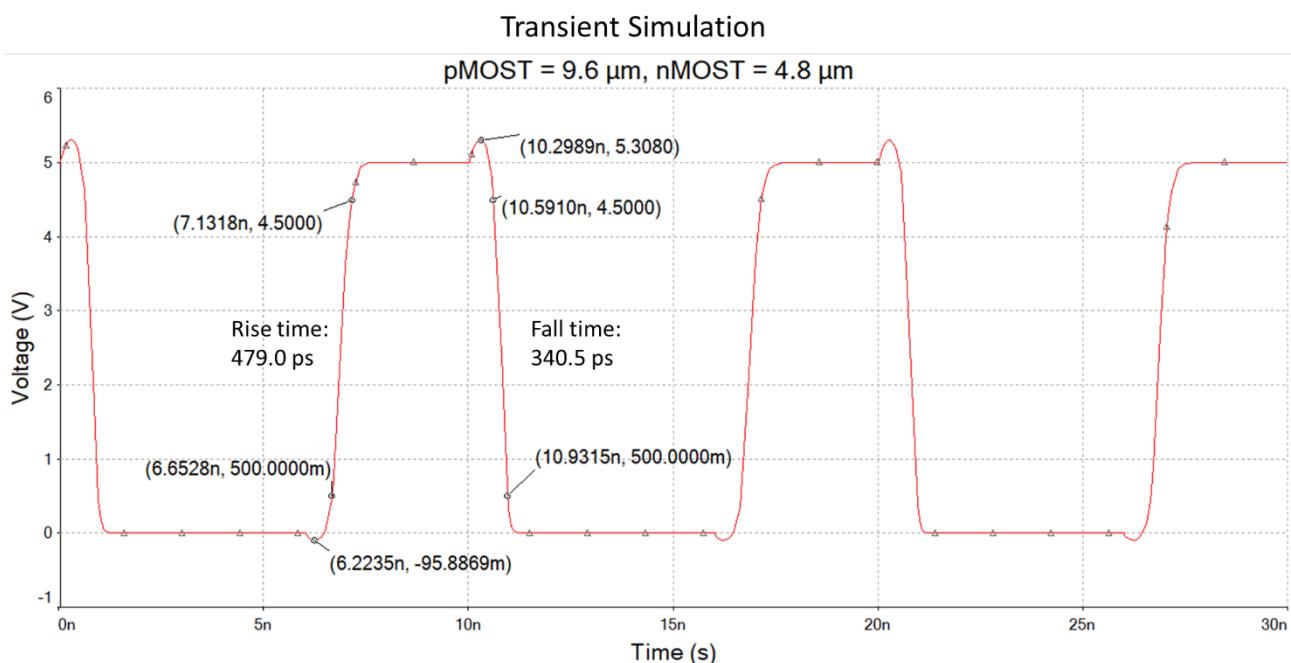


Figure 1 Transient Simulation of width of p-MOST = 9.6 μm and width of n-MOST = 4.8 μm .

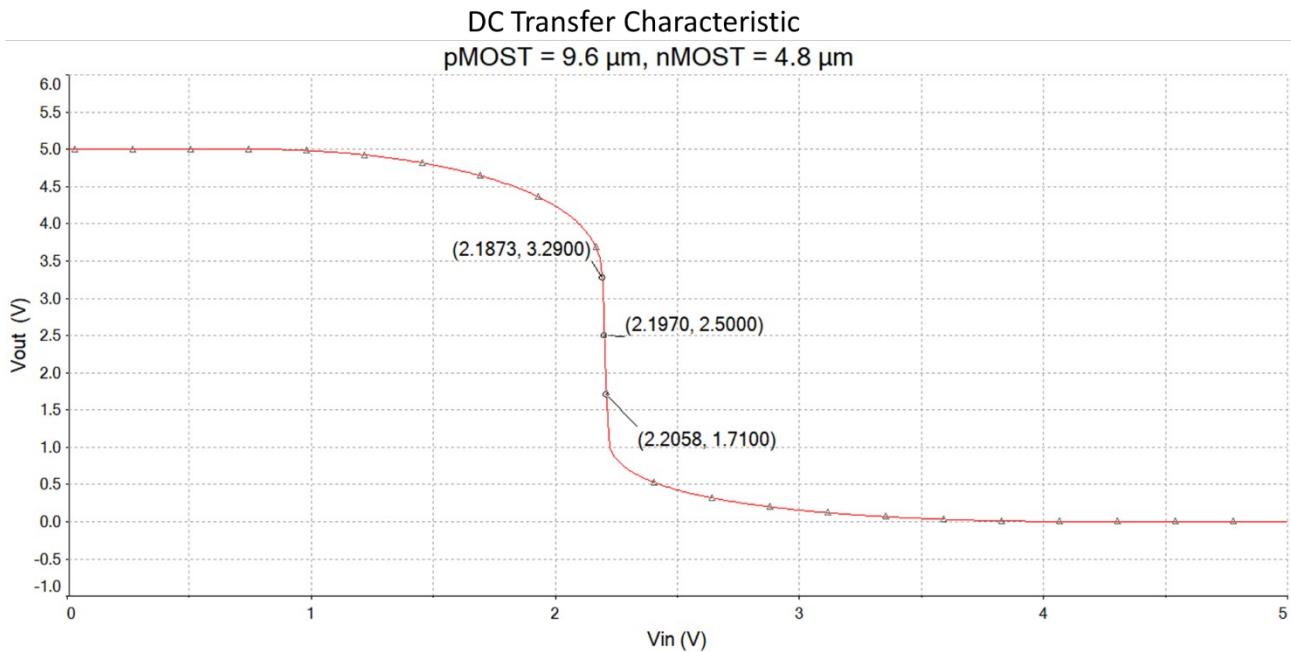


Figure 2 DC Simulation of width of p-MOST = 9.6 μm and width of n-MOST = 4.8 μm .

- b) Set the widths of both n-MOST and p-MOST equal to the number assigned to you. Paste screenshots of the transient and DC simulations below and discuss overshoot, undershoot, rise- and fall times.

[5/100]

n-MOST have a width of 9.6 μm and a length of 2.4 μm so $\beta_n = 0.39 \text{ mA/V}^2$.

p-MOST have a width of 9.6 μm and a length of 2.4 μm so $\beta_p = 0.12 \text{ mA/V}^2$.

With β_p being lower than β_n , the rise time, governed by the depletion load (pull-up) transistor, tends to be slower than the fall time, which is influenced by the enhancement (pull-down) n-MOST. This relationship is apparent in Figure 3, where the rise time in transient analysis measures 456.4 ps, exceeding the fall time of 281.1 ps. The overshoot is 6.27%, when the undershoot is 2.10%. The observed undershoot in the simulation contradicts the theoretical assumption of no n-MOS current during the rising period.

From $\beta_n / \beta_p = 3.25$ in this circuit design, compared to previous design that $\beta_n / \beta_p = 1.58$, it can be observed from Figure 4 that the switching threshold voltage shifts further to the left. It shifts to the point where $V_{in} = 1.89$ V, whereas previously it was at 2.18 V. In theory it should be at 2.5 V.

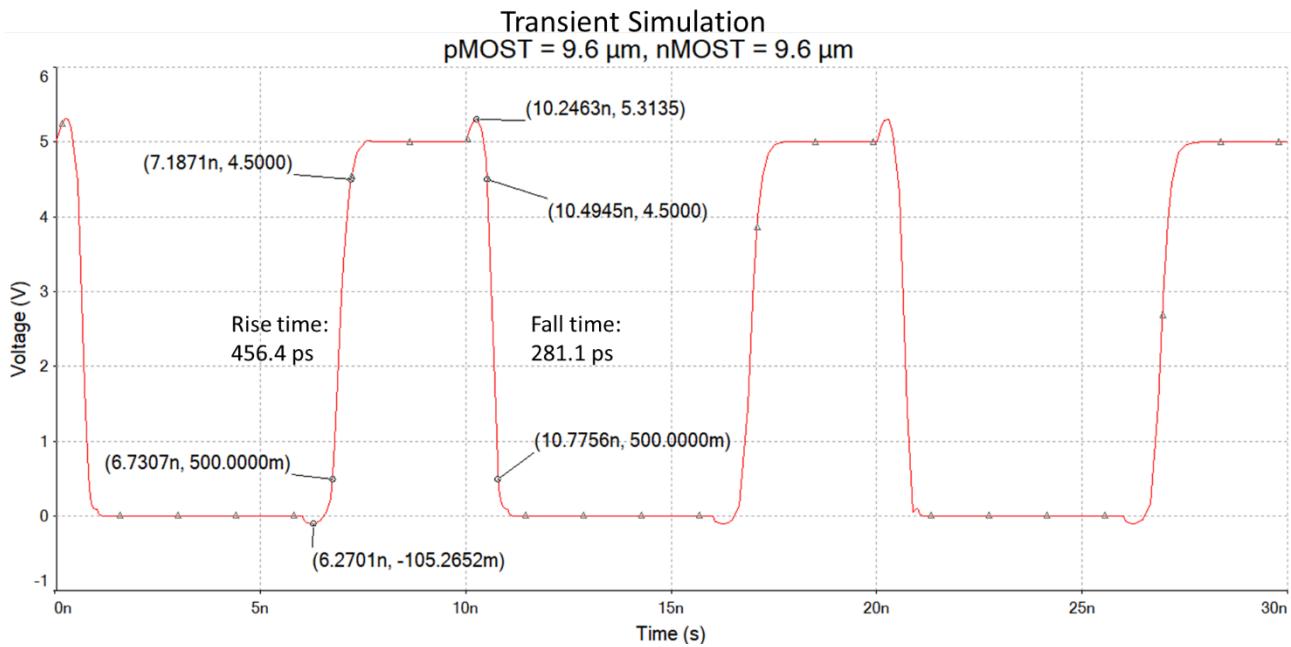


Figure 3 Transient Simulation of width of p-MOST = 9.6 μ m and width of n-MOST = 9.6 μ m.

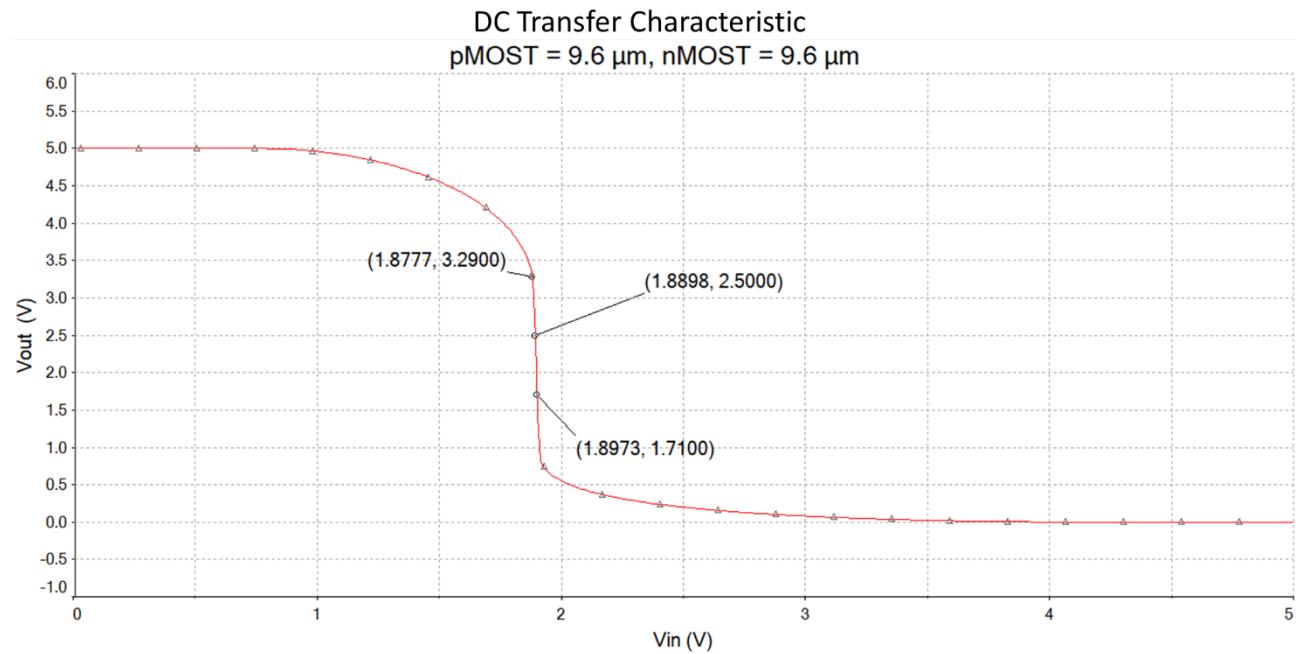


Figure 4 DC Simulation of width of p-MOST = 9.6 μ m and width of n-MOST = 9.6 μ m.



- c) Set the widths of the nMOS and pMOS devices to be equal to 1.2 μm . Paste screenshots of the transient and DC simulation below and discuss overshoot, undershoot, rise- and fall times.

[5/100]

n-MOST have a width of 1.2 μm and a length of 2.4 μm so $\beta_n = 48 \mu\text{A/V}^2$.
p-MOST have a width of 1.2 μm and a length of 2.4 μm so $\beta_p = 15 \mu\text{A/V}^2$.

In Figure 5, the rise time and fall time of transient analysis are compared for a circuit where β_p is lower than β_n . The rise time, controlled by the depletion load transistor, is slower than the fall time governed by the enhancement n-MOST. Specifically, the rise time measures 1.89 ns, while the fall time is 636 ps. The overshoot is calculated as 1.6%, while the undershoot is 1.5%. Compared to previous designs, the values of β_n and β_p in this circuit are lower. Consequently, the undershoot and overshoot are reduced compared to previous designs, attributable to the smaller size of the transistor.

With a β_n / β_p ratio of 3.2 in this circuit design, compared to 1a) where $\beta_n / \beta_p = 1.58$, Figure 6 indicates a shift in the switching voltage to the left, reaching 1.86 V. This deviation from the desired behaviour suggests a potential issue in the design.

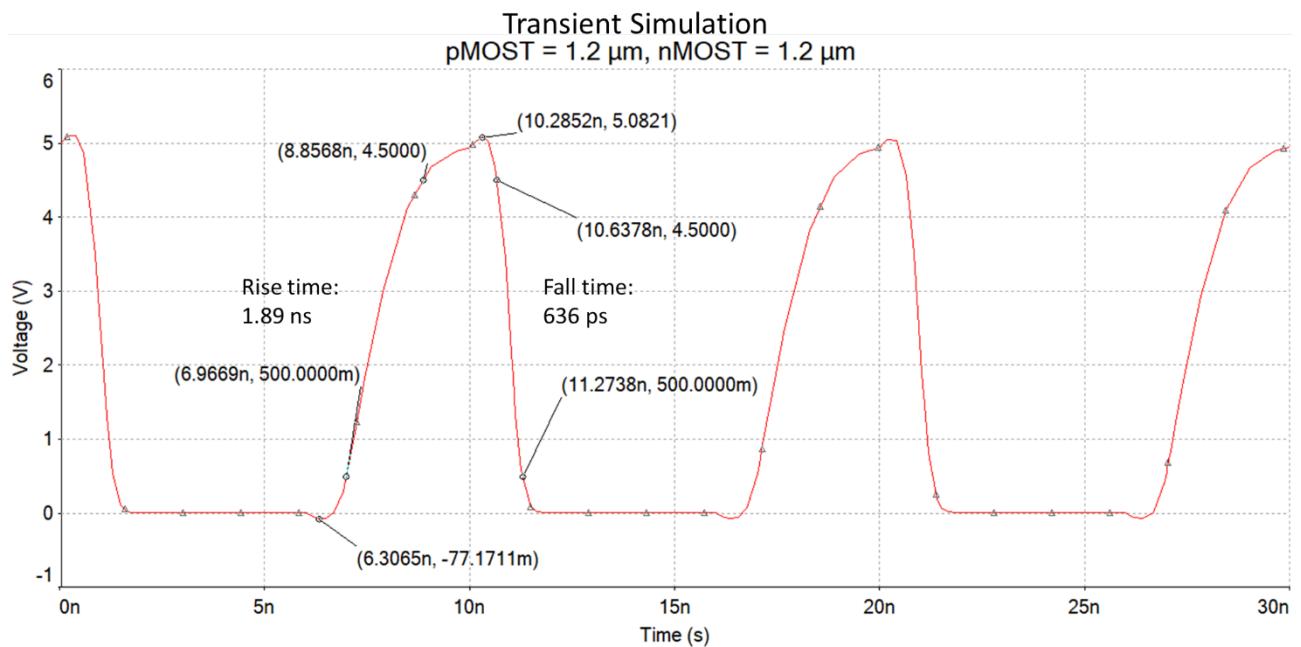


Figure 5 Transient Simulation of width of p-MOST = 1.2 μm and width of n-MOST = 1.2 μm .

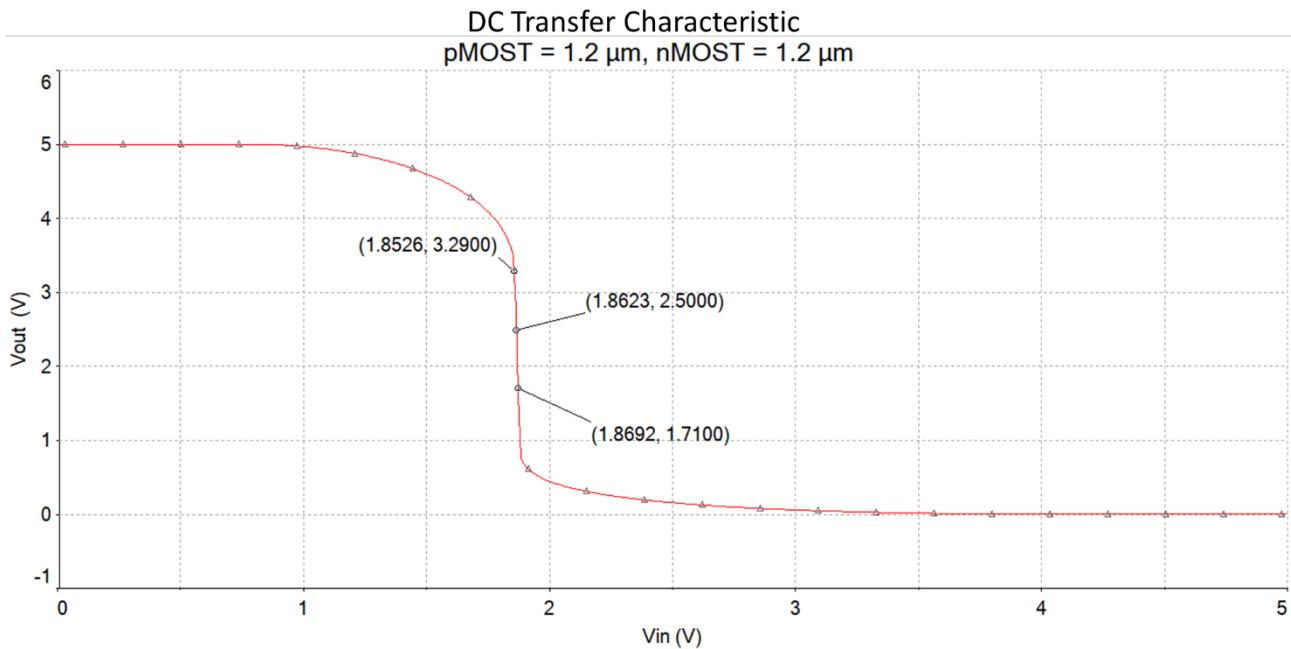


Figure 6 DC Simulation of width of p-MOST = 1.2 μm and width of n-MOST = 1.2 μm.

- d) Set the pMOS to the width assigned to you and design a matched inverter (where rise and fall times are similar) by adjusting the width of the nMOS. Paste screenshots of the transient and DC simulation below and discuss overshoot, undershoot, rise- and fall times. Discuss how you arrived at the width of the nMOS and how well the design is matching.

[10/100]

To design a matched inverter, we assume that β_p equals β_n .

From $\beta_p = \mu_p * W_p / L_p$ and $\beta_n = \mu_n * W_n / L_n$ and $L_p = L_n = 2.4 \mu m$

$$\beta_p = \beta_n$$

$$\mu_p * W_p / L_p = \mu_n * W_n / L_n$$

$$29.4 \mu A/V^2 * \frac{9.6 \mu m}{2.4 \mu m} = 96.5 \mu A/V^2 * \frac{W_n \mu m}{2.4 \mu m}$$

Thus, nMOS have a width of $2.92 \mu m$.

However, considering a minimum feature size of $1.2 \mu m$, the width of the nMOS width should be rounded up to $3.6 \mu m$.



For matched device, nMOS have a width of 3.6 μm and a length of 2.4 μm so $\beta_n = 0.14 \text{ mA/V}^2$. and pMOS have a width of 9.6 μm and a length of 2.4 μm so $\beta_p = 0.12 \text{ mA/V}^2$.

In Figure 7, the transient analysis compares the rise time and fall time for a circuit in which β_p is lower than β_n . Here, the rise time, primarily governed by the depletion load transistor, is slower than the fall time, controlled by the n-MOST. Specifically, the rise time measures 508 ps, while the fall time is 357.2 ps. Despite the small difference in β values, this matched design demonstrates nearly equal rise and fall times compared to the design from 1a) and 1b). The overshoot is calculated as 6.35%, while the undershoot is 1.81%.

Figure 8 shows DC simulation results for a circuit with matched devices. When V_{in} is 2.5 V, V_{out} is approximately 2.43 V, aligning with theory. The steep slope indicates a well-designed circuit. Matched devices ensure identical rise and fall times, yielding symmetrical switching waveforms, a key advantage over ratioed logic.

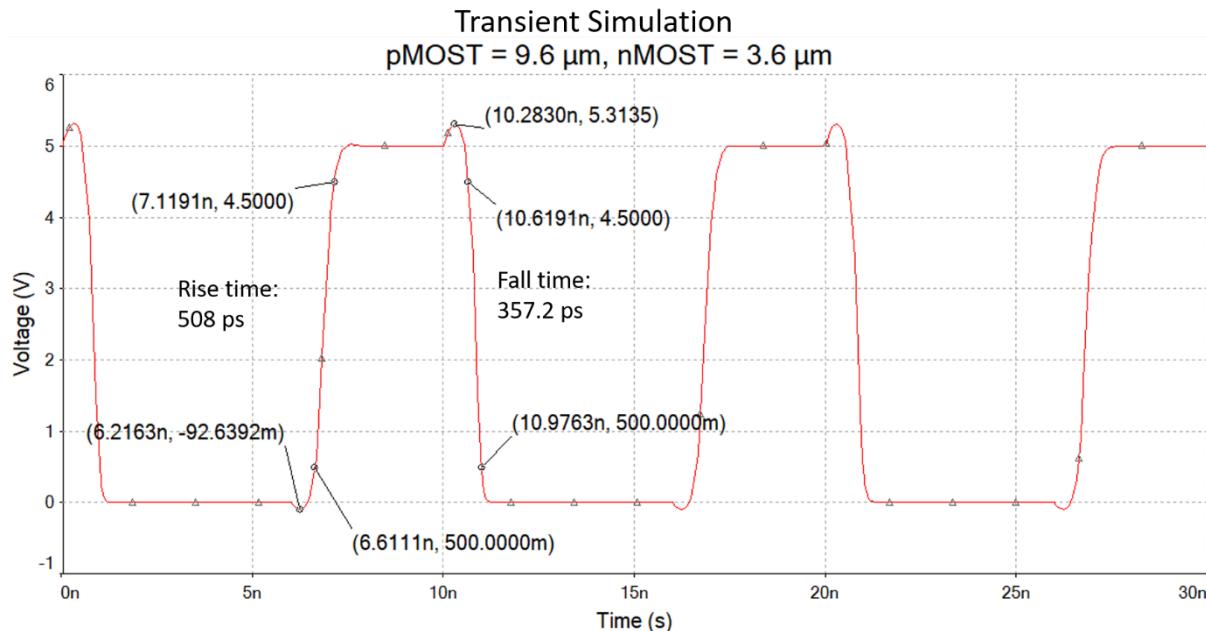


Figure 7 Transient Simulation of width of p-MOST = 9.6 μm and width of n-MOST = 3.6 μm .

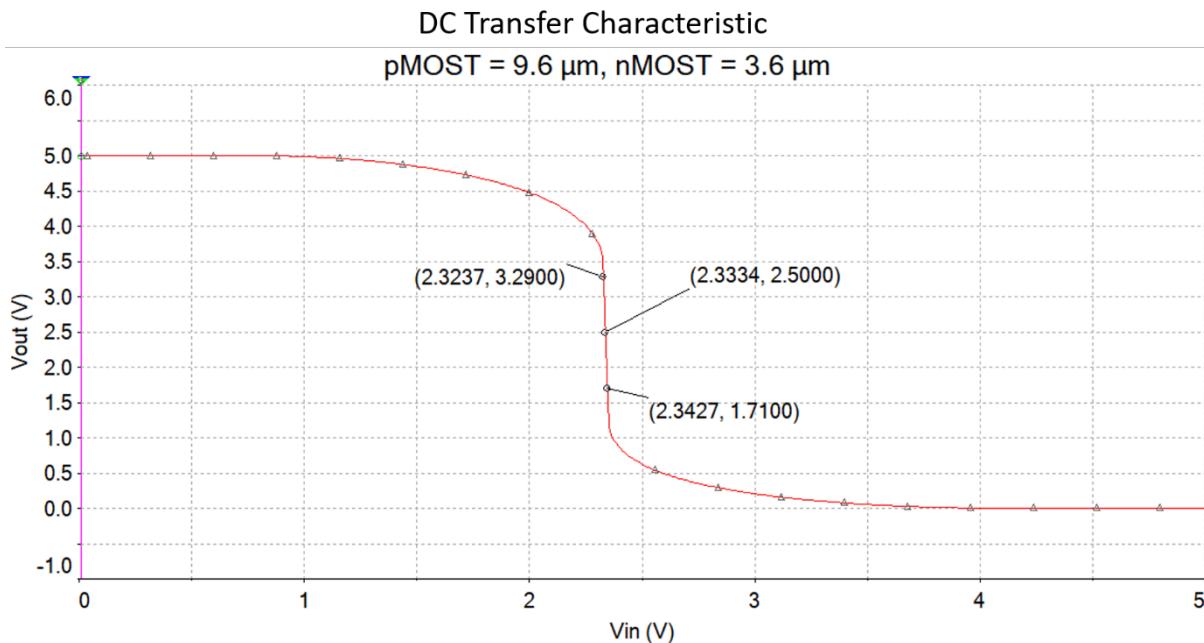


Figure 8 DC Simulation of width of p-MOST = 9.6 μm and width of n-MOST = 3.6 μm.

- e) Discuss the performance of your circuit and how different transistor widths affect it.

[5/100]

The rise time (τ_r) and the fall time (τ_f) in a CMOS circuit are denoted by the equations:

$$\tau_r = \frac{C_L}{\beta(V_{DD}-V_T)} \left\{ \frac{2(V_T-0.1V_{DD})}{(V_{DD}-V_T)} + \ln \left[\frac{0.9V_{DD}(2(V_{DD}-V_T)-V_T)}{V_T(2(V_{DD}-V_T)-0.9V_{DD})} \right] \right\}$$

$$\tau_f = \frac{C_L}{\beta(V_{DD}-V_T)} \left\{ \frac{2(V_T-0.1V_{DD})}{(V_{DD}-V_T)} + \ln \left[\frac{2(V_{DD}-V_T)-0.1V_{DD}}{0.1V_{DD}} \right] \right\}$$

Here, β represents the aspect ratio of the transistor ($\mu * W/L$) where μ is the mobility, W is the width, and L is the length of the transistor. When β is larger, both the rise time and fall time become faster. Therefore, increasing the width of the transistor will result in faster rise and fall times as shown in Figure 9 and Table 1.



Table 1 Fall time & Rise time as function of n-MOST width.

nMOST width (μm)	18.0	9.6	4.8	3.6	1.2
fall time (ps)	262.9	281.1	340.5	357.2	532.2
rise time (ps)	457.1	456.4	479.0	508.0	568.7

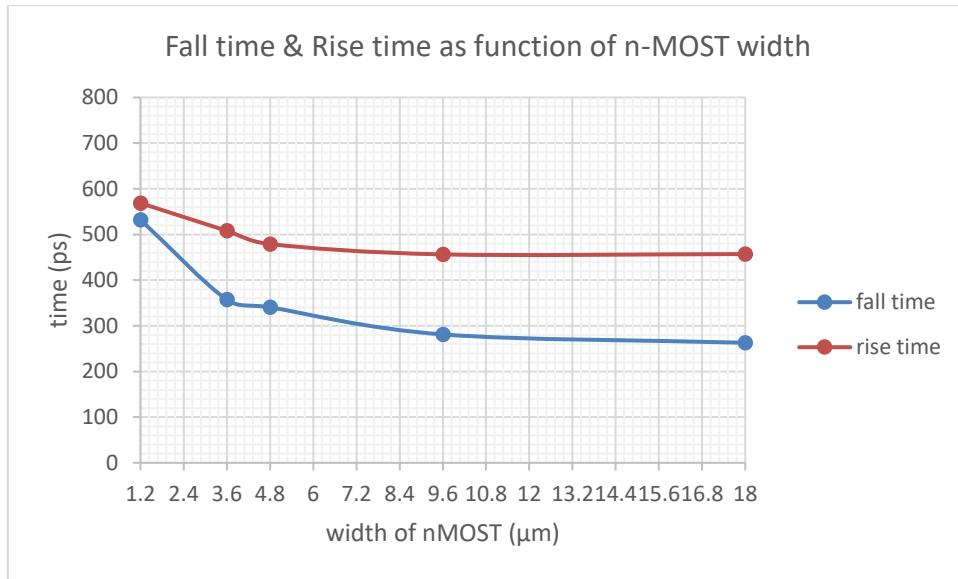


Figure 9 Fall time & Rise time as function of n-MOST width

f) Sketch a cross-sectional and a top layout view of the CMOS inverter.

[5/100]

A cross-sectional view of a CMOS inverter offers a vertical perspective (as shown in Figure 10) revealing the internal structure of its transistors, including the arrangement of source, drain, and gate regions within the semiconductor substrate. This view provides insights into the physical dimensions and layout of the various components. Conversely, a top layout view offers a planar depiction showcasing the spatial arrangement of transistors and interconnections on the semiconductor surface. It reveals crucial details about the layout design, such as transistor sizing and interconnect routing, crucial for ensuring proper functionality and performance of the CMOS inverter circuit. For matched devices, the width of the n-MOST is $3.6 \mu\text{m}$ (3λ), with a length of $2.4 \mu\text{m}$ (2λ) ($W/L = 3 \lambda/2 \lambda$). Similarly, the width of the p-MOST is $9.6 \mu\text{m}$ (8λ), with a length of $2.4 \mu\text{m}$ (2λ) ($W/L = 8 \lambda/2 \lambda$).

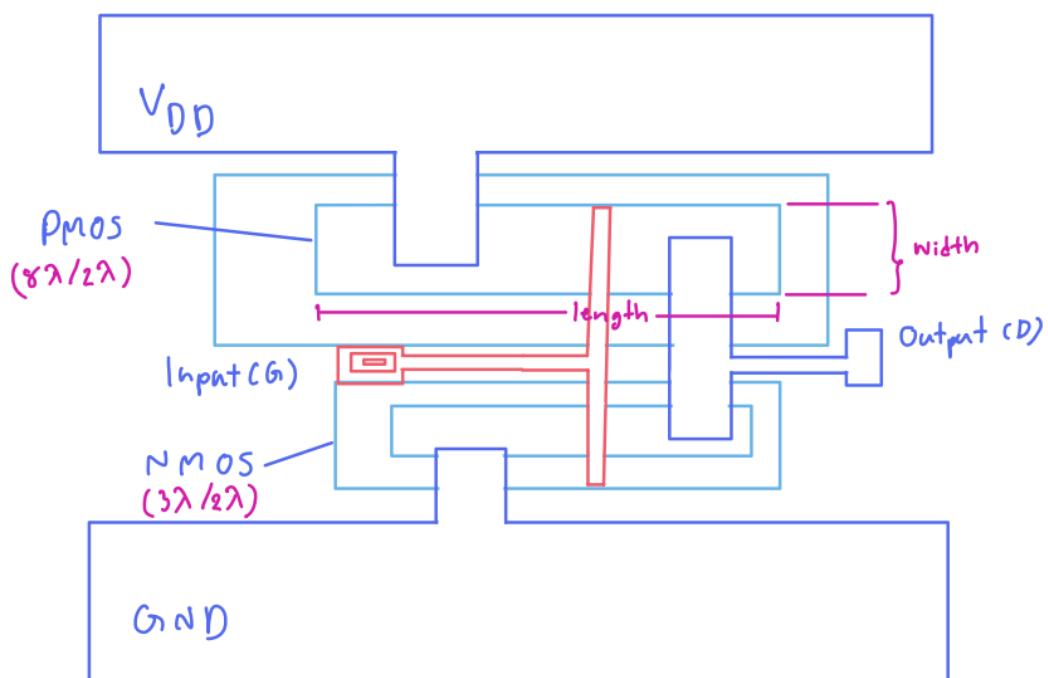
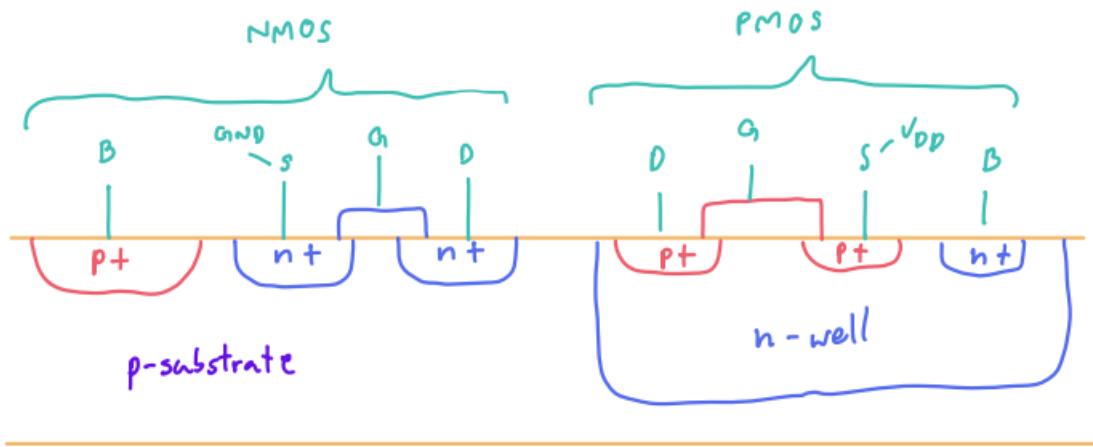


Figure 10 Cross-sectional and a Top layout view of the CMOS inverter.



- g) Explain the physical nature of contact and active area masks and qualitatively how punch-through/DIBL/GIDL are affected by reducing the channel length.

[5/100]

As the channel length decreases in semiconductor devices, the electric field between the source and drain regions intensifies. This heightened electric field raises the likelihood of carriers punching through the channel region, thereby elevating leakage current and potentially leading to device failure. Consequently, the reduction in channel length can exacerbate punch-through effects.

DIBL, or Drain-Induced Barrier Lowering, describes the reduction in the barrier potential between the source and drain regions due to the influence of drain bias. With decreasing channel length, the drain-induced electric field penetrates deeper into the channel, diminishing the effective barrier between the source and drain. This effect becomes more pronounced as channel lengths shorten, contributing to increased subthreshold leakage current and diminished device performance.

Gate-Induced Drain Leakage (GIDL) occurs due to the gate's influence on lowering the drain barrier potential. As channel length diminishes, the gate gains greater control over a larger portion of the channel region. Consequently, the gate's impact extends deeper into the channel, resulting in amplified gate-induced leakage. This phenomenon is particularly notable in short-channel devices, where the gate's influence extends more extensively into the channel, leading to an increase in off-state leakage current.

To sum up, the reduction of channel length in semiconductor devices can exacerbate punch-through, DIBL, and GIDL effects. This occurs due to heightened electric fields and improved gate control, leading to increased leakage currents and potential reliability issues. Thus, it becomes imperative to implement proper device design and optimization strategies to mitigate these effects and ensure sustained and reliable device operation.



Section 2: Investigate the power dissipation of a loaded CMOS inverter

- a) Discuss briefly how the power measurement circuit works (including a circuit diagram) and you arrived at the values for C and current gain (k) (assuming $R = 100M\Omega$)

[5/100]

The circuit, as shown in Figure 11, measures the current drawn from the power supply using a current-controlled current source. The voltage signal from the current sensing element is used to control a current source. The current source generates a current proportional to the sensed current, but scaled by a factor, k, determined by the circuit design. The scaled current from the current source is integrated over the switching period using a capacitor. The capacitor accumulates charge proportional to the integrated current. The voltage across the capacitor, which represents the accumulated charge, is proportional to the average power dissipation over the switching period. This voltage is measured and used to calculate the average power consumption.

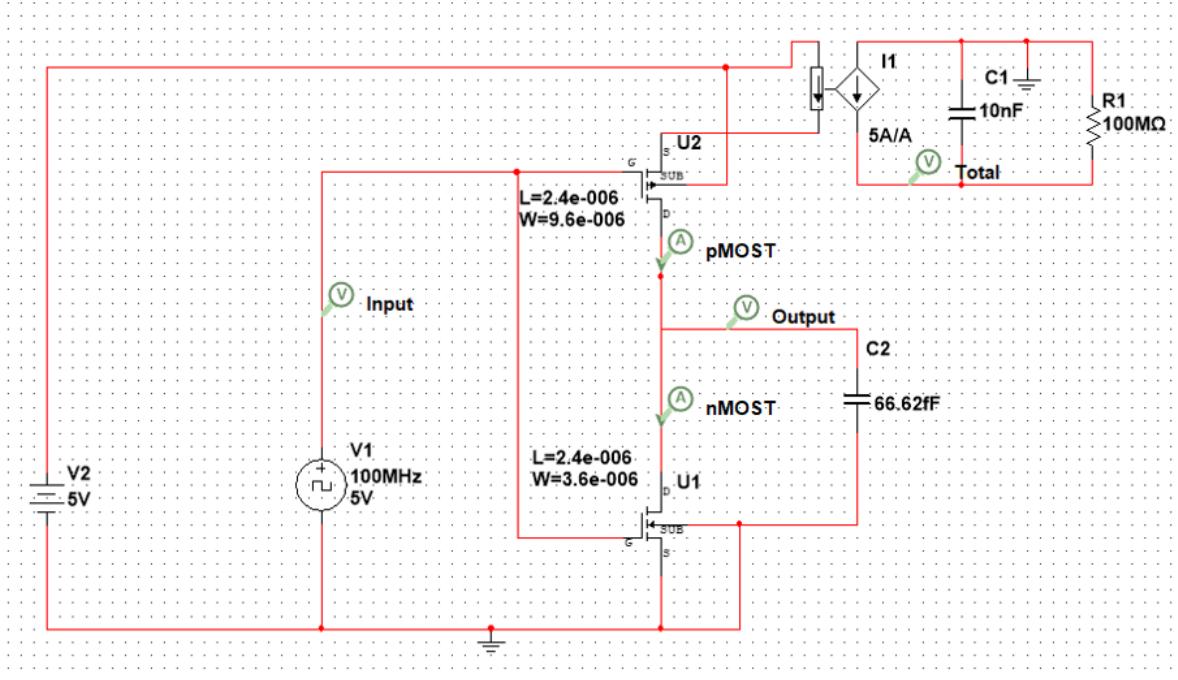


Figure 11 Circuit diagram of power measurement.



Given the clock frequency of 100 MHz, the switching period (T) is calculated as

$$T = \frac{1}{100\text{MHz}} = 10 \text{ ns.}$$

To calibrate the meter using the equation $\frac{k}{C} = \frac{V_{DD}}{T}$, where V_{DD} is the supply voltage, we are given that $C=10 \text{ nF}$ and $V_{DD}=5 \text{ V}$.

Solving for k , we have = 5.

So, the scaling factor k for the current-controlled current source is 5.

Using the ‘matched design’ from section 1d) and the script from the assignment 1 model, C_L is calculated to be 66.62 fF.

- b) Plot the total power dissipation, drain current of p-MOST and n-MOST and input and output signal. Discuss your results.

[5/100]

Consider the rise time whereby the load capacitance charges via the pMOS (we assume no current in the nMOS). The energy drawn for the supply, denoted as E_{DD} over this period can be found as follows: $E_{DD} = \int_0^{V_{DD}} i(t)V_{DD} dt = V_{DD} \int_0^{V_{DD}} C_L \frac{dV_o}{dt} dt$.

Figure 12 illustrates input and output signals, as well as the drain currents of the p-MOST and n-MOST transistors, along with power dissipation. The input signal has a period of 10 ns, matching the frequency of the voltage source. The rise time of the output signal is measured at 903 ps, while the fall time is 605 ps. The light blue line corresponds to the drain current of the n-MOST, whereas the pink line represents the drain current of the p-MOST.

Simulation results demonstrate that when the drain current of the p-MOST dominates, there is a rise time observed in the output signal. Conversely, when the drain current of the n-MOST dominates, a fall time is observed. However, it's worth noting that there is some drain current from the p-MOST during the fall time and from the n-MOST during the rise time, which contradicts the assumptions typically made in theoretical discussions.



Input and Output signal, Drain current of p-MOST and n-MOST, and Power Dissipation

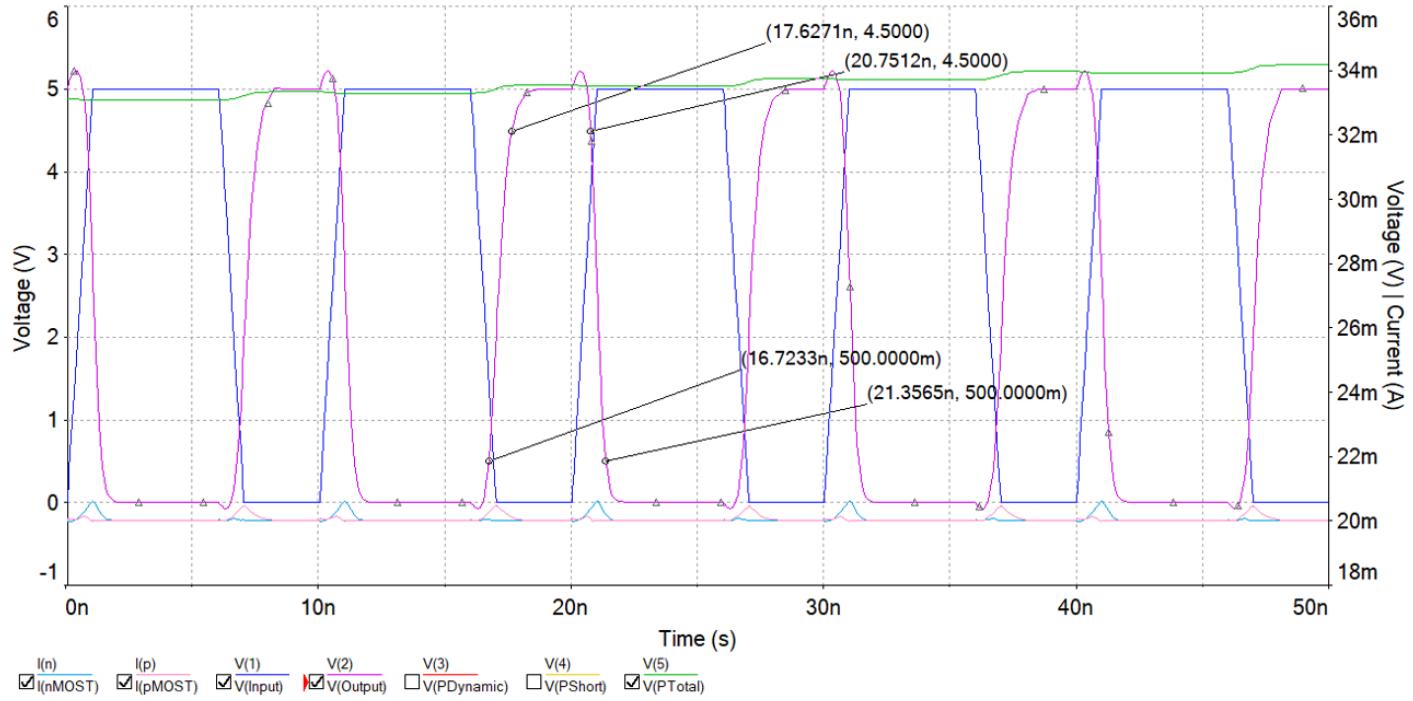


Figure 12 Input and Output signal, Drain current of p-MOST and n-MOST, and Power Dissipation.

- c) Plot the dynamic and short circuit power, show and explain your circuit (include a circuit diagram) and explain your results and discuss how it relates to 2a)

[10/100]

In Figure 13, P_{dyn} represents the dissipation associated with the capacitor being charged through the pMOS transistor and discharged through the nMOS transistor. Hence this component is directly related to the circuit capacitance (C_L), the square of the supply voltage, and the clock frequency (switching activity) (f_{clk}) as denoted by the formula:

$$\begin{aligned} P_{dyn} &= C_L V_{DD}^2 f_{clk} \\ &= 66.6 \text{ f} * 5 * 5 * 100 \text{ M} \\ &= 167 \mu\text{W} \end{aligned}$$

From Figure 14, the dynamic power is $179-15 = 164 \mu\text{W}$.

Short circuit power in integrated circuit design refers to the power dissipated when both the pMOS and nMOS transistors are partially turned on simultaneously, causing a temporary direct connection between the power supply and ground.

$$\begin{aligned} P_{sc} &= V_{DD} I_{max} f_{clk} \frac{(t_r + t_f)}{2} \\ &= 5 * 470 \mu\text{A} * 10 \text{n} * (85 + 65) \text{p} / 2 = 17.6 \mu\text{W} \end{aligned}$$

From Figure 14, the short circuit power is $21.0622 - 21.0476 = 0.0146 \text{ mW} = 15 \mu\text{W}$.

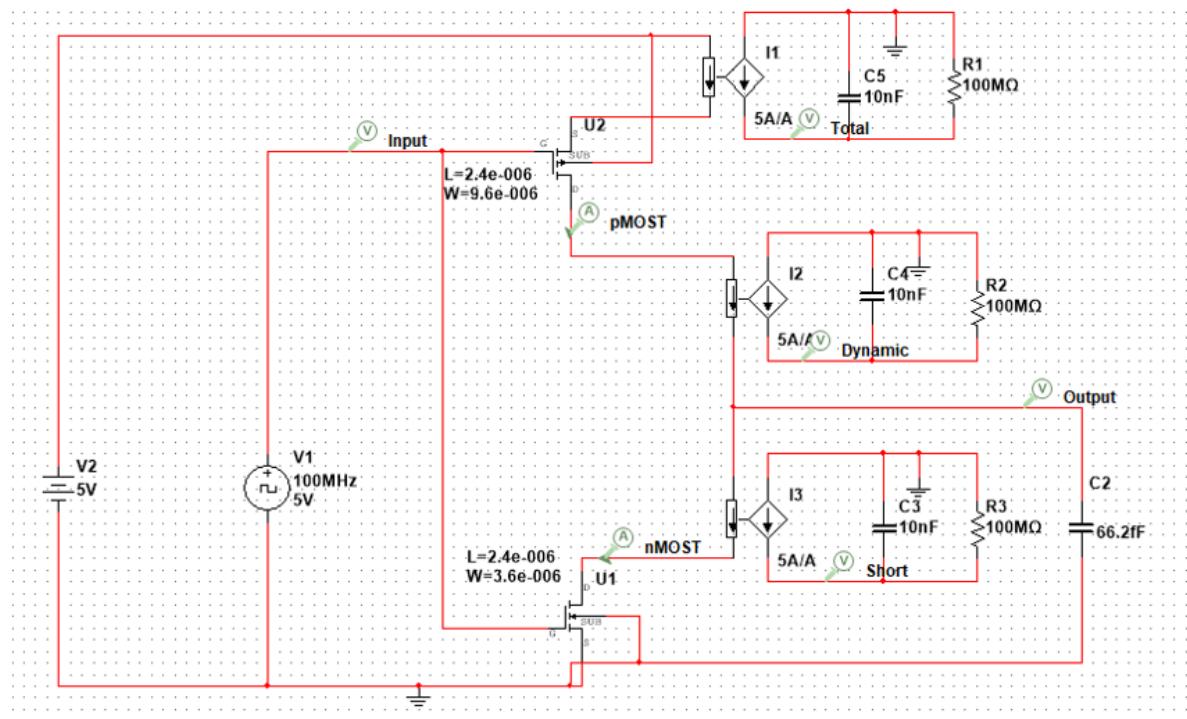


Figure 13 Circuit diagram of power measurement.

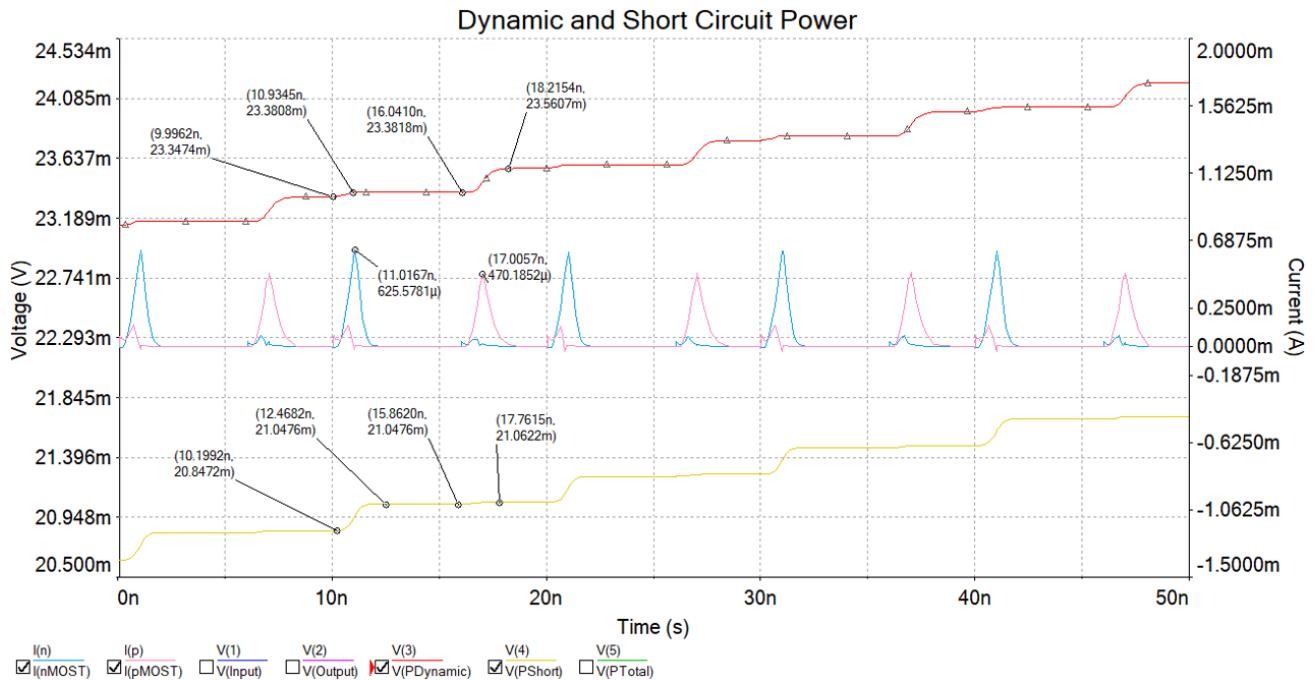


Figure 14 Drain current of p-MOST and n-MOST, Dynamic and Short Circuit Power.

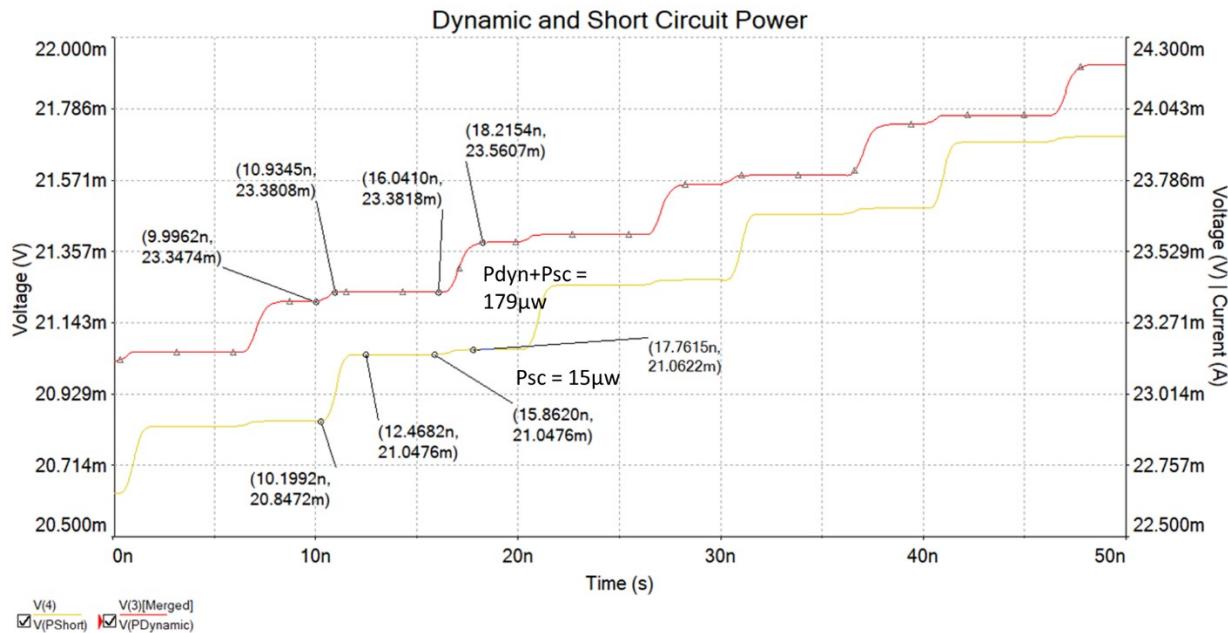


Figure 15 Dynamic and Short Circuit Power.

- d) Plot the power consumption at a lower frequency and put the results into context to above.

[5/100]

Figure 16 and Figure 17 provide insights into power consumption dynamics at lower frequencies, specifically 50 MHz and 1 MHz. In both figures, the yellow line, representing short circuit power, closely mirrors the behaviour of the magenta line, which indicates dynamic power.

At lower frequencies, such as 1 MHz, the overall switching activity decreases due to the reduced frequency of voltage changes. As a result, the contribution of dynamic power to the total power consumption diminishes. Conversely, short circuit power, which is associated with the transient current flow during transistor switching, becomes relatively more significant in influencing the overall power consumption.

In Figure 16 and Figure 17, the proximity of the yellow and magenta lines at 1 MHz compared to 50 MHz highlights this shift in power consumption dynamics. At lower frequencies, the dominance of short circuit power becomes more pronounced, leading to a convergence of the two power components. This observation underscores the importance of considering frequency-dependent power consumption characteristics when designing and optimizing circuits, especially in applications where lower frequencies are prevalent.

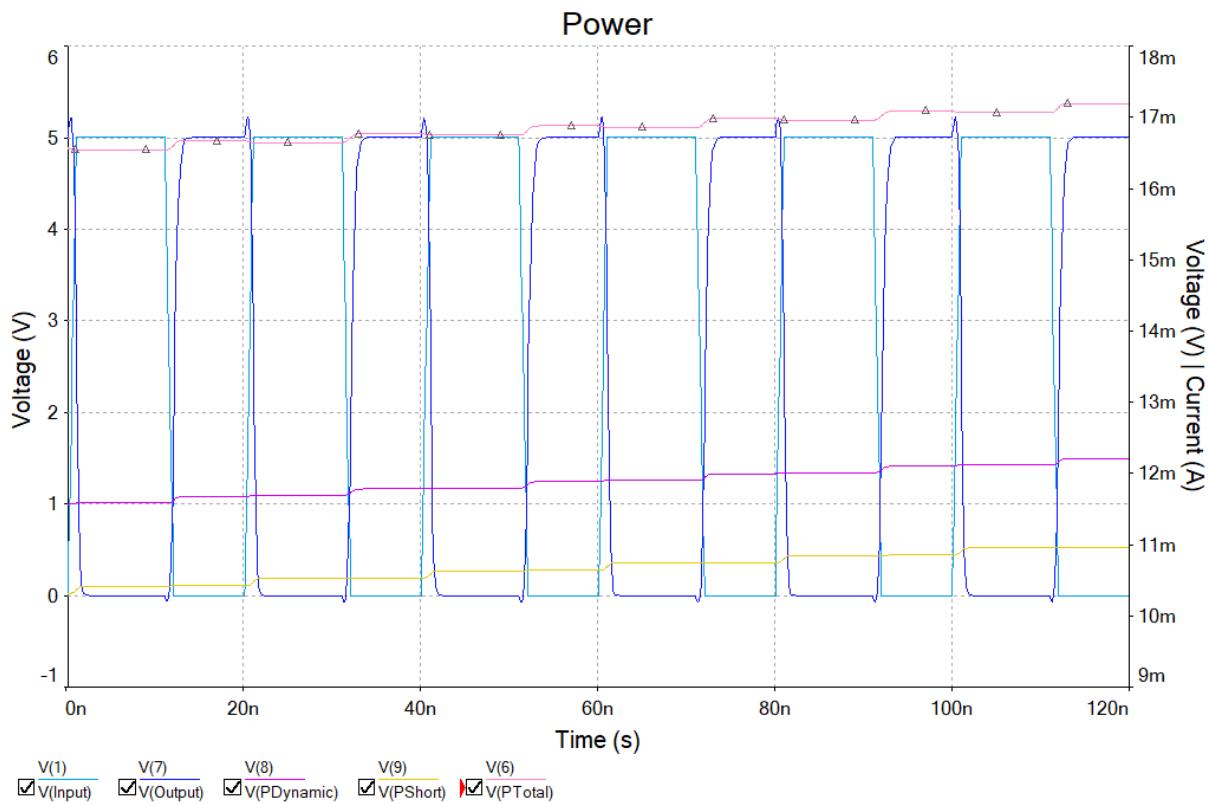


Figure 16 Power consumption at a lower frequency ($f = 50\text{MHz}$)

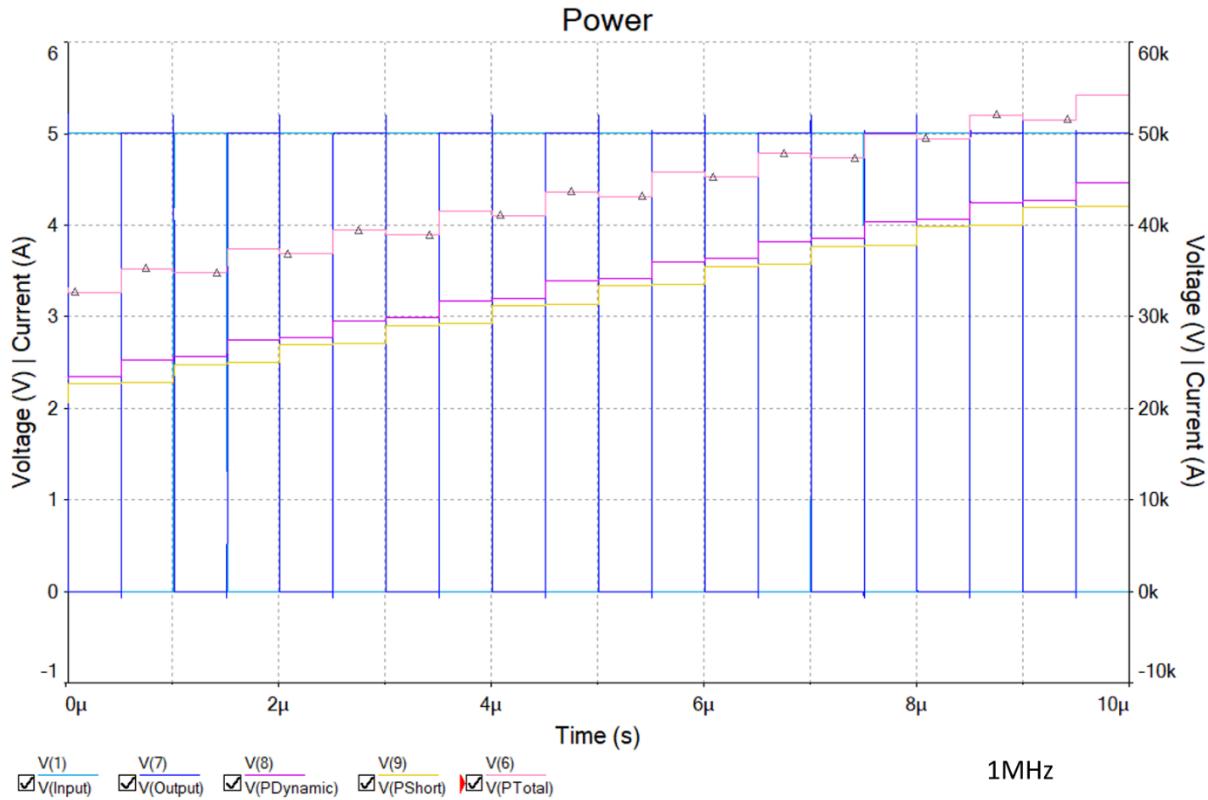


Figure 17 Power consumption at a lower frequency ($f = 1\text{MHz}$)



Section 3: Design and investigate the DC and transient response of a 2-input NAND gate by analysis and simulation.

- a) The two pMOS widths are to be equal to the number assigned to you and the length of $2.4 \mu\text{m}$. The two nMOS should have a width of $4.8 \mu\text{m}$ and a length of $2.4 \mu\text{m}$. Perform DC and transient simulations. Look at any internal nodes as well.

[5/100]

nMOS have a width of $4.8 \mu\text{m}$ and a length of $2.4 \mu\text{m}$ so $\beta_n = 0.19 \text{ mA/V}^2$.

pMOS have a width of $9.6 \mu\text{m}$ and a length of $2.4 \mu\text{m}$ so $\beta_p = 0.12 \text{ mA/V}^2$.

Because of β_p is less than β_n so the rise time, which is controlled by the pMOS would be slower than the fall time, which is controlled by the nMOS as shown in Figure 18 that the rise times of transient analysis are 603 and 776 ps which is slower than the fall times (which are 470 and 573 ps).

Furthermore, in the NAND gate, two input voltages with different frequencies (50 MHz and 100 MHz) are present. Therefore, the period for the first input is 10 ns, while the period for the second input is 20 ns. Consequently, there are instances where the first input transitions from high (5V) to low (0V) while the second input remains high (5V) (occurs around 10 ns to 20 ns in Figure 18, resulting in voltage dropping. This phenomenon is due to additional rise and fall times (yellow and purple lines). Such occurrences repeat every 20 ns, noticeable during 30 ns, 50 ns, and 70 ns intervals.

The overshoot is calculated as 8.7%, while the undershoot is 1.4%. Within the internal circuitry, the voltage is approximately half of the output voltage. This phenomenon occurs because the widths of the nMOS are identical, aligning closely with theoretical expectations where the internal voltage typically shares nearly half of the output voltage.

Figure 19 represents the DC simulation of a NAND gate with p-MOST width = $9.6 \mu\text{m}$ and n-MOST width = $4.8 \mu\text{m}$. There is a shift in the switching threshold voltage from $VDD/2$ (which is 2.5 V) to the left. Due to the NAND gate configuration, there are two voltage frequencies (100 MHz and 50 MHz). When the V_{in} of 50MHz is 5 V, the V_{in} of 100 MHz shifts to 2.2 V. Conversely, when the V_{in} of 100MHz is 5 V, the V_{in} of 50 MHz shifts to 2.35 V.

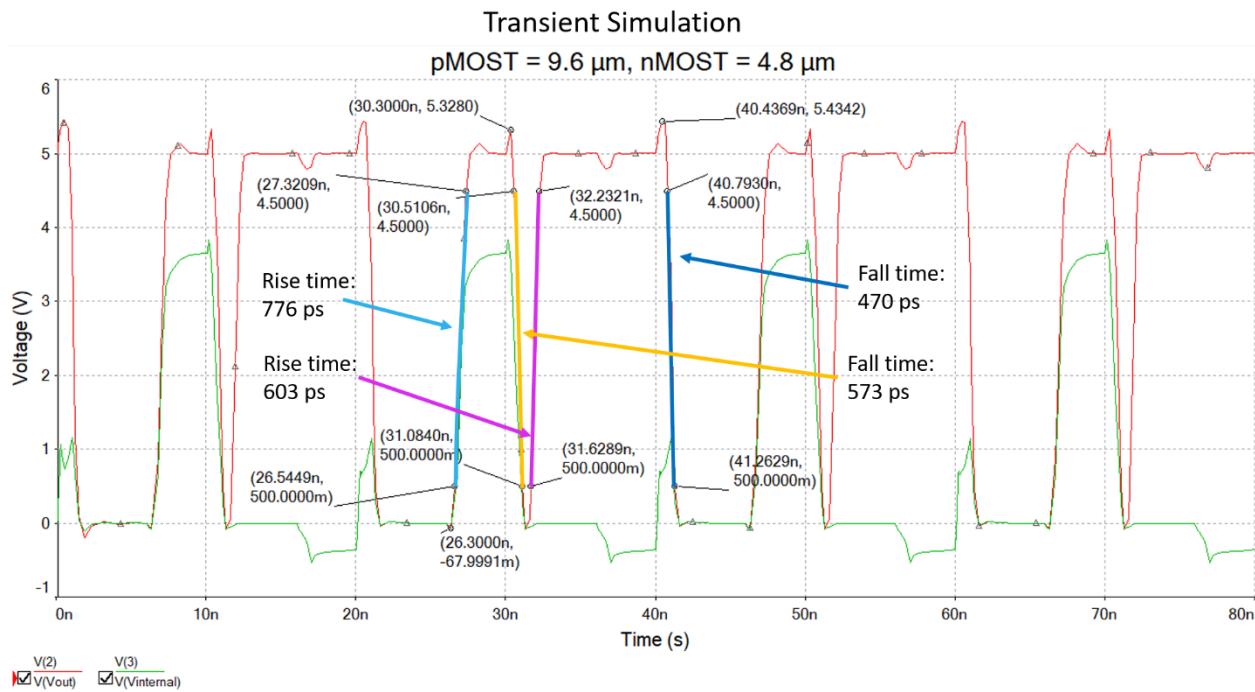


Figure 18 Transient Simulation of NAND Gate with p-MOST width = 9.6 μm and n-MOST width = 4.8 μm .

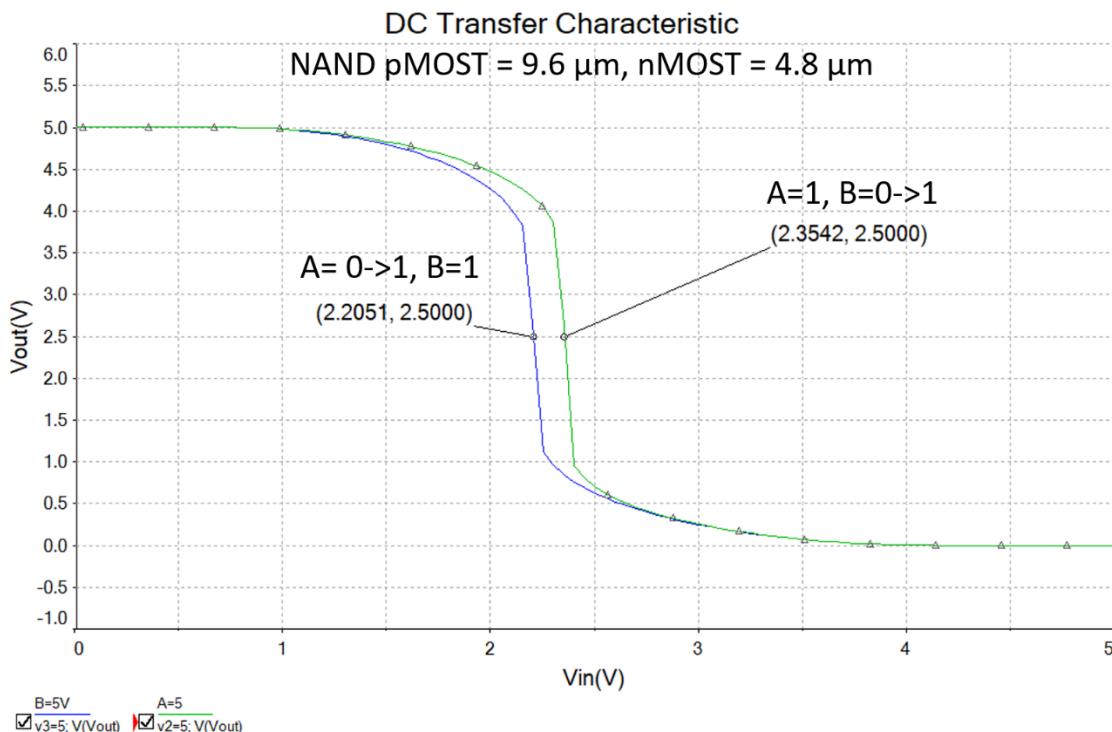


Figure 19 DC Simulation of NAND Gate with p-MOST width = 9.6 μm and n-MOST width = 4.8 μm .



- b) Investigate the rise/fall times when the width of both pMOSFs and the widths of each nMOSF are varied. Document with simulation screenshots and relevant parameters.

[5/100]

Figures 20 and 21 depict transient simulations of a NAND gate. In these simulations, the p-MOSF width remains constant at 9.6 μm , while the n-MOSF width varies incrementally from 2.4 μm to 10.8 μm , with a step size of 1.2 μm , for both rise time and fall time analysis. Figure 22 and Table 2 provide a summary of the rise time and fall time results. It is observed that the rise time, primarily influenced by the width of the p-MOSF (which remained constant throughout the experiment), mostly remains consistent at around 700-750 ps. However, there may be instances where the rise time exceeds this range, possibly due to current from the n-MOSF (despite theoretical expectations of no n-MOSF current during rise time analysis). Conversely, in the fall time analysis, increasing the width of the n-MOSF results in reduced fall times. This phenomenon is attributed to the larger width leading to a higher beta value, as explained in section 1e), consequently yielding faster fall times.

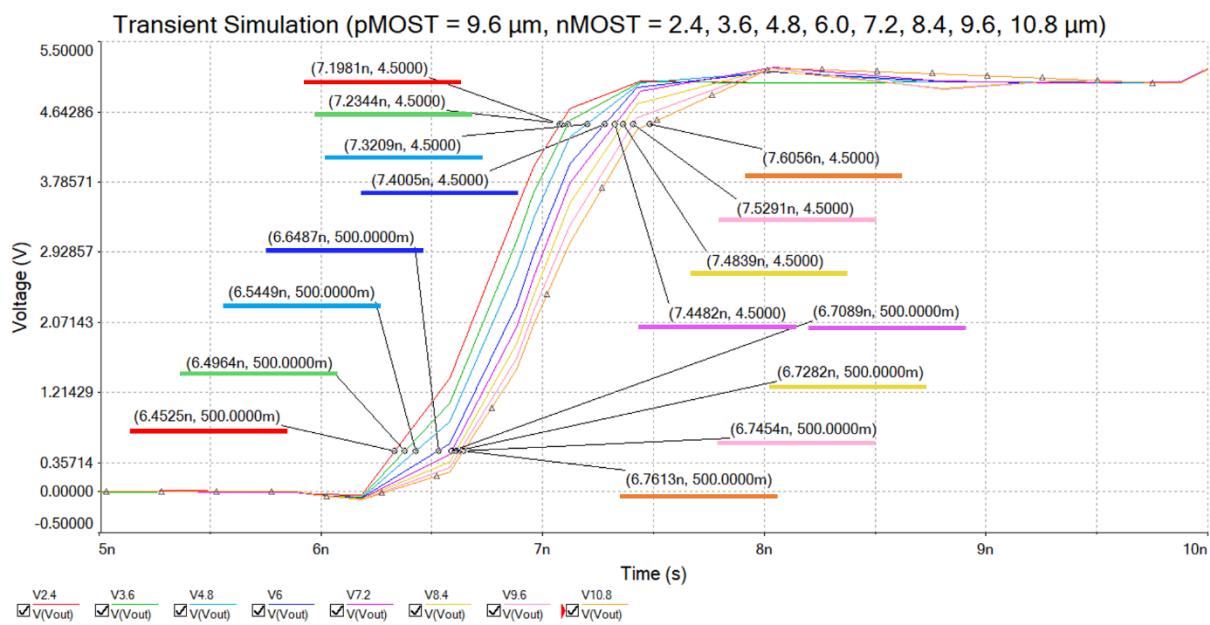


Figure 20 Transient Simulation of NAND Gate with p-MOSF width = 9.6 μm and n-MOSF width = 2.4, 3.6, 4.8, 6.0, 7.2, 8.4, 9.6, and 10.8 μm (Rise time).

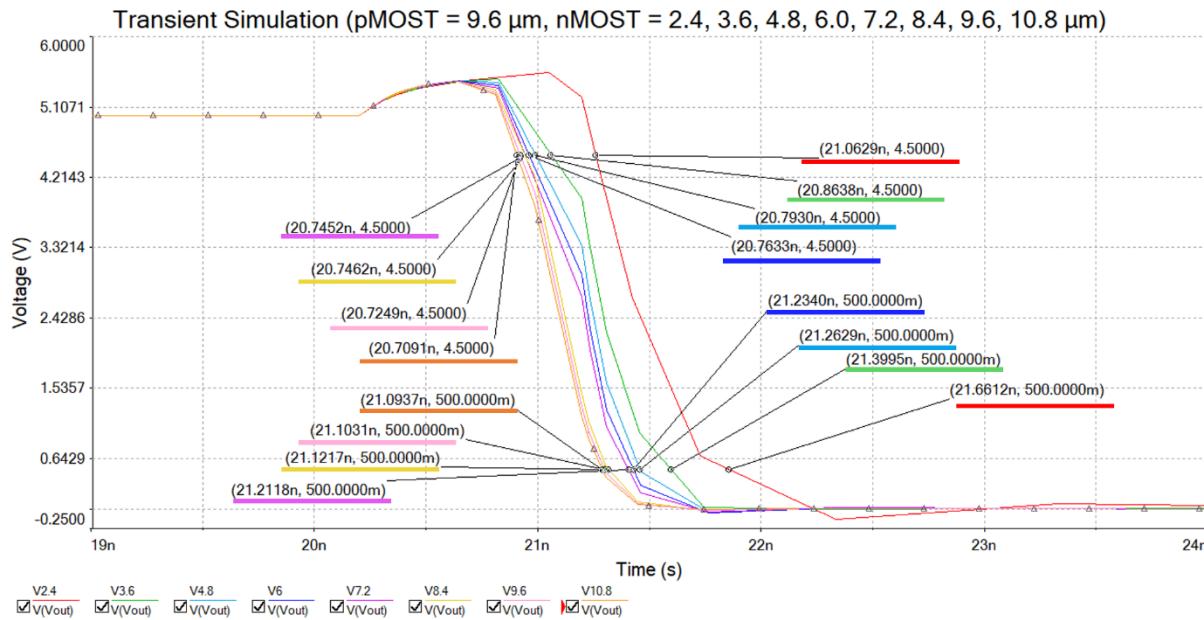


Figure 21 Transient Simulation of NAND Gate with p-MOST width = 9.6 μm and n-MOST width = 2.4, 3.6, 4.8, 6.0, 7.2, 8.4, 9.6, and 10.8 μm (Fall time).

Table 2 Fall time & Rise time of NAND gate as function of nMOS width.

nMOS width (μm)	10.8	9.6	8.4	7.2	6	4.8	3.6	2.4
fall time (ps)	384.6	378.2	375.5	466.6	470.7	470.0	535.7	598.3
rise time (ps)	844.3	783.7	755.7	739.3	751.8	776.0	738.0	745.6

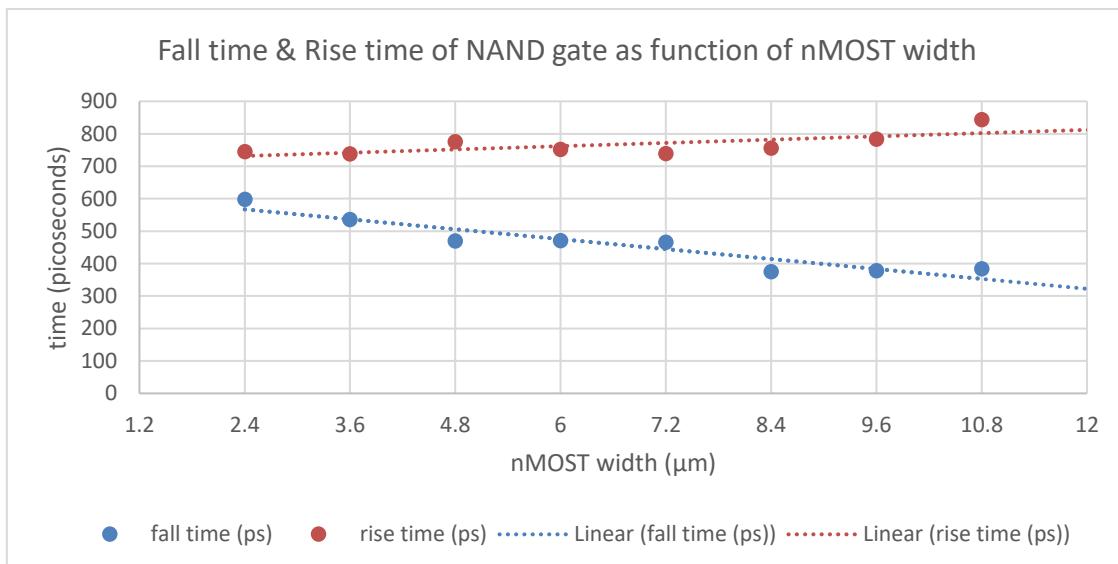


Figure 22 Fall time & Rise time of NAND gate as function of n-MOST width.

- c) Repeat the above and adjust the value of the load capacitance C_L to compensate for the different widths of the new transistors. Use your script from assignment 1 to calculate an appropriate load capacitance. Document with simulation screenshots and relevant parameters.

[5/100]

In the script from assignment 1, the load capacitance (C_L) is calculated for the inverter circuit. However, in the NAND gate configuration, the nMOSFs are arranged in series, while the pMOSFs are connected in parallel. Consequently, the new value of C_L is determined to be 58.1 fF.

In Figure 23, the transient analysis compares the rise time and fall time for a circuit. The rise time measures 1.9 ns, while the fall time is 1.7 ns. The overshoot is calculated as 6.5%, while the undershoot is 0.6%. Additionally, voltage drops are observed in the simulation due to the switching voltage of the two inputs, as indicated by the red arrows in Figure 23. The input voltages (A and B) are offset by -5V on the y-axis for easy visualization.

As evident, when altering the load capacitance, the dropping voltage decreases (when A is high and B changes to low) compared to scenario 3a).

The DC simulation of a NAND gate with a p-MOST width of 9.6 μm and an n-MOST width of 4.8 μm , utilizing the new capacitance value of 58.1 fF, yields the same switching voltage as observed in scenario 3a.

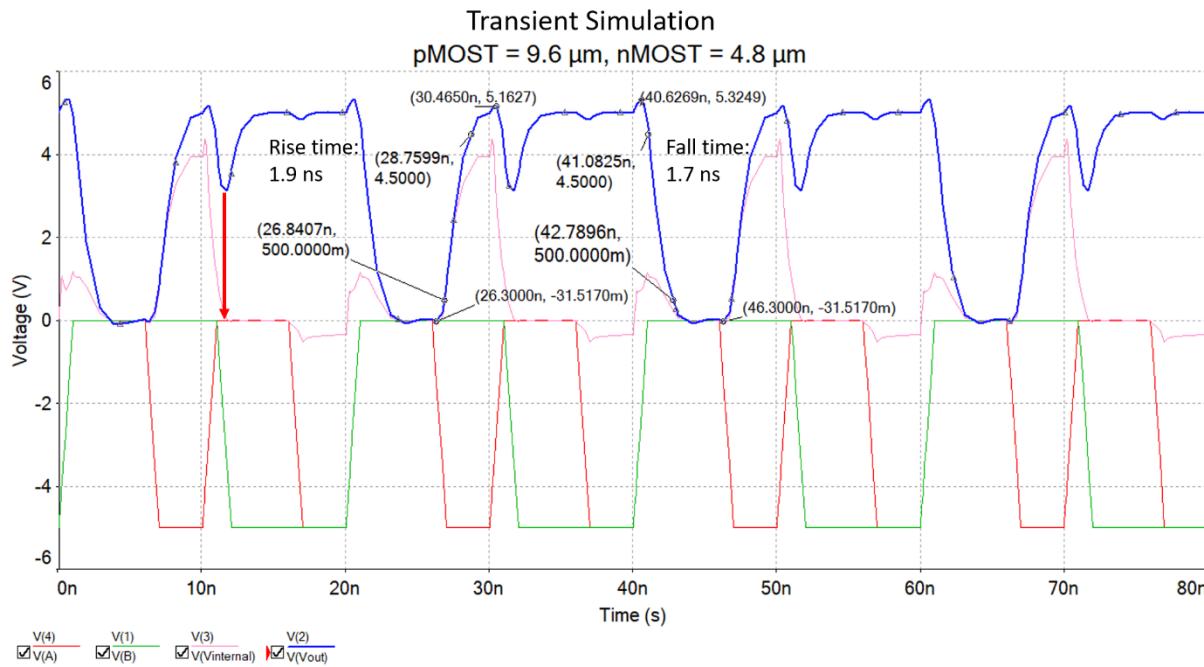


Figure 23 Transient Simulation of NAND Gate with p-MOST width = 9.6 μm and n-MOST width = 4.8 μm .

- d) Modify the nMOS width to design a ‘matched’ NAND gate. Document with simulation screenshots and relevant parameters. Discuss how you achieved matching.

[5/100]

In the NAND gate configuration, the nMOS transistors are arranged in series, while the pMOS transistors are connected in parallel. Due to this arrangement, there are no series connections in the pMOS transistors. Consequently, the formula: $\mu_p * W_p / L_p = \mu_n * W_n / L_n$ remains applicable for maintaining the balance between the transistors' dimensions.

Given that the nMOS transistor has a width of 2.92 μm , and rounding up to meet the minimum feature size of 1.2 μm to 3.6 μm .

In Figure 25, the transient analysis compares the rise time and fall time for a circuit. The rise time measures 1.8 ns, while the fall time is 1.9 ns. The overshoot is calculated as 7%, while the undershoot is 0.5%. Additionally, voltage drops are observed in the simulation due to the switching voltage of the two inputs, as indicated by the red arrows in Figure 25. The input voltages (A and B) are offset by -5V on the y-axis for easy visualization.



Figure 26 represents the DC simulation of a NAND gate for a matched design with p-MOST width = 9.6 μm and n-MOST width = 3.6 μm . There is a shift in the switching threshold voltage from VDD/2 (which is 2.5 V) to the left. Due to the NAND gate configuration, there are two voltage frequencies (100 MHz and 50 MHz). When the Vin of 50 MHz is 5 V, the Vin of 100 MHz shifts to 2.3 V. Conversely, when the Vin of 100 MHz is 5 V, the Vin of 50 MHz shifts to 2.49 V.

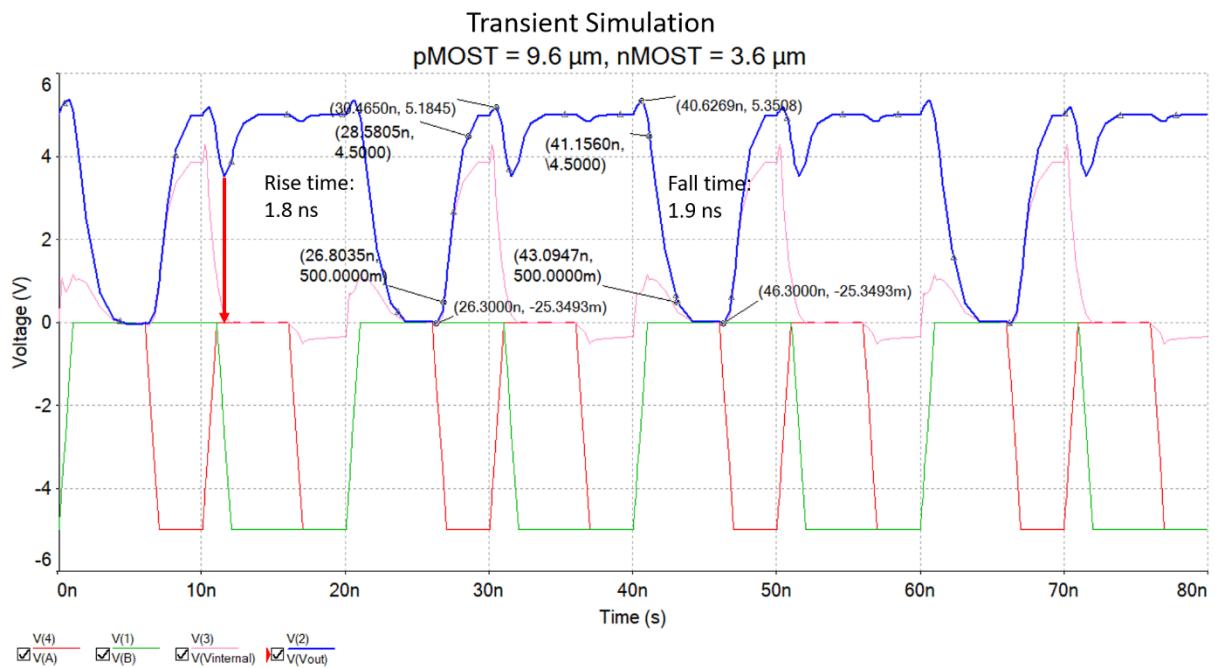


Figure 24 Transient Simulation of NAND Gate for matched device
(p-MOST width = 9.6 μm and nMOS width = 3.6 μm .)

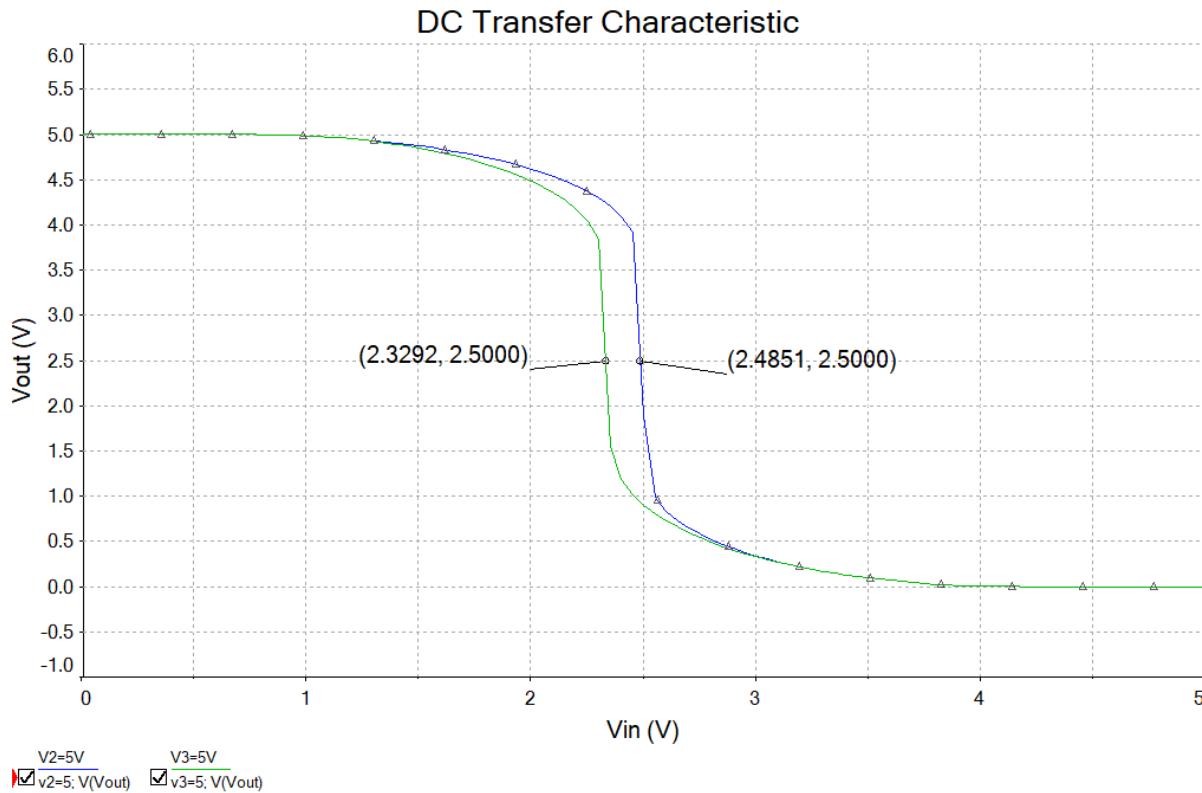


Figure 25 DC Simulation of NAND Gate with matched design
(p-MOST width = 9.6 μm and n-MOST width = 3.6 μm).

- e) Discuss the performance of your circuit and how different transistor widths affect it.

[5/100]

Given β represents the aspect ratio of the transistor (μ^*W/L) where μ is the mobility, W is the width, and L is the length of the transistor. When β of n-MOST is smaller, the fall time become slower. Comparing scenario 3c), where both nMOS have a width of 4.8 μm , to scenario 3d), where both nMOS have a width of 3.6 μm , the fall time of the design is slower, increasing from 1.7 ns to 1.9 ns. Therefore, increasing the width of the nMOS transistor will result in faster fall times, similar to an inverter configuration. Additionally, upon comparing the DC simulation, it is evident that the matched nMOS width yields a better switching voltage, nearly reaching 2.5V.

In summary, the choice of transistor widths significantly impacts the overall performance, speed, power consumption, signal integrity, and robustness of the circuit.



f) Discuss the influence of the load capacitance on the circuit performance.

[5/100]

The load capacitance (C_L) plays a crucial role in determining the performance characteristics of the circuit. Here are some key points discussing its influence:

1. Signal Propagation Delay: The load capacitance directly affects the signal propagation delay in the circuit. A larger load capacitance results in a longer propagation delay because it takes more time to charge and discharge the capacitance. This can lead to slower overall circuit speed.
2. Power Consumption: The load capacitance contributes to the dynamic power consumption of the circuit. Charging and discharging the capacitance during signal transitions require energy, leading to increased power consumption, particularly in high-frequency circuits where these transitions occur frequently.
3. Signal Integrity: The load capacitance affects signal integrity by influencing voltage levels and noise margins. Higher load capacitance can cause voltage droops or overshoots, leading to signal distortion and reduced noise margins. This can impact the reliability and robustness of the circuit, especially in high-speed or high-frequency applications.
4. Slew Rate: The load capacitance affects the slew rate of the output signal, which is the rate of change of voltage with respect to time. A larger load capacitance results in a slower slew rate because it requires more time to change the voltage across the capacitance.
5. Frequency Response: The load capacitance also affects the frequency response of the circuit. Higher load capacitance can cause a decrease in the bandwidth of the circuit, limiting its ability to operate effectively at higher frequencies.

In summary, the load capacitance has a significant impact on various aspects of circuit performance, including speed, power consumption, signal integrity, slew rate, and frequency response. Therefore, careful consideration and optimization of the load capacitance are essential for achieving the desired performance characteristics in electronic circuits.



- g) In assignment 1, you calculated the capacitance of an inverter, and discuss why this model is still appropriate for a NAND gate.

[5/100]

In assignment 1, the capacitance of an inverter was calculated to understand its behaviour under different conditions. Despite being a different logic gate, the model developed for the inverter remains applicable for a NAND gate due to certain similarities in their underlying principles. Both gates involve the charging and discharging of capacitors during switching operations. In the case of a NAND gate, although the internal configuration differs (with nMOS in series and pMOS in parallel), the fundamental behaviour of capacitive charging and discharging remains consistent. Therefore, the model developed for the inverter can be effectively adapted and remains appropriate for analysing the operation of a NAND gate. For the NOR gate configuration, the width of pMOS needs to be multiplied by 2 to account for the number of series connections of pMOS, as illustrated in Figure 23.

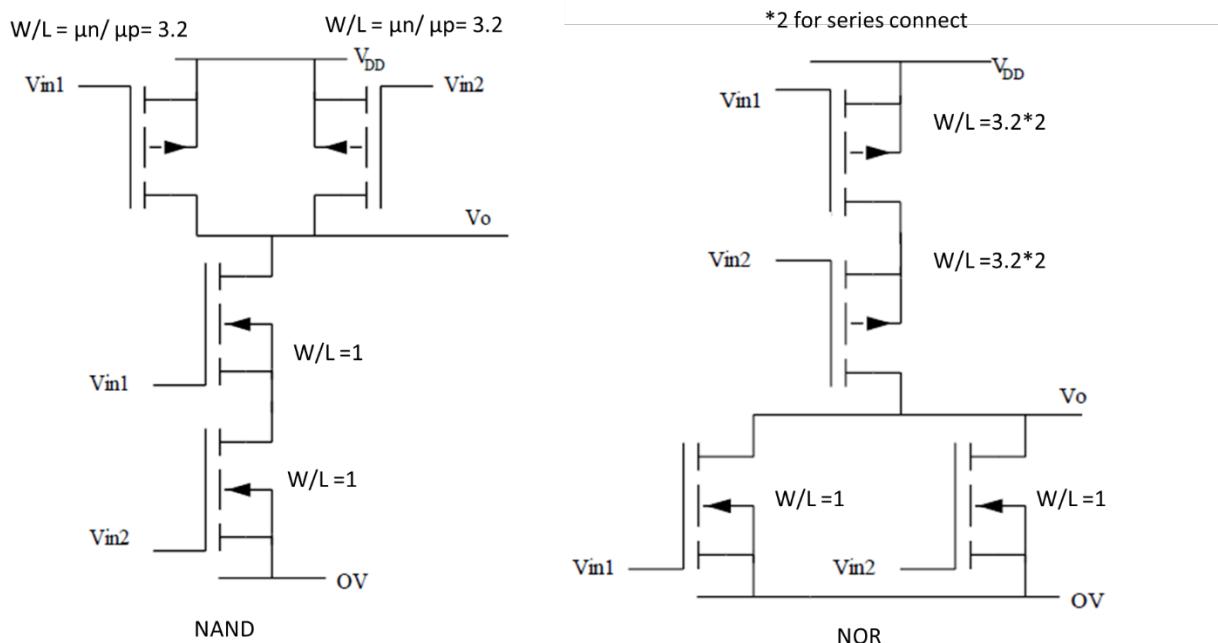


Figure 26 Comparison of NAND and NOR gate.