Sound Steering FPGA RTL (FSM)

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States and transitions:

- Otherwise (A - Reset)
- A - Reset — en = '1' → B - ADC Init
- Otherwise (B - ADC Init)
- B - ADC Init — counter_done = '0' → J - ADC Init Buffer
- Otherwise (J - ADC Init Buffer)
- J - ADC Init Buffer — counter_done = '1' → C - Idle
- Otherwise (C - Idle)
- ** reconfig = '1' — User requested a reconfig of ADC
- * reg_read = '1' — User requested a readback from ADC
- *** flag = '1' — User requested a channel change
- counter_done = '1' and reg_read = '0'

- F - ADC Reg Read — Otherwise
- F - ADC Reg Read — counter_done = '1' → G - Reg Read Buffer
- Otherwise (G - Reg Read Buffer)
- G - Reg Read Buffer — counter_done = '0' → L - Reg Read Buffer 2
- Otherwise (L - Reg Read Buffer 2)
- L - Reg Read Buffer 2 — counter_done = '1' → M - NOP
- Otherwise (M - NOP)
- M - NOP — counter_done = '0' → N - Reg Read Exit
- Otherwise (N - Reg Read Exit)

- ADC Running Loop
- C - Idle — en = '1' && fifo_full = '1' && flag = '0' → D - ADC Run
- Otherwise (D - ADC Run)
- D - ADC Run — counter_done = '1' → E - ADC Run Buffer
- Otherwise (E - ADC Run Buffer)
- E - ADC Run Buffer — counter_done = '0' → K - ADC Check Stop
- E - ADC Run Buffer — elsif counter_done = '1' → (loop)
- (en = '0' or flag = '1') and counter_done = '1'

- H - Init Refill FIFO — Unconditional → I - Refill Loop
- Otherwise (I - Refill Loop)
- I - Refill Loop — fifo_full = '1'

-- FSM System Input Ports
clk
rstn

-- FSM Control Inputs From Datapath
counter_done
fifo_full
flag
reg_read
reconfig
en

-- FSM Control Outputs to Datapath
sda_reg_clr
adc_en
gpio_level
rom_strobe
sdi_sel
shiftreg_clr
flag_ack
fan_pwm_en
tx_active_pwm_en
heartbeat_pwm_en
state

NOTE:

At idle state, state D has highest priority, followed by state H (refill FIFO after channel change), then state A (reconfig ADC), then state F (readback of ADC register contents). The flag signal is set by changing the audio channel through the AXI register interface, whereas the other two signals correspond directly to AXI register bits. They should be set concurrently as the device is disabled (see AXI register map).

The RTL design is such that FSM burden is minimized. The majority of necessary synchronization is ensured by the components in the datapath.