SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-572103

(An Autonomous Institute under Visvesvaraya Technological University, Belagavi)

Project Report on

"LOW POWER COMPARATOR USING CADENCE TOOL"

submitted in partial fulfillment of the requirement for the completion of VI semester of

BACHELOR OF ENGINEERING

in

ELECTRONICS & COMMUNICATION ENGINEERING

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SIDDAGANGA INSTITUTE OF TECHNOLOGY, TUMAKURU-572103

(An Autonomous Institute under Visvesvaraya Technological University, Belagavi)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

CERTIFICATE

Certified that the mini project work entitled "DESIGN, SIMULATION AND ANALYSIS OF LOW POWER COMPARATOR USING CADENCE TOOL " is bonafide work carried out by AAISH KUMAR BARBIGAHIYA (1SI21EC001), KUMAR HARSH (1SI21EC050), NARENDRA KUMAR JHA (1SI21EC062) and SUMAN KUMAR (1SI21EC097) in partial fulfillment for the completion of VI Semester of Bachelor of Engineering in Electronics & Communication Engineering from Siddaganga Institute of Technology, an autonomous institute under Visvesvaraya Technological University, Belagavi during the academic year 2023-24. It is certified that all corrections/suggestions indicated for internal assessment have been incorporated in the report deposited in the department library. The Mini project report has been approved as it satisfies the academic requirements in respect of project work prescribed for the Bachelor of Engineering degree.

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1.

2.

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Course Outcomes

CO1: To identify a problem through literature survey and knowledge of contemporary engineering technology.

CO2: To consolidate the literature search to identify issues/gaps and formulate the engineering problem.

CO3: To prepare a project schedule for the identified design methodology and engage in budget analysis, and share responsibility for every member in the team.

CO4: To provide a sustainable engineering solution considering health, safety, legal, and cultural issues and also demonstrate concern for the environment.

CO5: To identify and apply the mathematical concepts, science concepts, engineering, and management concepts necessary to implement the identified engineering problem.

CO6: To select the engineering tools/components required to implement the proposed solution for the identified engineering problem.

CO7: To analyze, design, and implement an optimal design solution, interpret the results of experiments, and draw valid conclusions.

CO8: To demonstrate effective written communication through the project report, the one-page poster presentation, and preparation of the video about the project and the four-page IEEE/Springer paper format of the work.

CO9: To engage in effective oral communication through a power point presentation and demonstration of the project work.

CO10: To demonstrate compliance with the prescribed standards/ safety norms and abide by the norms of professional ethics.

CO11: To perform in the team, contribute to the team and mentor/lead the team.

CO-PO Mapping

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO-1												3		3
CO-2		3											3	
CO-3											3			3
CO-4						3	3							3
CO-5	3	3											3	
CO-6					3									3
CO-7			3	3									3	
CO-8										3				3
CO-9										3				3
CO-10								3						3
CO-11									3					3

Attainment level: 1: Slight (low) 2: Moderate (medium) 3: Substantial (high)

POs: PO1: Engineering Knowledge, PO2: Problem analysis, PO3: Design/Development of solutions, PO4: Conduct investigations of complex problems, PO5: Modern tool usage, PO6: Engineer and society, PO7: Environment and sustainability, PO8: Ethics, PO9: Individual and team work, PO10: Communication, PO11: Project management and finance, PO12: Lifelong learning

Abstract

The importance of low-power comparators is evident in numerous everyday applications, from digital circuits and processors to consumer electronics and automotive systems. They facilitate precise decision-making and signal processing while conserving energy. Without low-power comparators, many modern conveniences would not function efficiently. For instance, microprocessors would face challenges with sorting and decision-making, and devices such as thermostats, battery chargers, and digital clocks would lack essential comparative functions. Efficient and accurate low-power comparators are crucial in digital systems, highlighting the need to optimize their design for improved performance and energy efficiency.

The main objective of this project is to design, analyze, and compare different adder architectures specifically Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Increment Adder (CIA) based on power consumption, delay, and area. The chosen adder design will be used to develop a 32-bit comparator optimized for minimal area, delay, and power consumption. Using the Cadence tool suite, Verilog code will be simulated with Incisive to analyze output waveforms and functionality, while Genus will calculate power consumption and area. The layout of the 32-bit comparator will also be created. The final optimized 32-bit comparator design will be validated through simulation and demonstrated on a Spartan 6 FPGA board with a 16-bit comparator, showcasing its practical applicability. This approach ensures thorough evaluation and optimization of the comparator design, effectively addressing key performance metrics.

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Chapter 1

Introduction

This chapter outlines the project's motivation, objectives, and the organization of the report. It provides a foundational understanding of the project's purpose and scope, setting the stage for the detailed exploration that follows.

The design of low-power comparators is crucial in modern digital systems for efficiency and sustainability. They are vital in portable devices, wearable technology, and battery-operated electronics, where minimizing energy consumption enhances device longevity and performance. In high-performance computing and embedded systems, low-power comparators ensure precise decision-making and signal processing while conserving energy, achieving optimal performance without compromising power efficiency.

This project aims to design, analyze, and compare low-power adder architectures for a 32-bit comparator. Using Cadence tools, Verilog code will be simulated with Incisive to verify functionality, and Genus will be used to measure power consumption and area. The optimized design will undergo simulation and validation. Additionally, a 16-bit version will be demonstrated on a Spartan 6 FPGA board to showcase practical applicability. This approach ensures thorough evaluation and optimization of the comparator, focusing on key metrics like area, delay, and power consumption. .

1.1 Motivation

Modern systems require efficient comparators for tasks such as sorting data and comparing memory addresses. The rapid advancements in technology and the increasing demand for high-performance digital systems motivate the design of an optimized 32-bit comparator.

Comparators play a crucial role in ensuring accurate decision-making and signal processing, thereby enhancing overall circuit performance. By focusing on reducing power consumption, delay, and area, this project aims to improve the efficiency and performance of digital circuits.

Inspired by the industry's push towards low-power and high-speed digital components, this project seeks to develop a faster, more reliable, and energy-efficient 32-bit comparator.

Using the Cadence tool suite for comprehensive evaluation, the goal is to meet the growing demands of modern technology with an innovative design.

1.2 Objectives of the project

The objectives of this project are as follows:

a) Simulation and comparison of three different full adders.

b) Design and simulation of a 32-bit comparator using the best chosen adder.

c) Analysis of area, power, and delay of the 32-bit comparator.

d) Implementing a 16-bit comparator on a Spartan-6 FPGA board.

1.3 Organisation of the report

The report is divided into 7 Chapters . Chapter 1 introduces the project's Motivation, Objectives, and Organization, followed by Chapter 2's Literature Survey on comparator design and adder architectures. Chapters 3 to 5 detail the Design Methodology, Hardware and Software components, and experimental setup using the SPARTAN 6 FPGA BOARD. Chapter 6 presents the Results, including simulations, synthesis, and FPGA implementation, while Chapter 7 concludes with findings, implications, and future research directions.

Chapter 2

Literature Survey

This chapter reviews existing research on low power comparator design and adder architectures. It provides context and background for the project's contributions, highlighting gaps and opportunities in the current body of knowledge.

The analysis of low power consumption in 32-bit comparators was simulated in different process technologies using the Cadence tool. A new method of implementation was done on comparators by adding an additional balancing circuitry to reduce power consumption [1].

The hybrid-CMOS full adder, implemented using 90 nm CMOS technology, combines static CMOS, dynamic CMOS, and transmission gate logic to optimize power and delay. This design achieves improved speed and power efficiency compared to conventional CMOS full adders by minimizing critical path delay and optimizing transistor usage. Cadence tools were utilized for simulation and verification [2].

In the implementation results of 10T comparators, the leakage power and leakage current are reduced by 36% and 64%, respectively. The stability during operation is increased by 13% compared to conventional 6T, 7T, 8T, and 9T comparator topologies [3].

The power reduction technique used is the Sleep approach, where the comparator circuit has an additional PMOS transistor placed between VDD and the pull-up network, and an NMOS transistor is placed between the ground and the pull-down network. An overall analysis of static power dissipation shows a significant reduction compared to the original comparator circuits [4].

The novel comparator design suffers from an intrinsic data instability problem due to the direct access of data storage nodes during the operation. To optimize this problem, a comprehensive electrical performance metric is evaluated, comparing the 6T, 7T, 8T, and

9T comparator designs based on process parameters and supply voltage fluctuations [5].

Different comparator topologies (6T, 7T, 8T, 9T, 10T) are compared in terms of leakage current, leakage power, and operational behavior. New emerging technologies have significantly contributed to power reduction in comparator and memory cells: lower charging capacitance due to partial activation of multi-divided arrays and lower operating voltages resulting from external power supply reduction, half-VDD pre-charging, and on-chip voltage down conversion schemes [6].

Process corner analysis has been carried out for 6T, 8T, and 10T comparator cells at various temperatures. The inference drawn from the corner analysis at different temperatures is that the Data Retention Voltage (DRV) value is preferable at SS, TT, and FF for higher temperature ranges, while the corners FS and SF are not preferred for any temperature for DRV estimation [7].

An 8x8 comparator array is designed to accumulate 128 bits. The memory array includes blocks such as arrays of comparator cells, Write Driver Circuits, Revived Circuits, Address Decoders, and Sense Amplifiers. Cadence simulation is performed at 90 nanometer technology [8].

The stability of 6T and 8T comparator cells is compared based on static noise margin, computed using the Cadence Virtuoso Design Environment at 28 nanometer CMOS technology. Cells are operated at two different voltages, 1.05V and 0.5V. Results obtained for Hold margin, Read Margin, and Write Margin at process corner variations indicate that improved noise margin is achieved by reducing the supply voltage [9].

The performance of a low-power, high-speed dynamic comparator designed using 65 nm CMOS technology is evaluated. This design incorporates a double-tail architecture to enhance speed and reduce power consumption. Simulations using the Cadence Virtuoso Design Environment demonstrate that this architecture achieves a lower power-delay product (PDP) and higher robustness under supply voltage variations and process corner variations [10].

2.1 Summary of Literature Survey

The summary of the literature survey has been mentioned below:

Existing research on low power comparator design and adder architectures has highlighted several areas for improvement. Studies on balancing circuitry for comparators have demonstrated significant power reductions but often lack detailed analysis on the impact of these circuits on speed and area utilization. Hybrid-CMOS full adders have shown improved speed and power efficiency by combining different logic styles, yet their complexity and potential for increased area remain challenging. Additionally, while 10T comparators effectively reduce leakage power and current, their intricate design can complicate manufacturing and scaling to smaller process technologies. Techniques such as the Sleep approach for power reduction introduce additional transistors, potentially affecting speed and area. Novel comparator designs face data instability issues, necessitating a comprehensive evaluation of electrical performance metrics. Process corner and temperature analyses have identified configurations that are less suitable for Data Retention Voltage (DRV) estimation, underscoring the need for robust designs.

To address these drawbacks, our methodology incorporates several improvements. We optimize comparator designs by integrating additional balancing circuitry to achieve significant power savings while maintaining speed and area efficiency. By evaluating various adder architectures, such as Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Increment Adder (CIA), we aim to select the best-performing design based on speed, power efficiency, and area utilization. The use of advanced simulation and verification tools like Cadence Incisive, Genus, Innovus, and Xilinx ISE ensures accurate analysis and optimization of the designs. Furthermore, we focus on designing robust comparators that maintain stability across different process corners and temperature variations, enhancing overall reliability and performance. Our comprehensive approach addresses the identified drawbacks, contributing to more efficient and reliable low-power comparator and adder designs.

Chapter 3

System Overview

This chapter discusses the design and experimental methodologies used in the project. It includes a flowchart illustrating the project's workflow, offering a comprehensive overview of the approach taken.

In modern electronics, low power comparators are vital due to their wide-ranging applications, particularly in battery-powered devices, sensors, and digital systems. A comparator is a circuit that compares two voltages or currents and outputs a digital signal indicating which is larger. The importance of low power consumption in these components cannot be overstated, especially in portable and energy-efficient systems.

3.1 Design Methodology

This project follows a structured methodology to design, analyze, and optimize a 32-bit comparator using various adder architectures. Initially, software requirements are identified, utilizing Cadence Incisive for Verilog simulation, Cadence Genus for logic synthesis, Cadence Innovus for physical design and optimization, and Xilinx ISE for FPGA implementation.

The Verilog code development phase involves creating code for Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), and Carry Increment Adder (CIA), as well as for the 32-bit comparator. Simulation is conducted by developing test benches for each design to verify functionality, using Cadence Incisive to simulate and analyze waveform outputs. Implementation focuses on the 32-bit comparator using the CLA architecture, with further simulations to ensure functionality. The synthesis and optimization phase uses Cadence Genus to synthesize the Verilog designs, generating netlists and reports on power consumption and area utilization, followed by an initial performance analysis to identify improvement areas. Finally, the FPGA implementation involves synthesizing and implementing a 16-bit comparator design on the Spartan 6 FPGA board using Xilinx ISE, programming the FPGA, and verifying functionality using LEDs, with comparator outputs mapped to FPGA I/O pins for easy observation.

3.2 32-bit Comparator

A 32-bit comparator is a fundamental digital circuit used to compare two 32-bit binary numbers, A and B, determining their relationship through output signals indicating whether A is greater than, equal to, or less than B. Figure 3.1, the Block Diagram of the 32-bit Comparator using CLA, illustrates its architecture employing a Carry Lookahead Adder (CLA). This advanced design accelerates comparison by predicting carry bits across multiple bits simultaneously, reducing critical path delays crucial for high-speed arithmetic tasks in modern digital systems.The CLA-based comparator optimizes design efficiency by balancing performance, compact area utilization, and minimal power consumption, essential for applications demanding efficient data comparison and decision-making. Figure 3.2 complements this understanding, offering additional insights into the structural and operational details crucial for optimizing the comparator's performance characteristics.

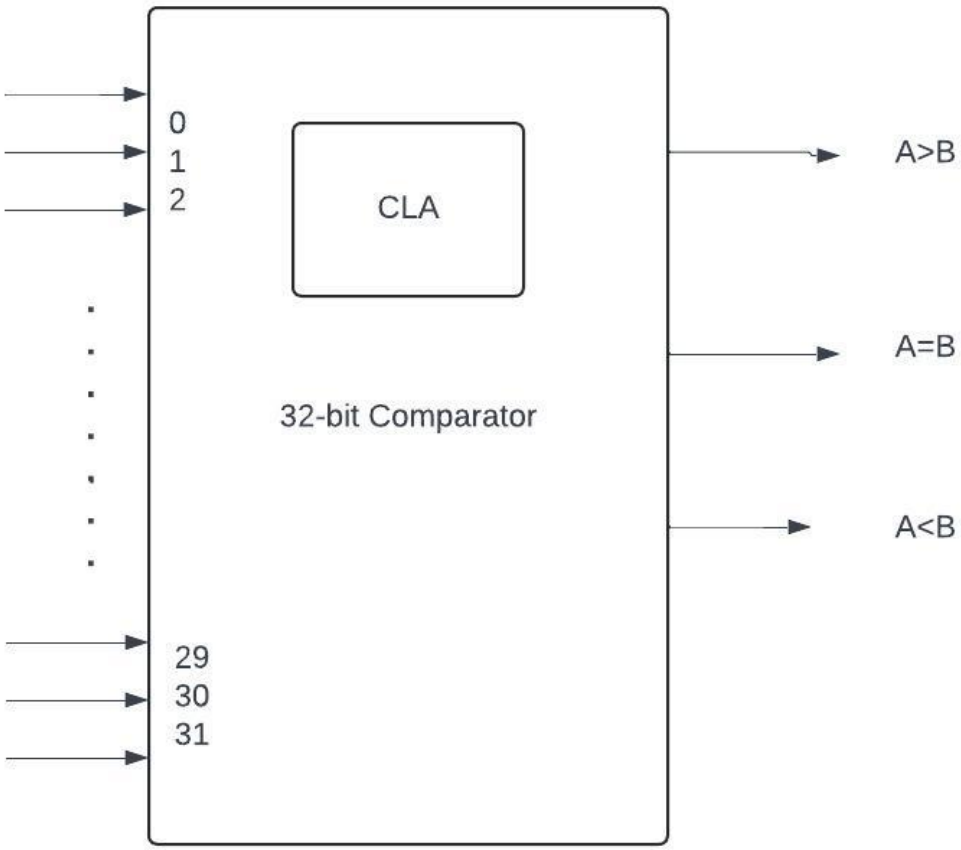


Figure 3.1: Block diagram of 32-bit Comparator using CLA.

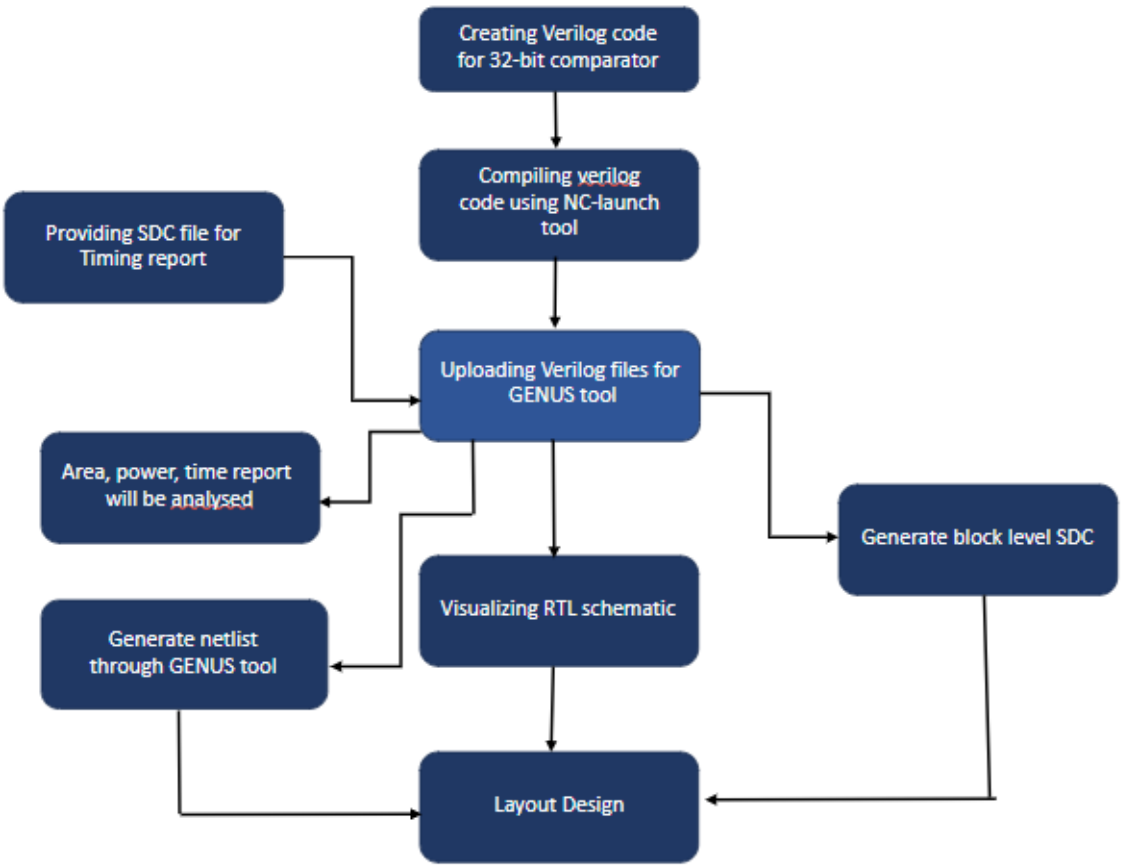


Figure 3.2: System overview flow chart for 32-bit comparator .

Chapter 4

System Hardware

This chapter covers the hardware aspects of the project, focusing on General-Purpose Input/Output (GPIO) and the use of the SPARTAN 6 FPGA BOARD for implementation and testing. It details the hardware setup and components involved.

4.1 SPARTAN-6 FPGA BOARD

The Spartan-6 family is a series of Field-Programmable Gate Array(FPGA) devices from Xilinx as shown in Figure 4.1, designed to provide a balance of area, power, and delay

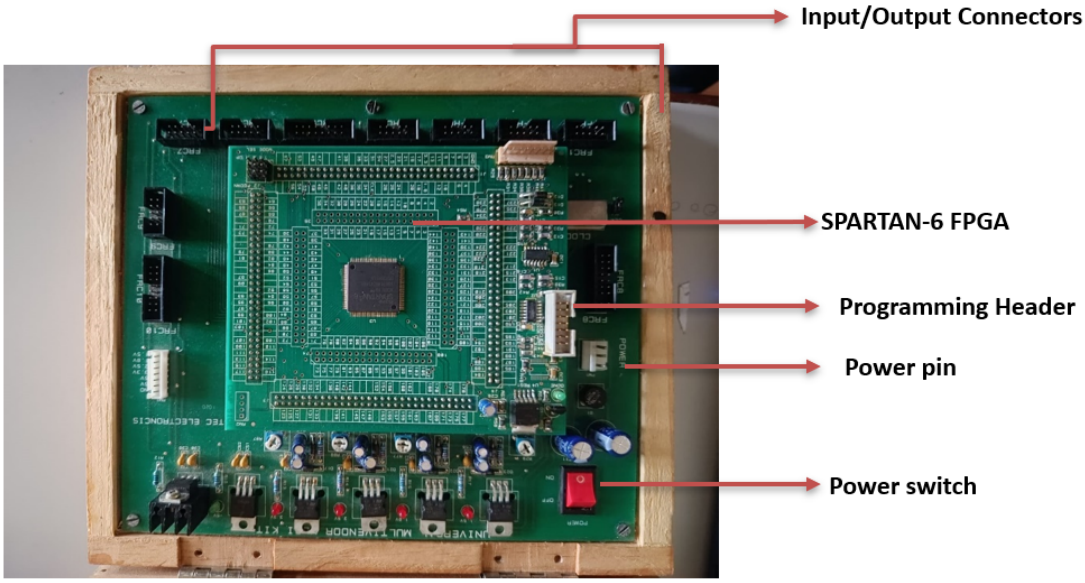


Figure 4.1: SPARTAN-6 FPGA board used to perform a specific task.

4.2 General Purpose Input/Output (GPIO)

GPIO stands for General Purpose Input/Output. It's a type of pin found on microcontrollers and other embedded systems as shown in Figure 4.2 used for interfacing with other hardware. GPIO pins can be configured to either read input signals or output signals, making them highly versatile for a wide range of applications.

1.Program the FPGA

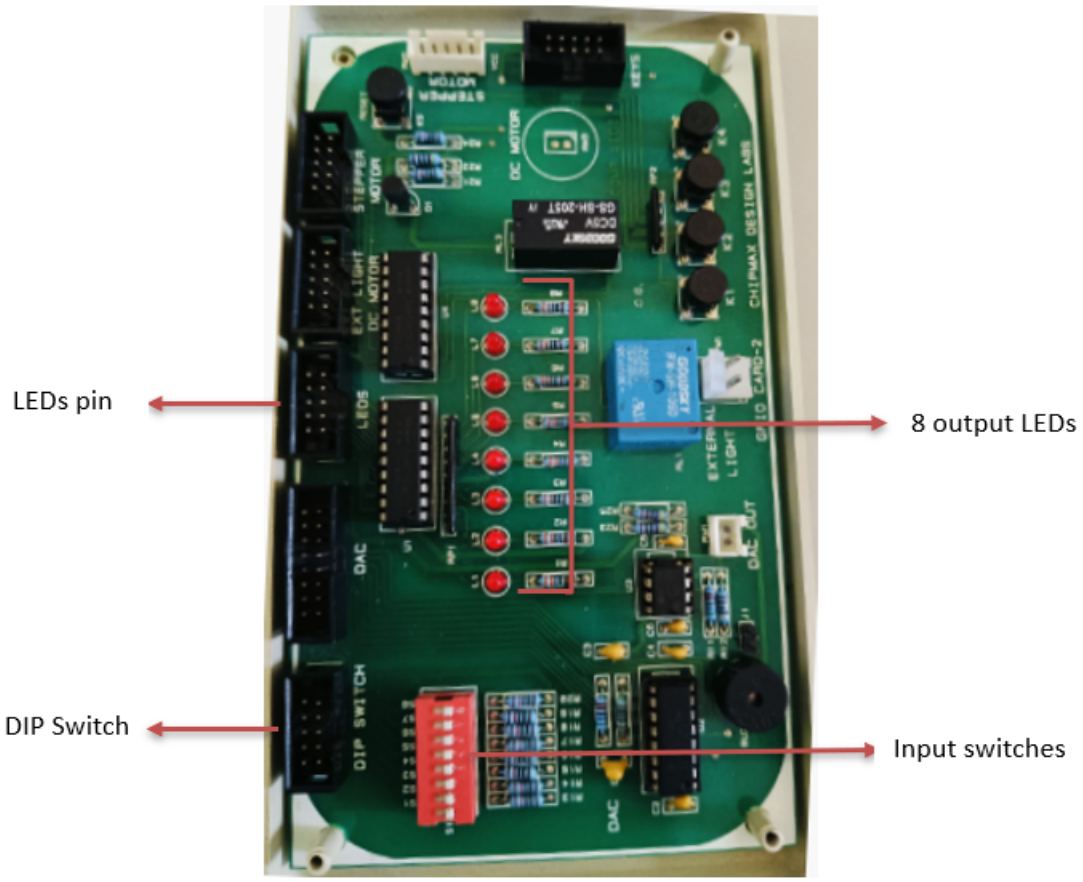


Figure 4.2: GPIO used for digital I/O pin interfacing with SPARTAN-6.

1. I/O Standards: Spartan-6 supports multiple I/O standards. Set the appropriate standard for the application.

2. I/O Banks: GPIO pins are grouped into banks. Each bank can be configured independently for different voltage levels and I/O standards.

3. Pin Constraints: Use the User Constraints File(UCF) to map the logical signals to physical pins on the FPGA.

4.3 Implementation of 16-bit Comparator

Implementation of 16-bit Comparator is shown in Figure 4.3 (Flow chart of 16-bit comparator using GPIO on Spartan-6 FPGA)

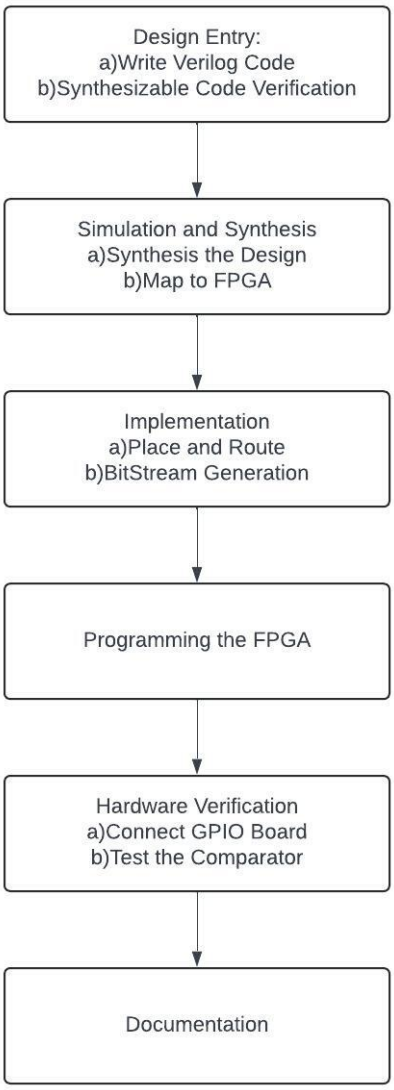


Figure 4.3: Flow chart of 16-bit comparator using GPIO on Spartan-6 FPGA

Uses of Spartan-6 FPGA for a 16-bit Comparator

1. Design and Implementation:

• Design of a 16-bit comparator using Hardware Description Language(HDL) like Verilog.

• Synthesized and implemented on the FPGA to test its functionality.

2. Flexibility and Reconfigurability:

• The FPGA can be reprogrammed to modify the comparator design or add new features without changing the hardware.

• Multiple designs can be tested and compared quickly.

3. High-Speed Processing:

• The FPGA provides parallel processing capabilities, making it suitable for high-speed

comparisons.

Uses of GPIO on Spartan-6 FPGA for a 16-bit Comparator

1. Input Interface:

• Switches or Buttons: GPIO pins are connected to switches to provide the 16-bit inputs (A and B) for the comparator.

• External Sensors: GPIO interfaces with external sensors or devices that provide digital outputs.

Output Interface:

• LEDs: GPIO pins are used to drive LEDs that indicate the comparator's output (A Greater than B, A Equal to B, A Less than B).

3. Communication with Other Systems:

• Debugging and Testing: GPIO is used for debugging purposes, allowing for easy testing and verification of the comparator's functionality. Implementation of 16-bit comparator using Spartan-6 is shown in Figure 4.4

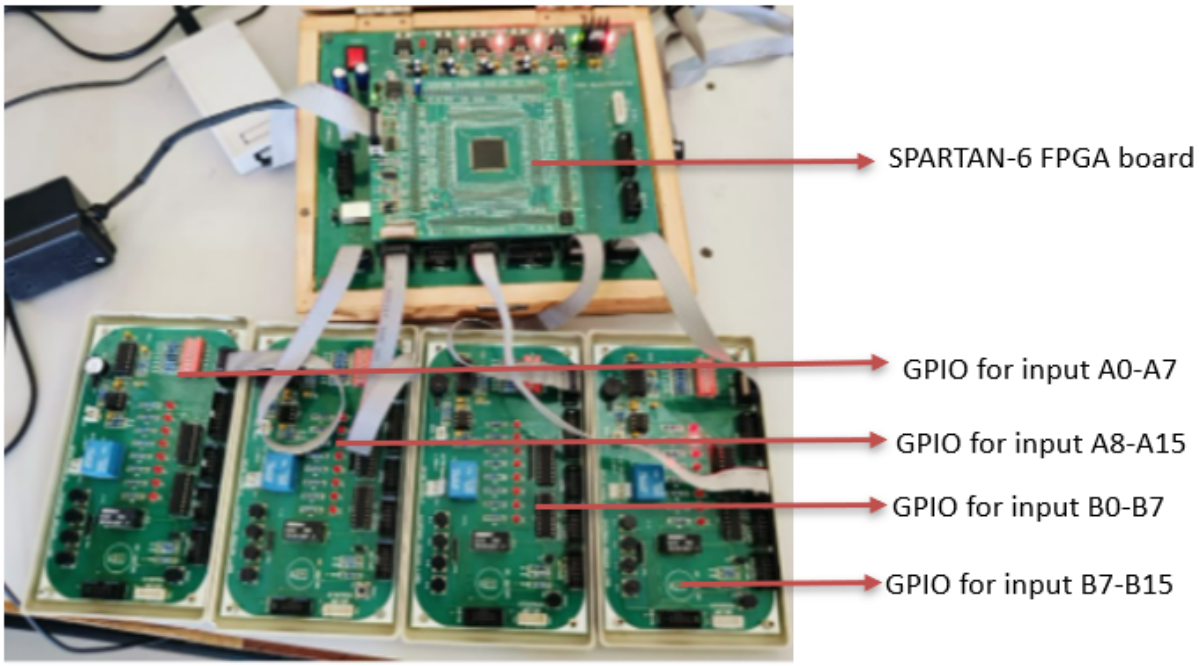


Figure 4.4: Implementation of 16-bit comparator using Spartan-6

Chapter 5

System Software

This chapter describes the software requirements and algorithms implemented in Verilog. It provides insights into the software design and the coding strategies used to achieve the project's objectives.

5.1 Software Requirements

Cadence Tools:

Cadence is a prominent provider of electronic design automation (EDA) software, offering a comprehensive suite of tools essential for designing and verifying integrated circuits. For the project involving a 32-bit comparator, the following Cadence tools are crucial:

1. **Incisive**:

    - **Verilog Code Development**: Incisive is used for writing, editing, and debugging Verilog code, which defines the behavior and functionality of digital circuits, including the 32-bit comparator.
    - **Simulation**: It provides a simulation environment to validate the functionality of the Verilog code. Waveform analysis in Incisive allows designers to inspect signals and verify correct operation.

2. **Genus**:

    - **Synthesis**: Genus is utilized for logic synthesis, which translates the RTL (Register Transfer Level) description of the design (written in Verilog) into a gate-level netlist.
    - **Power and Area Analysis**: Genus also performs power estimation and area analysis based on the synthesized netlist, providing insights into power consumption and physical size requirements of the comparator design.

Xilinx Tools (ISE):

Xilinx, known for its FPGA (Field-Programmable Gate Array) products, provides software tools that are essential for designing and implementing digital circuits on FPGA platforms. For the project:

ISE (Integrated Software Environment):

- **Verilog Code Writing**: ISE includes tools for writing and editing Verilog code, which defines the behavior and structure of the 32-bit comparator.
- **Simulation**: It offers simulation capabilities to verify the functionality of the Verilog code before synthesis and implementation on an FPGA.
- **Implementation**: ISE facilitates the implementation of the design on Xilinx FPGA devices, ensuring compatibility and functionality validation on hardware.

In the context of designing a 32-bit comparator:

- **Verilog Code Development**: Both Cadence Incisive and Xilinx ISE are used. Incisive is primarily used for detailed functional verification through simulation, ensuring the Verilog code accurately reflects the desired behavior of the comparator. ISE provides a platform-specific environment for writing and further simulating the Verilog code, ensuring compatibility with Xilinx FPGA architectures.
- **Synthesis and Implementation**: Cadence Genus is employed for logic synthesis, optimizing the Verilog code into a gate-level netlist that can be implemented on FPGA hardware. Xilinx ISE facilitates the final steps of design implementation, ensuring that the synthesized design meets timing and performance requirements on the chosen Xilinx FPGA platform.

5.2 Algorithm

Designing and implementing a 32-bit comparator involves a systematic approach to ensure functionality, efficiency, and compatibility within digital systems. Beginning with defining software requirements, essential tools such as Cadence's Incisive for Verilog development and simulation, Genus for logic synthesis, and Xilinx's ISE for FPGA compatibility are identified. The Verilog code is meticulously crafted to implement the comparator using

the efficient Carry Look-Ahead Adder (CLA) architecture, detailing how it processes two 32-bit inputs to produce accurate comparison results. Cadence Incisive is then used to simulate the Verilog code, validating its operation through waveform analysis under various input conditions. Subsequently, Cadence Genus performs logic synthesis to optimize performance metrics such as speed and power consumption, followed by logic equivalence checking to ensure fidelity between the Verilog specification and synthesized design. The validated design is implemented on a Spartan 6 FPGA board using Xilinx ISE, demonstrating practical applicability and validating the design's performance in real-world scenarios, thereby contributing to advancements in digital circuit efficiency and reliability.

5.3 Block Diagrams and Algorithms

5.3.1 Ripple Carry Adder

A ripple carry adder (RCA) sequentially adds bits from two binary numbers, propagating any carry bit to the next higher bit position. Figure 5.1 shows its block diagram and Figure 5.2 shows the flowchart of RCA . Equations 5.1 and 5.2, represents the sum and carry expressions respectively. Equation 5.1 computes the sum bit S_i for each bit position i as $S_i = (a_i \oplus b_i) \oplus C_{i-1}$, where a_i and b_i are input bits, and C_{i-1} is the previous carry. Equation 5.2 calculates the carry output C_i as $C_i = (a_i \cdot b_i) + (C_{i-1} \cdot (a_i \oplus b_i))$, determining if a carry is generated from bits a_i and b_i and including the carry propagated from C_{i-1}.

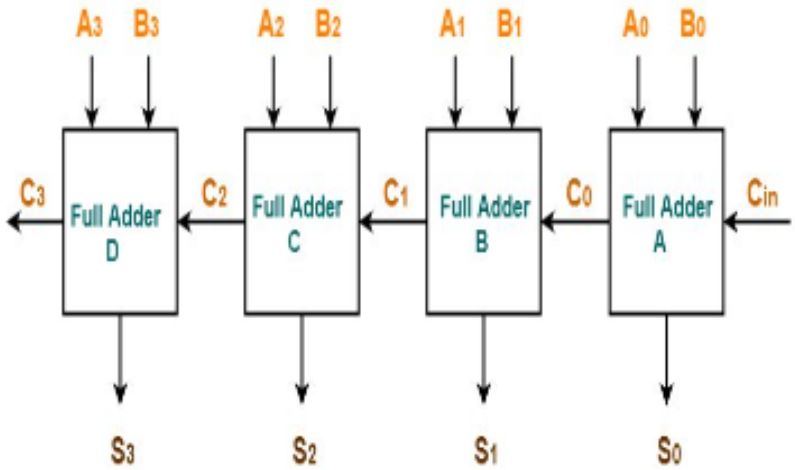


Figure 5.1: Block Diagram of RCA

Expression:-

Sum bit (S) for each bit position i:

$$S_i = (a_i \oplus b_i) \oplus C_{i-1} \tag{5.1}$$

Carry output (C_out) for each bit position i:

$$C_i = (a_i \cdot b_i) + (C_{i-1} \cdot (a_i \oplus b_i)) \tag{5.2}$$

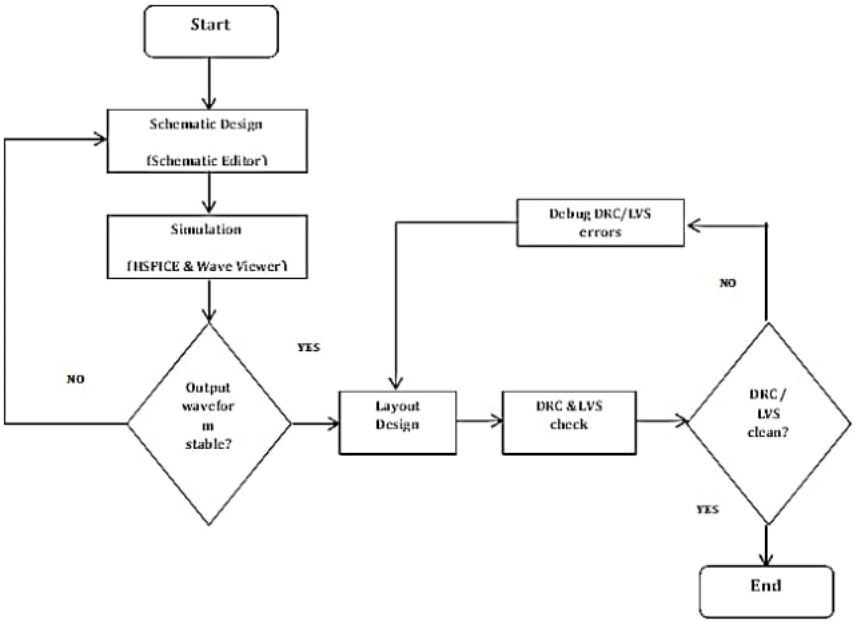


Figure 5.2: Flowchart of RCA

5.3.2 Disadvantages of Ripple Carry Adder

- **Propagation Delay**: Linear increase in delay with the number of bits due to sequential carry propagation.
- **Scalability**: Less efficient for larger bit-width operations.
- **Power Consumption**: Higher power usage due to longer delays.
- **Glitches**: Potential for temporary glitches or unwanted transitions.
- **Area**: Increased area usage on an integrated circuit for adders with many bits.

5.3.3 Carry Increment Adder

A Carry Increment Adder (CIA) enhances traditional adders like the ripple carry adder (RCA) by minimizing carry propagation delays. In the context of the CIA, $G_i = a_i \cdot b_i$ Equation 5.3 determines if a carry is generated at bit i by performing a logical AND operation on input bits a_i and b_i. $P_i = a_i \oplus b_i$ Equation 5.4 indicates whether a carry will propagate through bit i, using a logical XOR operation. The carry output C_i Equation 5.5 is computed based on G_i and the previous carry C_{i-1}, optimizing carry computation efficiency. $S_i = P_i \oplus C_{i-1}$ Equation 5.6 calculates the sum bit at bit i, utilizing the propagate term P_i and the previous carry C_{i-1}. Equations 5.3 to 5.6 collectively define the operations within the CIA, aiming to reduce overall propagation delay and improve arithmetic performance.

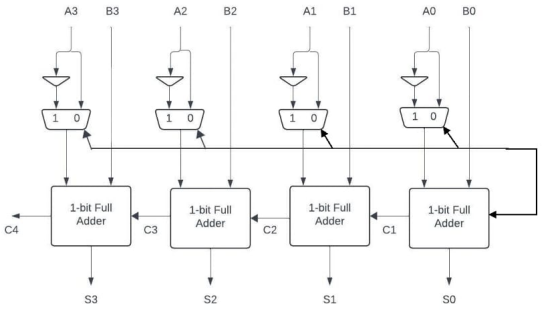


Figure 5.3: Block Diagram of CIA .

Expression:-

$$G_i = a_i \cdot b_i \tag{5.3}$$

$$P_i = a_i \oplus b_i \tag{5.4}$$

$$C_i = G_i + (P_i \cdot C_{i-1}) \tag{5.5}$$

$$S_i = P_i \oplus C_{i-1} \tag{5.6}$$

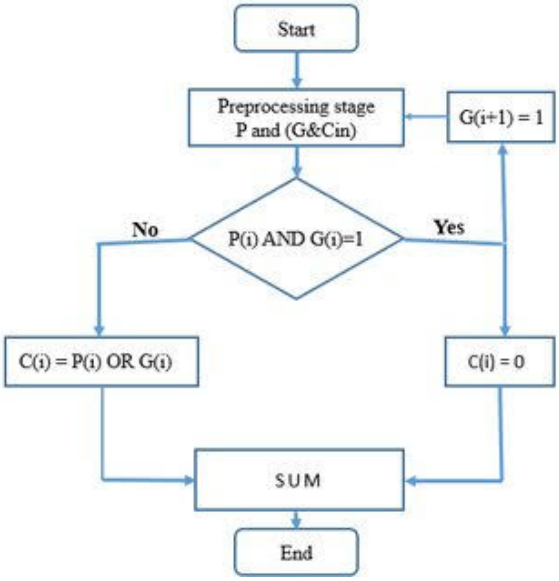


Figure 5.4: Flowchart of CIA .

5.3.4 Disadvantages of Carry Increment Adder

- **Propagation Delay Variation**: The propagation delay can vary based on inputs and block configurations, leading to less predictable performance. This variation can cause timing issues, particularly in high-speed circuits where consistent delay is critical for synchronization.

- **Complexity**: The Carry Increment Adder requires additional circuitry for carry increments and block division.

- **Area Usage**: The increased logic required for carry increments and block sums results in larger chip sizes.

- **Power Consumption**: More components and additional logic lead to higher power consumption.

- **Design Difficulty**: Designing a Carry Increment Adder requires careful handling of carry increments and sum adjustments.

5.3.5 Carry Look-ahead Adder

A Carry Lookahead Adder (CLA) is a type of adder designed to address the carry propagation delay issue in ripple carry adders. Figure 5.5 shows the block diagram of the CLA,

and Figure 5.6 provides the corresponding flowchart. The relevant equations, numbered from 5.7 to 5.14, define the operations within the CLA. The generate term G_i (Equation 5.7) indicates if a carry is generated at bit position i, while the propagate term P_i (Equation 5.8) indicates if a carry will be propagated through bit position i. The initial carry input is $C_0 = 0$ (Equation 5.9). Subsequent carry outputs are calculated as $C_{i+1} = G_i + (P_i \cdot C_i)$ (Equations 5.10 to 5.13), and the sum bits are given by $S_i = P_i \oplus C_i$ (Equation 5.14). These equations allow the CLA to compute carries more efficiently, reducing overall delay.

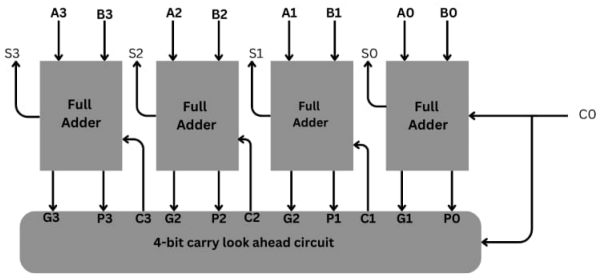


Figure 5.5: Block Diagram of CLA .

Expression:-

$$G_i = a_i \cdot b_i \tag{5.7}$$

$$P_i = a_i \oplus b_i \tag{5.8}$$

$$C_0 = 0 \tag{5.9}$$

$$C_1 = G_0 + (P_0 \cdot C_0) \tag{5.10}$$

$$C_2 = G_1 + (P_1 \cdot C_1) \tag{5.11}$$

$$C_{i+1} = G_i + (P_i \cdot C_i) \tag{5.12}$$

$$S_i = P_i \oplus C_i \tag{5.13}$$

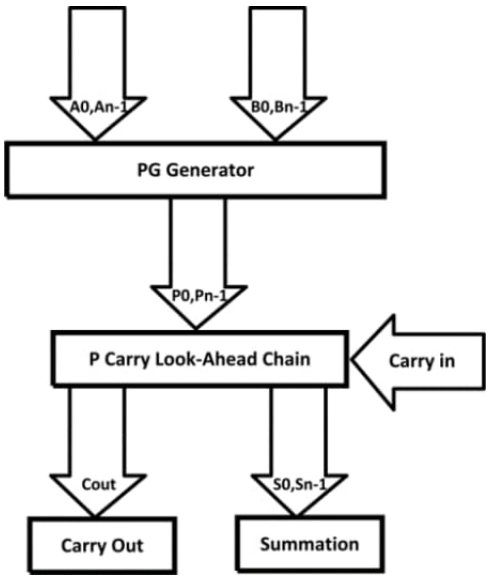


Figure 5.6: Flowchart Of CLA .

5.3.6 Advantages Of Carry Look-ahead Adder

- **Reduced Propagation Delay**: Minimizes carry propagation delay using generate and propagate signals.
- **Scalability**: Efficiently scales to larger bit-widths, maintaining high performance.
- **Parallel Processing**: Processes multiple bits in parallel, enhancing performance.
- **High Throughput**: Achieves higher throughput with reduced delays and parallel processing.

5.3.7 32-bit comparator using CLA

A 32-bit comparator using a Carry Lookahead Adder (CLA) efficiently compares two 32-bit binary numbers, leveraging the fast carry generation and propagation capabilities of the CLA architecture. As depicted in Figure 5.7, the block diagram of the 32-bit comparator integrates multiple CLA blocks to manage the carry signals in parallel, significantly reducing the overall propagation delay compared to traditional ripple carry adders. This design enhances both speed and reliability in digital circuits. Furthermore, the flow chart in Figure 5.8 illustrates the step-by-step process of the comparison operation, highlighting the parallelism and efficiency achieved through the CLA-based approach. This method balances speed, area, and power consumption, making it highly suitable for high-performance applications where rapid and accurate comparisons are essential. The CLA-based comparator is thus an optimal choice for modern digital systems requiring high-speed and reliable performance. Additionally, its architecture allows for scalable designs, making it adaptable for various bit-width requirements. This ensures that the CLA-based comparator remains a versatile component in advanced digital design.

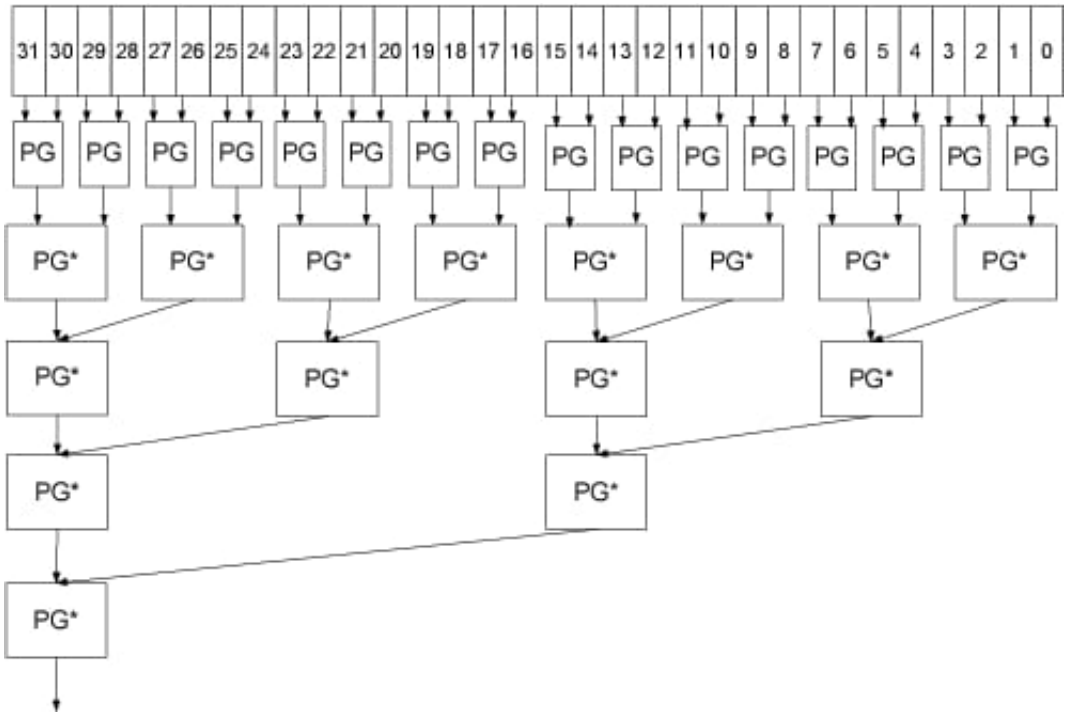


Figure 5.7: Block Diagram of 32-bit comparator using CLA.

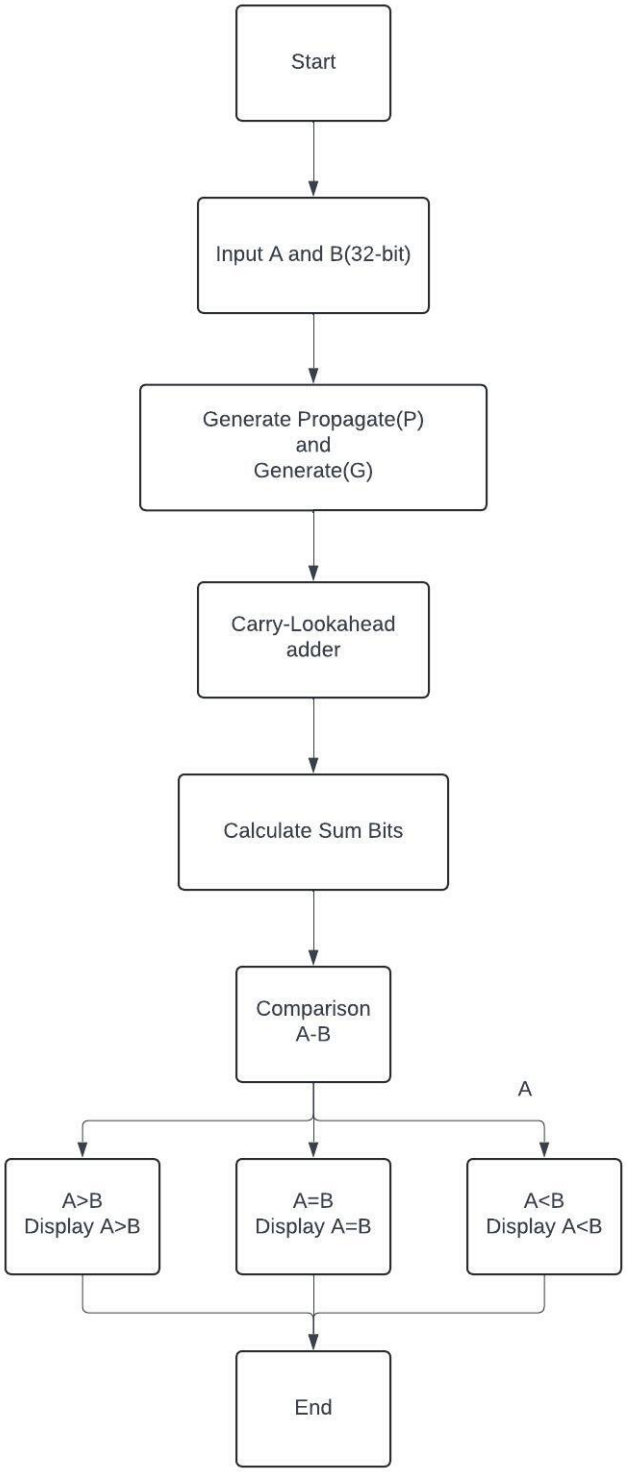


Figure 5.8: Flow chart of 32-bit comparator using CLA.

Chapter 6

Results

This chapter presents the results of the project, including Verilog simulation results with Cadence Incisive, synthesis results with Cadence Genus before and after optimization, and FPGA implementation details. It also includes snapshots of the project setup.

6.1 Simulation and comparision of 3 adders

6.1.1 Results of RCA

A 32-bit Ripple Carry Adder, RCA, is a digital circuit that sequentially adds two 32-bit binary numbers, generating a sum and a carry output. The RCA waveform, Figure 6.1, illustrates the sequential addition process, and the RTL Schematic of RCA, Figure 6.2, provides a detailed view of its structure and connections. The 32-bit RCA occupies more chip area compared to other adders, as detailed in the RCA area report, Figure 6.3. The power consumption is relatively high since each full adder consumes power, and the total power increases with the number of adders, as shown in the RCA power report, Figure 6.4. The timing performance is characterized by a linear increase in propagation delay with the number of bits, analyzed in the RCA delay report, Figure 6.5.

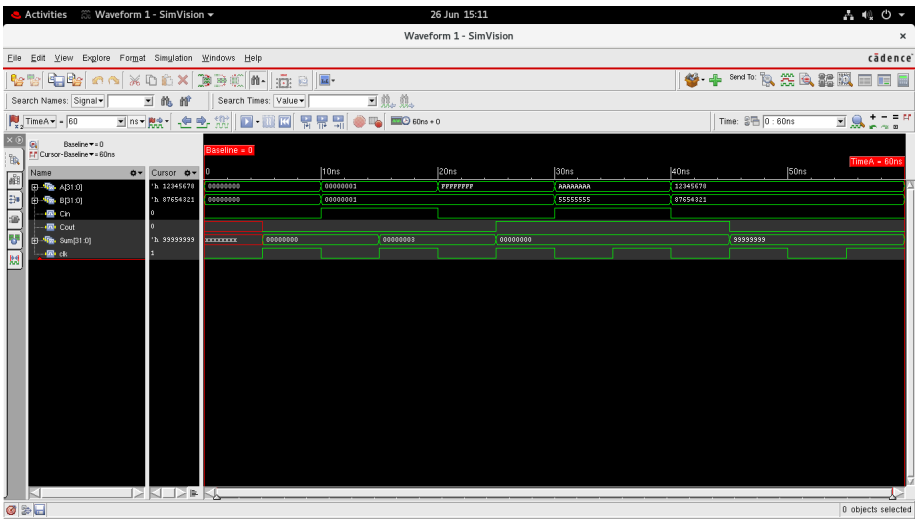


Figure 6.1: RCA waveform

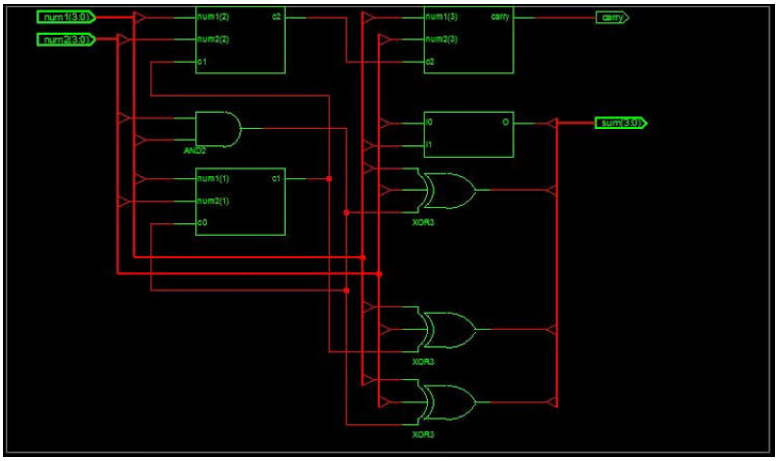


Figure 6.2: RTL Schematic of RCA

```
@genus:root: 11> report_area
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Jun 26 2024  03:23:39 pm
  Module:                 RCA_32bit
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

 Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------
RCA_32bit                 72   1174.709     0.000     1174.709 <none> (D)
  (D) = wireload is default in technology library
@genus:root: 12>
```

Figure 6.3: RCA area report

```
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     3.04080e-06  6.11805e-05  0.00000e+00  6.42213e-05  67.81%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     2.92895e-06  1.60865e-05  7.06241e-06  2.60779e-05  27.54%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  4.40640e-06  4.40640e-06   4.65%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     5.96975e-06  7.72670e-05  1.14688e-05  9.47056e-05 100.00%
  Percentage           6.30%       81.59%       12.11%      100.00% 100.00%
  ------------------------------------------------------------------------------
@genus:root: 13>
```

Figure 6.4: RCA power report

```
Path 1: MET (8 ps) Setup Check with Pin Sum_reg[31]/CK->D
          Group: clk
     Startpoint: (F) B[0]
          Clock: (R) clk
       Endpoint: (R) Sum_reg[31]/D
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   10000            0
        Drv Adjust:+      0            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=   10000            0

              Setup:-    216
     Required Time:=   9784
      Launch Clock:-      0
       Input Delay:-   2000
         Data Path:-   7776
             Slack:=      8
```

Figure 6.5: RCA delay report

6.1.2 Results of CIA

The Carry Increment Adder, CIA, enhances the Ripple Carry Adder, RCA, by utilizing lookahead logic to reduce carry propagation delay, thus significantly improving performance. However, the additional logic for lookahead carry generation increases power consumption compared to the RCA. Despite this, the CIA often occupies less area due to its optimized logic design, which minimizes chip space.

The CIA architecture consists of three main stages: block-wise addition, carry increment, and final sum computation. By parallelizing addition and using efficient carry management, the CIA balances speed and hardware complexity, making it ideal for high-speed arithmetic operations.

Figure 6.6 illustrates the CIA waveform, showing its timing and carry propagation efficiency. Figure 6.7 presents the RTL schematic, detailing the logical arrangement. Figure 6.8 demonstrates area efficiency, highlighting minimized chip space. Figure 6.9 offers a power report, indicating dynamic power consumption. Figure 6.10 provides a delay report, showing reduced critical path delays, underscoring the CIA's enhanced performance.

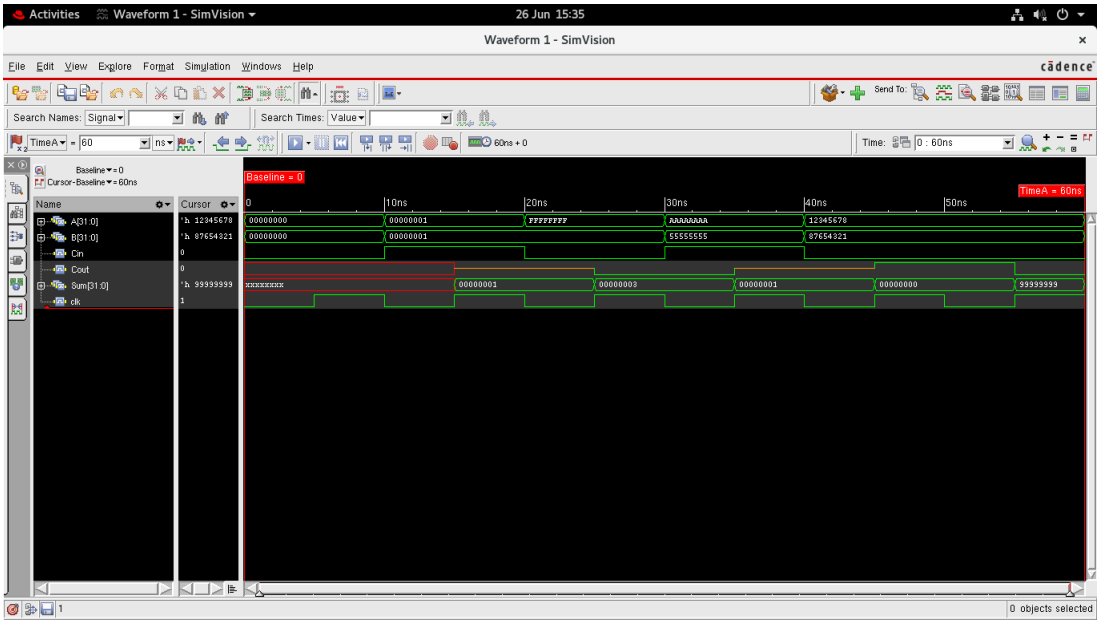


Figure 6.6: CIA waveform

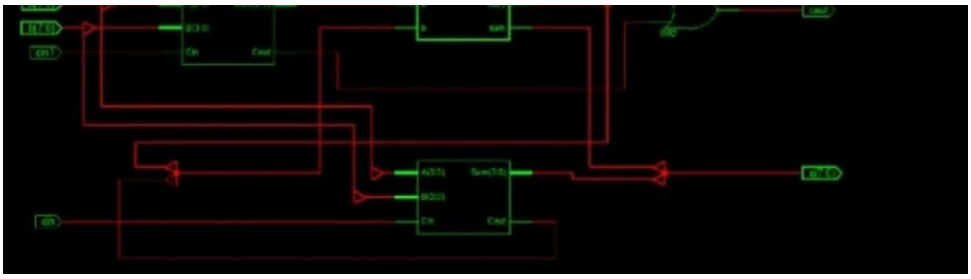


Figure 6.7: RTL Schematic of CIA .

```
@genus:root: 10> report_area
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Jun 26 2024  03:41:50 pm
  Module:                 CIA_32bit
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

 Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
------------------------------------------------------------------------------
CIA_32bit               122     913.578     0.000      913.578 <none> (D)
  (D) = wireload is default in technology library
```

Figure 6.8: CIA area report

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	3.04080e-06	5.78822e-06	0.00000e+00	8.82902e-06	69.47%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	1.42795e-06	1.79828e-06	6.54108e-07	3.88034e-06	30.53%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	4.46876e-06	7.58649e-06	6.54108e-07	1.27094e-05	100.00%
Percentage	35.16%	59.69%	5.15%	100.00%	100.00%

Figure 6.9: CIA power report

```
                   Capture       Launch
       Clock Edge:+   10000            0
       Drv Adjust:+       0            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

            Setup:-     212
    Required Time:=    9788
     Launch Clock:-       0
      Input Delay:-    2000
        Data Path:-    2401
            Slack:=    5387

Exceptions/Constraints:
  input_delay             2000           cia_constraints.sdc_line_7_64_1
```

Figure 6.10: CIA delay report

6.1.3 Results of CLA

The Carry Lookahead Adder (CLA) is an advanced digital circuit design that computes carry signals in parallel, minimizing propagation delay compared to Ripple Carry Adders (RCA). This parallel computation speeds up arithmetic operations, making CLA ideal for high-performance applications. However, CLA typically consumes more power due to its complex lookahead logic, which predicts carry signals across multiple bits simultaneously. Despite higher power consumption, CLA occupies less chip area than RCA, thanks to its optimized logic design and efficient use of logic gates. This efficiency makes CLA a preferred choice where speed and space utilization are critical factors. CLA's architecture includes stages for carry generation, lookahead logic, and sum computation, each contributing to its efficient operation. Figure 6.11, illustrating the CLA waveform,

provides insights into its operational timing and the efficiency of its carry propagation mechanism. Figure 6.12, presenting the RTL schematic of CLA, details the structural arrangement of its components and the logic gates involved in carry lookahead. Figures like 6.13 (CLA area report), 6.14 (CLA power report), and 6.15 (CLA delay report) offer detailed assessments crucial for designers. They highlight CLA's minimized chip space utilization, dynamic power characteristics, and reduced critical path delays, underscoring its enhanced performance in arithmetic operations. CLA's performance advantages, such as reduced critical path delays and enhanced computational throughput, make it essential in fields requiring rapid data processing and real-time computations. Ongoing advancements in semiconductor technology continue to refine CLA designs, aiming to further optimize its speed, power efficiency, and overall performance.

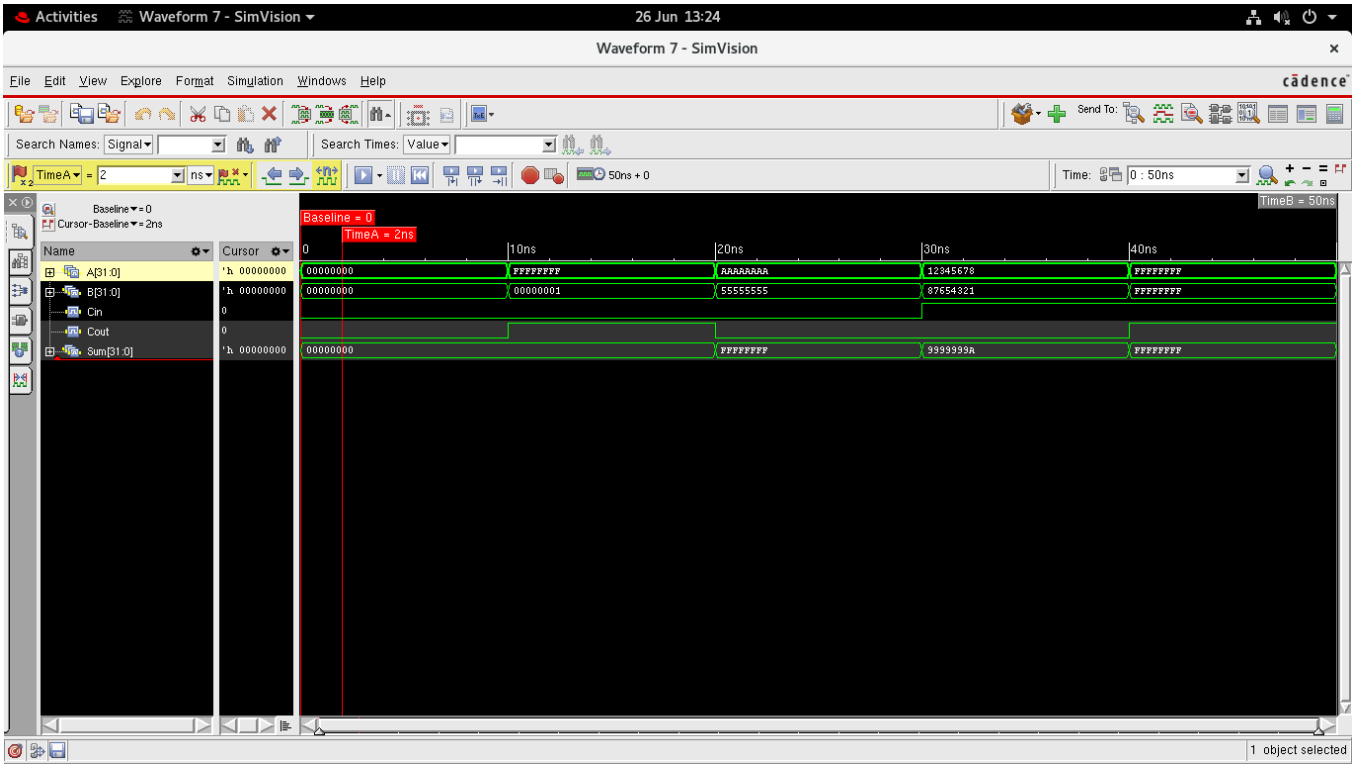


Figure 6.11: CLA waveform

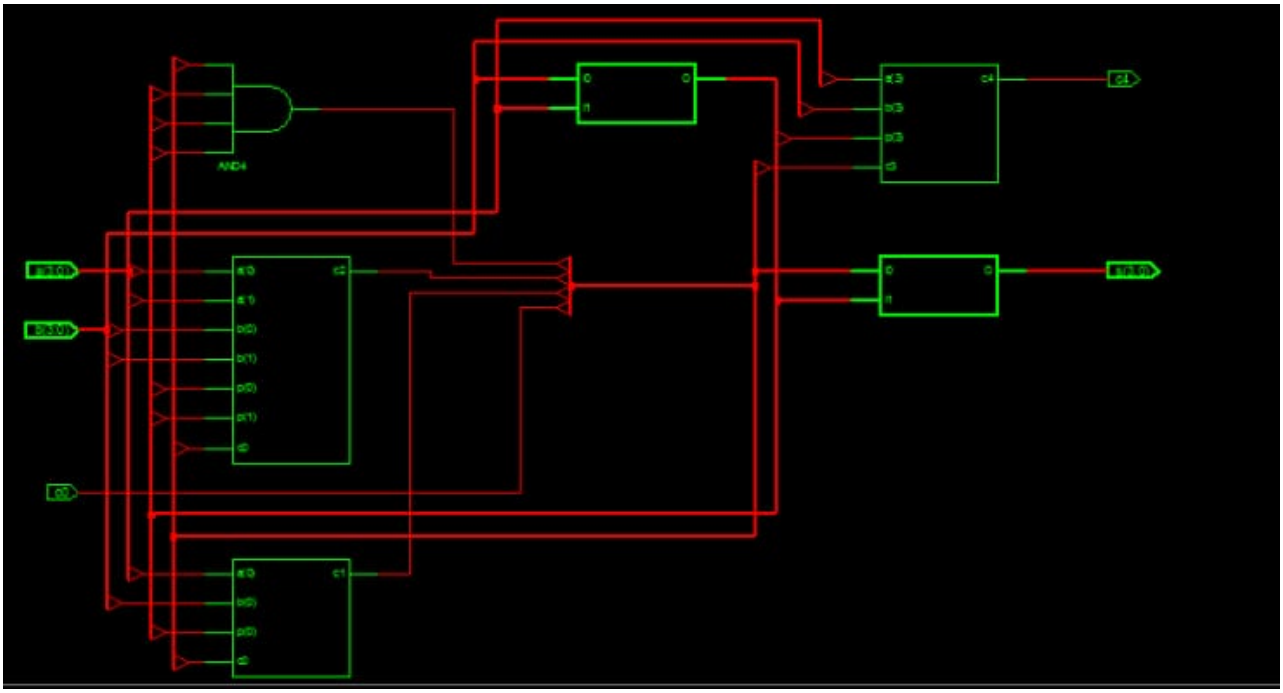


Figure 6.12: RTL Schematic of CLA

```
@genus:root: 14> report_area
================================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Jun 26 2024  02:39:09 pm
  Module:                 CLA_32bit
  Technology library:     slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
================================================================

 Instance Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-------------------------------------------------------------------------
CLA_32bit               129   1204.228     0.000     1204.228 <none> (D)
```

Figure 6.13: CLA area report

```
Instance: /CLA_32bit
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     4.24059e-06  7.03946e-05  0.00000e+00  7.46352e-05  71.40%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     3.34056e-06  1.30236e-05  8.99688e-06  2.53610e-05  24.26%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  4.53600e-06  4.53600e-06   4.34%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     7.58115e-06  8.34182e-05  1.35329e-05  1.04532e-04 100.00%
  Percentage           7.25%       79.80%       12.95%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Figure 6.14: CLA power report

```
Path 1: MET (1745 ps) Setup Check with Pin Cout_reg/CK->D
          Group: clk
     Startpoint: (R) B[0]
          Clock: (R) clk
       Endpoint: (F) Cout_reg/D
          Clock: (R) clk

                     Capture       Launch
       Clock Edge:+   10000            0
       Drv Adjust:+       0            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   10000            0

            Setup:-      85
     Required Time:=    9915
      Launch Clock:-       0
       Input Delay:-    2000
         Data Path:-    6169
             Slack:=    1745

Exceptions/Constraints:
  input_delay             2000           constraints.sdc_line_7_63_1
```

Figure 6.15: CLA delay report

6.1.4 Comparison of 3 adders

6.1.5 Selection of CLA:

Reason for Selecting CLA:

- **Low Delay**: The CLA (Carry Lookahead Adder) has the lowest delay among the three architectures, which is critical for the performance of the 32-bit comparator. A lower delay ensures faster computation.

- **Smaller Area**: Although the power consumption of the CLA is slightly higher than the RCA, it has the smallest area, making it more efficient in terms of space.

Table 6.1: Comparison of 3 adders

CONSTRAINTS	CLA	RCA	CIA
POWER (μW)	104.532	94.7056	12.7994
AREA	913.578	1174.709	1204.228
DELAY (ps)	1745	7776	2491

- **Trade-off in Power**: The slight increase in power consumption (104.532 µW) is a reasonable trade-off considering the significant benefits in terms of delay and area.

Given these considerations and observering the Table 6.1, the CLA is selected for the 32-bit comparator design due to its superior performance in delay and area, which are crucial for high-speed and efficient comparator operations.

6.2 Simulation Results of 32-bit Comparator with Cadence Incisive

6.2.1 Waveform Analysis

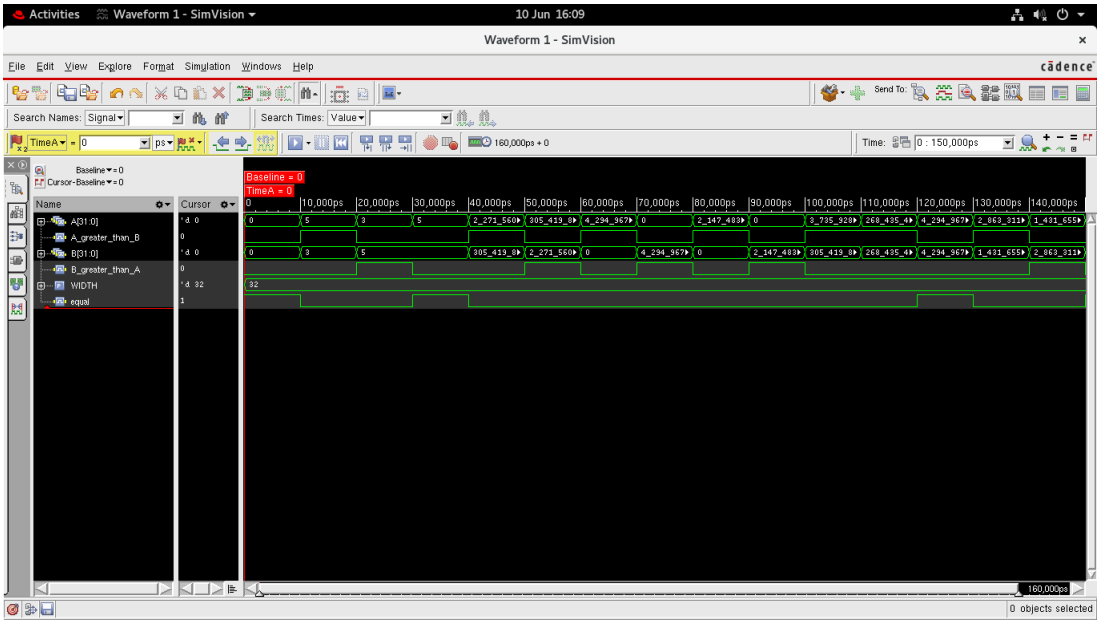


Figure 6.16: Waveform using Cadence Incisive of 32-bit comparaor using CLA.

Figure 6.17: RTL Schematic of 32-bit comparator using CLA.

6.2.2 Discussion

The waveform analysis conducted using Cadence Incisive provides valuable insights into the operational characteristics and performance of the designed circuit. The findings from this analysis contribute to a deeper understanding of the circuit's behavior under simulated conditions and guide further refinement or optimization efforts as part of the design process.

6.3 Synthesis Results with Cadence Genus

6.3.1 Before Optimization

The synthesis results before optimization, including power consumption and area utilization, are illustrated in Figures, 6.18 and 6.19

```
Info   : PWRA-0007 [PwrInfo] Completed successfully.
       : Info=6, Warn=2, Error=0, Fatal=0
Instance: /CLA_32bit_comparator
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     4.99510e-06  1.61103e-05  7.62090e-06  2.87263e-05 100.00%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------------
    Subtotal     4.99510e-06  1.61103e-05  7.62090e-06  2.87263e-05 100.00%
  Percentage          17.39%       56.08%       26.53%      100.00% 100.00%
  ------------------------------------------------------------------------------
```

Figure 6.18: Power report of 32-bit comparator before optimization using Cadence Genus.

```
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Jun 21 2024  04:23:52 pm
  Module:                 CLA_32bit_comparator
  Technology libraries:   slow
                          slow
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

     Instance       Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-----------------------------------------------------------------------------------
CLA_32bit_comparator               183    979.429     0.000      979.429 <none> (D)
```

Figure 6.19: Area report of 32-bit comparator before optimization using Cadence Genus.

From the synthesis with Cadence Genus before optimization, it is observed that the power consumption was 2.8726e-05 and the area utilization was 183 cells. These metrics indicate the initial performance and resource usage of the design prior to any optimization efforts.

6.3.2 Optimization using Cadence Genus

Power Consumption and Area Utilization

The synthesis results after optimization, including power consumption and area utilization, are illustrated in Figure 6.20 and 6.21

```
Power Unit: W
PDB Frames: /stim#0/frame#0
  ------------------------------------------------------------------------
    Category         Leakage     Internal    Switching        Total    Row%
  ------------------------------------------------------------------------
      memory     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
    register     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       latch     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       logic     4.85252e-06  1.55269e-05  7.25478e-06  2.76342e-05 100.00%
        bbox     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
       clock     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
         pad     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
          pm     0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00   0.00%
  ------------------------------------------------------------------------
    Subtotal     4.85252e-06  1.55269e-05  7.25478e-06  2.76342e-05 100.00%
  Percentage          17.56%       56.19%       26.25%      100.00% 100.00%
  ------------------------------------------------------------------------
```

Figure 6.20: Power report of 32-bit comparator after optimization using Cadence Genus.

After optimization with Cadence Genus, improvements were achieved in the design's power consumption and area utilization. The power consumption decreased from 2.8726×10^{-5} to 2.76342×10^{-5}, marking a reduction of approximately 3.80%. Similarly, the area utilization decreased from 183 cells to 181 cells, representing an improvement of about 1.09%. These results demonstrate the effectiveness of the optimization process in enhancing efficiency and reducing resource usage within the design.

```
@genus:root: 2> report_area
============================================================
  Generated by:           Genus(TM) Synthesis Solution 21.14-s082_1
  Generated on:           Jun 21 2024  03:19:30 pm
  Module:                 CLA_32bit_comparator
  Operating conditions:   slow (balanced_tree)
  Wireload mode:          enclosed
  Area mode:              timing library
============================================================

      Instance       Module  Cell Count  Cell Area  Net Area   Total Area   Wireload
-------------------------------------------------------------------------------------
CLA_32bit_comparator                181    906.766     0.000      906.766 <none> (D)
```

Figure 6.21: Area report of 32-bit comparator after optimization using Cadence Genus.

6.3.3 Layout of 32-bit Comparator

The layout design of the 32-bit comparator is a critical phase in digital circuit design, ensuring optimal functionality and efficiency in physical implementation. Figure 6.22, depicting the layout of the 32-bit comparator after optimization using Cadence Genus, provides a detailed illustration of the physical arrangement. This layout strategically places components such as transistors and interconnections to enhance performance, minimize power consumption, and reduce area utilization. In this optimized layout, each

component is meticulously positioned to meet stringent design constraints, including timing, power, and area requirements. The physical design process involves careful planning to ensure minimal signal delay and efficient power distribution throughout the comparator circuit. This blueprint serves as a guide for fabricating the integrated circuit, highlighting the precise arrangement and connectivity of all internal components. By leveraging

Cadence Genus for optimization, the layout of the 32-bit comparator achieves enhanced reliability and performance. The tool's capabilities in placement and routing contribute to the efficient integration of logic gates and routing tracks, further optimizing the overall functionality of the comparator design. This meticulously crafted layout not only ensures adherence to design specifications but also enhances the circuit's robustness and operational efficiency in real-world applications.

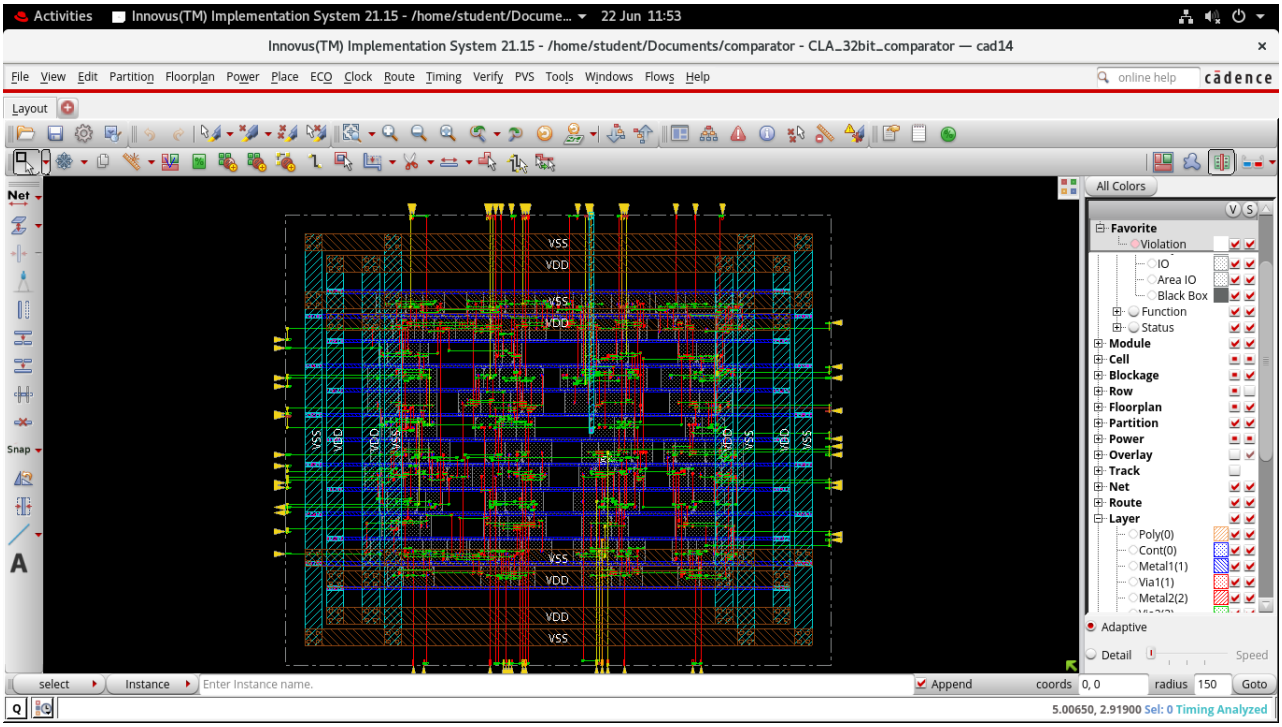


Figure 6.22: Layout of 32-bit Comparator after optimization using Cadence Genus.

6.4 Result of 16-bit Comparator using Spartan-6

The 16-bit comparator designed using the Spartan-6 FPGA effectively compares two 16-bit binary numbers, providing outputs that indicate whether the first number (A) is equal to, less than, or greater than the second number (B). Figure 6.23, illustrating the RTL schematic of the 16-bit comparator, details its internal structure and logic arrangement, showcasing how A and B are processed to determine their relationship.

Figures 6.25, 6.26, and 6.27 demonstrate the implementation of the 16-bit comparator on the Spartan-6 FPGA under different conditions: when A is greater than B, when A is less than B, and when A is equal to B, respectively. These figures visually confirm the correct operation of the design, depicting the comparator's response through simulated waveforms or timing diagrams.

The implementation was carried out using the Xilinx ISE Design Suite, a comprehensive toolset that facilitated synthesis, simulation, and FPGA implementation of the 16-bit comparator design. This tool suite enabled efficient development and validation of the comparator's functionality, ensuring that it met design specifications for accuracy, speed, and reliability in comparing 16-bit binary numbers.

Overall, the RTL schematics and implementation figures validate the successful operation

of the 16-bit comparator design on the Spartan-6 FPGA, highlighting its capability to accurately determine the relationship between two 16-bit binary inputs.

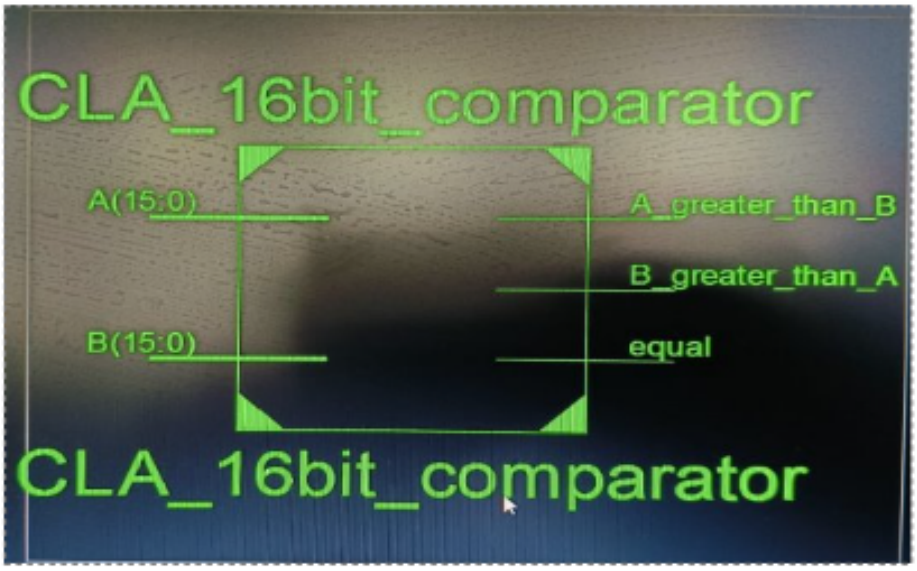


Figure 6.23: RTL Schematic of 16-bit Comparator

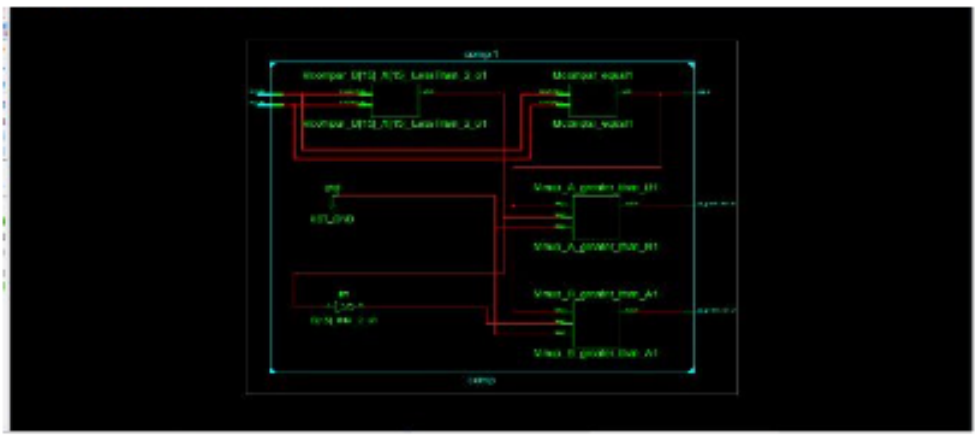


Figure 6.24: RTL Schematic of 16-bit Comparator

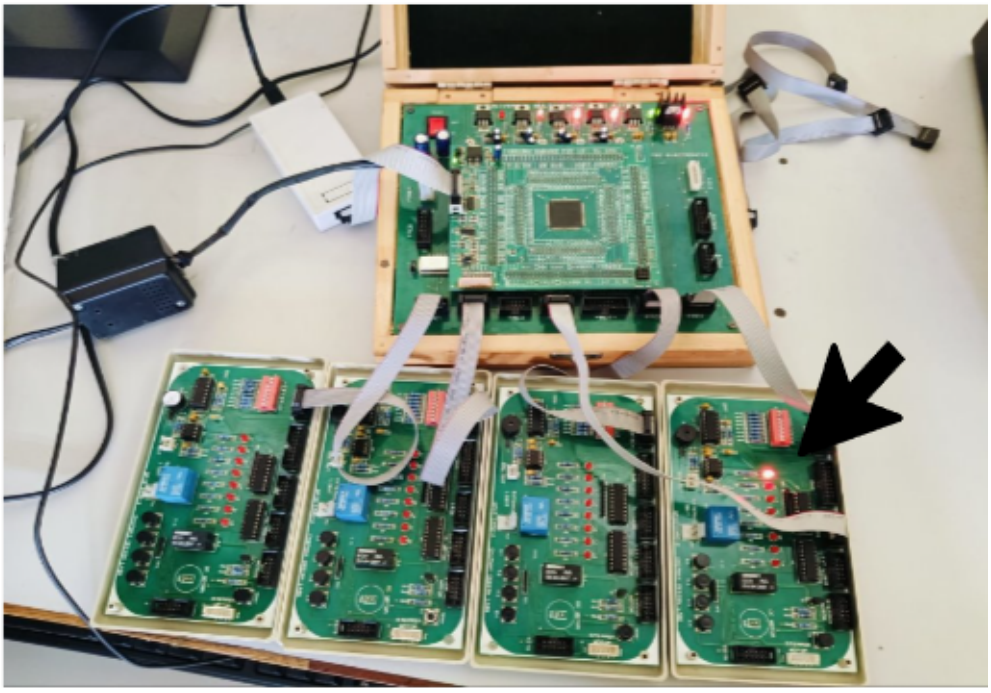


Figure 6.25: Implementation of 16-bit comparator using spartan-6 when A greater than B

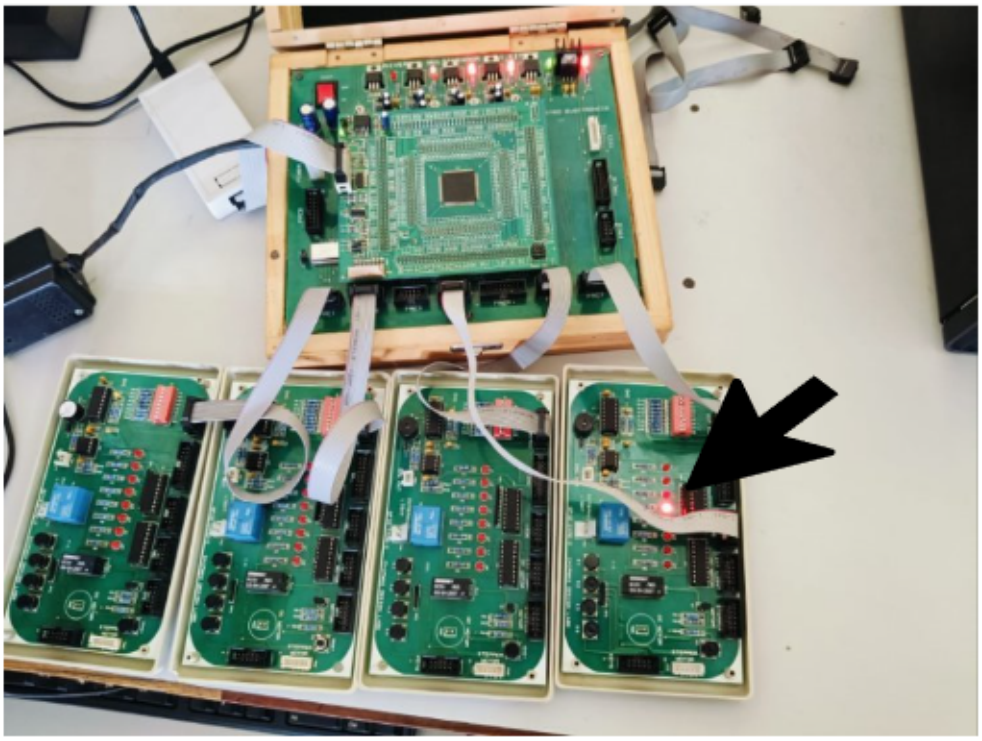


Figure 6.26: Implementation of 16-bit comparator using spartan-6 when A less than B

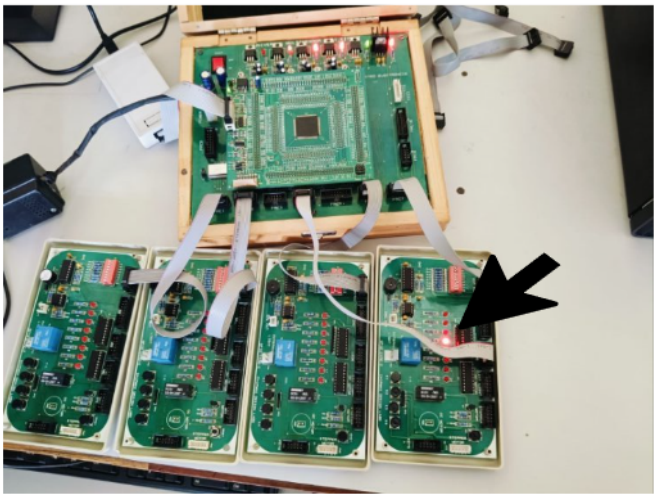


Figure 6.27: Implementation of 16-bit comparator using spartan-6 when A equal to B

6.5 Timing , Power and Area Report of 16-bit comparator without CLA

A 16-bit comparator without a Carry Lookahead Adder (CLA) typically exhibits longer propagation delays due to sequential carry computation, impacting timing performance compared to CLA-based designs. Figure 6.28, the Timing and Power Report of the 16-bit comparator, details its propagation delay characteristics and power consumption profile, reflecting the effects of sequential carry propagation. Figure 6.29, the Area Report of the 16-bit comparator, illustrates its chip area utilization, which may be higher compared to CLA implementations despite simpler logic design.

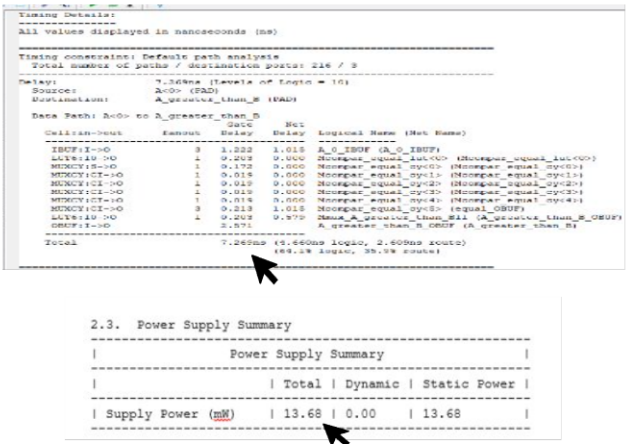
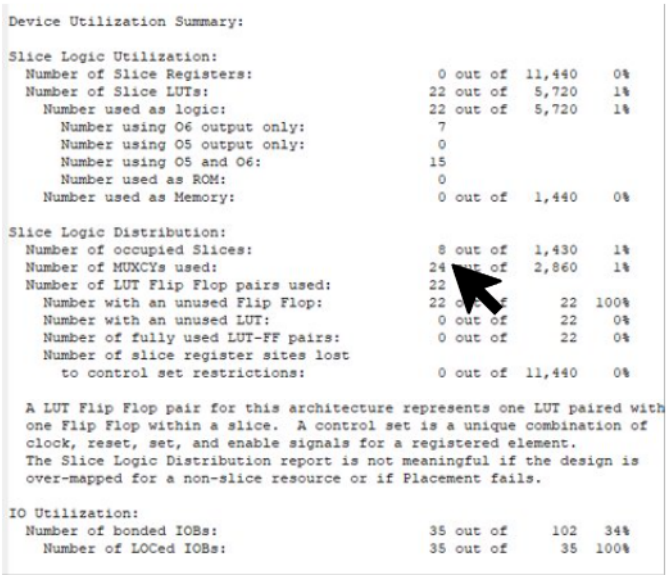


Figure 6.28: Timing and Power Report of 16-bit Comparator without CLA

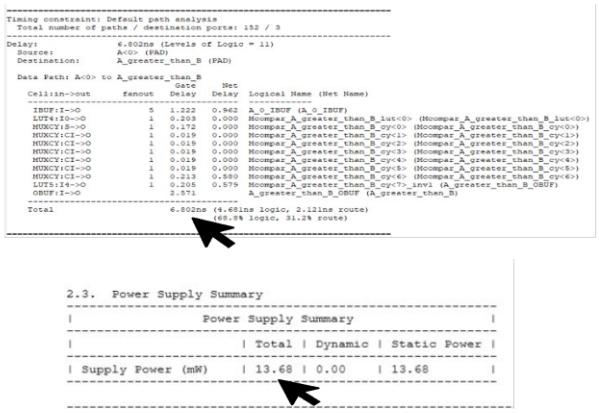


```
Device Utilization Summary:

Slice Logic Utilization:
  Number of Slice Registers:                     0 out of  11,440    0%
  Number of Slice LUTs:                         22 out of   5,720    1%
    Number used as logic:                       22 out of   5,720    1%
      Number using O6 output only:               7
      Number using O5 output only:               0
      Number using O5 and O6:                   15
      Number used as ROM:                        0
    Number used as Memory:                       0 out of   1,440    0%

Slice Logic Distribution:
  Number of occupied Slices:                     8 out of   1,430    1%
  Number of MUXCYs used:                        24 out of   2,860    1%
  Number of LUT Flip Flop pairs used:           22
    Number with an unused Flip Flop:            22 out of      22  100%
    Number with an unused LUT:                   0 out of      22    0%
    Number of fully used LUT-FF pairs:           0 out of      22    0%
    Number of slice register sites lost
      to control set restrictions:               0 out of  11,440    0%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        35 out of     102   34%
    Number of LOCed IOBs:                       35 out of      35  100%
```

Figure 6.29: Area Report 16-bit Comparator without CLA

6.6 Timing , Power and Area Report of 16 bit comparator with CLA

A 16-bit comparator employing a Carry Lookahead Adder (CLA) reduces propagation delay through parallel carry computation, significantly enhancing timing performance compared to traditional Ripple Carry Adders (RCA). Figure 6.30 details the Timing and Power Report of the 16-bit comparator without CLA, highlighting its propagation delay characteristics and power consumption profile. Meanwhile, Figure 6.31 illustrates the Area Report of the comparator without CLA, showing minimized chip area utilization despite the design's increased complexity.



```
Timing constraint: Default path analysis
  Total number of paths / destination ports: 152 / 3
--------------------------------------------------------------------------------
Delay:               6.802ns (Levels of Logic = 11)
  Source:            A<0> (PAD)
  Destination:       A_greater_than_B (PAD)

  Data Path: A<0> to A_greater_than_B
                                        Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5    1.222   0.962  A_0_IBUF (A_0_IBUF)
     LUT4:I0->O            1    0.203   0.000  Mcompar_A_greater_than_B_lut<0> (Mcompar_A_greater_than_B_lut<0>)
     MUXCY:S->O            1    0.172   0.000  Mcompar_A_greater_than_B_cy<0> (Mcompar_A_greater_than_B_cy<0>)
     MUXCY:CI->O           1    0.019   0.000  Mcompar_A_greater_than_B_cy<1> (Mcompar_A_greater_than_B_cy<1>)
     MUXCY:CI->O           1    0.019   0.000  Mcompar_A_greater_than_B_cy<2> (Mcompar_A_greater_than_B_cy<2>)
     MUXCY:CI->O           1    0.019   0.000  Mcompar_A_greater_than_B_cy<3> (Mcompar_A_greater_than_B_cy<3>)
     MUXCY:CI->O           1    0.019   0.000  Mcompar_A_greater_than_B_cy<4> (Mcompar_A_greater_than_B_cy<4>)
     MUXCY:CI->O           1    0.019   0.000  Mcompar_A_greater_than_B_cy<5> (Mcompar_A_greater_than_B_cy<5>)
     MUXCY:CI->O           1    0.213   0.580  Mcompar_A_greater_than_B_cy<6> (Mcompar_A_greater_than_B_cy<6>)
     LUT5:I4->O            1    0.205   0.579  Mcompar_A_greater_than_B_cy<7>_inv1 (A_greater_than_B_OBUF)
     OBUF:I->O                 2.571          A_greater_than_B_OBUF (A_greater_than_B)
    ----------------------------------------  ------------
    Total                      6.802ns (4.481ns logic, 2.121ns route)
                                       (65.8% logic, 31.2% route)
--------------------------------------------------------------------------------
```

```
2.3.  Power Supply Summary
-------------------------------------------------------------------
|                    Power Supply Summary                         |
-------------------------------------------------------------------
|                        | Total | Dynamic | Static Power |
-------------------------------------------------------------------
| Supply Power (mW)      | 13.68 | 0.00    | 13.68        |
-------------------------------------------------------------------
```

Figure 6.30: Timing and Power Report of 16-bit Comparaor with CLA

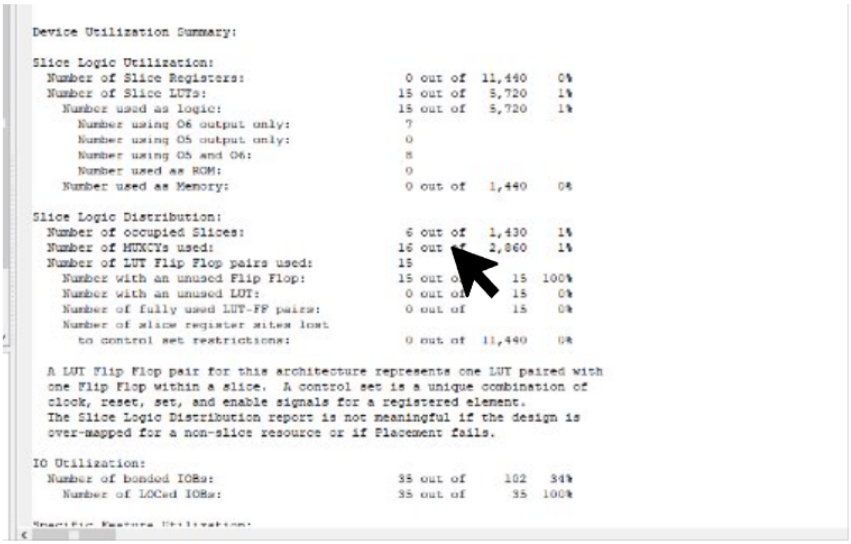


Figure 6.31: Area Report of 16-bit Comparator with CLA

6.7 Comparison of 16-bit comparator using CLA and without using CLA

The comparison table for the 16-bit comparator using CLA and without using CLA, as shown in Table 6.2, highlights the advantages of incorporating the CLA. The table demonstrates that the 16-bit comparator with CLA exhibits significantly lower delay and reduced area compared to the one without CLA. This performance improvement makes the CLA-based design more suitable for high-speed applications where efficiency and quick response times are critical.

Table 6.2: Comparison table for 16-bit comparator using CLA and without using CLA

CONSTRAINTS	16-BIT COMPARATOR USING CLA	16-BIT COMPARATOR
TIME (ns)	6.802	7.269
POWER (mW)	13.68	13.68
AREA (cells)	8 out of 1430	6 out of 1430

Chapter 7

Conclusion

This chapter summarizes the project's findings, discusses the implications of the results, and suggests future areas of research. It provides a comprehensive wrap-up of the project's objectives, methodologies, results, and conclusions.

A 32-bit comparator was successfully designed, simulated, and optimized using the Carry Look-Ahead Adder (CLA) with Cadence tools: Incisive for simulation, Genus for synthesis, and Innovus for optimization. Power consumption, delay, and area utilization were analyzed, revealing significant improvements in power efficiency and area reduction after optimization. The practical applicability and functionality of the optimized 16-bit comparator were demonstrated through implementation on a Spartan-6 FPGA. The robustness and efficiency of the design were validated through waveform analysis, providing valuable insights into digital circuit design, optimization, and addressing VLSI design challenges and solutions.

7.1 Scope for Future Work

The current project lays a solid foundation for further advancements and optimizations in the design of digital comparators. Future work could explore the following avenues:

- **Remote Monitoring and Control:** Implementing features for remote monitoring and control of the comparator performance in IoT networks, enabling real-time adjustments and diagnostics to maintain optimal operation in diverse applications.
- **Advanced Signal Processing:** Investigating the use of advanced signal processing techniques to improve the accuracy and speed of comparators in digital systems, enabling more precise and efficient data processing in various applications.

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