Ch 11 : Basic I/O Interface (11.1 upto 384, 11.2, 11.3 upto 399, 414-421, 11.4 upto 429 and 11.5)

11.1 Introduction to I/O Interface

- IN and OUT:
  - IN: to read info from an I/O device
  - OUT: transfers info to an I/O device
- INS and OUTS transfer strings of data between memory and I/O device
  - can be prefixed with the REP prefix, allow-ing more than one byte, word, or doubleword to be transferred
- DX register is used to store I/O address
- Intel calls the 8-bit form (p8) a fixed address because it is stored with the instruction, usually in a ROM.
- The 16-bit I/O address in DX is called a variable address because it is stored in a DX, and then used to address the I/O device.
- a 16-bit port is actually two consecutive 8-bit ports.
  - 32-bit I/O port is actually four 8-bit ports.
  - the latter always has most significant part
- data appears on address bus
- port number : I/O address
  - decoded the same manner as memory address
- the first 256 I/O port addresses(00H–FFH) are accessed by both the fixed(IN and OUT) and variable I/O instructions, but any I/O address from0100H to FFFFH is only accessed by the variable I/O instruction(INS and OUTS)
- In many dedicated systems, only the rightmost 8 bits of the address are decoded, thus reducing the amount of circuitry required for decoding
- In a PC computer, all 16 address bus bits are decoded with locations 0000H–03FFH, which are the I/O addresses used for I/O inside the PC on the ISA (industry standard architecture) bus.
- *Isolate and Memory-Mapped I/O*
  - two ways to interface I/O:
    - Isolated :the instructions transfer data between the microprocessor's accumulator or memory and the I/O device
    - Memory mapped : any instruction that references memory can accomplish the transfer.
    - Both are in use
  - Isolated I/O:
    - I/O locations are isolated from memory
    - addresses are called ports
    - thus, memory can be expanded to full size
    - only IN, INS, OUT, OUTS can be used
    - Separate control signals for the I/O space are developed (using M/IO and W/R), which indicate an I/O read(IORC overbar) or an I/O write (IOWC overbar) operation
    - used to control peripheral devices
  - Memory-Mapped I/O:
    - any instruction can be used
    - a portion of memory system is used as I/O map
    - decreased available memory space
- *Personal Computer I/O Map*
  - I/O space between ports 0000H and 03FFH is normally reserved for the computer system and the ISA bus.
  - 0400H–FFFFH are generally available for user applications, main-board functions, and the PCI bus.
  - 00F8H–00FFH for communications
    - So, Intel reserves I/O ports 00F0H–00FFH.
  - 80386–Core2 use I/O ports 800000F8–800000FFH for communications to their coprocessors.
  - The I/O ports located between 0000H and 00FFH are accessed via the fixed port I/O instructions;
  - the ports located above 00FFH are accessed via the variable I/O port instructions.
- *Basic Input and Output Interfaces*
  - set of 3 state buffers:
    - Input:
      - The external TTL data are connected to the inputs of the buffers.
      - The outputs of the buffers connect to the data bus.
      - *Fig 11-3 and explanation of pdf page 401-402*
    - Output:

        - receives data from the microprocessor and usually must hold it for some external device.
        - Its latches or flip-flops, like buffers, are often built into the I/O device.
        - Latches are needed to hold the data because when the microprocessor executes an OUT instruction, the data are only present on the data bus for less than 1.0 µs.
        - *Fig 11-4 and explanation on pdf page 402-403*
- *Handshaking*
    - also called polling
    - synchronizes the I/O device with the microprocessor in case I/O device has a slower rate
    - tests the Busy pin
    - E.g. parallel printer with 100 CPS speed
        - *explanation on pdf page 403*

11.2 I/O Port Address Decoding

- *difference between memory decoding and isolated I/O decoding given on pdf page 407*
- *8 bit*
    - address connections A7–A0 for an 8-bit I/O port address are decoded
    - The PLD is a better decoder circuit because the number of integrated circuits has been reduced to one device.
- *16 bit*
    - A15 - A0 are decoded
    - The NAND gate decodes part of the address (A15, A14, A13, and A11) because the PLD does not have enough address inputs.
- *8 and 16 bit Wide I/O Ports*
    - Data transferred to an 8-bit I/O device exist in one of the I/O banks in a 16-bit microprocessor such as the 80386SX.
    - There are 64K different 8-bit ports, but only 32K different 16-bit ports
    - Because two I/O banks exist, any 8-bit I/O write requires a separate write strobe
    - The only time that a read can cause problems is when the I/O device responds incorrectly to a read operation
    - When selecting 16-bit-wide I/O devices, the (A0) and pins have no function because both I/O banks are selected together.
- *32 bit Wide I/O Ports*
    - uncommon

11.3 The Programmable Peripheral Interface

- PPI is popular and low cost
- has 24 pins for I/O that are programmable in groups of 12 pins,
- has groups that operate in three distinct modes of operation
- mediator bw IO device and mp
- allows multiple io device to connect to mp
- *Basic Description of 82C55*
    - 2 groups(A and B), 3 ports (A, B and C)
        - group A : port A (PA7 - PA0) and upper half of port C (PC7 - PC4)
        - groupB : port B (PB7 - PB0) and lower half of port C (PC4 - PC0)
- *Programming 82C55*
    - Command bytes
    - if 7th byte is 1 its A else B
    - *Fig 11-20 on pdf page 418..important*
- *Mode 0*
    - basic i/o mode that allows pins of group b to be programmed as simple input and latched output connections
    - 8C255 functions as a buffered input device(buffered till used) and latched output device(sent only after all collected by mediator)
    - if data exists in place immediate write occurs
- *Mode 1*
    - operation is strobed operation for group B connections.
    - data is transferred through port B
    - *Fig 11-27*
    - i/o through strobe
        - signals are used
        - if data exists, write signal is checked to be active before data is written
- *Mode 2*
    - bidirectional data
    - same port can read or write
- Handshaking signals are provided by port C

11.5: 16550 programmable communications interface,
- Asynchronous Serial Data
- Functional Description
- Pin Functions
- Programming