Ch 18 : The Pentium and Pentium Pro Microprocessors (18.1 734-738, 18.5 except pin functions and pin diagram)

18.1 Introduction to Pentium Microprocessor

- *The memory system*
  - 4G bytes in size
  - difference is of 64 bit data bus
  - 64 bit is divided into 8 banks of 512M bytes
  - each bank stores byte wide data with 1 bit parity
  - double precision floating point can be done in 1 clock cycle while it takes 2 clock cycles in 80386 or 80486
  - banks are helpful in writing byte or word or doubleword or quadword
  - AP pin for parity check for address bus A31- A5.
  - bad parity is indicated by APCHK overbar
  - any error by parity is informed but doesnt handle itself
- *I/O system*
  - compatible to all
  - A15- A3 on address bus
  - bank enable signals select actual memory bank for io transfer
  - in case an io location is blocked , type 13 interrupt occurs
- *System timing*
  - one cycle divided into clocking periods
    - below versions(till 80386) had 4 clocking periods
  - ADS issued at T1 combined with W/R and M/IO
    - W/R by flip flop
  - At T2, sync occurs and read/write occurs
    - operation is done by the end of T2
  - Wait states depend of BRDY overbar input
    - should become 0 by the end of T2 else wait state enters till brdy becomes 0
  - burst cycle:
    - more efficient
    - 4 64-bit numbers are done in one burst cycle.
    - has 5 clocking periods
    - requires a transfer rate of 15.2ns
      - has no wait states
      - can be achieved if level 2 cache is in place
      - wait is inserted if no cache thus increased time
- *Branch Prediction Logic*
  - on compile time, branch instructions are fetched before execution to reduce branch time during execution
  - only in case of short or near
  - instructions are loaded into instruction cache
  - allows completion in one clocking period
  - but disadvantage is that in case of error 3 extra clocking periods will be used
    - errors are rare
- *Cache Structure*
  - different from 80486
  - two 8K byte caches instead of one
  - instruction cache and data cache
  - hit rate becomes faster thus fast execution
- *Superscalar Architecture*
  - lower level mps has 1 execution unit
  - pentium has 3 execution unit: 1 for floating and rest two(U pipe and V pipe) for integer
  - 3 instructions can be executed together

18.2 Pentium Pro Microprocessors

- *Internal Structure*
  - *Fig 18-13 on pdf page 769*

- level 2 caches
- data from external bus goes to level 2 cache
- BIU(internal bus sends them to level 1 cache (instruction or data)
- instructions goes to Instruction Fetch and Decode Unit(IFDU)
  - can decode 3 types of instructions simultaneously
  - 1 floating and rest two integer
  - any branch instructions are fetched and address retrieved, kept in instruction pool
- 2 types of instructions:
  - those that are decoded but not executed
  - those that are decoded and executed
- dispatch and execute unit(DEU) retrieves instructions that are only decoded and executes them and returns to instruction pool with result
- retire unit(RU) check executed instructions and removes them from the pool, returns through data cache
- pentium pro only differs from pentium in error correction. it is in built for pro
- branch prediction logic is in IFDU
- *DEU diagram in ppt*

- *Memory System of Pro*
  - similar to Pentium
  - additional memory can be enabled by bit position 5 of CR4
  - only accessible if paging system is 2M enabled
  - built in ECC allows correction of 1 bit error and detection of 2-bit error
    - 64 bit number stored in memory has an 8 bit extra number to do this
- *I/O system*
  - same as Pentium
- *System timing*
  - same as Pentium
  - TRDY overbar signal instead of BRDY