Ch 10 : Memory Interface (upto 10.4)

Introduction

- Read-Only Memory(ROM): contains system software and permanent system data
- Random Access Memory(RAM): contains temporary data and application software
- Pins with an overbar are active at logic 0.
- The OE pin is activated by the 8088 RD signal or the MRDC(memory read control) signal of other family members.

10.1 Memory Devices

- read-only memory (ROM), flash memory (EEPROM), static random access memory (SRAM), and dynamic random access memory (DRAM).
- Pin connections common to all memory devices are the address inputs, data outputs or input/outputs, some type of selection input, and at least one control input used to select a read or write operation
- *Address Connections:*
  - To select memory location within memory device
  - A0 - An, n depends on number address pins which depend on the number of memory locations (1K to 1G)
    - 1K (1024) memory locations has 10 pins, 11 pins for 2048 (in the power of 2)
    - 400H represents 1K byte section (e.g. 10000H - 103FFH, 400-1 = 3FF)
    - 1000H is 4K, 10000H is 64K, 1M is 100000H
- *Data Connections:*
  - points at which data are entered for storage or extracted for reading.
  - D0 - D7 for 8 bit wide memory i.e byte wide
  - Catalog listings of memory devices often refer to memory locations times bits per location.
    - E.g. a memory device with 1K memory locations and 8 bits in each location is often listed as a 1K ×8 by the manufacturer.
  - Memory devices are often classified according to total bit capacity.
  - E.g. a 64K ×4 memory is listed as a 256K device
- *Selection Connections:*
  - To select or enable memory device
  - input often called as Chip Select (CS), Chip Enable (CE), or select (S).
  - RAM has atleast one CS or S and ROM has atleast one CE
  - If these are active (logic 0), read or write is performed
  - All CS connections have to be active
- *Control Connections:*
  - one for ROM,
    - output enable(OE) or gate(G): allows data to flow out of the output data pins
    - output is enabled if OE and CE are both active
    - OE enables and disables a set of three-state buffers located within the memory device and must be active to read data.
  - one or two for RAM
    - if one, R or W : selects a read operation or a write operation only if the device is selected by the selection input (CS).
    - if two, WE/W(write enable) and OE/G : WE must be active(0) for write, OE must be active for read. never active together
- *ROM:*
  - permanently stores programs and data that are resident to the system and must not change when power supply is disconnected i.e. Non Volatile.
  - EPROM :
    - used when software must be changed often or when too few are in demand.
    - programmed in the field on a device called an EPROM programmer.
    - erasable if exposed to high-intensity ultra-violet light for about 20 minutes or so
    - provides information to the system on the size and the speed of the memory device for plug-and-play applications.
  - PROM(Programmable ROM): programmed in the field by burning open tiny NI-chrome or silicon oxide fuses; cannot be erased.
  - RMM (read mostly memory)/ Flash memory/ EEPROM (Electrically erasable PROM)/ EAROM (electrically alterable ROM), or a NOVRAM (nonvolatile RAM):
    - take time to erase.
    - used to store setup information for systems such as the video card in the computer.
    - Replaced EPROM for BIOS memory
  - *Fig 10-3 on page 352 for timing of EPROM and explanation on 351&352*
  - input goes low at the same time that the address inputs become stable

- requires wait states to operate properly with the 8086/8088 microprocessors because of its rather long access time.
- If wait states are not desired, higher-speed versions of the EPROM can be used

- *Static RAM (SRAM) Devices:*
  - retain data for as long as DC power is applied i.e. static or volatile.
  - used when the size of the read/write memory is relatively small i.e. less than 1M.
  - The OE pin is labeled G, the CS pin is S, and the WE pin is W. functions same
- *Dynamic RAM (DRAM) Memory:*
  - same as SRAM, except that it retains data for only 2 or 4 ms on an integrated capacitor. No S input
  - rewritten afterwards because capacitors (store logic 1 or 0) lose charge
  - entire contents of the memory are refreshed with 256 reads in a 2- or 4-ms interval.
  - Disadvantage: requires so many address pins that the manufacturers have decided to multiplex the address inputs
  - only way that 16 address bits can be forced into 8 address pins is in two 8-bit increments.
    - the column address strobe(CAS) and row address strobe(RAS) are reqd
    - *practice explained on page 356-359 of pdf*
  - CAS also performs the function of the chip selection input to the DRAM.
  - RAS selects which part of the address is applied to the address inputs.
  - the internal row address latch is edge-triggered, it captures the row address before the address at the inputs changes to the column address.

10.2 Address Decoding

- the EPROM has 11 address connections and the microprocessor has 20.
- the memory address is of 20 bits.
- So EPROM sees 1M bytes instead of 2K bytes, the address pins are decoded
- *Simple NAND Gate Decoder:*
  - A10 - A0 connect to EPROM and A19 - A11 connect to NAND decoder
  - decoder selects the EPROM
  - NAND output connected to CE to enable EPROM
  - If the 20-bit binary address, decoded by the NAND gate, is written so that the leftmost nine bits are 1s and the rightmost 11 bits are don't cares (X), the actual address range of the EPROM can be determined.
    - assuming Xs to be 0 gives start and Xs to be 1 gives end (*Example 10-1 pdf page 362)*
  - A don't care is a logic 1 or a logic 0, whichever is appropriate.
  - rarely used because each memory device requires its own NAND gate decoder.
  - expensive
- *the 3-to-8 Line Decoder (74LS138):*
  - Only if all enable inputs (G2A overbar, G2B overbar and G1) are active(0,0,1) , a decoder output can be 0.
  - the select inputs decide which output will be 0, thus, only one
  - *Fig 10-14 on pdf page 362 diagram and truth table*
  - Sample Decoder Circuit:
    - decoder selects eight 8K-byte blocks of memory for a total memory capacity of 64K bytes.
    - *explained on pdf page 363*
    - Address range of entire decoder is determined (only first 4 bits are not dont cares) by *Example 10-2 page 363*
    - Address range of each memory device attached to decoder output determined by (CBA not dont cares but the actual value) *example 10-3 & 10-4 pdf page 364*
- *The Dual 2-to-4 Line Decoder (74LS139):*
  - Used where the EPROM is located at the top of the memory space and the SRAM at the bottom.
  - *Fig 10-16 on pdf page 365*
- *PLD Programmable Decoders:*
  - SPLDs (Simple PLDs) :
    - PLA (programmable logic array), PAL (programmable array logic), and GAL (gated array logic)
    - PAL and PLA are fuse programmed like PROM
    - some are erasable
    - used when concentration is on decoding addresses
  - Complex PLDs:
    - CPLDs (complex programmable logic devices),FPGAs (field programmable gate arrays), and FPICs (field programmable interconnect).
    - used when concentration is on a complete system
    - referred to as an ASIC (application-specific integrated circuit).
  - Combinatorial Programmable Logic Arrays:

        - internally structured as a programmable array of combinational logic circuits
        - *Fig and explanation on pdf page 365-366*
        - recently, PLD design is accomplished using HDL(hardware description language) or VHDL (verilog HDL)
            - *Fig and explanation on pdf page 366-368*
            - Comments in VHDL programming begin with a pair of minus signs
            - The keyword not is used for logical inversion and the keyword and is used for the logical and operation.

10.3 8088 and 80188(8-bit) Memory Interface

- methods used to address the memory are slightly different in microprocessors that contain different data bus widths
- Most ideal
- *Basic 8088/80188 Memory Interface:*
    - 8 bit data bus
    - simple controller
    - the memory system must decode the address to select a memory component. It must also use the RD overbar, WR overbar , and IO/M overbar control signals to control the memory system.
    - in maximum mode, the IO/M signal is combined with RD to generate the MRDC overbar signal, and IO/M is combined with WR to generate the MWTC overbar signal.
        - The maximum mode control signals are developed inside the 8288 bus controller.
    - In minimum mode, the memory sees the 8088 or the 80188 as a device with 20 address connections (A19–A0), eight data bus connections (AD7–AD0), and the control signals IO/M, RD, and WR.
    - Interfacing EPROM to the 8088:
        - *Fig 10-20*
            - 3 decoders being used sized 32K x 8, total 96K x 8
            - U1 starts at E8000H - EFFFFH
            - U2 at F0000H - F7FFFH
            - U3 at F8000H - FFFFFH
        - selected for address range starting at E8000H to FFFFFH
            - this section is for EPROM
        - Whenever a MP restarts it begins at location FFFF0H called cold start location
            - There's a jump statement that takes you to the location where ROM is stored (E8000H to FFFFFH)
    - Interfacing RAM to the 8088:
        - easier to interface than EPROM because wait states are not reqd
        - ideal section is bottom
            - because interrupt vector addresses are at bottom (0-255)
            - ROM at top
            - important to encode this section with RAM
                - because interrupt vectors are often modified by software packages
        - 16 62256 SRAMs interfaced at 8088 beginning at 00000H till E8000H-1 rest is ROM
        - decoders decide which 16 RAMs and other decoders for apt memory sections
- *Interfacing Flash Memory:*
    - fast memory
    - used for fast occurring processes
    - common to store setup info on video cards and system BIOS in PCs
    - in MP3 and USB
    - stores occasionally changing memory
    - requires 12V to erase and write new data
        - this is how its different from SRAM
        - new versions use 5V or 3.3V
    - The SRAM can perform a write operation in as little as 10 ns, but the flash memory requires approximately 0.4 seconds to erase a byte.
    - EEPROM is a flash memory available as parallel or serial interface
        - expansion in serial is small but can store information as I/O like in flash drive
    - has two signal lines.
        - One is a serial clock (SCL)
        - other is a bidirectional serial data line (SDA).
    - The clock frequency can be anything up to 400 KHz,
        - thus, not meant to replace the main memory in a system.
        - It is fast enough for music or other low-speed data

- *Error Correction*
  - recent error correcting circuits
  - e.g. 74LS636:
    - an 8-bit error correction and detection circuit that corrects any single-bit memory read error and flags any 2-bit error called SECDED (single error correction/double error correction).
    - found in high-end computer systems because of the cost of implementing a system that uses error correction.
    - corrects errors by storing five parity bits with each byte of memory data.
    - This increases the amount of memory required, but provides automatic error correction for single-bit errors.
    - Error not detected if more than 2 bits are incorrect
      - Expensive to implement
      - Whenever a memory component fails completely, its bits are all high or all low.
      - the circuit *flags* the processor with a multiple-bit error indication.
    - has eight data I/O pins, five check bit I/O pins, two control inputs (SO and SI), and two error outputs: single-error flag (SEF)and double-error flag (DEF).
    - The control inputs select the type of operation to be performed
    - When a single error is detected, the 74LS636 places a 01 on S0 and S1 by causing a wait and then a read following error correction.
    - if the data are to be accessed from the memory before the RD strobe goes low, the S or CS overbar pin is grounded and data bus buffers control the flow to the system bus
    - On the next negative edge of the clock after the RD signal, it checks the SEF to determine whether an error has occurred.
    - If it has, a correction cycle causes the single-error defect to be corrected.
    - If a double error occurs, an interrupt request is generated by the DEF output, which is connected to the NMI pin of the microprocessor.
  - new systems using DDR memory with ECC
  - Since Pentium, mp incorporates this circuitry
    - ECC memory is 72-bits wide using the additional 8 bits to store the ECC code.

10.4 8086, 80186, 80286 and 80386SX(16-bit) Memory Interface

- differ from the 8088/80188 :
  - The data bus is 16 bits wide instead of 8 bits wide as on the 8088;
  - the IO/M pin of the 8088 is replaced with an M/IO pin;
  - there is a new control signal called bus high enable (BHE overbar).
  - The address bit A0 or BLE overbar is also used differently
- for 8086/80186 and 80286/80386SX:
  - latter contains a 24-bit address bus (A23–A0) instead of the 20-bit address bus (A19–A0) of the 8086/80186.
  - The former contains an M/IO signal, while the latter contains control signals MRDC overbar and MWTC overbar instead of RD and WR.
- *16-bit Bus Control*
  - divided into 2 separate 8 bit wide sections (or banks)
  - processor can write on either half or both halves
  - low or high:
    - low has even numbered memory location
    - high has odd numbered
  - bank selection is done by:
    - separate write signal to select write to each or both bank
      - used mostly
      - least costly
    - separate decoder:
      - used only when power needs to be saved
      - not cost effective
      - not speed effective
  - Separate Bank Decoders:
    - least effective way to decode memory address
    - E.g. 74LS138
    - *Table 10-2 on pdf page 377 for truth table*
  - Separate Bank Write Strobes:
    - *Fig 10-29 on pdf page 379*
    - 3 input signals: BHE, WR and A0

    - if all three are 0, high bank is used
    - if only A0 is 1, both banks
    - at 1, 0, 1 respectively , low bank
    - WR will mostly be 0
- Example 7: GAL22V10