Ch 13 : Direct Memory Access and DMA Controlled I/O (13.1-13.2)

13.1 Basic DMA Operation

- 2 control signals: request and acknowledge DMA
- DMA removes mp from between i/o devices and memory
- used for fast memory access
- almost obsolete now
- HOLD pin: input used to requests a DMA action
  - higher priority than INTR and NMI
  - HOLD > NMI > INTR
  - when NMI comes, current instruction gets complete before listening to NMI
  - when HOLD comes, immediately everything paused and listened to HOLD
  - only reset pin has higher priority than HOLD
- HLDA pin : output used to acknowledge DMA action
  - bus goes to high impedance state
  - its a signal to the requesting device that the processor has relinquished control of memory and io space
- DMA read transfers data from memory to IO
- DMA write transfers data from IO to memory
- memory and IO are controlled simultaneously thus separate control signals
- whenever read is issued, both MRDC and IOWC are activated
- whenever write is issued both MWTC and IORC are activated
- DMA controller is needed by 8086/8088. is like a mp for memory and io mediation
  - provides which io device and which memory address
- newer ones have different parts(inbuilt) for this thus no dma controller
- data transfer speed for DMA depends on speed of memory device or DMA controller
  - if memory speed is 50ns then DMA transfers at rate of 1/50 ns or 20M bytes per second
  - if DMA controller has speed 15MHz with 50 ns memory, transfer rate is 15 MHz because DMA controller is slower than memory
- DMA controller slows the speed mostly
- Now used PCI express(20Gbps), Serial ATA(300Mbps)

13.2 The 8237 DMA Controller

- supplies memory and IO with control signals and address info during DMA transfer
- its like a small mp
- dedicated functioning
- 4 channel device expandable to any number of channels
- adequate for small systems
- transfer rates upto 1.3M bps
- address 64K bytes and transfer with a single programming
- *Pin Definitions on pdf page 512-517*
  - clock to be inverted
- Internal Registers
  - CAR: current address register
    - 16 bit memory address is held for DMA transfer
    - increments or decrements on every byte of data transferred depends on programming
  - CWCR : current word count register
    - no of bytes to be transferred is stored here
    - one less than the total is stored
  - BA and BWC (base address and base word count)
    - used when auto initialisation is selected
      - when same amount as previous transfer is to be retransferred
    - dont have to request DMA again if u know once wont be enough
  - CR (command register):
    - programs operation of 8237 DMA controller
    - uses bit position 0 selects the mode (memory to memory or io to memory)
    - Fig 13-4 for each bit
  - MR (mode register)
    - Programs the mode of operation

        - each channel has its own selected by bit 1 and 0
        - rest bits decide operation , auto initialisation , inc/dec, and mode
        - demand mode: data transfers until EOP signal comes
        - single mode : transfers current word count, DMA may have to be requested again
        - block mode: all data transferred at once
        - cascade mode : when multiple DMA controllers
    - BR bur request:
        - requests DMA transfer via software
        - external signal not available for dma transfer
        - used in case of memory to memory
        - external signal is generated when io accesses dma
        - fig 13-6 for bit numbers
    - MRSR (mask register set/reset)
        - to disable channels, set mask
        - different commands for each channel
        - reset enables all
        - fig 13-7
    - MSR mask register:
        - to disable or enable all channels at once
        - used combined with MRSR
    - SR status register
        - show status of each dma channel
        - whether channel has reached TC (terminal count) i.e. transferred all its bytes)
            - if yes, terminated
        - fig 13-9
- Software Commands
    - to control operations
    - can be controlled by direct commands not binary bit
    - master clear: same as RESET signal, disables all channels
    - clear mask register: enables all 4 dma channels
    - clear first/last flip flop: selects which byte high word/ low word is written in current address
        - F/L =0, low ; F/L= 1, high
    - to program 8237:
        - F/L is cleared using clear F/L command
        - channel is disabled
        - Least Significant Bit and Most SB of address are programmed
        - LSB and MSB of count are programmed