Ch 9 : Interfacing (8086/8088 Hardware Specifications upto 9.4)

Introduction

- clock generation, bus buffering, bus latching, timing, wait states, and minimum mode operation versus maximum mode operation.
- it is possible to connect or interface anything to the microprocessor
- The Interrupt flag(IF) is a flag bit in the CPU's FLAGS register, which determines whether or not the will respond immediately to maskable hardware interrupts. If the flag is set to 1 maskable interrupts are enabled. If reset, such interrupts will be disabled until interrupts are enabled.

9.1 Pin-Outs and the Pin Functions

- 8086 and 8088 are packaged with 40-pin dual in-line packages (DIPs)
- +5.0 V required with supply voltage tolerance of +-10%
- operate in ambient temperatures between 32° F and 180° F.
- CMOS version:
  - requires a very low supply current and has an extended temperature range.
  - The 80C88 and 80C86 are CMOS versions, requiring only 10 mA of power supply current and function in temperature extremes of -40° F through +225° F.
- Knowledge of input current requirement for an input pin and the output current drive capability for an output pin allows the hardware designer to select the proper interface components for use with the microprocessor without the fear of damaging anything.
- Input Characteristics:
  - *Table 9-1 on pdf page324 for input characteristics*
  - compatible with all the standard logic components available today
  - The input current levels are very small because the inputs are the gate connections of MOSFETs and represent only leakage currents.
- Output Characteristics:
  - *Table 9-2 on pdf page324 for output characteristics*
  - The logic 0 voltage level is not compatible with that of most standard logic families.
    - Standard logic circuits have a maximum logic 0 voltage of 0.4 V,
    - the 8086/8088 has a maximum of 0.45 V.
    - Thus, there is a difference of 0.05 V.
    - This difference reduces the noise immunity from a standard level of 400 mV (0.8 V – 0.45 V)to 350 mV.
      - The noise immunity is the difference between the logic 0 output voltage and the logic 0 input voltage levels.
    - The reduction in noise immunity may result in problems with long wire connections or too many loads.
    - It is recommended that no more than 10 loads of any type or combination be connected to an output pin without buffering.
    - If this loading factor is exceeded, noise will begin to take its toll in timing problems.
  - The best choice of component types for the connection to output pin is an LS, 74ALS, or 74HC logic component
  - if a fan-out of more than 10 unit loads is required, the system should be buffered.
  - *Table 9-3 on pdf page324 for fan-out*

Basis
Sub-basis
8086
8088
Pin Outs
type
16-bit microprocessor with a 16-bit data bus
16-bit microprocessor with an 8-bit data bus.
pin connections
AD_0–AD_{15}

AD_0–AD_7
Control Signals
has an M/IO pin
has an IO/M pin.
Pin 34 of IC (hardware)
BHE/S7 pin on Pin 34 of IC
SS0 pin on Pin 34 of IC
Power Supply Requirements
maximum supply current
360 mA
340 mA
Demultiplexing
Multiplexed pins
AD15- AD0, A19/S6–A16/S3, and BHE/S7.
only AD7–AD0 and A19/S6–A16/S3

- *Pin Connections:*
  - address/data bus lines (AD), address/status bits (A/S) are multiplexed
  - The pins enter a high-impedance state when a hold acknowledge occurs.
  - AD_7 - AD_0: Contain the rightmost 8 bits of the memory address or I/O port number whenever ALE is active (logic 1) or data whenever ALE is inactive (logic 0).
  - A_{15} - A_8: The 8088 address bus provides the upper-half memory address bits that are present throughout a bus cycle.
  - AD_{15} - AD_8: contain address bits A_{15}–A_8 whenever ALE is a logic 1, and data bus connections D_{15}–D_8 when ALE is a logic 0.
  - A_{19}/S_6 - A_{16}/S_3:
    - S_6 is always a logic 0, bit S_5 indicates the condition of the IF flag bit, and $S_4$and S_3 show which segment is accessed during the current bus cycle.
    - $S_4$and S_3 could be used to address four separate 1M byte memory banks by decoding them as $A_{21}$and A_{20}
  - RD: Read Signal. When 0, data bus is receptive to data
  - READY:
    - controlled to insert wait states into the timing of the microprocessor.
    - MP enters wait state if 0 else no effect
  - INTR:
    - Interrupt Request requests hardware interrupt.
    - Held high when IF=1, and INTA becomes active i.e. MP enters interrupt acknowledge cycle
  - TEST: if 0, WAIT functions as NOP else it waits for TEST to becomes 0.
  - NMI: Non-Maskable Interrupt. If active, interrupt vector 2 is used
  - RESET: MP resets if this pin is active for 4 clock periods i.e. instructions execute from location FFFF0H and IF clears thus no more interrupts
  - CLK: Clock pin. Provides basic timing signal. Duty to be high for one third of clocking period and low for rest
  - VCC: Power supply. provides a +5.0 V, ±10 % signal.
  - GND: Ground. return for power supply. usually a pair
  - BHE S_7: Bus high enable pin. Enables most significant data bus bits (D_{15} - D_8) during read/write. S_7 is always logic 1.
  - MN/MX: min/max. selects the mode (min or max). +5.0 V for min
    - *Minimum Mode Pins:* connect the MN/MX pin directly to +5.0 V
      - IO/M or M/IO: Indicates whether address bus contains memory or I/O port address.

        - WR: Write line is a strobe indicating output. Valid data at 0
        - INTA: Interrupt acknowledge gates the interrupt vector number onto data bus as a response to INTR enable.
        - ALE: Address Latch Enable shows A/D bus contains address information. Does not float during hold ack
        - DT/R: Data transmit/receive shows transmission of data (at 1) and receiving at 0.
        - DEN: data bus enable actives external data bus buffers
        - HOLD: requests DMA. At 1, MP puts A, D and control bus at high impedance
        - HLDA: Hold acknowledge indicates entering hold state
        - SS0: status line. Equivalent to S_0 pin in max mode. combined with IO/andDT/to decode the function of the current bus cycle
    - *Maximum mode pins:* connect the MN/MX pin to ground
        - S2, S1, S0: status bits indicate function of current bus cycle.
        - RQ/ GT1 and RQ/GT0: request/grant pin requests DMA and are bidirectional
        - LOCK: locks peripherals off the system.
        - QS1 and QS0: queue status bits show status of internal instruction queue

9.2 Clock Generator (8284A)

- Ancillary component.
- provides functions for clock generation, RESET synchronization, READY synchronization, and a TTL-level peripheral clock signal
- *Pin functions:*
    - AEN1 and AEN2 : address enable pins qualify busy ready signals, RDY1 and RDY2
    - RDY1 and RDY2: bus ready inputs cause wait states
    - ASYNC : ready synchronisation selects stages of sync
    - READY: output pin connects to READY input and syncs with RDY
    - X1 and X2: crystal oscillator pins connect to an external crystal used as the timing source for the clock generator and all its functions.
    - F/C : frequency/crystal chooses clocking source.
        - an external clock is provided to the EFI input pin if 1 and external frequency input is used;
        - the internal crystal oscillator provides the timing signal if 0.
    - CLK: clock output provides CLK input signal. same cycle as input
    - PCLK: peripheral clock is 1/6 of EFI input freq. 50% duty cycle. for peripheral equipment
    - OSC: oscillator output is a TTL level signal same freq as EFI input
    - RES: reset output.
    - CSYNC: clock sync. whenever EFI input provides sync in systems with multi MPs. grounded if internal crystal oscillator
    - GND; ground
    - VCC: power supply pin
- *Operation of 8284A*
    - *Fig 9-3 pdf page 329 and explanation*
    - when F/ C is a logic 0, the oscillator output is steered through to the divide-by-3 counter. If F/ C is a logic 1, then EFI is steered through to the counter.
    - The D-type flip-flop ensures that the timing requirements of the 8086/8088 RESET input are met.
    - Correct reset timing requires the RESET input to come a logic 1 no later than four clocks after system power is applied, and to be held high for at east 50 µs. made sure by D flip flop

9.3 Bus Buffering and Latching

- multiplexed buses must be demultiplexed before use
- Multiplexing is done to reduce the no. of pins on IC
- Memory and I/O require that the address remains valid and stable throughout a read or write cycle.
- If the buses are multiplexed, the address changes at the memory and I/O, which causes them to read or write data in the wrong locations.
- Buses:
    - Address to provide memory address or I/O port number
    - data to transfer data b/w MP and memory or I/O
    - control bus to provide control signals to memory and I/O
- *In 8088,*
    - two 74LS373 or 74LS573 transparent latches are used
    - They remember the input and pass to output as soon as ALE becomes 1.
    - separate data bus allows connection to any 8-bit peripheral

- *In 8086,*
  - three 74LS373 latches
  - address bus considered 20-bit, data bus 16-bit, control bus three-line
- *The Buffered System*
  - Latches are designed to drive the high-capacitance buses encountered in microcomputer systems
  - The buffer's output currents have been increased so that more TTL unit loads may be driven:
    - A logic 0 output provides up to 32 mA of sink current,
    - a logic 1 output provides upto 5.2 mA of source current.
  - If more than 10 unit loads are attached to any bus pin, the entire 8086 or 8088 system must be buffered.
  - A fully buffered signal introduces a timing delay to the system.
    - This causes no difficulty unless memory or I/O devices are used, which function at near the maximum speed of the bus.
  - *Fully Buffered 8088:*
    - A15–A8 use a 74LS244 octal buffer;
    - D7–D0, use a 74LS245 octal bidirectional bus buffer;
    - the control bus signals M/IO, RD and WR use a 74LS244 buffer.
    - requires two 74LS244s, one74LS245, and two 74LS373s.
    - The direction of the 74LS245 is controlled by the DT/R signal and is enabled and disabled by the DEN signal.
  - *Fully Buffered 8086:*
    - data bus uses two 74LS245 octal bidirectional bus buffers;
    - the control bus signals, M/IO, RD and WR ,use a 74LS244 buffer.
    - requires one 74LS244, two 74LS245s, and three74LS373s.
    - requires one more buffer than the 8088 because of the extra eight data bus connections, D15–D8.
    - has a BHE signal that is buffered for memory-bank selection.

9.4 Bus Timing

- If data are written to the memory, the microprocessor outputs the memory address on the address bus, outputs the data to be written into memory on the data bus, and issues a write (WR) to memory and IO/M= 0 for the 8088 and M/IO= 1 for the 8086.
- If data are read from the memory , the microprocessor outputs the memory address on the address bus, issues a read memory signal (RD), and accepts the data via the data bus.
- *General Timing*
  - memory and I/O are used in periods called bus cycles
  - Each bus cycle is 4 system clocking periods (T states)
    - One complete in 800ns if operated at 5Hz
    - Can read or write data at a maximum rate of 1.25 million times a second
  - *Fig 9-10 and explanation on pdf page 336*
  - At T1, The address of the memory or I/O location is sent out via the address bus and the address/data bus connections.
  - At T2, RD/WR signal and DEN. data appears on data bus (in case of write)
    - READY is sampled at the end
  - At T3, it waits if not READY, else, data is accessed. In case of read, data is sampled at the end
  - At T4, bus signals deactivated for next cycle. data bus connections are sampled
    - Write is performed here
- *Read Timing*
  - Memory is chosen by its access time, which is the fixed amount of time that the microprocessor allows it to access data for the read operation
  - Memory access time starts when the address appears on the memory address bus and continues until the microprocessor samples the memory data at T3.
  - Memory access time is three clocking states minus the sum of T_{CLAV} and T_{DVCL}
    - the data setup time (T_{DVCL}), occurs before T3.
    - The address does not appear until T_{CLAV} time
  - the width of the RD strobe is a timing factor that may affect memory operation
- *Write Timing*
  - When interfacing some memory devices, timing may be especially critical between the point at which WR becomes a logic 1 and the time when the data are removed from the data bus.
  - memory data are written at the trailing edge of the WR strobe