Milestone 1:

- Developed Euclid's Algorithm and 'relprime' in 90 minutes.
- Prepared assembly code as a preliminary model for instruction set architecture (ISA) development. This preparation was completed before the team meeting to facilitate immediate discussion on ISA.

Team Meeting on 1/2/2024 (Duration: 40 minutes):

- The team agreed on developing a load-store based processor.
- We allocated 16 bits among registers, types, etc., and engaged in detailed discussions on optimizing and limiting the function and opcode to 4 bits, allowing for a maximum of 16 different instructions.

Team Meeting on 1/9/2024 (Duration: 2.5 hours):

- Began drafting Milestone 1, focusing on design philosophy and reviewing our ISA, including bit allocation for each type and instruction.
- Assigned opcodes and functions to each instruction and reviewed the process of converting these to machine language.

Milestone 2:

Meeting Scribe (Duration: 1 hour):

- Recorded notes during the meeting and implemented suggestions post-meeting.
- Revised the documentation to simplify language and correct errors discussed.

Reviewed RTLs (Duration: 30 minutes):

- Re-examined all implemented Register Transfer Languages (RTLs) and made minor adjustments.
- Tested RTLs.

Reviewed Design Components (Duration: 20 minutes):

- Reviewed  essential design components necessary for Milestone 3 datapath designing.

Concised Alternative Logic (Duration: 1 hour):

- Examined logic for minimal branching, focusing on reducing byte offset and minimizing jumping. Currently trying to further minimize jumping and total instructions to implement relprime